# AK4492

## Quality Oriented 32-Bit 2ch DAC

## 1. General Description

The AK4492 is a new generation Premium 32-bit 2ch DAC with VELVET SOUND™ technology, achieving industry's leading level low distortion characteristics. The OSR-Doubler technology establishes low power consumption and low distortion characteristics. Moreover, the AK4492 has six types of 32-bit digital filters, realizing simple and flexible sound tuning in wide range of applications. The AK4492 accepts up to 768kHz PCM data and 11.2MHz DSD data, ideal for a high-resolution audio source playback that are becoming widespread in smartphone, portable audio player etc.

Application: Smart Cellular Phones, IC-Recorders, Bluetooth Headphones, CD/SACD Players, Network Audios, USB DACs, USB Headphones, Sound Plates/Bars, HD Audio/Voice Conference Systems, AV Receivers

## 2. Features

- **THD+N: -115 dB**
- **DR, S/N: 127 dB (2 Vrms Output)**
- **128 Times Over Sampling**
- **Sampling Rate: 8kHz ~ 768 kHz**
- **32-bit 8x Digital Filter**
  - **Short Delay Sharp Roll-off, GD=6.0/fs, Ripple: ±0.005dB, Attenuation: 100dB**
  - **Short Delay Slow Roll-off, GD=5.0/fs**
  - **Sharp Roll-off**
  - **Slow Roll-off**
  - **Low-dispersion Short Delay Filter**
  - **Super Slow Roll-off**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **2.8 MHz, 5.6 MHz, 11.2 MHz DSD Input Support**
  - **Filter1 (fc = 39 kHz, 2.8 MHz mode)**
  - **Filter2 (fc = 76 kHz, 2.8 MHz mode)**
- **Digital De-emphasis for 32, 44.1and 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step + mute)**
- **Mono Mode**
- **External Digital Filter Interface**
- **Audio I/F Format: 24/32 bit MSB justified, 16/20/24/32 bit LSB justified, I²S, DSD, TDM**
- **Master Clock**
  - **8 kHz ~ 32 kHz: 256 fs or 384 fs or 512 fs or 768 fs or 1024 fs or 1152 fs**
  - **8 kHz ~ 54 kHz: 256 fs or 384 fs or 512 fs or 768 fs**
  - **8 kHz ~ 108 kHz: 256 fs or 384 fs**
  - **108 kHz ~ 216 kHz: 128 fs or 192 fs**
  - **~384 kHz: 32 fs or 48 fs or 64 fs or 96 fs**
  - **~768 kHz: 16 fs or 32 fs or 48 fs or 64 fs**
- **3-wire, I²C-bus Interface**

- **Power Supply:**
  **(by Internal LDO)TVDD=AVDD= 3.0 ~ 3.6V, VDDL/R= 4.75 ~ 5.25V**
  **(by external supply)TVDD=AVDD= (DVDD) ~ 3.6V, DVDD=1.7 ~ 1.98V,**
  **VDDL/R= 4.75 ~ 5.25V**
- **Operational Temperature Rnage: −40 ~ 85 °C**
- **Digital Input Level: CMOS**
- **Package: 96-pin WLCSP**

## 3. Table of Contents

## 4. Block Diagram

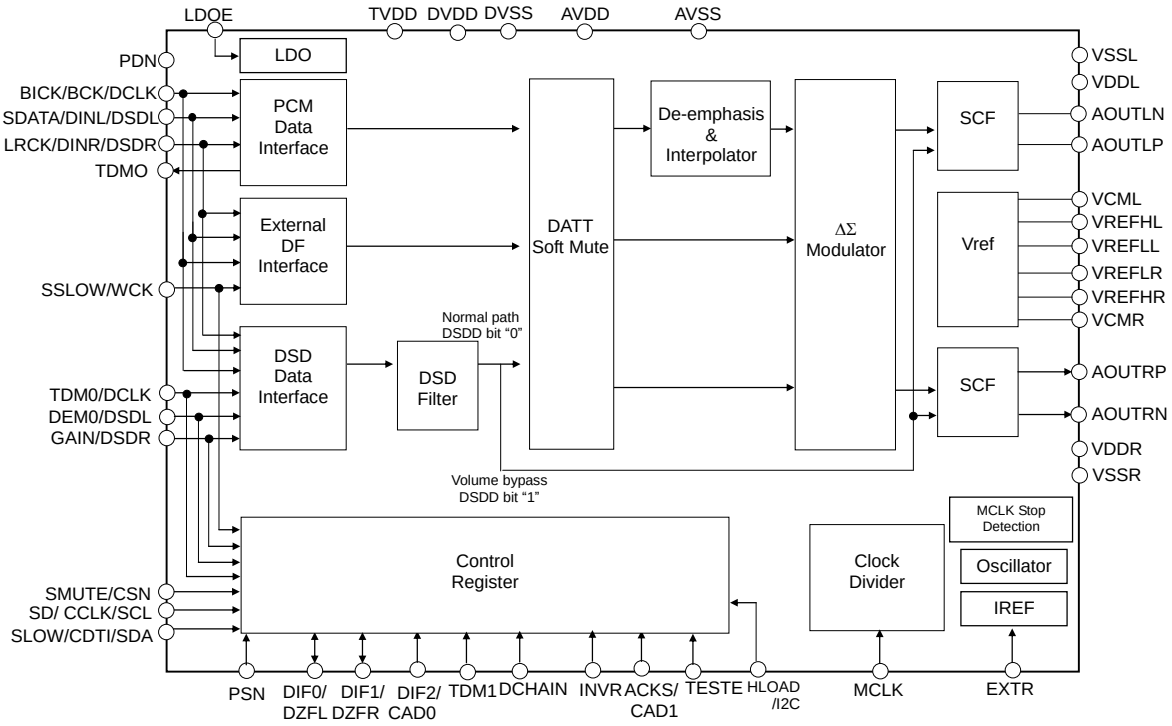
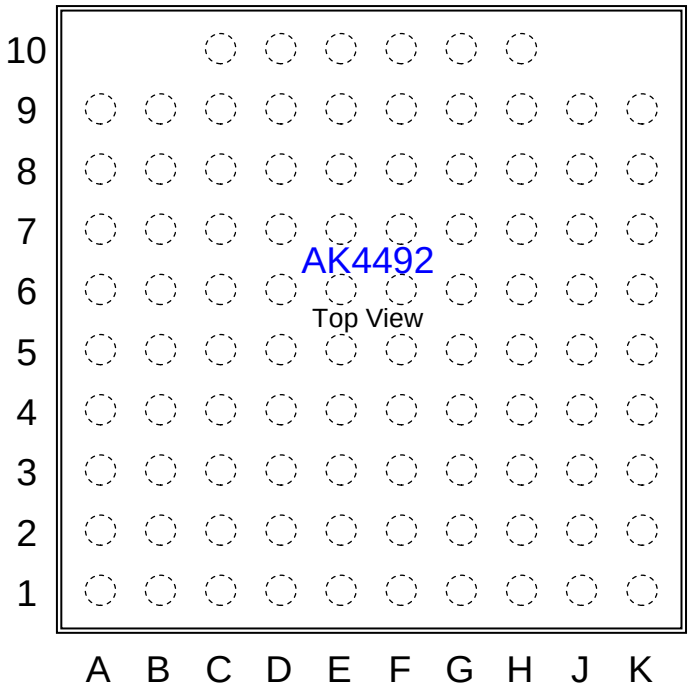



Figure 1. Block Diagram

## 5. Pin Configurations and Functions

### ■ Pin Configurations




| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 10 | | | VDDR | VSSR | VSSR | VSSL | VSSL | VDDL | | |
| 9 | AOUTRN | AOUTRP | VDDR | VDDR | VSSR | VSSL | VDDL | VDDL | AOUTLP | AOUTLN |
| 8 | VREFLR | VCMR | NC | NC | NC | NC | NC | NC | VCML | VREFLL |
| 7 | VREFLR | NC | NC | NC | NC | NC | NC | NC | NC | VREFLL |
| 6 | VREFHR | NC | NC | NC | NC | NC | NC | NC | NC | VREFHL |
| 5 | VREFHR | TESTE | NC | NC | NC | NC | NC | NC | EXTR | VREFHL |
| 4 | INVR | DCHAIN | NC | NC | NC | NC | NC | NC | AVSS | AVDD |
| 3 | TDM0/ DCLK | TDM1 | NC | PSN | NC | NC | NC | LDOE | MCLK | DVDD |
| 2 | ACKS/ CAD1 | GAIN/ DSDR | HLOAD/ I2C | DIF2/ CAD0 | SD/ CCLK/ SCL | TDMO | SSLOW/ WCK | PDN | TVDD | DVSS |
| 1 | NC | DEM0/ DSDL | DIF1/ DZFR | DIF0/ DZFL | SLOW/ CDTI/ SDA | SMUTE/ CSN | LRCK/ DINR/ DSDR | SDATA/ DINL/ DSDL | BICK/ BCK/ DCLK | NC |
| | A | B | C | D | E | F | G | H | J | K |

Figure 2. Pin Configurations

The exposed pad on the bottom surface of the package must be connected to VSS.

## ■ Pin Functions

| No. | Pin Name | I/O | Protection Diode | Function |
|---|---|---|---|---|
| A2 | ACKS | I | TVDD/DVSS | Auto Setting Mode Select Pin in Pin Control Mode (PSN pin = "H")<br>"L": Manual Setting Mode, "H": Auto Setting Mode |
| | CAD1 | I | | Chip Address 1 Pin in Register Control Mode (PSN pin = "L") |
| A3 | TDM0 | I | TVDD/DVSS | TDM Mode Select Pin in Pin Control mode (PSN pin="H") |
| | DCLK | I | | DSD Clock Pin in DSD Mode (PSN pin="L", DSDPATH bit ="0") |
| A4 | INVR | I | TVDD/DVSS | Rch signal Invert pin in Pin Control Mode |
| A5 | VREFHR | I | VDDR/VSSR | Rch High Level Voltage Reference Input Pin |
| A6 | VREFHR | I | VDDR/VSSR | Rch High Level Voltage Reference Input Pin |
| A7 | VREFLR | I | VDDR/VSSR | Rch Low Level Voltage Reference Input Pin |
| A8 | VREFLR | I | VDDR/VSSR | Rch Low Level Voltage Reference Input Pin |
| A9 | AOUTRN | O | VDDR/VSSR | Rch Negative Analog Output Pin |
| B1 | DEM0 | I | TVDD/DVSS | De-emphasis Enable 0 Pin in Pin Control Mode (PSN pin="H") |
| | DSDL | I | | DSD Lch Data Input Pin in DSD Mode (PSN pin = "L", DSDPATH bit = "0") |
| B2 | GAIN | I | TVDD/DVSS | Output Gain Control Pin in Pin Control Mode (PSN pin = "H")<br>"L":Output Level 2.8 Vpp, "H": Output Level 3.75 Vpp |
| | DSDR | I | | DSD Rch Data Input Pin in DSD Mode (PSN pin = "L", DSDPATH bit = "0") |
| B3 | TDM1 | I | TVDD/DVSS | TDM Mode Select Pin in Pin Control Mode |
| B4 | DCHAIN | I | TVDD/DVSS | Daisy Chain Mode Select Pin in Pin Control Mode |
| B5 | TESTE | I | TVDD/DVSS | Test mode Enable Pin(Internal pull-down pin) |
| B8 | VCMR | I | VDDR/VSSR | Right channel Common Voltage Pin,<br>Normally connected to VREFLR with a 1uF electrolytic cap.<br>This pin is inhibited to connect other devices. |
| B9 | AOUTRP | O | VDDR/VSSR | Rch Positive Analog Output Pin |
| C1 | DIF1 | I | TVDD/DVSS | Digital Input Format 1 Pin in Pin Control Mode (PSN pin = "H") |
| | DZFR | O | | Rch Zero Input Detect Pin in Register Control Mode (PSN pin = "L") (Internal pull-down pin) |
| C2 | HLOAD | I | TVDD/DVSS | Heavy Load Mode Enable Pin in Pin Control Mode (PSN pin = "H")<br>"L":Normal Drive Mode, "H": Heavy Load Drive Mode |
| | I2C | I | | Resister Control Interface Pin in Register Control Mode (PSN pin = "L") "L": 3 Wire Serial Mode, "H": $I^2C$-Bus Mode |
| C9 | VDDR | - | - | Rch Analog Power Supply Pin |
| C10 | VDDR | - | - | Rch Analog Power Supply Pin |
| D1 | DIF0 | I | TVDD/DVSS | Digital Input Format 0 Pin in Pin Control Mode (PSN pin = "H") |
| | DZFL | O | | Lch Zero Input Detect Pin in Register Control Mode (PSN pin="L")(Internal pull-down pin) |
| D2 | DIF2 | I | TVDD/DVSS | Digital Input Format 2 Pin in Pin Control Mode (PSN pin = "H") |
| | CAD0 | I | | Chip Address 0 Pin in Register Control Mode (PSN pin = "L") |
| D3 | PSN | I | TVDD/DVSS | Pin Control Mode or Register Control Mode Select Pin<br>(Internal pull-down pin)<br>"L": Register Control Mode, "H": Pin Control Mode |
| D9 | VDDR | - | - | Rch Analog Power Supply Pin |
| D10 | VSSR | - | - | Analog Ground Pin |

| No. | Pin Name | I/O | Protection Diode | Function |
|---|---|---|---|---|
| E1 | SLOW | I | ― /DVSS | Digital Filter Select Pin in Pin Control Mode (PSN pin = “H”) |
| | CDTI | I | | Control Data Input Pin in Register Control Mode (PSN pin = “L”, I2C pin = “L”) |
| | SDA | I/O | | Control Data Input Pin (PSN pin = “L”, I2C pin = “H”) |
| E2 | SD | I | ― /DVSS | Digital Filter Select Pin in Pin Control Mode (PSN pin = “H”) |
| | CCLK | I | | Control Data Clock Pin in Register Control Mode (PSN pin = “L”, I2C pin = “L”) |
| | SCL | I | | Control Data Clock Input Pin (PSN pin = “L”, I2C pin = “H”) |
| E9 | VSSR | - | - | Analog Ground Pin |
| E10 | VSSR | - | - | Analog Ground Pin |
| F1 | SMUTE | I | TVDD/DVSS | Soft Mute Pin in Pin Control Mode (PSN pin = “H”)<br>When this pin is changed to “H”, soft mute cycle is initiated.<br>When returning “L”, the output mute releases. |
| | CSN | I | | Chip Select Pin in Register Control Mode (PSN pin = “L”, I2C pin = “L”) |
| | | | | This Pin should be connected to DVSS (PSN pin = “L”, I2C pin = “H”) |
| F2 | TDMO | O | TVDD/DVSS | Audio Data Onput in Daisy Chain Mode (Internal pull-down pin) |
| F9 | VSSL | - | - | Analog Ground Pin |
| F10 | VSSL | - | - | Analog Ground Pin |
| G1 | LRCK | I | TVDD/DVSS | L/R Clock Pin in PCM Mode |
| | DINR | I | | Rch Audio Data Input Pin in EXDF Mode |
| | DSDR | I | | DSD Rch Data Input Pin in DSD Mode (DSDPATH bit = “1”) |
| G2 | SSLOW | I | TVDD/DVSS | Digital Filter Select Pin in Pin Control Mode (PSN pin= “H”) |
| | WCK | I | | Word Clock input Pin in EXDF Mode (PSN pin = “L”) |
| G9 | VDDL | - | - | Lch Analog Power Supply Pin |
| G10 | VSSL | - | - | Analog Ground Pin |
| H1 | SDATA | I | TVDD/DVSS | Audio Data Input Pin in PCM Mode |
| | DINL | I | | Lch Audio Data Input Pin in EXDF Mode |
| | DSDL | I | | DSD Lch Data Input Pin in DSD Mode (DSDPATH bit = “1”) |
| H2 | PDN | I | TVDD/DVSS | Power-Up, Power-Down Pin<br>When at “L”, the AK4492 is in power-down mode and is held in reset.The AK4492 must always be reset upon power-up. |
| H3 | LDOE | I | TVDD/DVSS | Internal LDO Enable Pin. “L”: Disable, “H”: Enable |
| H9 | VDDL | - | - | Lch Analog Power Supply Pin |
| H10 | VDDL | - | - | Lch Analog Power Supply Pin |
| J1 | BICK | I | TVDD/DVSS | Audio Data Clock Pin in PCM Mode |
| | BCK | I | | Audio Data Clock Pin in EXDF Mode |
| | DCLK | I | | DSD Clock Pin in DSD Mode (DSDPATH bit = “1”) |
| J2 | TVDD | - | - | Digital Power Supply Pin.<br>LDOE pin = “L”: (DVDD) ~ 3.6 V / LDOE pin = “H”: 3.0 ~ 3.6V |
| J3 | MCLK | I | AVDD/AVSS | Master Clock Input Pin |
| J4 | AVSS | - | - | Analog Ground Pin |
| J5 | EXTR | I | VDDL/VSSL | External Resistor Connect Pin<br>Rext=33 kΩ(±1 %, Note 1) toAVSS |
| J8 | VCML | - | VDDL/VSSL | Left channel Common Voltage Pin,<br>Normally connected to VREFLL with a 1 uF electrolytic cap. This pin is inhibited to connect other devices. |
| J9 | AOUTLP | O | VDDL/VSSL | Lch Positive Analog Output Pin |

| No. | Pin Name | I/O | Protection Diode | Function |
|---|---|---|---|---|
| K2 | DVSS | - | - | Digital Ground Pin |
| K3 | DVDD | O | - | (LDOE pin = “H”)<br>LDO Output Pin, This pin should be connected to DVSS with 1.0 µF.<br>This pin is inhibited to connect other devices. |
| | | - | | (LDOE pin = “L”)<br>1.8 V Power Input Pin |
| K4 | AVDD | - | - | Analog Power Supply Pin.<br>LDOE pin = “L”: (DVDD) ~ 3.6 V / LDOE pin = “H”: 3.0 ~ 3.6 V |
| K5 | VREFHL | I | VDDL/VSSL | Lch High Level Voltage Reference Input Pin |
| K6 | VREFHL | I | VDDL/VSSL | Lch High Level Voltage Reference Input Pin |
| K7 | VREFLL | I | VDDL/VSSL | Lch Low Level Voltage Reference Input Pin |
| K8 | VREFLL | I | VDDL/VSSL | Lch Low Level Voltage Reference Input Pin |
| K9 | AOUTLN | O | VDDL/VSSL | Lch Negative Analog Output Pin |

Note 1. It is recommended to use a resistor with 0.1% absolute error in Fs Auto Detect Mode.
Note 2. All input pins except for internal pull-up/down pins must not be left floating.
Note 3. Reset by PDN pin when changing control mode(Pin Control ⇔ Register Control) by PSN pin.
Note 4. PCM mode, DSD mode and EXDF mode are controlled by register settings.

## ■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

(1) Pin Control Mode (PCM mode only)

| Classification | Pin Name | Status |
|---|---|---|
| Analog | AOUTLP, AOUTLN, AOUTRP, AOUTRN | Open |
| | TESTE | Connect to AVSS or Open |

(2) Resister Control Mode

1. PCM Mode

| Classification | Pin Name | Status |
|---|---|---|
| Analog | AOUTLP, AOUTLN, AOUTRP, AOUTRN | Open |
| | TESTE | Connect to AVSS or Open |
| Digital | DCLK, DSDL, DSDR, WCK, TDM1, DCHAIN, INVR | Connect to DVSS |
| | TDMO, DZFR, DZFL | Open |
| | CSN | Connect to DVSS (I2C pin = "H") |

2. DSD Mode

DSDPATH bit = "0"

| Classification | Pin Name | Status |
|---|---|---|
| Analog | AOUTLP, AOUTLN, AOUTRP, AOUTRN | Open |
| | TESTE | Connect to AVSS or Open |
| Digital | WCK, TDM1, DCHAIN, INVR | Connect to DVSS |
| | TDMO, DZFR, DZFL | Open |
| | CSN | Connect to DVSS (I2C pin = "H") |

DSDPATH bit = "1"

| Classification | Pin Name | Status |
|---|---|---|
| Analog | AOUTLP, AOUTLN, AOUTRP, AOUTRN | Open |
| | TESTE | Connect to AVSS or Open |
| Digital | DCLK, DSDL, DSDR, WCK, TDM1, DCHAIN, INVR | Connect to DVSS |
| | TDMO, DZFR, DZFL | Open |
| | CSN | Connect to DVSS (I2C pin = "H") |

3. EXDF Mode

| Classification | Pin Name | Status |
|---|---|---|
| Analog | AOUTLP, AOUTLN, AOUTRP, AOUTRN | Open |
| | TESTE | Connect to AVSS or Open |
| Digital | DCLK, DSDL, DSDR, TDM1, DCHAIN, INVR | Connect to DVSS |
| | TDMO, DZFR, DZFL | Open |
| | CSN | Connect to DVSS (I2C pin = "H") |

4. Pull-up, Pull-down Pin List

| Classification | Pin Name | Status |
|---|---|---|
| Pull-down pin (typ = 100 kΩ) | TDMO, DZFL, DZFR, PSN | DVSS |
| | TESTE | DVSS |

## 6. Absolute Maximum Ratings

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0 V; Note 5)

| Parameter | | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supplies: | Digital I/O | TVDDam | –0.3 | 6.0 | V |
| | Digital Core | DVDDam | –0.3 | 2.5 | V |
| | Clock Ineterface | AVDDam | –0.3 | 6.0 | V |
| | Analog | VDDL/Ram | –0.3 | 6.0 | V |
| | \|AVSS – DVSS\| (Note 6) | ΔGND | - | 0.3 | V |
| Input Current, Any Pin Except Supplies | | IIN | - | ±10 | mA |
| Digital Input Voltage (Note 7) | | VIND | –0.3 | (TVDD+0.3) or 6.0 | V |
| Ambient Temperature (Power supplied) | | Ta | –40 | 85 | °C |
| Storage Temperature | | Tstg | –65 | 150 | °C |

Note 5. All voltages with respect to ground.
Note 6. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.
Note 7. Max value of VIND is lower either of (TVDD + 0.3) or 6.0V.

**WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.**

## 7. Recommended Operating Conditions

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0 V; Note 5)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power Supplies | ■ LDOE pin = "L" | | | | | |
| | Digital I/O | TVDD | DVDD | 1.8 | 3.6 | V |
| | Clock Ineterface | AVDD | DVDD | 1.8 | 3.6 | V |
| | Digital Core | DVDD | 1.7 | 1.8 | 1.98 | V |
| | Analog | VDDL/R | 4.75 | 5.0 | 5.25 | V |
| | ■ LDOE pin = "H" | | | | | |
| | Digital I/O | TVDD | 3.0 | 3.3 | 3.6 | V |
| | Clock Ineterface | AVDD | 3.0 | 3.3 | 3.6 | V |
| | Analog | VDDL/R | 4.75 | 5.0 | 5.25 | V |
| Voltage Reference (Note 8) | "H" voltage reference | VREFHL/R | VDDL/R-0.5 | - | VDDL/R | V |
| | "L" voltage reference | VREFLL/R | - | VSSL/R | - | V |

Note 5. All voltages with respect to ground.
Note 8. The analog output voltage scales with the voltage of (VREFHL/R – VREFLL/R).
Note 9. TVDD and AVDD must be connected to the same ground plane and powered up at the same time. When not using the LDO (LDOE pin = "L"), all power supplies (DVDD (1.8V), TVDD and AVDD (3.3V) and VDDL/R (5V)) should be powered up at the same time or sequentially in the order of 3.3V (TVDD, AVDD), 1.8V (DVDD) and 5V (VDDL/R).
Note 10. The internal LDO outputs DVDD (1.8V) when the LDOE pin = "H". 3.3V (TVDD and AVDD) power supplies must be powered up before or at the same time with 5V (VDDL/R) power supplies when the LDOE pin = "H".

*** AKM assumes no responsibility for the usage beyond the conditions in this data sheet.**

## 8. Electrical Characteristics

### ■ Analog Characteristics

### ■ PCM Mode

(Ta = 25 °C; LDOE pin = “L”, AVDD = TVDD = DVDD = 1.8 V, AVSS = DVSS = VSSL/R = 0 V; VREFHL/R = VDDL/R = 5.0 V, VREFLL/R= 0V; Input data = 24 bit; BICK = 64 fs; Signal Frequency = 1 kHz; Sampling Frequency = 44.1 kHz; Measurement bandwidth = 20 Hz ~ 20 kHz; 2 Vrms output mode (GC[2:0] bits = “000” or GAIN pin = “L”); Heavy load drive mode = off(HLOAD bit = “0” or HLOAD pin = “L”); unless otherwise specified.)

| Parameter | | | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Resolution | | | | | - | - | 32 | Bit |
| **Dynamic Characteristics** (Note 11) | | | | | | | | |
| THD+N | fs=44.1kHz | BW=20kHz | 0dBFS | GC[2:0]= “000” or GAIN=“L” | - | -115 | - | dB |
| | | | | GC[2:0]=“100” or GAIN=“H” | - | -111 | - | dB |
| | | | –60dBFS | | - | -61 | - | dB |
| | fs=96kHz | BW=40kHz | 0dBFS | | - | -111 | - | dB |
| | | | –60dBFS | | - | -57 | - | dB |
| | fs=192kHz | BW=40kHz | 0dBFS | | - | -111 | - | dB |
| | | | –60dBFS | | - | -57 | - | dB |
| | | BW=80kHz | –60dBFS | | - | -52 | - | dB |
| Dynamic Range (–60dBFS with A-weighted) | | | | | - | 123 | - | dB |
| | | | | (Note 12) | - | 127 | - | dB |
| S/N (A-weighted) | GC[2:0]= “000” or GAIN=“L” | | | | - | 123 | - | dB |
| | | | | (Note 12) | - | 127 | - | dB |
| | GC[2:0]= “100” or GAIN=“H” | | | | - | 125 | - | dB |
| | | | | (Note 12) | - | 129 | - | dB |
| Interchannel Isolation (1kHz) | | | | | 110 | 120 | - | dB |
| **DC Accuracy (Note 13)** | | | | | | | | |
| Interchannel Gain Mismatch | | | | | - | 0.15 | 0.3 | dB |
| Gain Drift | | | | | - | 20 | - | ppm/°C |
| Output Voltage | GC[2:0]=“000” or GAIN pin=“L” (Note 14) | | | | ±2.65 | ±2.8 | ±2.95 | Vpp |
| | GC[2:0]=“100” or GAIN pin=“H” (Note 15) | | | | ±3.55 | ±3.75 | ±3.95 | Vpp |
| Load Resistance (Note 16) | HLOAD=“0” or HLOAD pin=“L” | | | | 400 | - | - | Ω |
| | HLOAD=“1” or HLOAD pin=“H” | | | | 300 | - | - | Ω |
| Load Capacitance | | | | (Note 17) | - | - | 25 | pF |

Note 11. Measured by Audio Precision APx555. Averaging mode.

Note 12. The value of as IC single AK4492. It is a calculated value to remove the noise of External Circuit Figure 77 and the measuring instrument.

Note 13. The value of as IC single AK4492.

Note 14. The analog output voltage with 0dBFS input signal when GC[2:0] bits = “000” or the GAIN pin = “L” is calculated by the following formula.

AOUTL/R (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFHL/R – VREFLL/R)/5.

Note 15. The analog output voltage with 0dBFS input signal when GC[2:0] bits = “100” or the GAIN pin = “H” is calculated by the following formula.

AOUTL/R (typ.@0dB) = (AOUT+) – (AOUT–) = ±3.75Vpp × (VREFHL/R – VREFLL/R)/5.

Note 16. The load resistance value with respect to ground. 10.3 System Design Analog Output shows the circuits and the calculataion example.

Note 17. The load capacitance value with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.

Note 18. It is recommended to use a resistor with 0.1% absolute error for the output stage of the adding circuit.

(Ta = 25 °C; LDOE pin = “L”, AVDD = TVDD = DVDD = 1.8 V, AVSS = DVSS = VSSL/R = 0 V; VREFHL/R = VDDL/R = 5.0 V, VREFLL/R = 0V; Input data = 24 bit; BICK = 64 fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; 2 Vrms output mode (GC[2:0] bits = “000” or GAIN pin = “L”); Heavy load drive mode = off(HLOAD bit=“0” or HLOAD pin=“L”); unless otherwise specified.)

| **Power Supplies** | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Power Supply Current | | | | |
| Normal operation (PDN pin = “H”) | | | | |
| VDDL+VDDR | - | 27 | 40 | mA |
| VREFHL+VREFHR | - | 1.6 | 3 | mA |
| AVDD | - | 0.4 | 1.5 | mA |
| TVDD | | | | |
| LDOE pin = “H” fs = 44.1 kHz | | 6 | 9 | mA |
| LDOE pin = “H” fs = 96 kHz | - | 10 | 15 | mA |
| LDOE pin = “H” fs = 192 kHz | - | 18 | 27 | mA |
| LDOE pin = “L” | - | 0.3 | 1.5 | mA |
| DVDD | | | | |
| LDOE pin = “L” fs = 44.1 kHz | - | 6 | 9 | mA |
| LDOE pin = “L” fs = 96 kHz | - | 10 | 15 | mA |
| LDOE pin = “L” fs = 192 kHz | - | 18 | 27 | mA |
| Total Idd (fs = 44.1 kHz, LDOE pin = “L”) | - | 35.4 | 55 | mA |
| Power down (PDN pin = “L”) (Note 19) TVDD + AVDD + VDDL + VDDR + DVDD | - | 0.4 | 100 | μA |

Note 19. In power down mode, the PSN pin = TVDD and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held to DVSS.

Note 20. The DVDD pin becomes an output pin when the LDOE pin = “H”.

## ■ DSD Mode

(Ta = 25 °C; LDOE pin = “L”, AVDD = TVDD = DVDD = 1.8 V; AVSS = DVSS = VSSL/R = 0 V; VREFHL/R = VDDL/R = 5.0 V, VREFLL/R = 0 V; Signal Frequency = 1 kHz; Measurement bandwidth = 20 Hz ~ 20 kHz; External Circuit: Figure 77; 2 Vrms output mode (GC[2:0] bits = “000” or GAIN pin = “L”); unless otherwise specified.)

| Parameter | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Dynamic Characteristics** | | | | | | |
| THD+N (Note 21) | DSD data stream: 2.8224 MHz | 0dB | - | -111 | - | dB |
| | DSD data stream: 5.6448 MHz | 0dB | - | -112 | - | dB |
| | DSD data stream: 11.2896 MHz | 0dB | - | -107 | - | dB |
| S/N (A-weighted, Normal path) (Note 21) | DSD data stream: 2.8224 MHz | Digital“0” (Note 24) | - | 123 | - | dB |
| | DSD data stream: 5.6448 MHz | Digital“0” (Note 24) | - | 123 | - | dB |
| | DSD data stream: 11.2896 MHz | Digital“0” (Note 24) | - | 123 | - | dB |
| **DC Accuracy** | | | | | | |
| Output Voltage (Normal path) | | (Note 25) | ±2.65 | ±2.8 | ±2.95 | Vpp |
| Output Voltage (Volume Bypass) | | (Note 25) | ±2.38 | ±2.5 | ±2.63 | Vpp |

Note 21. References values in using AK4137 as the input source. This value does not change by increasimg the signal amplitude with gain adjustment function.

Note 22. The peak level of DSD signal should be in the range of 25% ~ 75% duty according to the SACD format book (Scarlet Book).

Note 23. The output level is assumed as 0dB when a 1kHz 25% ~ 75% duty sine wave is input. Click noise may occur if the input signal exceeds 0dB.

Note 24. Digital “0” is a digital zero code pattern (“01101001”) according to the SACD format book (Scarlet Book).

Note 25. In case of GC[2:0] = “000” and DSDD bit = “1”, the analog output voltage at input signal = 0dB is following equation.

AOUTL/R (typ.@0 dB) = (AOUTLP/RP) − (AOUTLN/RN) = ±2.5 Vpp × (VREFHL/R − VREFLL/R)/5

.

## ■ Sharp Roll-Off Filter Characteristics

### Sharp Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta = -40~85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7 ~ 1.98 V; Normal Speed Mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin ="0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency Response | ±0.01 dB<br>−6.0 dB (Note 26) | -<br>- | 0<br>- | <br>22.05 | 20.0<br>- | kHz<br>kHz |
| Passband | (Note 27) | PB | 0 | | 20.0 | kHz |
| Stopband | (Note 27) | SB | 24.1 | | | kHz |
| Passband Ripple | (Note 28) | PR | | | ±0.005 | dB |
| Stopband Attenuation | (Note 26) | SA | 100 | | | dB |
| Group Delay | (Note 29) | GD | - | 29.2 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 20.0 kHz | | | -0.7 | - | +0.1 | dB |

### Sharp Roll-Off Filter Characteristics (fs=96kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6V, DVDD = 1.7~1.98V; Double Speed Mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency Response | ±0.01dB<br>−6.0 dB (Note 26) | -<br>- | 0<br>- | <br>48.0 | 43.5<br>- | kHz<br>kHz |
| Passband | (Note 27) | PB | 0 | | 43.5 | kHz |
| Stopband | (Note 27) | SB | 52.5 | | | kHz |
| Passband Ripple | (Note 28) | PR | | | ±0.005 | dB |
| Stopband Attenuation | (Note 26) | SA | 100 | | | dB |
| Group Delay | (Note 29) | GD | - | 29.2 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 40.0 kHz | | | -1.9 | - | +0.1 | dB |

### Sharp Roll-Off Filter Characteristics (fs=192kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency Responce | ±0.01 dB<br>−6.0 dB (Note 26) | -<br>- | 0<br>- | <br>96.0 | 87.0<br>- | kHz<br>kHz |
| Passband | (Note 27) | PB | 0 | | 87.0 | kHz |
| Stopband | (Note 27) | SB | 104.9 | | | kHz |
| Passband Ripple | (Note 28) | PR | | | ±0.005 | dB |
| Stopband Attenuation | (Note 26) | SA | 100 | | | dB |
| Group Delay | (Note 29) | GD | - | 29.2 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 80.0kHz | | | -5.0 | - | +0.1 | dB |

Note 26. Frequency response refers to the output level (0dB) of a 1kHz, 0dB sine wave input.

Note 27. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 28. The first stage of the Interpolator. This is a passband gain amplitude of the 4 times oversampling filter.

Note 29. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

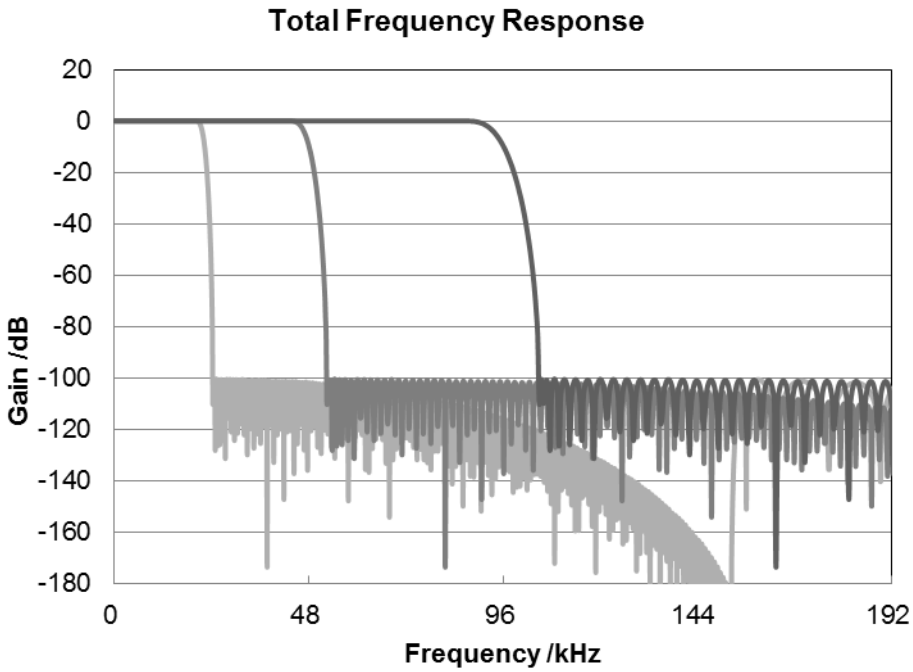



Figure 3. Sharp Roll-off Filter Frequency Response

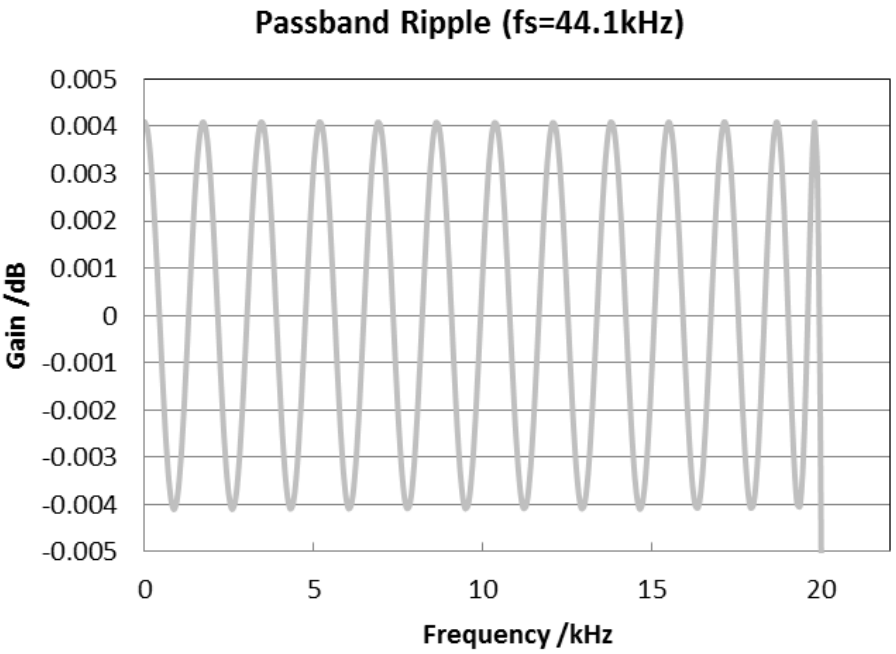



Figure 4. Sharp Roll-off Filter Passband Ripple

## ■ Slow Roll-Off Filter Characteristics

**Slow Roll-Off Filter Characteristics (fs = 44.1kHz)**

(Ta = -40 ~ 85° C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Normal Speed Mode; DEM = OFF; SD bit or SD pin = “0”, SLOW bit or SLOW pin = “1”, SSLOW bit or SSLOW pin = “0”)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency Response | ±0.01dB<br>−6.0dB (Note 26) | -<br>- | 0<br>- | <br>21.0 | 8.0<br>- | kHz<br>kHz |
| Passband | (Note 30) | PB | 0 | | 8.0 | kHz |
| Stopband | (Note 30) | SB | 39.2 | | | kHz |
| Passband Ripple | (Note 28) | PR | | | ±0.007 | dB |
| Stopband Attenuation | (Note 26) | SA | 92 | | | dB |
| Group Delay | (Note 29) | GD | - | 6.5 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 20.0 kHz | | | -5.5 | - | +0.1 | dB |

**Slow Roll-Off Filter Characteristics (fs = 96kHz)**

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Double Speed Mode; DEM = OFF; SD bit or SD pin = “0”, SLOW bit or SLOW pin = “1”, SSLOW bit or SSLOW pin = “0”)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency Responce | ±0.01 dB<br>−6.0 dB (Note 26) | -<br>- | 0<br>- | <br>45.6 | 17.6<br>- | kHz<br>kHz |
| Passband | (Note 30) | PB | 0 | | 17.6 | kHz |
| Stopband | (Note 30) | SB | 85.4 | | | kHz |
| Passband Ripple | (Note 28) | PR | | | ±0.007 | dB |
| Stopband Attenuation | (Note 26) | SA | 100 | | | dB |
| Group Delay | (Note 29) | GD | - | 6.5 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 40.0 kHz | | | -5.1 | - | +0.1 | dB |

**Slow Roll-Off Filter Characteristics (fs = 192kHz)**

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit or SD pin = “0”, SLOW bit or SLOW pin = “1”, SSLOW bit or SSLOW pin = “0”)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency Responce | ±0.01 dB<br>−6.0 dB (Note 26) | -<br>- | 0<br>- | <br>91.2 | 35.2<br>- | kHz<br>kHz |
| Passband | (Note 30) | PB | 0 | | 35.2 | kHz |
| Stopband | (Note 30) | SB | 170.7 | | | kHz |
| Passband Ripple | (Note 28) | PR | | | ±0.007 | dB |
| Stopband Attenuation | (Note 26) | SA | 100 | | | dB |
| Group Delay | (Note 29) | GD | - | 6.5 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 80.0kHz | | | -8.0 | - | +0.1 | dB |

Note 30. The passband and stopband frequencies scale with fs. For example, PB = 0.1836 × fs (@±0.01dB), SB = 0.8889 × fs.

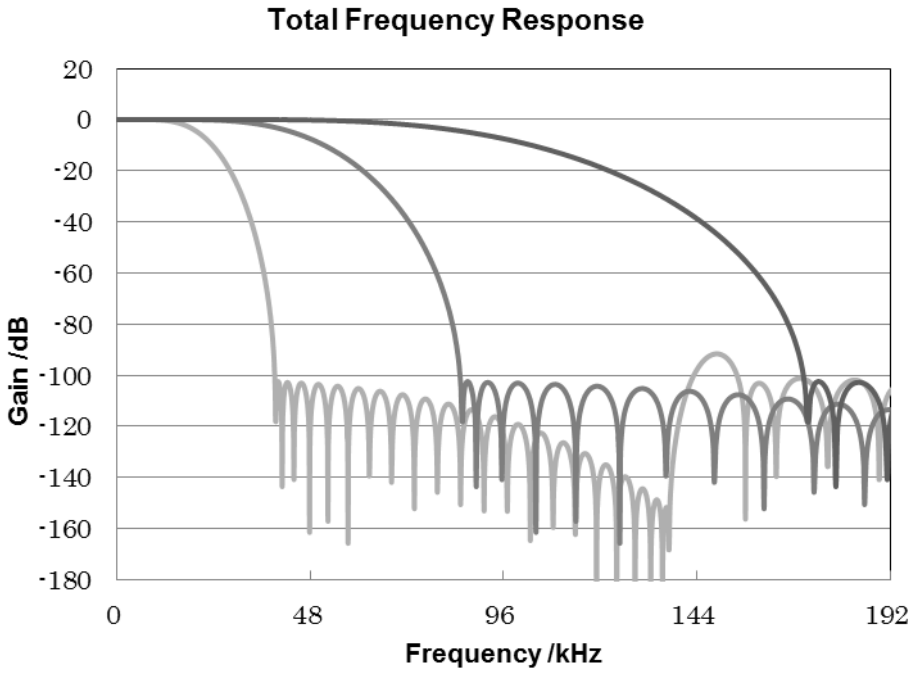



Figure 5. Slow Roll-off Filter Frequency Response

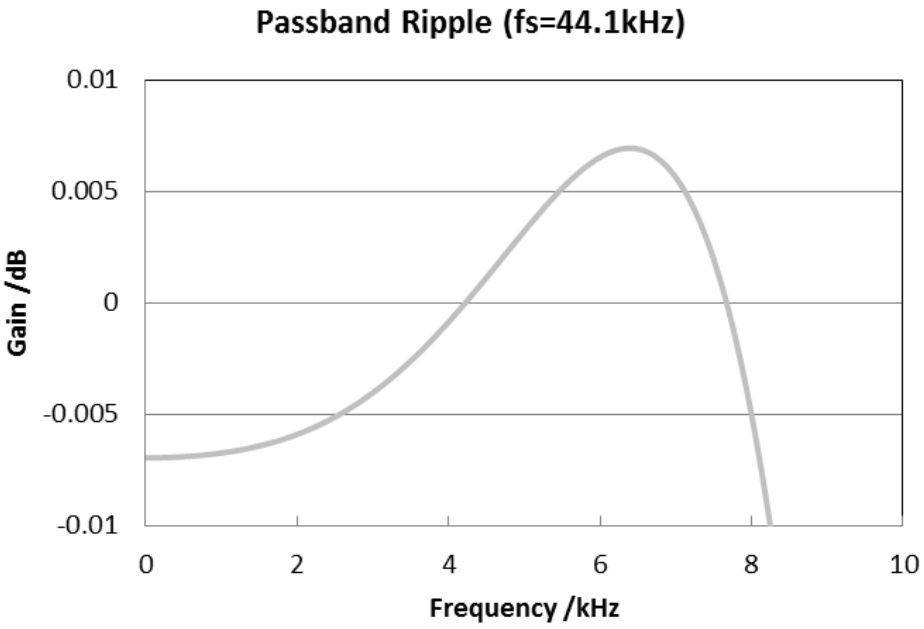



Figure 6. Slow Roll-off Filter Passband Ripple

## ■ Short Delay Sharp Roll-Off Filter Characteristics

**Short Delay Sharp Roll-Off Filter Characteristics (fs = 44.1kHz)**

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Normal Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency | ±0.01 dB | - | 0 | | 20.0 | kHz |
| Responce | −6.0 dB (Note 26) | - | - | 22.05 | - | kHz |
| Passband (Note 31) | | PB | 0 | | 20.0 | kHz |
| Stopband (Note 31) | | SB | 24.1 | | | kHz |
| Passband Ripple (Note 30) | | PR | | | ±0.005 | dB |
| Stopband Attenuation (Note 26) | | SA | 100 | | | dB |
| Group Delay (Note 29) | | GD | - | 6.0 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 20.0 kHz | | | -0.7 | - | +0.1 | dB |

**Short Delay Sharp Roll-Off Filter Characteristics (fs = 96kHz)**

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Double Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency | ±0.01 dB | - | 0 | | 43.5 | kHz |
| Responce | −6.0 dB (Note 26) | - | - | 48.0 | - | kHz |
| Passband (Note 31) | | PB | 0 | | 43.5 | kHz |
| Stopband (Note 31) | | SB | 52.5 | | | kHz |
| Passband Ripple (Note 28) | | PR | | | ±0.005 | dB |
| Stopband Attenuation (Note 26) | | SA | 100 | | | dB |
| Group Delay (Note 29) | | GD | - | 6.0 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 40.0 kHz | | | -1.9 | - | +0.1 | dB |

**Short Delay Sharp Roll-Off Filter Characteristics (fs = 192kHz)**

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency | ±0.01 dB | - | 0 | | 87.0 | kHz |
| Responce | −6.0 dB (Note 26) | - | - | 96.0 | - | kHz |
| Passband (Note 31) | | PB | 0 | | 87.0 | kHz |
| Stopband (Note 31) | | SB | 104.9 | | | kHz |
| Passband Ripple (Note 28) | | PR | | | ±0.005 | dB |
| Stopband Attenuation (Note 26) | | SA | 100 | | | dB |
| Group Delay (Note 29) | | GD | - | 6.0 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 80.0 kHz | | | -5.0 | - | +0.1 | dB |

Note 31. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

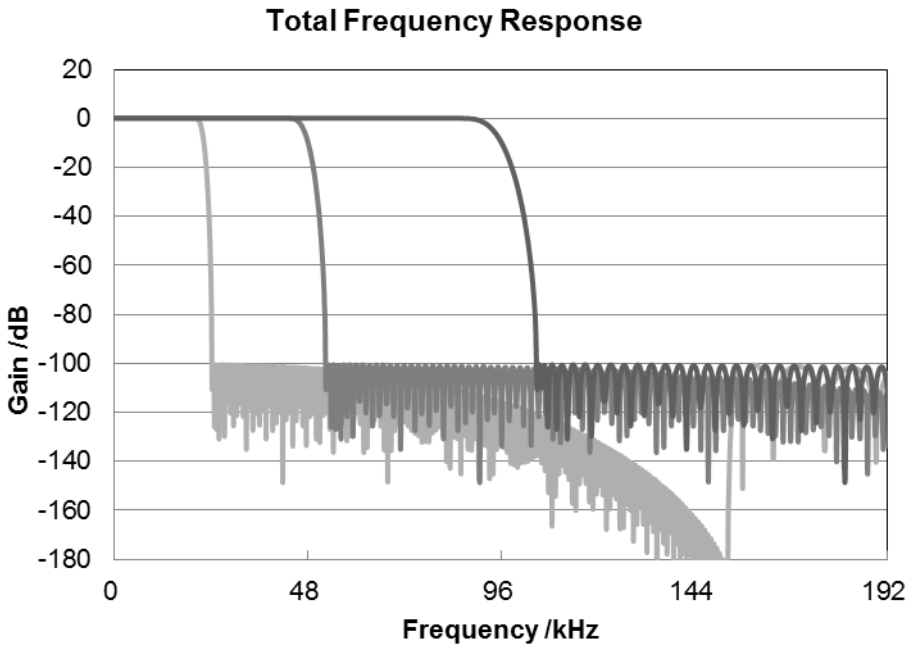



Figure 7. Short Delay Sharp Roll-off Filter Frequency Response

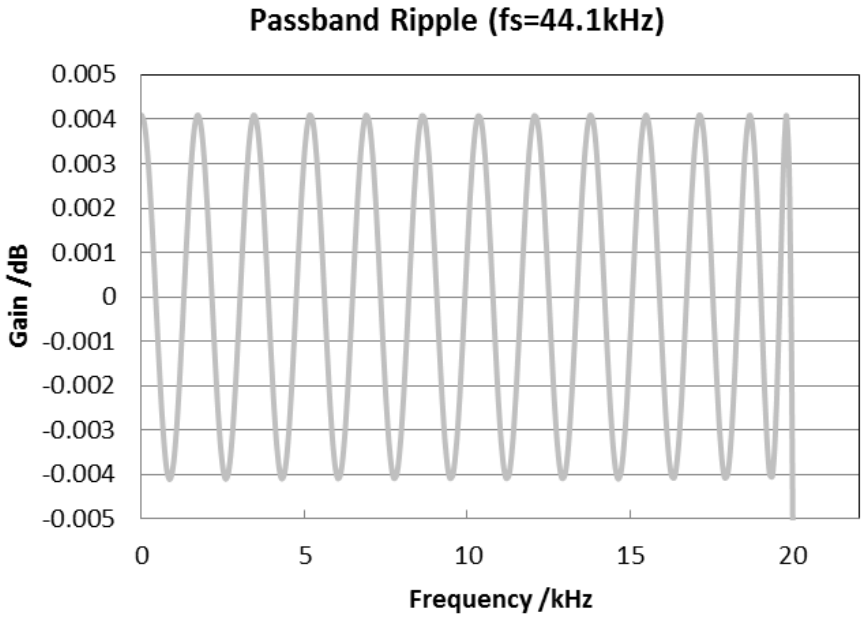



Figure 8. Short Delay Sharp Roll-off Filter Passband Ripple

## ■ Short Delay Slow Roll-Off Filter Characteristics

**Short Delay Slow Roll-Off Filter Characteristics (fs = 44.1kHz)**

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Normal Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency | ±0.01 dB | - | 0 | | 8.0 | kHz |
| Responce | −6.0 dB (Note 26) | - | - | 21.0 | - | kHz |
| Passband (Note 32) | | PB | 0 | | 8.0 | kHz |
| Stopband (Note 32) | | SB | 39.2 | | | kHz |
| Passband Ripple (Note 28) | | PR | | | ±0.007 | dB |
| Stopband Attenuation (Note 26) | | SA | 92 | | | dB |
| Group Delay (Note 29) | | GD | - | 5.0 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 20.0 kHz | | | -5.5 | - | +0.1 | dB |

**Short Delay Slow Roll-Off Filter Characteristics (fs = 96kHz)**

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Double Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency | ±0.01 dB | - | 0 | - | 17.6 | kHz |
| Response | −6.0 dB (Note 26) | - | - | 45.6 | - | kHz |
| Passband (Note 32) | | PB | 0 | - | 17.6 | kHz |
| Stopband (Note 32) | | SB | 85.4 | - | - | kHz |
| Passband Ripple (Note 28) | | PR | - | - | ±0.007 | dB |
| Stopband Attenuation (Note 26) | | SA | 100 | - | - | dB |
| Group Delay (Note 29) | | GD | - | 5.0 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 40.0 kHz | | | -5.1 | - | +0.1 | dB |

**Short Delay Slow Roll-Off Filter Characteristics (fs = 192kHz)**

(Ta = -40 ~ 85 °C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency | ±0.01 dB | - | 0 | - | 35.2 | kHz |
| Response | −6.0 dB (Note 26) | - | - | 91.2 | - | kHz |
| Passband (Note 32) | | PB | 0 | - | 35.2 | kHz |
| Stopband (Note 32) | | SB | 170.7 | - | - | kHz |
| Passband Ripple (Note 28) | | PR | - | - | ±0.007 | dB |
| Stopband Attenuation (Note 26) | | SA | 100 | - | - | dB |
| Group Delay (Note 29) | | GD | - | 5.0 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 80.0 kHz | | | -8.0 | - | +0.1 | dB |

Note 32. The passband and stopband frequencies scale with fs. For example, PB = 0.1836 × fs (@±0.01dB), SB = 0.8866 × fs.

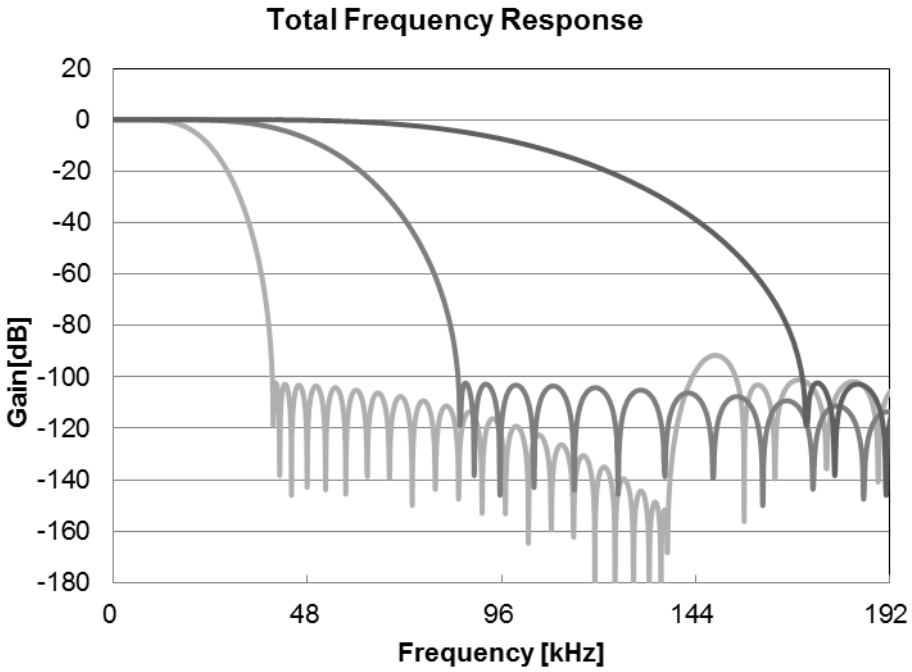



Figure 9. Short Delay Slow Roll-off Filter Frequency Response

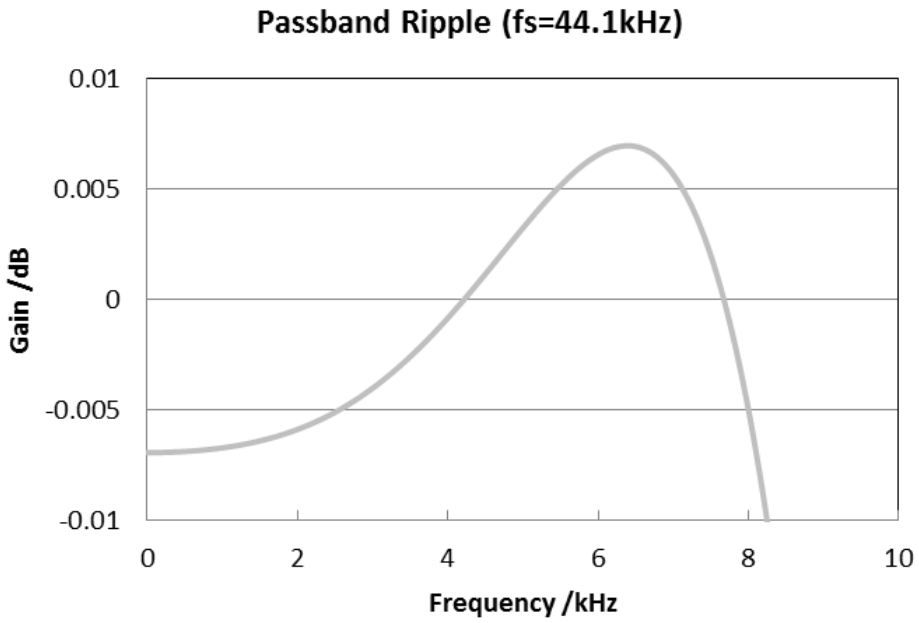



Figure 10. Short Delay Slow Roll-off Filter Passband Ripple

## ■ Low-dispersion Short Delay Filter Characteristics

### Low-dispersion Short Delay Filter Characteristics (fs = 44.1kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Normal Speed Mode; DEM = OFF; SD bit pr SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "1")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency Response | ±0.05 dB<br>−6.0 dB (Note 26) | -<br>- | 0<br>- | -<br>22.05 | 18.4<br>- | kHz<br>kHz |
| Passband | (Note 33) | PB | 0 | - | 18.4 | kHz |
| Stopband | (Note 33) | SB | 25.7 | - | - | kHz |
| Passband Ripple | (Note 33) | PR | - | - | ±0.05 | dB |
| Stopband Attenuation | (Note 26) | SA | 80 | - | - | dB |
| Group Delay | (Note 29) | GD | - | 10.0 | - | 1/fs |
| Group Delay Distortion | | ΔGD | - | ±0.035 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 20.0 kHz | | | -1.2 | - | +0.1 | dB |

### Low-dispersion Short Delay Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Double Speed Mode; DEM = OFF; SD bit pr SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "1")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency Response | ±0.05 dB<br>−6.0 dB (Note 26) | -<br>- | 0<br>- | -<br>48.0 | 40.1<br>- | kHz<br>kHz |
| Passband | (Note 33) | PB | 0 | - | 40.1 | kHz |
| Stopband | (Note 33) | SB | 55.9 | - | - | kHz |
| Passband Ripple | (Note 28) | PR | - | - | ±0.05 | dB |
| Stopband Attenuation | (Note 26) | SA | 80 | - | - | dB |
| Group Delay | (Note 29) | GD | - | 10.0 | - | 1/fs |
| Group DelayDistortion | | ΔGD | - | ±0.035 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 40.0 kHz | | | -1.9 | - | +0.1 | dB |

### Low-dispersion Short Delay Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit pr SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "1")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Frequency Response | ±0.05 dB<br>−6.0 dB (Note 26) | -<br>- | 0<br>- | -<br>96.0 | 80.2<br>- | kHz<br>kHz |
| Passband | (Note 33) | PB | 0 | - | 80.2 | kHz |
| Stopband | (Note 33) | SB | 111.8 | - | - | kHz |
| Passband Ripple | (Note 28) | PR | - | - | ±0.05 | dB |
| Stopband Attenuation | (Note 26) | SA | 80 | - | - | dB |
| Group Delay | (Note 29) | GD | - | 10.0 | - | 1/fs |
| Group Delay Distortion | | ΔGD | - | ±0.035 | - | 1/fs |
| **Digital Filter + SCF** (Note 26) | | | | | | |
| Frequency Response: 0 ~ 80.0 kHz | | | -5.0 | - | +0.1 | dB |

Note 33. The passband and stopband frequencies scale with fs. For example, PB = 0.418 × fs (@±0.05dB), SB = 0.582 × fs.

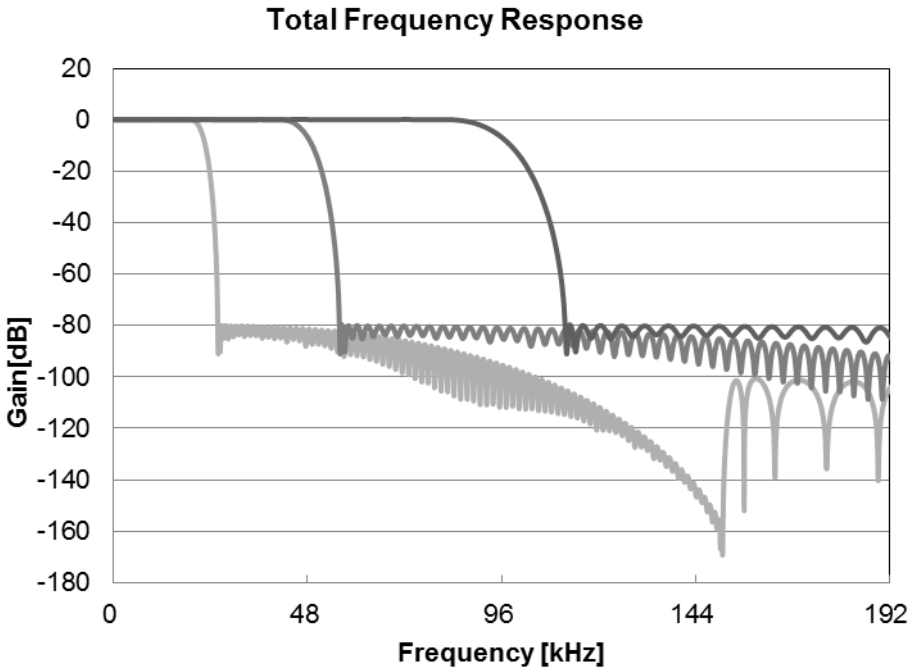



Figure 11. Low Dispersion Shortdelay Filter Frequency Responce

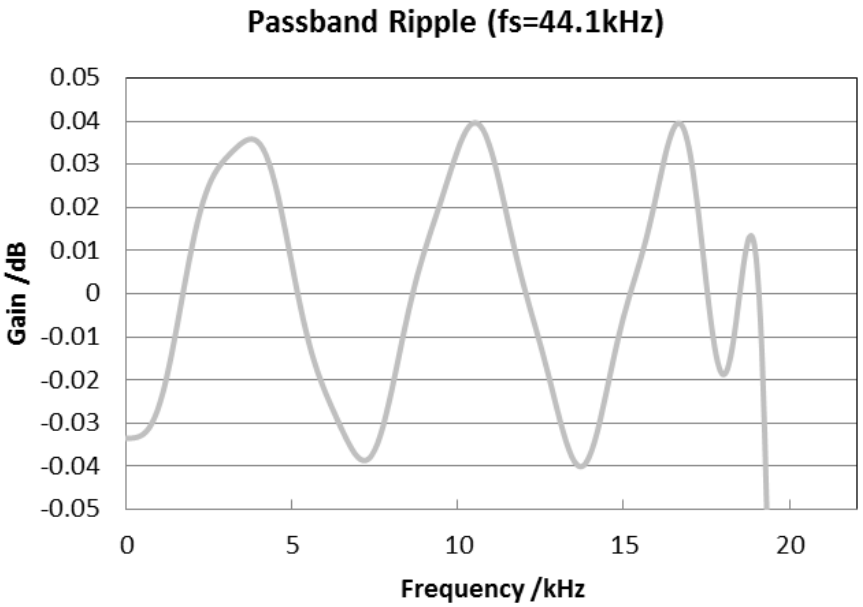



Figure 12. Low Dispersion Shortdelay Filter PassbandRipple

## ■ DSD Filter Characteristics

(Ta = -40 ~ 85 °C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; fs = 44.1 kHz; DP bit = "1", DSDSEL[1:0] bits = "00")

| Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Digital Filter Response** (Note 34) | | | | | |
| DSDF bit = "0" | 20 kHz | - | -0.77 | - | dB |
| | 50 kHz | - | -5.25 | - | dB |
| | 100 kHz | - | -18.80 | - | dB |
| DSDF bit = "1" | 20 kHz | - | -0.19 | - | dB |
| | 100 kHz | - | -5.29 | - | dB |
| | 150 kHz | - | -15.57 | - | dB |

Note 34. 0dB is the output level when a 1kHz 25% ~ 75% duty sibne wave is input.

Note 35. The frequency(20 k,100 k,150 kHz) is doubled in 128 fs(DSDSEL[1:0] bits = "01"), and it is four times in 256 fs(DSDSEL[1:0] bits = "10").

## ■ DC Characteristics

(Ta = -40 ~ 85 °C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = 1.7~3.6 V, DVDD = 1.7~1.98 V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| AVDD=TVDD=1.7 ~ 3.0 V | | | | | |
| High-Level Input Voltage | VIH | 80%TVDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 20%TVDD | V |
| AVDD=TVDD=3.0V ~ 3.6 V | | | | | |
| High-Level Input Voltage | VIH | 70%TVDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 30%TVDD | V |
| High-Level Output Voltage (TDMO, DZFL, DZFR pins: Iout = -100 µA) | VOH | TVDD−0.5 | - | - | V |
| Low-Level Output Voltage (except SDA pin: Iout= 100µA) | VOL | - | - | 0.5 | V |
| (SDA pin, 2.0 V ≤ TVDD ≤ 3.6 V: Iout = 3mA) | VOL | - | - | 0.4 | V |
| (SDA pin, 1.7 V ≤ TVDD ≤ 2.0 V: Iout = 3mA) | VOL | - | - | 20%TVDD | V |
| Input Leakage Current (Note 36) | Iin | - | - | ±10 | µA |

Note 36. The TESTE, TDMO, PSN, DIF0 and DIF1 pins have internal pull-down. The value of resistance is 100 kohm(typical).Therefore the TESTE, TDMO, PSN, DIF0 and DIF1 pins are not included in this specification.

## ■ Switching Characteristics

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = 1.7~3.6V, DVDD = 1.7~1.98 V, $C_L$ = 20 pF)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Master Clock Timing** | | | | | |
| Frequency | fCLK | 2.048 | - | 49.152 | MHz |
| Duty Cycle | dCLK | 40 | - | 60 | % |
| Minimum Pulse Width | tCLKH | 9.155 | - | - | nsec |
| | tCLKL | 9.155 | - | - | nsec |
| **LRCK Clock Timing** (Note 37) | | | | | |
| **Normal Mode (TDM[1:0] bits = "00")** | | | | | |
| Normal Speed Mode | fsn | 8 | - | 54 | kHz |
| Double Speed Mode | fsd | 54 | - | 108 | kHz |
| Quad Speed Mode | fsq | 108 | - | 216 | kHz |
| Oct speed mode | fso | 216 | - | 388 | kHz |
| Hex speed mode | fsh | 388 | - | 776 | kHz |
| Duty Cycle | Duty | 45 | - | 55 | % |
| **TDM128 mode (TDM[1:0] bits = "01")** | | | | | |
| Normal Speed Mode | fsn | 8 | - | 54 | kHz |
| Double Speed Mode | fsd | 54 | - | 108 | kHz |
| Quad Speed Mode | fsq | 108 | - | 216 | kHz |
| High time | tLRH | 1/128fs | - | - | nsec |
| Low time | tLRL | 1/128fs | - | - | nsec |
| **TDM256 mode (TDM[1:0] bits = "10")** | | | | | |
| Normal Speed Mode High time | fsn | 8 | - | 54 | kHz |
| Double Speed Mode | fsd | 54 | - | 108 | kHz |
| High time | tLRH | 1/256fs | - | - | nsec |
| Low time | tLRL | 1/256fs | - | - | nsec |
| **TDM512 mode (TDM[1:0] bits = "11")** | | | | | |
| Normal Speed Mode | fsn | 8 | - | 54 | kHz |
| High time | tLRH | 1/512fs | - | - | nsec |
| Low time | tLRL | 1/512fs | - | - | nsec |

Note 37. The MCLK frequency must be changed while the AK4492 is in reset state by setting the PDN pin = "L" or RSTN bit = "0".

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, TVDD = AVDD = (DVDD) ~ 3.6V, DVDD = 1.7~1.98 V, $C_L$ = 20 pF, PSN pin = "L", AFSD bit = "1")

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Master Clock Timing (FS Auto Detect Mode)** | | | | | |
| Frequency | fCLK | 7.68 | - | 49.152 | MHz |
| Duty Cycle | dCLK | 40 | - | 60 | % |
| Minimum Pulse Width | tCLKH | 9.155 | - | - | nsec |
| | tCLKL | 9.155 | - | - | nsec |
| **LRCK Clock Timing (FS Auto Detect Mode)** (Note 38) | | | | | |
| **Normal Mode (TDM[1:0] bits = "00")** | | | | | |
| Normal Speed Mode | fsn | 30 | - | 54 | kHz |
| Double Speed Mode | fsd | 87 | - | 108 | kHz |
| Quad Speed Mode | fsq | 174 | - | 216 | kHz |
| Oct speed mode | fso | 348 | - | 388 | kHz |
| Hex speed mode | fsh | 696 | - | 776 | kHz |
| Duty Cycle | Duty | 45 | - | 55 | % |
| **TDM128 mode (TDM[1:0] bits = "01")** | | | | | |
| Normal Speed Mode | fsn | 30 | - | 54 | kHz |
| Double Speed Mode | fsd | 87 | - | 108 | kHz |
| Quad Speed Mode | fsq | 174 | - | 216 | kHz |
| High time | tLRH | 1/128fs | - | - | nsec |
| Low time | tLRL | 1/128fs | - | - | nsec |
| **TDM256 mode (TDM[1:0] bits = "10")** | | | | | |
| Normal Speed Mode High time | fsn | 30 | - | 54 | kHz |
| Double Speed Mode | fsd | 87 | - | 108 | kHz |
| High time | tLRH | 1/256fs | - | - | nsec |
| Low time | tLRL | 1/256fs | - | - | nsec |
| **TDM512 mode (TDM[1:0] bits = "11")** | | | | | |
| Normal Speed Mode | fsn | 30 | - | 54 | kHz |
| High time | tLRH | 1/512fs | - | - | nsec |
| Low time | tLRL | 1/512fs | - | - | nsec |

Note 38. Normal operation is not guaranteed if a frequency not shown above is input to the LRCK when the AK4492 is in Sampling Frequency Auto Detect Mode.

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **PCM Audio Interface Timing** | | | | | | |
| **Normal Mode (TDM[1:0] bits = "00")** | | | | | | |
| BICK Period | | | | | | |
| Normal Speed Mode | | tBCK | 1/256fsn | - | - | nsec |
| Double Speed Mode | | tBCK | 1/128fsd | - | - | nsec |
| Quad Speed Mode | | tBCK | 1/64fsq | - | - | nsec |
| Oct speed mode | | tBCK | 1/64fso | - | - | nsec |
| Hex speed mode | | tBCK | 1/64fsh | - | - | nsec |
| BICK Pulse Width Low | | tBCKL | 9 | - | - | nsec |
| BICK Pulse Width High | | tBCKH | 9 | - | - | nsec |
| BICK "↑" to LRCK Edge | (Note 39) | tBLR | 5 | - | - | nsec |
| LRCK Edge to BICK "↑" | (Note 39) | tLRB | 5 | - | - | nsec |
| SDATA Hold Time | | tSDH | 5 | - | - | nsec |
| SDATA Setup Time | | tSDS | 5 | - | - | nsec |
| **TDM128 mode (TDM[1:0] bits = "01")** | | | | | | |
| BICK Period | | | | | | |
| Normal Speed Mode | | tBCK | 1/128fsn | - | - | nsec |
| Double Speed Mode | | tBCK | 1/128fsd | - | - | nsec |
| Quad Speed Mode | | tBCK | 1/128fsq | - | - | nsec |
| BICK Pulse Width Low | | tBCKL | 14 | - | - | nsec |
| BICK Pulse Width High | | tBCKH | 14 | - | - | nsec |
| BICK "↑" to LRCK Edge | (Note 39) | tBLR | 14 | - | - | nsec |
| LRCK Edge to BICK "↑" | (Note 39) | tLRB | 14 | - | - | nsec |
| SDATA Hold Time | | tSDH | 5 | - | - | nsec |
| SDATA Setup Time | | tSDS | 5 | - | - | nsec |
| **TDM256 mode (TDM[1:0] bits = "10")** | | | | | | |
| BICK Period | | | | | | |
| Normal Speed Mode | | tBCK | 1/256fsn | - | - | nsec |
| Double Speed Mode | (Note 40) | tBCK | 1/256fsd | - | - | nsec |
| BICK Pulse Width Low | | tBCKL | 14 | - | - | nsec |
| BICK Pulse Width High | | tBCKH | 14 | - | - | nsec |
| BICK "↑" to LRCK Edge | (Note 39) | tBLR | 14 | - | - | nsec |
| LRCK Edge to BICK "↑" | (Note 39) | tLRB | 14 | - | - | nsec |
| TDMO Setup time BICK "↑" | | tBSS | 5 | - | - | nsec |
| TDMO Hold time BICK "↑" | (Note 42) | tBSH | 5 | - | - | nsec |
| SDATA Hold Time | | tSDH | 5 | - | - | nsec |
| SDATA Setup Time | | tSDS | 5 | - | - | nsec |
| **TDM512 mode (TDM[1:0] bits = "11")** | | | | | | |
| BICK Period | | | | - | - | |
| Normal Speed Mode | (Note 41) | tBCK | 1/512fsn | - | - | nsec |
| BICK Pulse Width Low | | tBCKL | 14 | - | - | nsec |
| BICK Pulse Width High | | tBCKH | 14 | - | - | nsec |
| BICK "↑" to LRCK Edge | (Note 39) | tBLR | 14 | - | - | nsec |
| LRCK Edge to BICK "↑" | (Note 39) | tLRB | 14 | - | - | nsec |
| TDMO Setup time BICK "↑" | | tBSS | 5 | - | - | nsec |
| TDMO Hold time BICK "↑" | (Note 42) | tBSH | 5 | - | - | nsec |
| SDATA Hold Time | | tSDH | 5 | - | - | nsec |
| SDATA Setup Time | | tSDS | 5 | - | - | nsec |

Note 39. BICK rising edge must not occur at the same time as LRCK edge.
Note 40. Daisy Chain Mode, fsd (max) = 96 kHz if "TVDD < 3.0V".
Note 41. Daisy Chain Mode, fsn (max) = 48 kHz if "TVDD < 3.0V".
Note 42. LDOE pin = "L", tBSH (min) = 4 nsec if "TVDD > 2.6V".

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **PCM Audio Interface Timing** | | | | | |
| **External Digital Filter Mode** | | | | | |
| BCK Period | tB | 27 | - | - | nsec |
| BCK Pulse Width Low | tBL | 10 | - | - | nsec |
| BCK Pulse Width High | tBH | 10 | - | - | nsec |
| BCK "↑" to WCK Edge | tBW | 5 | - | - | nsec |
| WCK Period | tWCK | 1.3 | - | - | usec |
| WCK Edge to BCK "↑" | tWB | 5 | - | - | nsec |
| WCK Pulse Width Low | tWCKL | 54 | - | - | nsec |
| WCK Pulse Width High | tWCKH | 54 | - | - | nsec |
| DINL/R Hold Time | tDH | 5 | - | - | nsec |
| DINL/R Setup Time | tDS | 5 | - | - | nsec |
| **DSD Audio Interface Timing** | | | | | |
| **Sampling Frequency** | fs | 30 | | 48 | kHz |
| **(64fs mode, DSDSEL [1:0] bits = "00")** | | | | | |
| DCLK Period | tDCK | - | 1/64fs | - | nsec |
| DCLK Pulse Width Low | tDCKL | 144 | - | - | nsec |
| DCLK Pulse Width High | tDCKH | 144 | - | - | nsec |
| DCLK Edge to DSDL/R (Note 43) | tDDD | −20 | - | 20 | nsec |
| **(128fs mode, DSDSEL [1:0] bits = "01")** | | | | | |
| DCLK Period | tDCK | - | 1/128fs | - | nsec |
| DCLK Pulse Width Low | tDCKL | 72 | - | - | nsec |
| DCLK Pulse Width High | tDCKH | 72 | - | - | nsec |
| DCLK Edge to DSDL/R (Note 43) | tDDD | −10 | - | 10 | nsec |
| **(256fs mode, DSDSEL [1:0] bits = "10")** | | | | | |
| DCLK Period | tDCK | - | 1/256fs | - | nsec |
| DCLK Pulse Width Low | tDCKL | 36 | - | - | nsec |
| DCLK Pulse Width High | tDCKH | 36 | - | - | nsec |
| DCLK Edge to DSDL/R (Note 43) | tDDD | −5 | - | 5 | nsec |

Note 43. DSD data transmitting device must meet this time. "tDDD" is defined from DCLK "↓" until DSDL/R edge when DCKB bit = "0" (default), "tDDD" is defined from DCLK "↑" until DSDL/R edge when DCKB bit = "1". If the audio data format is in phase modulation mode, "tDDD" is defined from DCLK edge "↓" or "↑" until DSDL/R edge regardless of DCKB bit setting.

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Control Interface Timing (3-wire IF mode):** | | | | | |
| CCLK Period | tCCK | 200 | - | - | nsec |
| CCLK Pulse Width Low | tCCKL | 80 | - | - | nsec |
| CCLK Pulse Width High | tCCKH | 80 | - | - | nsec |
| CDTI Setup Time | tCDS | 40 | - | - | nsec |
| CDTI Hold Time | tCDH | 40 | - | - | nsec |
| CSN "H" Time | tCSW | 150 | - | - | nsec |
| CSN "↓" to CCLK "↑" | tCSS | 50 | - | - | nsec |
| CCLK "↑" to CSN "↑" | tCSH | 50 | - | - | nsec |
| **Control Interface Timing ($I^2C$ Bus mode):** | | | | | |
| SCL Clock Frequency | fSCL | - | - | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | - | - | usec |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 0.6 | - | - | usec |
| Clock Low Time | tLOW | 1.3 | - | - | usec |
| Clock High Time | tHIGH | 0.6 | - | - | usec |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | - | - | usec |
| SDA Hold Time from SCL Falling (Note 44) | tHD:DAT | 0 | - | - | usec |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | - | - | usec |
| Rise Time of Both SDA and SCL Lines | tR | - | - | 0.3 | usec |
| Fall Time of Both SDA and SCL Lines | tF | - | - | 0.3 | usec |
| Setup Time for Stop Condition | tSU:STO | 0.6 | - | - | usec |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | - | 50 | nsec |
| Capacitive load on bus | Cb | - | - | 400 | pF |
| **Power-down & Reset Timing** (Note 45) | | | | | |
| PDN Accept Pulse Width | tAPD | 150 | - | - | nsec |
| PDN Reject Pulse Width | tRPD | - | - | 30 | nsec |

Note 44. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 45. The AK4492 should be reset by bringing the PDN pin "L" upon power-up.
Note 46. $I^2C$ -bus is a trademark of NXP B.V.

■ **Timing Diagram**

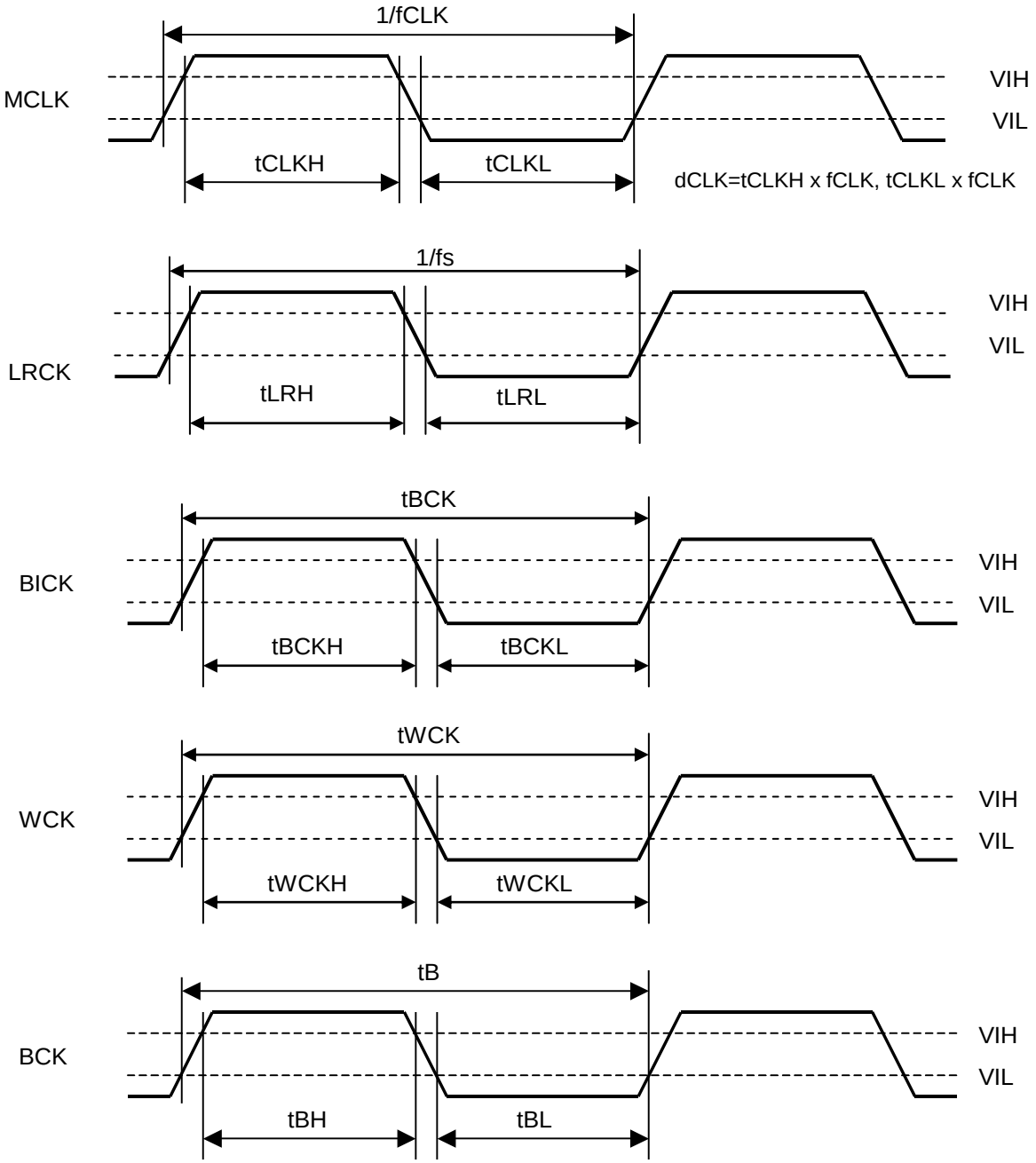



Figure 13. Clock Timing

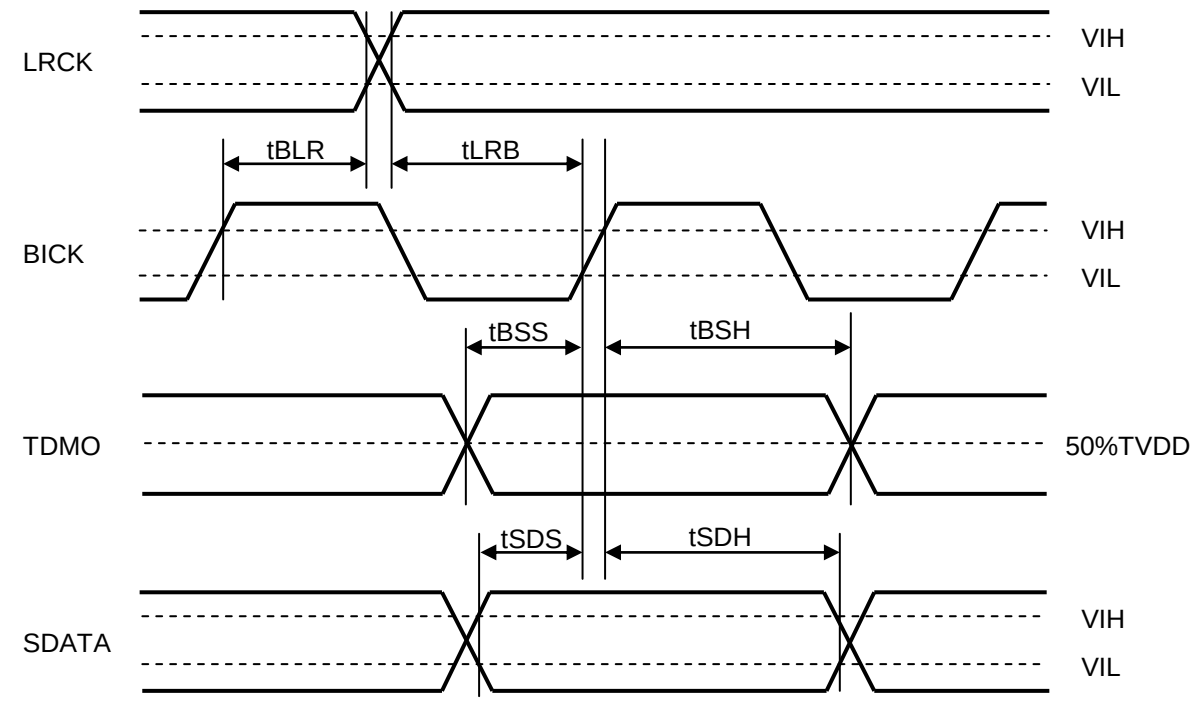



Figure 14. Audio Interface Timing (PCM Mode)

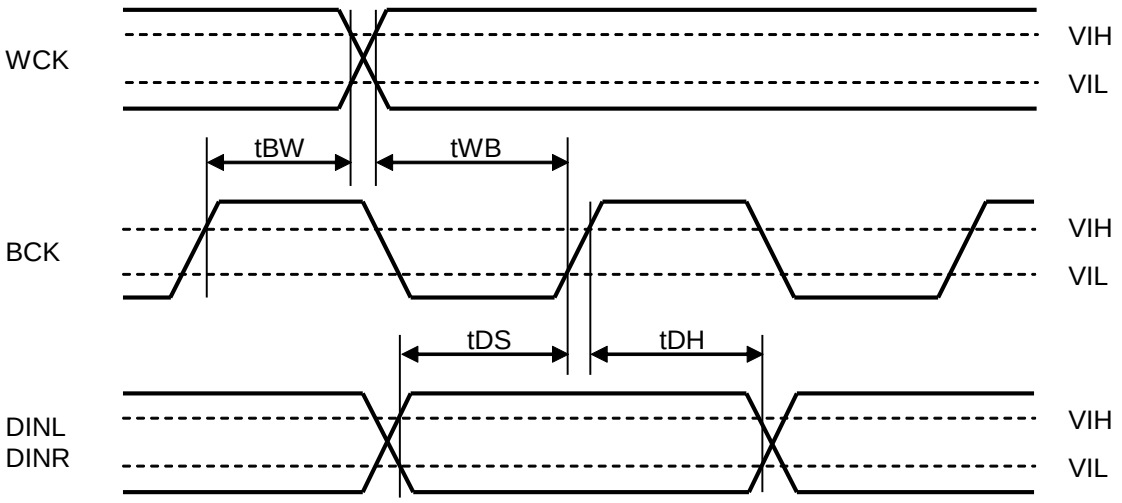
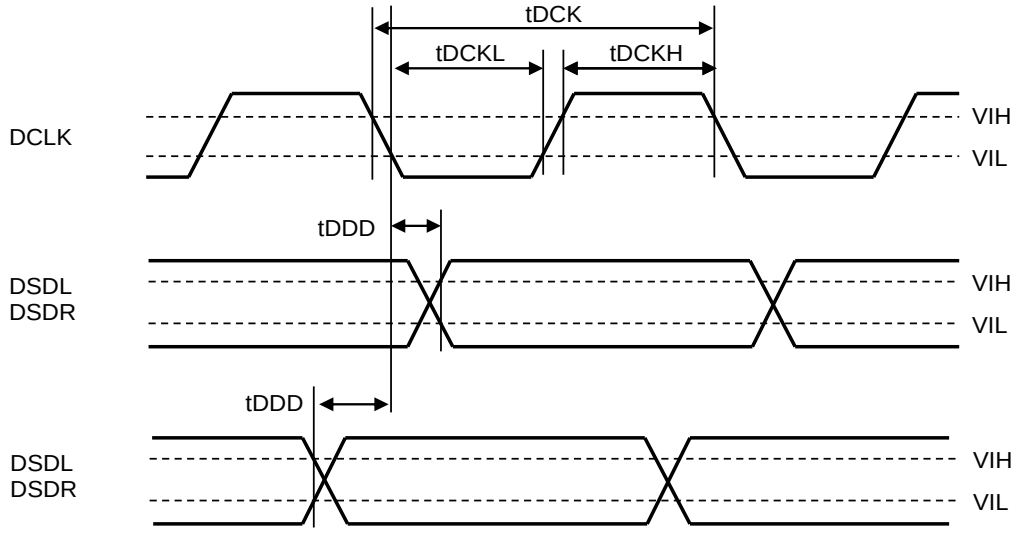



Figure 15. Audio Interface Timing (External Digital Filter I/F Mode)




DSD Audio Interface Timing (DSD64fs, 128fs, 256fs Mode)

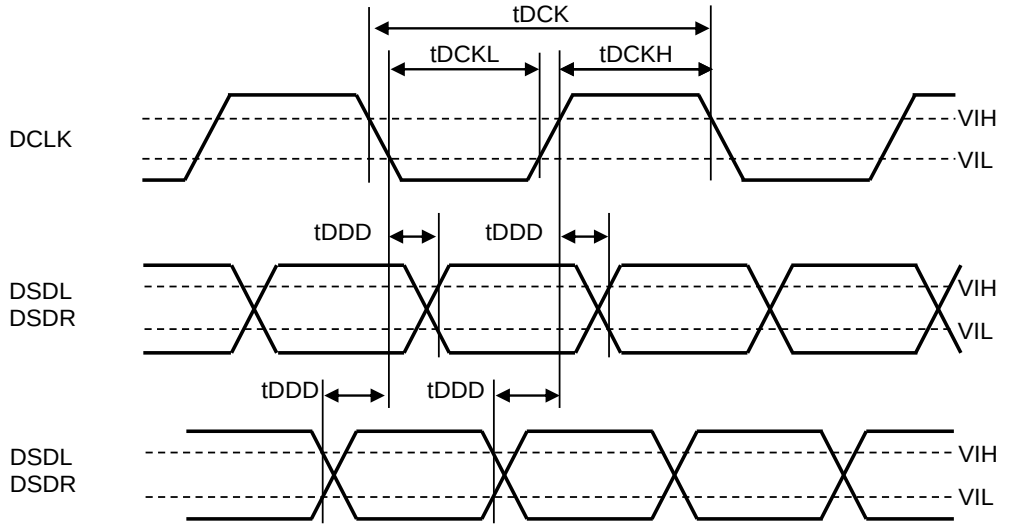



Figure 16. Audio Interface Timing (DSD Phase Modulation Mode, DCKB bit = “0”)

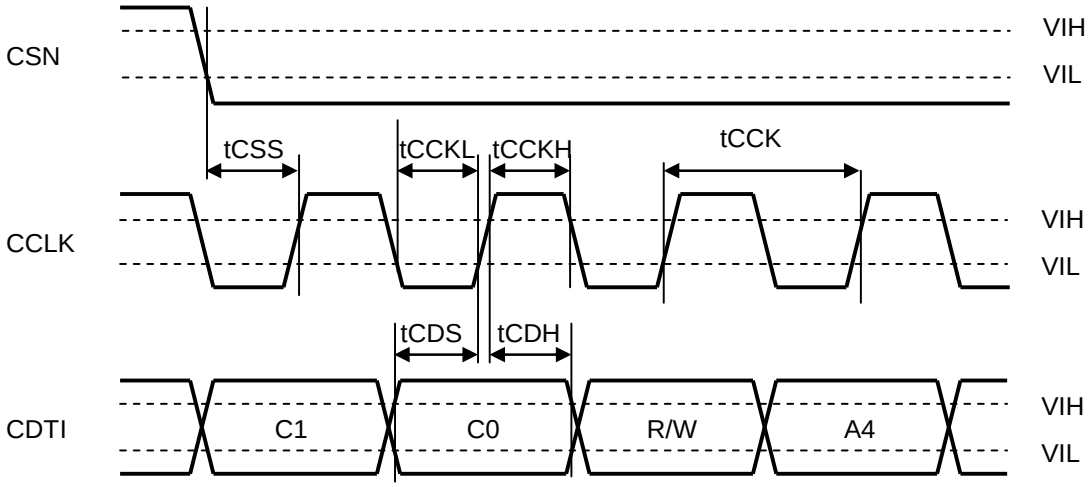



Figure 17. 3 Wire Serial Mode WRITE Command Input Timing

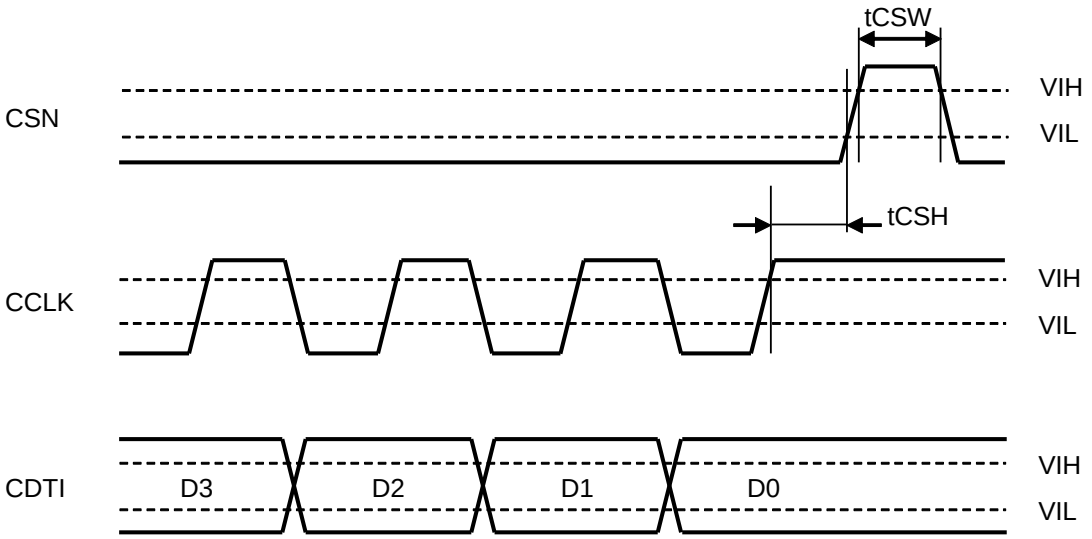



Figure 18. 3 Wire Serial Mode WRITE Data Input Timing

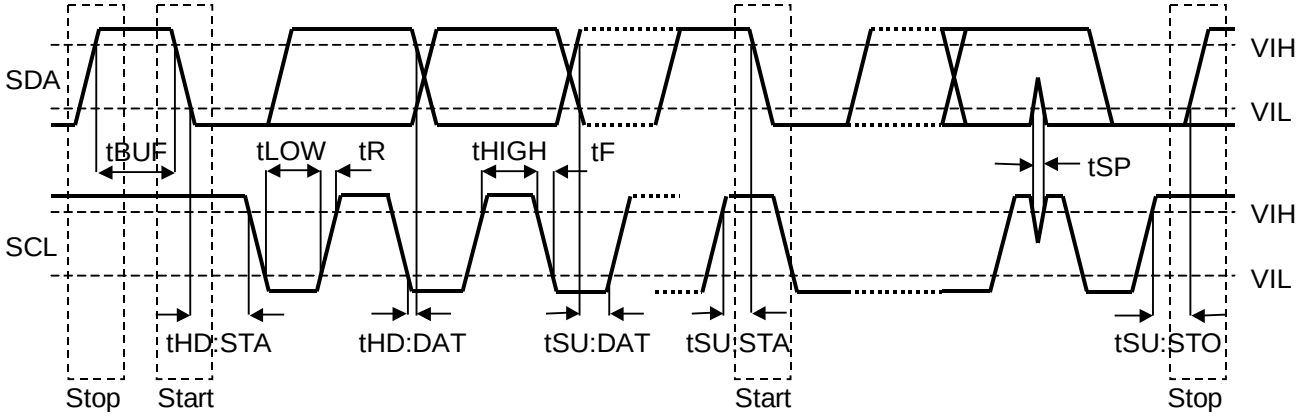



Figure 19. I²C Bus Mode Timing

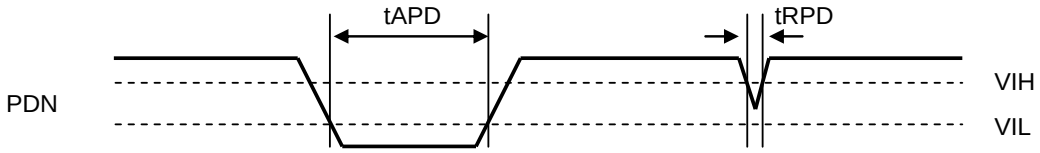



Figure 20. Power Down & Reset Timing

## 9. Functional Descriptions

Each function of the AK4492 is controlled by Pins (pin control mode) and Registers (register control mode) (Table 1). Select the control mode by setting the PSN pin. The AK4492 must be powered down when changing the PSN pin setting. There is a possibility of malfunction if the device is not powered down when changing the control mode since the previous setting is not initialized. Register settings are invalid in pin control mode, and pin settings are invalid in register control mode.

Table 2 shows available functions of each control mode and Table 3 shows available functions in PCM/DSD/EXDF mode.

Table 1. Pin/Register Control Mode Select

| PSN pin | Control Mode |
|---|---|
| L | Register Control Mode |
| H | Pin Control Mode |

Table 2. Function List @Pin/Register Control Mode

(Y: Available, -: Not available)

| Function | Pin Control Mode | Register Control Mode |
|---|---|---|
| DSD/EXDF Mode Select | - | Y |
| System Clock Setting Select | Y | Y |
| Audio Format Select | Y | Y |
| TDM Mode | Y | Y |
| Digital Filter Select | Y | Y |
| De-emphasis Filter Select | Y | Y |
| Digital Attenuator | - | Y |
| Zero Detection | - | Y |
| Mono Mode | - | Y |
| Output signal select (Monoral,Channel select) | - | Y |
| Output Signal Polarity Select (Invert) | Y | Y |
| DSD Full Scale Detect | - | Y |
| Soft Mute | Y | Y |
| Register Reset | - | Y |
| Clock Synchronization Function | - | Y |
| Resistor Control | - | Y |
| Gain Control | Y | Y |
| Heavy Load Mode | Y | Y |

Table 3. Function List of PCM/EXDF/DSD Mode @Register Control Mode
(Y: Available, N/A: Not available)

| Function | Default | Addr | Bit | PCM | EXDF | DSD |
|---|---|---|---|---|---|---|
| PCM/DSD/EXDF Mode Select | PCM mode | 00H<br>02H | EXDF<br>DP | Y | Y | Y |
| System clock setting @DSD mode | 256fs | 02H | DCKS | - | - | Y |
| Systemclock setting @ EXDF mode | 16fs<br>(fs = 44.1 kHz) | 00H | ECS | - | Y | - |
| Digital Filter select @ DSD mode | 39 kHz filter | 09H | DSDF | - | - | Y |
| Digital Filter select @ PCM mode | Short delay sharp roll off filter | 01-02-05H | SD<br>SLOW<br>SSLOW | Y | - | - |
| De-emphasis Response | Off | 01H | DEM[1:0] | Y | - | - |
| Path select @ DSD mode | Normal Path | 06H | DSDD | - | - | Y |
| Audio Data Interface Format @ PCM Mode | 32 bit MSB | 00H | DIF[2:0] | Y | - | - |
| Audio Data Interface Format @ EXDF Mode | 32 bit LSB | 00H | DIF[2:0] | - | Y | - |
| TDM Interface Format | Normal Mode | 0AH | TDM[1:0] | Y | - | - |
| Daisy Chain | Normal Mode | 0BH | DCHAIN | Y | - | - |
| Attenuation Level | 0 dB | 03-04H | ATT[7:0] | Y | Y | Y |
| Data Zero Detect Enable | Disable | 01H | DZFE | Y | Y | Y |
| Inverting Enable of DZF | “H” active | 02H | DZFB | Y | Y | Y |
| Mono/Stereo mode select | Stereo | 02H | MONO | Y | Y | Y |
| Data Invert mode select | Off | 05H | INVL/R | Y | Y | Y |
| The data selection of L channel and R channel | R channel | 02H | SELLR | Y | Y | Y |
| DSD Mute Function @ Full scale Detected | Disable | 06H | DDM | - | - | Y |
| Soft Mute Enable | Normal Operation | 01H | SMUTE | Y | Y | Y |
| Reset | Reset | 00H | RSTN | Y | Y | Y |
| Clock Synchronization Function | Enable | 07H | SYNCE | Y | Y | - |

## ■ D/A Conversion Mode (PCM Mode, DSD Mode, EXDP Mode)

The AK4492 can perform D/A conversion for either PCM data or DSD data. When PCM mode, PCM data can be input from the BICK, LRCK and SDATA pins. When DSD mode, DSD data can be input from the A3, B1 and B2 pins if DSDPATH bit = "0" and DSD data can be input from the J1, H1, and G1 pins if DSDPATH bit = "1". The DP bit controls PCM/DSD mode. The AK4492 must be reset by setting RSTN bit = "0" when PCM/DSD mode is changed by DP bit or when DSD signal input pins are changed by DSDPATH bit. It takes about 2 ~ 3/fs to change the mode. Wait 4/fs or more to change RSTN bit after changing these settings.

External digital filter I/F can be selected by setting DP bit = "0" and EXDF bit = "1". When using an external digital filter (EXDF I/F mode), data is input to each MCLK, BCK, WCK, DINL and DINR pin. EXDF bit controls the modes. When switching internal and external digital filters by EXDF bit, the AK4492 must be reset by RSTN bit. A Digital filter switching takes 2~3k/fs. The AK4492 is in DSD mode when DP bit = "1" and EXDF bit "1".

Table 4. PCM/DSD/EXDF Mode Control

| DP bit | EXDF bit | DSDPATH bit | D/A Conv. Mode | Pin Assignment | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | J1 pin | H1 pin | G1 pin | A3 pin | B1 pin | B2 pin |
| 0 (default) | 0 (default) | x | PCM | BICK | SDATA | LRCK | Not Use | Not Use | Not Use |
| 1 | x | 0 (default) | DSD | Not Use | Not Use | Not Use | DCLK | DSDL | DSDR |
| 1 | x | 1 | DSD | DCLK | DSDL | DSDR | Not Use | Not Use | Not Use |
| 0 | 1 | x | EXDF | BCK | DINL | DINR | Not Use | Not Use | Not Use |

(x: Do not care)

## ■ D/A Conversion Mode Switching Timing

Figure 21 and Figure 22 show switching timing of PCM/EXDF and DSD modes. To prevent noise caused by excessive input, DSD signal should be input 4/fs after setting RSTN bit = "0" until the device is completely reset internally when the conversion mode is changed to DSD mode from PCM/ESDF mode. DSD signal should be stopped 4/fs after setting RSTN bit = "0"until the device is completely reset internally when the conversion mode is changed to PCM/EXDE from DSD mode.

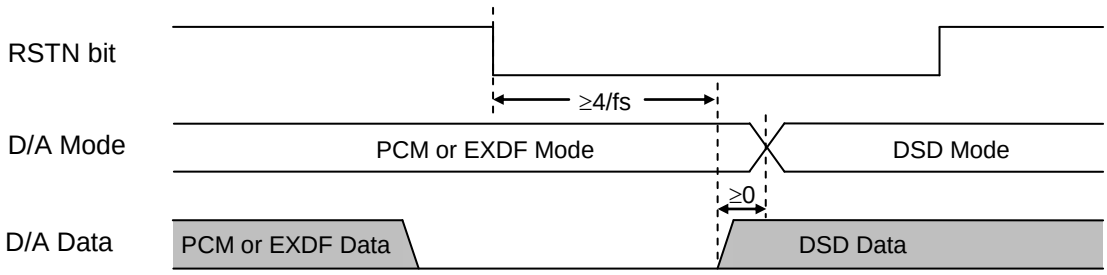



Figure 21. D/A Mode Switching Timing (from PCM or EXDF to DSD)

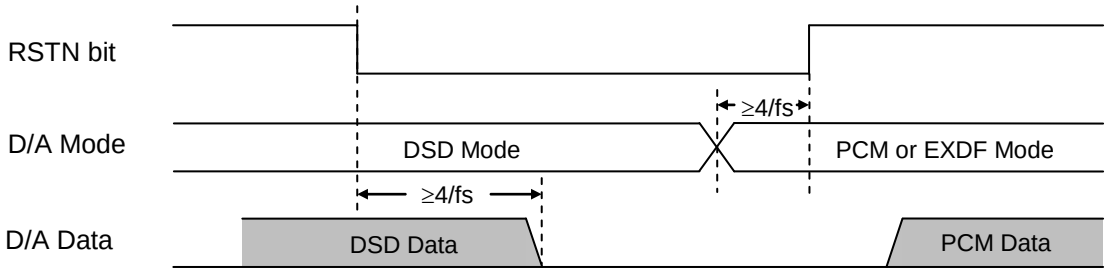



Figure 22. D/A Mode Switching Timing (from DSD to PCM or EXDF)

Figure 23 shows switching timing of PCM and EXDF modes. Set EXDF bit 4/fs after setting RSTN bit = "0" until the device is completely reset internally when changing the conversion mode.

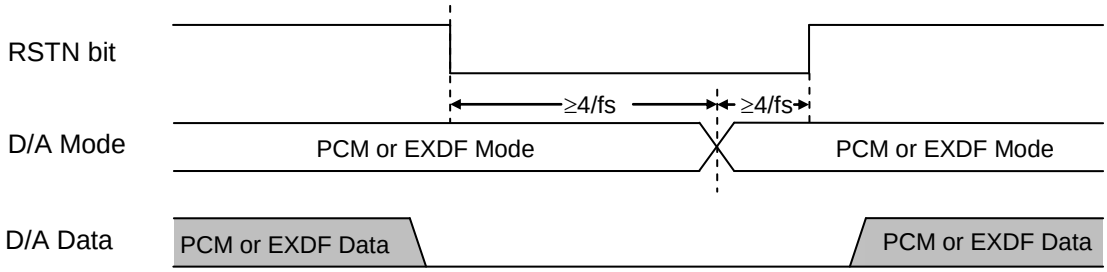



Figure 23. D/A Mode Switching Timing (PCM ⇔ EXDF)

## ■ System Clock

### [1] PCM Mode

The external clocks, which are required to operate the AK4492, are MCLK, BICK and LRCK. MCLK, BICK and LRCK should be synchronized but the phase is not critical. The MCLK is used to operate the digital interpolation filter, the delta-sigma modulator and SCF.
There are Manual Setting Mode, Auto Setting Mode and Fs Auto Detection mode for MCLK frequency setting(Table 5). In manual setting mode (ACKS pin="L" or ACKS bit="0"), MCLK frequency is set automatically but the sampling speed (LRCK frequency) is set by DFS[2:0] bits (Table 6). Sampling frequency is fixed to normal speed mode in pin control mode (PSN pin = "H"), and it is set by DFS[2:0] bits in register control mode (PSN pin = "L"). In register control mode, the AK4492 is in manual setting mode when power-down is released (PDN pin = "L" → "H").
In auto setting mode (ACKS pin = "H" or ACKS bit="1"), sampling speed and MCLK frequency are detected automatically (Table 7, Table 11) and then the initial master clock is set to the appropriate frequency (Table 8, Table 9, Table 15, Table 16).
In FS auto detect mode (AFSD bit= "1"), sampling speed is automatically detected (Table 7, Table 11) and the initial master clock is set to the appropriate frequency. In this mode, ACKS bit and DFS[2:0] bits settings are invalid. Fs auto detect mode is not supported by pin control mode.

The AK4492 is automatically placed in power-down state when MCLK is stopped for more than 1us during a normal operation (PDN pin ="H"), and the analog output becomes Hi-z state. When MCLK is input again, the AK4492 exits power-down state and starts operation. The AK4492 is in power-down mode until MCLK BICK and LRCK are supplied and the analog output is floating state.

Table 5. System Clock Setting Mode @Register Control Mode

| AFSD bit | ACKS bit | Mode | |
|---|---|---|---|
| 0 | 0 | Manual setting Mode | (default) |
| | 1 | Auto setting Mode | |
| 1 | x | FS Auto Detect Mode | |

(x: Do not care)

**(1) Pin Control Mode (PSN pin = "H")**

(1)-1. Manual Setting Mode (ACKS pin = "L")
The MCLK frequency corresponding to each sampling speed should be provided externally (Table 6). DFS1-0 bits are fixed to "00". In this mode, quad speed and double speed modes are not available.

Table 6. System Clock Example (Manual Setting Mode @Pin Control Mode)

| LRCK | MCLK (MHz) | | | | | | | | BICK |
|---|---|---|---|---|---|---|---|---|---|
| fs | 128fs | 192fs | 256fs | 384fs | 512fs | 768fs | 1024fs | 1152fs | 64fs |
| 32.0 kHz | N/A | N/A | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 | 36.8640 | 2.0480 MHz |
| 44.1 kHz | N/A | N/A | 11.2896 | 16.9344 | 22.5792 | 33.8688 | N/A | N/A | 2.8224 MHz |
| 48.0 kHz | N/A | N/A | 12.2880 | 18.4320 | 24.5760 | 36.8640 | N/A | N/A | 3.0720 MHz |

(N/A: Not available)

(1)-2. Auto Setting Mode (ACKS pin = "H")
In auto setting mode, MCLK frequency and sampling frequency are detected automatically (Table 7). MCLK of corresponded frequency to each sampling speed mode should be input externally (Table 8, Table 9).

Table 7. Sampling Speed (Auto Setting Mode @Pin Control Mode)

| MCLK | | Sampling Speed |
|---|---|---|
| 1152fs/1024fs | | Normal (fs ≤ 32 kHz) |
| 512fs/256fs | 768fs/384fs | Normal |
| 256fs | 384fs | Double |
| 128fs | 192fs | Quad |
| 64fs | 96fs | Oct |
| 32fs | 48fs | Hex |

Table 8. System Clock Example 1 (Auto Setting Mode @Pin Control Mode)

| LRCK | MCLK (MHz) | | | | | | Sampling Speed |
|---|---|---|---|---|---|---|---|
| Fs | 32fs | 48fs | 64fs | 96fs | 128fs | 192fs | |
| 32.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | Normal |
| 44.1 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 48.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 88.2 kHz | N/A | N/A | N/A | N/A | N/A | N/A | Double |
| 96.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 176.4 kHz | N/A | N/A | N/A | N/A | 22.5792 | 33.8688 | Quad |
| 192.0 kHz | N/A | N/A | N/A | N/A | 24.5760 | 36.8640 | |
| 384 kHz | N/A | N/A | 24.576 | 36.864 | N/A | N/A | Oct |
| 768 kHz | 24.576 | 36.864 | N/A | N/A | N/A | N/A | Hex |

(N/A: Not available)

Table 9. System Clock Example 2 (Auto Setting Mode @Pin Control Mode)

| LRCK | MCLK (MHz) | | | | | | Sampling Speed |
|---|---|---|---|---|---|---|---|
| Fs | 256fs | 384fs | 512fs | 768fs | 1024fs | 1152fs | |
| 32.0 kHz | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 | 36.8640 | Normal |
| 44.1 kHz | 11.2896 | 16.9344 | 22.5792 | 33.8688 | N/A | N/A | |
| 48.0 kHz | 12.2880 | 18.4320 | 24.5760 | 36.8640 | N/A | N/A | |
| 88.2 kHz | 22.5792 | 33.8688 | N/A | N/A | N/A | N/A | Double |
| 96.0 kHz | 24.5760 | 36.8640 | N/A | N/A | N/A | N/A | |
| 176.4 kHz | N/A | N/A | N/A | N/A | N/A | N/A | Quad |
| 192.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 384 kHz | N/A | N/A | N/A | N/A | N/A | N/A | Oct |
| 768 kHz | N/A | N/A | N/A | N/A | N/A | N/A | Hex |

(N/A: Not available)

When MCLK= 256fs/384fs, auto setting mode supports sampling rate of 8kHz~96kHz (Table 10). However, the DR and S/N performances will degrade approximately 3dB as compared to when MCLK = 256fs/384fs for DR and MCLK= 512fs/768fs for S/N, respectively if the sampling rate is under 54kHz.

Table 10. DR and S/N Relationship with MCLK Frequency (fs = 44.1kHz)

| ACKS pin | MCLK | DR, S/N |
|---|---|---|
| L | 256fs/384fs/512fs/768fs | 123 dB |
| H | 256fs/384fs | 120 dB |
| H | 512fs/768fs | 123 dB |

Note 47. This Characteristic is supported by using External Circuit (Figure 77)

**(2) Register Control Mode (PSN pin = "L")**

(2)-1. Manual Setting Mode (AFSD bit = "0", ACKS bit = "0")
MCLK frequency is detected automatically and the sampling speed is set by DFS[2:0] bits (Table 11). The MCLK frequency corresponding to each sampling speed that should be provided externally (Table 12, Table 13). The AK4492 is set to Manual Setting Mode at power-up (PDN pin = "L" →"H"). When DFS2-0 bits are changed, the AK4492 should be reset by RSTN bit.

Table 11. Sampling Speed (Manual Setting Mode @Register Control Mode)

| DFS2 bit | DFS1 bit | DFS0 bit | Sampling Rate (fs) | | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Normal Speed Mode | 8 kHz ~ 54 kHz | (default) |
| 0 | 0 | 1 | Double Speed Mode | 54 kHz ~ 108 kHz | |
| 0 | 1 | 0 | Quad Speed Mode | 108 kHz ~ 216 kHz | |
| 0 | 1 | 1 | Quad Speed Mode | 108 kHz ~ 216 kHz | |
| 1 | 0 | 0 | Oct Speed Mode | 216 kHz ~ 388 kHz | |
| 1 | 0 | 1 | Hex Speed Mode | 388 kHz ~ 776 kHz | |
| 1 | 1 | 0 | Oct Speed Mode | 216 kHz ~ 388 kHz | |
| 1 | 1 | 1 | Hex Speed Mode | 388 kHz ~ 776 kHz | |

Table 12. System Clock Example 1 (Manual Setting Mode @Register Control Mode)

| LRCK | MCLK (MHz) | | | | | | Sampling Speed |
|---|---|---|---|---|---|---|---|
| Fs | 16fs | 32fs | 48fs | 64fs | 96fs | 128fs | |
| 32.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | Normal |
| 44.1 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 48.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 88.2 kHz | N/A | N/A | N/A | N/A | N/A | N/A | Double |
| 96.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 176.4 kHz | N/A | N/A | N/A | N/A | N/A | 22.5792 | Quad |
| 192.0 kHz | N/A | N/A | N/A | N/A | N/A | 24.5760 | |
| 384 kHz | N/A | 12.288 | 18.432 | 24.576 | 36.864 | N/A | Oct |
| 768 kHz | 12.288 | 24.576 | 36.864 | 49.152 | N/A | N/A | Hex |

(N/A: Not available)

Table 13. System Clock Example 2 (Manual Setting Mode @Register Control Mode)

| LRCK | MCLK (MHz) | | | | | | | Sampling Speed |
|---|---|---|---|---|---|---|---|---|
| fs | 192fs | 256fs | 384fs | 512fs | 768fs | 1024fs | 1152fs | |
| 32.0 kHz | N/A | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 | 36.8640 | Normal |
| 44.1 kHz | N/A | 11.2896 | 16.9344 | 22.5792 | 33.8688 | N/A | N/A | |
| 48.0 kHz | N/A | 12.2880 | 18.4320 | 24.5760 | 36.8640 | N/A | N/A | |
| 88.2 kHz | N/A | 22.5792 | 33.8688 | 45.1584 | N/A | N/A | N/A | Double |
| 96.0 kHz | N/A | 24.5760 | 36.8640 | 49.1520 | N/A | N/A | N/A | |
| 176.4 kHz | 33.8688 | 45.1584 | N/A | N/A | N/A | N/A | N/A | Quad |
| 192.0 kHz | 36.8640 | 49.1520 | N/A | N/A | N/A | N/A | N/A | |
| 384 kHz | N/A | N/A | N/A | N/A | N/A | N/A | N/A | Oct |
| 768 kHz | N/A | N/A | N/A | N/A | N/A | N/A | N/A | Hex |

(N/A: Not available)

(2)-2. Auto Setting Mode (AFSD bit= “0”, ACKS bit = “1”)

MCLK frequency and the sampling speed are detected automatically (Table 14) and DFS[2:0] bits are ignored. The MCLK frequency corresponding to each sampling speed should be provided externally (Table 15, Table 16).

Table 14. Sampling Speed (Auto Setting Mode)

| MCLK | | Sampling Speed |
|---|---|---|
| 1152fs/1024fs | | Normal (fs ≤ 32kHz) |
| 512fs/256fs | 768fs/384fs | Normal |
| 256fs | 384fs | Double |
| 128fs | 192fs | Quad |
| 64fs | 96fs | Oct |
| 32fs | 48fs | Hex |

Table 15. System Clock Example (Auto Setting Mode)

| LRCK | MCLK (MHz) | | | | | Sampling Speed |
|---|---|---|---|---|---|---|
| fs | 32fs | 48fs | 64fs | 96fs | 128fs | |
| 32.0 kHz | N/A | N/A | N/A | N/A | N/A | Normal |
| 44.1 kHz | N/A | N/A | N/A | N/A | N/A | |
| 48.0 kHz | N/A | N/A | N/A | N/A | N/A | |
| 88.2 kHz | N/A | N/A | N/A | N/A | N/A | Double |
| 96.0 kHz | N/A | N/A | N/A | N/A | N/A | |
| 176.4 kHz | N/A | N/A | N/A | N/A | 22.5792 | Quad |
| 192.0 kHz | N/A | N/A | N/A | N/A | 24.5760 | |
| 384 kHz | N/A | N/A | 24.576 | 36.864 | N/A | Oct |
| 768 kHz | 24.576 | 36.864 | N/A | N/A | N/A | Hex |

(N/A: Not available)

Table 16. System Clock Example (Auto Setting Mode)

| LRCK | | MCLK (MHz) | | | | | | Sampling Speed |
|---|---|---|---|---|---|---|---|---|
| fs | 192fs | 256fs | 384fs | 512fs | 768fs | 1024fs | 1152fs | |
| 32.0 kHz | N/A | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 | 36.8640 | Normal |
| 44.1 kHz | N/A | 11.2896 | 16.9344 | 22.5792 | 33.8688 | N/A | N/A | |
| 48.0 kHz | N/A | 12.2880 | 18.4320 | 24.5760 | 36.8640 | N/A | N/A | |
| 88.2 kHz | N/A | 22.5792 | 33.8688 | N/A | N/A | N/A | N/A | Double |
| 96.0 kHz | N/A | 24.5760 | 36.8640 | N/A | N/A | N/A | N/A | |
| 176.4 kHz | 33.8688 | N/A | N/A | N/A | N/A | N/A | N/A | Quad |
| 192.0 kHz | 36.8640 | N/A | N/A | N/A | N/A | N/A | N/A | |
| 384 kHz | N/A | N/A | N/A | N/A | N/A | N/A | N/A | Oct |
| 768 kHz | N/A | N/A | N/A | N/A | N/A | N/A | N/A | Hex |

(N/A: Not available)

When MCLK= 256fs/384fs, auto setting mode supports sampling rate from 8kHz to 96kHz (Table 14). However, the DR and S/N performances will degrade approximately 3dB as compared to when MCLK = 256fs/384fs for DR and MCLK= 512fs/768fs for S/N, respectively if the sampling rate is under 54kHz.

Table 17. DR and S/N Relationship with MCLK Frequency (fs = 44.1kHz)

| ACKS bit | MCLK | DR, S/N |
|---|---|---|
| 0 | 256fs/384fs/512fs/768fs | 123 dB |
| 1 | 256fs/384fs | 120 dB |
| | 512fs/768fs | 123 dB |

Note 48. This Characteristic is supported by using External Circuit (Figure 77)

(2)-3. Sampling Frequency (FS) Auto Detect Mode (AFSD bi = “1”)

MCLK frequency and the sampling rate is detected automatically (Table 14). In this mode, DFS[2:0] bits and ACKS bit settings are invalid. The MCLK frequency corresponding to each sampling speed should be provided externally (Table 18, Table 19). Internal operation sequence in FS auto detect mode is shown in Figure 24.

Table 18. System Clock Example 1 @PCM Mode

| LRCK | MCLK(MHz) | | | | | | Sampling Speed |
|---|---|---|---|---|---|---|---|
| fs | 16fs | 32fs | 48fs | 64fs | 96fs | 128fs | |
| 32.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | Normal |
| 44.1 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 48.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 88.2 kHz | N/A | N/A | N/A | N/A | N/A | N/A | Double |
| 96.0 kHz | N/A | N/A | N/A | N/A | N/A | N/A | |
| 176.4 kHz | N/A | N/A | N/A | N/A | N/A | 22.5792 | Quad |
| 192.0 kHz | N/A | N/A | N/A | N/A | N/A | 24.5760 | |
| 384 kHz | N/A | 12.288 | 18.432 | 24.576 | 36.864 | N/A | Oct |
| 768 kHz | 12.288 | 24.576 | 36.864 | 49.152 | N/A | N/A | Hex |

(N/A: Not available)

Table 19. System Clock Example 2 @PCM Mode

| LRCK | MCLK (MHz) | | | | | | | Sampling Speed |
|---|---|---|---|---|---|---|---|---|
| fs | 192fs | 256fs | 384fs | 512fs | 768fs | 1024fs | 1152fs | |
| 32.0 kHz | N/A | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.768 | 36.8640 | Normal |
| 44.1 kHz | N/A | 11.2896 | 16.9344 | 22.5792 | 33.8688 | N/A | N/A | |
| 48.0 kHz | N/A | 12.2880 | 18.4320 | 24.5760 | 36.8640 | N/A | N/A | |
| 88.2 kHz | N/A | 22.5792 | 33.8688 | 45.1584 | N/A | N/A | N/A | Double |
| 96.0 kHz | N/A | 24.5760 | 36.8640 | 49.1520 | N/A | N/A | N/A | |
| 176.4 kHz | 33.8688 | 45.1584 | N/A | N/A | N/A | N/A | N/A | Quad |
| 192.0 kHz | 36.8640 | 49.1520 | N/A | N/A | N/A | N/A | N/A | |
| 384 kHz | N/A | N/A | N/A | N/A | N/A | N/A | N/A | Oct |
| 768 kHz | N/A | N/A | N/A | N/A | N/A | N/A | N/A | Hex |

(N/A: Not available)

(2)-4. Power-down/up sequence in FS Auto Detect Mode when using internal LDO.

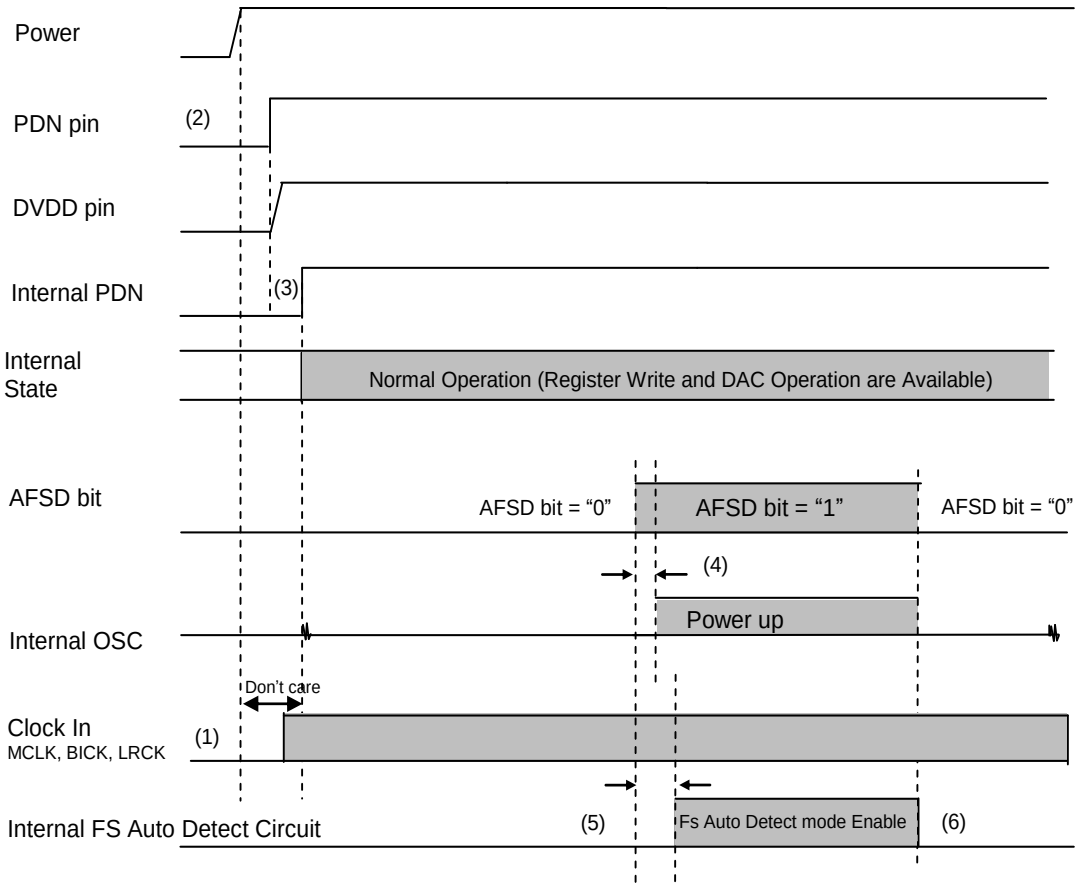



Figure 24. Power-down/up Sequence at FS AutoDetect Mode

Note:

(1) Do not input a clock when power supplies are powered down.
(2) The PDN pin must be held "L" for more than 150ns after turning on AVDD, TVDD and VDDL/R.
(3) When the LDOE pin = "H", the internal LDO starts operation after power up. The internal circuit will be powered up after the shutdown switch is ON (max. 2ms) following the internal oscillator count up.
When the LDOE pin = "L", the internal shutdown switch is ON. The internal circuit will be powered up after the shutdown switch is ON (max. 1ms).
(4) When AFSD bit = "1", the internal oscillator starts operation. It takes10 us (max) until the oscillation frequency is stabled.
(5) After AFSD bit = "1", Fs Auto Detect Mode is started in 8/fs~9/fs.
(6) After AFSD bit = "0", the Fs Auto Detect ciruit stops internal operation and the OSC is stopped.

### [2] DSD Mode

The AK4492 has a DSD playback function. The external clocks that are required in DSD mode are MCLK and DCLK. MCLK should be synchronized with DCLK but the phase is not critical. The frequency of MCLK is set by DCKS bit (Table 20).
The AK4492 is automatically placed in power-down state when MCLK is stopped during a normal operation (PDN pin ="H"), and the analog output becomes Hi-z state. When the reset is released (PDN pin = "L" → "H"), the AK4492 is in power-down state until MCLK and DCLK are input.

Table 20. System Clock (DSD Mode, fs = 32 kHz, 44.1 kHz, 48 kHz)

| DCKS bit | MCLK Frequency | DCLK Frequency | |
|---|---|---|---|
| 0 | 512fs | 64fs/128fs/256fs | (default) |
| 1 | 768fs | 64fs/128fs/256fs | |

The AK4492 supports DSD data stream of 2.8224MHz (64fs), 5.6448MHz (128fs) and 11.2896MHz (256fs). The data sampling speed is selected by DSDSEL[1:0] bits (Table 21). DSDSEL [1:0] bits are changed during RSTN bit = "0".

Table 21. DSD Data Stream Select

| DSDSEL1 | DSDSEL0 | DSD data stream | | | |
|---|---|---|---|---|---|
| | | fs = 32 kHz | fs = 44.1 kHz | fs = 48 kHz | |
| 0 | 0 | 2.048 MHz | 2.8224 MHz | 3.072 MHz | (default) |
| 0 | 1 | 4.096 MHz | 5.6448 MHz | 6.144 MHz | |
| 1 | 0 | 8.192 MHz | 11.2896 MHz | 12.288 MHz | |
| 1 | 1 | N/A | N/A | N/A | |

The AK4492 has a Volume bypass function for play backing DSD signal. Two modes are selectable by DSDD bit (Table 22). When setting DSDD bit = "1", the output volume control and zero detect functions are not available.

Table 22. DSD Playback Path Select

| DSDD | Mode | |
|---|---|---|
| 0 | Normal Path | (default) |
| 1 | Volume Bypass | |

### [3] External Digital Filter Mode (EXDF Mode)

The external clocks that are required in EXDF mode are MCLK, BCK and WCK. The BCK and MCLK clocks must be the same frequency and must not burst. BCK and MCLK frequencies for each sampling speed are shown in Table 23. ECS bit selects WCK frequency from 384kHz and 768kHz. DW indicates the number of BCK in one WCK cycle.

All circuits except the internal LDO are automatically placed in power-down state when MCLK edge is not detected for more than 1us during a normal operation (PDN pin ="H"), and the analog output becomes Hi-Z state. The power-down state is released and the AK4492 starts operation by inputting MCLK again. In this case, register settings are not initialized.
When the reset is released (PDN pin = "L" → "H"), the AK4492 is in power-down state until MCLK, BCK and WCK are input.

Table 23. System Clock Example (EXDF Mode)

| Sampling Speed[kHz] | MCLK&BCK [MHz] | | | | | | WCK | ECS | |
|---|---|---|---|---|---|---|---|---|---|
| | 128fs | 192fs | 256fs | 384fs | 512fs | 768fs | | | |
| 44.1(30~48) | N/A | N/A | N/A | N/A | 22.5792 | 33.8688 | 16fs | 0 | (default) |
| | | | | | 32 | 48 | DW | | |
| 44.1(30~48) | N/A | N/A | 11.2896 | 16.9344 | N/A | 33.8688 | 8fs | 1 | |
| | | | 32 | 48 | | 96 | DW | | |
| 96(54~96) | N/A | N/A | 24.576 | 36.864 | N/A | N/A | 8fs | 0 | |
| | | | 32 | 48 | | | DW | | |
| 96(54~96) | 12.288 | 18.432 | N/A | 36.864 | N/A | N/A | 4fs | 1 | |
| | 32 | 48 | | 96 | | | DW | | |
| 192(108~192) | 24.576 | 36.864 | N/A | N/A | N/A | N/A | 4fs | 0 | |
| | 32 | 48 | | | | | DW | | |
| 192(108~192) | N/A | 36.864 | N/A | N/A | N/A | N/A | 2fs | 1 | |
| | | 96 | | | | | DW | | |

## ■ Audio Interface Format

### [1] PCM Mode

(1) Input Data Format
Data is shifted in via the SDATA pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 pins (Pin control mode) or DIF[2:0] bits (Register control mode) as shown in Table 24. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Mode 2 can be used for 20-bit and 16-bit MSB justified formats by zeroing the unused LSBs.

**Normal Mode (TDM[1:0] bits = "00" or TDM1-0 pins = "LL")**
2ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 pins (Pin control mode) or DIF[2:0] bits (Register control mode) as shown in Table 24. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Mode 6 can be used for 24-bit, 20-bit and 16-bit MSB justified formats by zeroing the unused LSBs.

**TDM128 Mode (TDM[1:0] bits = "01" or TDM1-0 pins = "LH")**
4ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Data slot can be selected by SDS[2:0] bits (Table 25). BICK is fixed to 128fs. Six data formats are supported and selected by the DIF2-0 pins (Pin control mode) or DIF[2:0] bits (Register control mode) as shown in Table 24. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

**TDM256 Mode (TDM[1:0] bits = "10" or TDM1-0 pins = "HL")**
8ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Data slot can be selected by SDS[2:0] bits (Table 25). BICK is fixed to 256fs. Six data formats are supported and selected by the DIF2-0 pins (Pin control mode) or DIF[2:0] bits (Register control mode) as shown in Table 24. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

**TDM512 Mode (TDM[1:0] bits = "11" or TDM1-0 pins = "HH")**
16ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Data slot can be selected by SDS[2:0] bits (Table 25). BICK is fixed to 512fs. Six data formats are supported and selected by the DIF2-0 pins (Pin control mode) or DIF[2:0] bits (Register control mode) as shown in Table 24. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

Table 24. Audio Interface Format

| Mode | | TDM1 bit | TDM0 bit | DIF2 bit | DIF1 bit | DIF0 bit | SDATA Format | LRCK | BICK | Figure |
|---|---|---|---|---|---|---|---|---|---|---|
| Normal (Note 49) | 0 | 0 | 0 | 0 | 0 | 0 | 16-bit LSB justified | H/L | ≥ 32fs | Figure 25 |
| | 1 | | | 0 | 0 | 1 | 20-bit LSB justified | H/L | ≥ 40fs | Figure 26 |
| | 2 | | | 0 | 1 | 0 | 24-bit MSB justified | H/L | ≥ 48fs | Figure 27 |
| | 3 | | | 0 | 1 | 1 | 16-bit I²S Compatible | L/H | 32fs | Figure 28 |
| | | | | | | | 24-bit I²S Compatible | L/H | ≥ 48fs | |
| | 4 | | | 1 | 0 | 0 | 24-bit LSB justified | H/L | ≥ 48fs | Figure 26 |
| | 5 | | | 1 | 0 | 1 | 32-bit LSB justified | H/L | ≥ 64fs | Figure 29 |
| | 6 | | | 1 | 1 | 0 | 32-bit MSB justified | H/L | ≥ 64fs | Figure 30 |
| | 7 | | | 1 | 1 | 1 | 32-bit I²S Compatible | L/H | ≥ 64fs | Figure 31 |
| TDM128 | - | 0 | 1 | - | - | - | N/A | - | - | - |
| | - | | | - | - | - | N/A | - | - | - |
| | 8 | | | 0 | 1 | 0 | 24-bit MSB justified | H/L | 128fs | Figure 32 |
| | 9 | | | 0 | 1 | 1 | 24-bit I²S Compatible | L/H | 128fs | Figure 33 |
| | 10 | | | 1 | 0 | 0 | 24-bit LSB justified | H/L | 128fs | Figure 34 |
| | 11 | | | 1 | 0 | 1 | 32-bit LSB justified | H/L | 128fs | Figure 32 |
| | 12 | | | 1 | 1 | 0 | 32-bit MSB justified | H/L | 128fs | Figure 32 |
| | 13 | | | 1 | 1 | 1 | 32-bit I²S Compatible | L/H | 128fs | Figure 33 |
| TDM256 | - | 1 | 0 | - | - | - | N/A | - | - | - |
| | - | | | - | - | - | N/A | - | - | - |
| | 14 | | | 0 | 1 | 0 | 24-bit MSB justified | H/L | 256fs | Figure 35 |
| | 15 | | | 0 | 1 | 1 | 24-bit I²S Compatible | L/H | 256fs | Figure 36 |
| | 16 | | | 1 | 0 | 0 | 24-bit LSB justified | H/L | 256fs | Figure 37 |
| | 17 | | | 1 | 0 | 1 | 32-bit LSB justified | H/L | 256fs | Figure 35 |
| | 18 | | | 1 | 1 | 0 | 32-bit MSB justified | H/L | 256fs | Figure 35 |
| | 19 | | | 1 | 1 | 1 | 32-bit I²S Compatible | L/H | 256fs | Figure 36 |
| TDM512 | - | 1 | 1 | - | - | - | N/A | - | - | - |
| | - | | | - | - | - | N/A | - | - | - |
| | 20 | | | 0 | 1 | 0 | 24-bit MSB justified | H/L | 512fs | Figure 38 |
| | 21 | | | 0 | 1 | 1 | 24-bit I²S Compatible | L/H | 512fs | Figure 39 |
| | 22 | | | 1 | 0 | 0 | 24-bit LSB justified | H/L | 512fs | Figure 40 |
| | 23 | | | 1 | 0 | 1 | 32-bit LSB justified | H/L | 512fs | Figure 38 |
| | 24 | | | 1 | 1 | 0 | 32-bit MSB justified | H/L | 512fs | Figure 38 |
| | 25 | | | 1 | 1 | 1 | 32-bit I²S Compatible | L/H | 512fs | Figure 39 |

Note 49. BICK more than setting bit must be input to each channel. In the LRCK column, "H/L" indicates that L channel data can be input when LRCK is "H" and R channel data can be input when LRCK is "L". "L/H" indicates L channel data can be input when LRCK is "L" and R channel data can be input when LRCK is "H".

Note 50. The default settings in Register Control Mode are shown below.
TDM1 bit = "0", TDM0 bit = "0", DIF2 bit = "1", DIF1 bit = "1", DIF0 bit = "0"

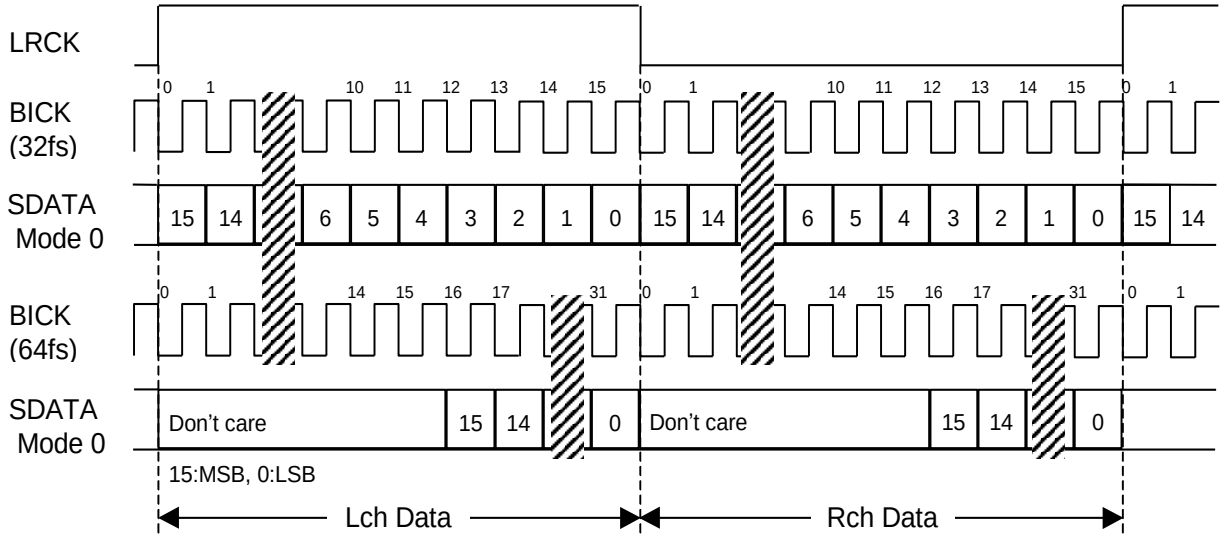



Figure 25. Mode 0 Timing

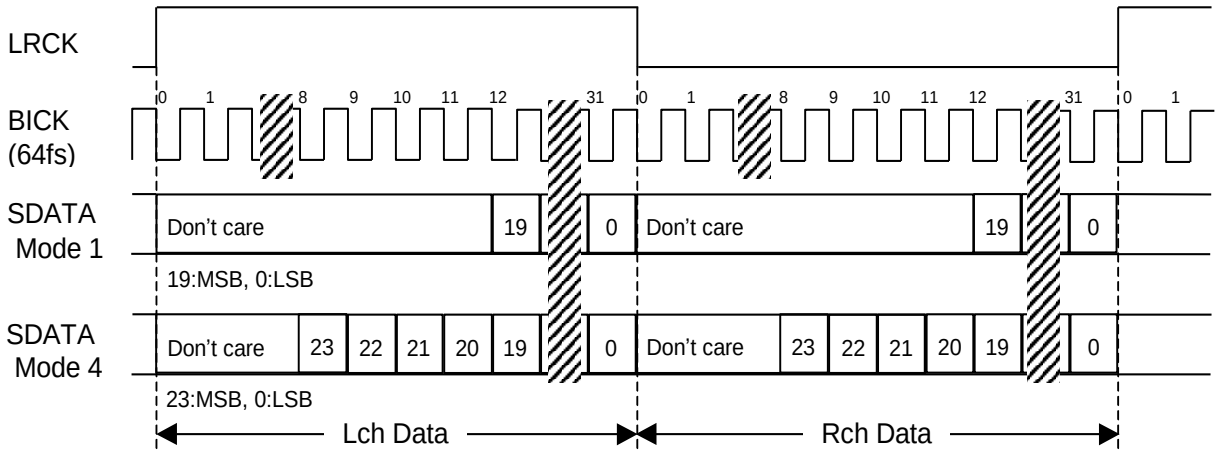



Figure 26. Mode 1, 4 Timing

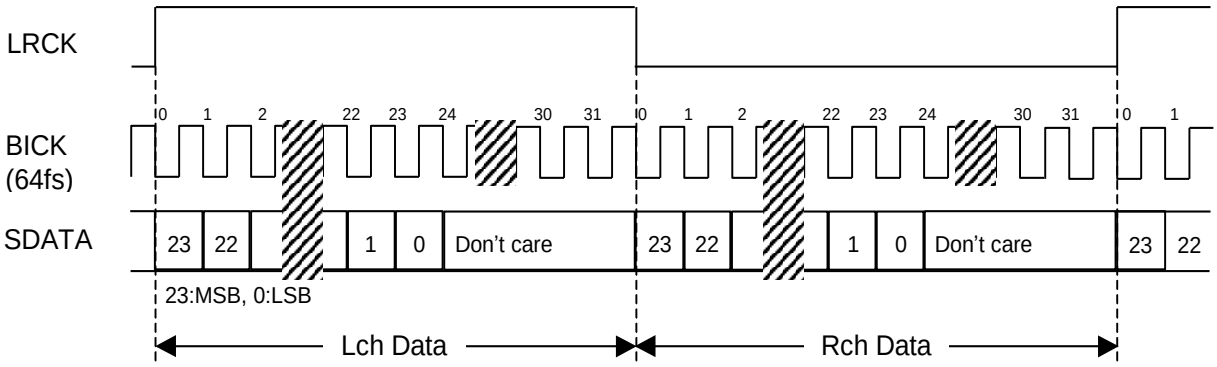



Figure 27. Mode 2 Timing

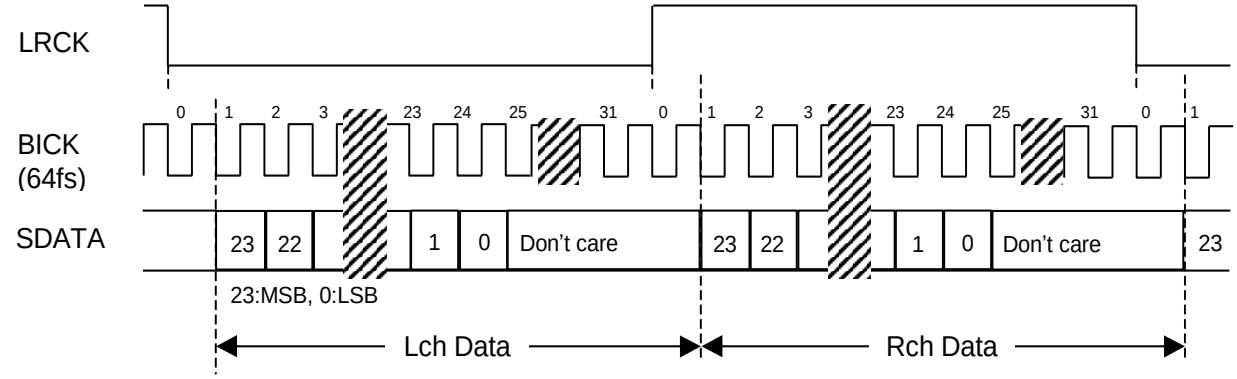



Figure 28. Mode 3 Timing

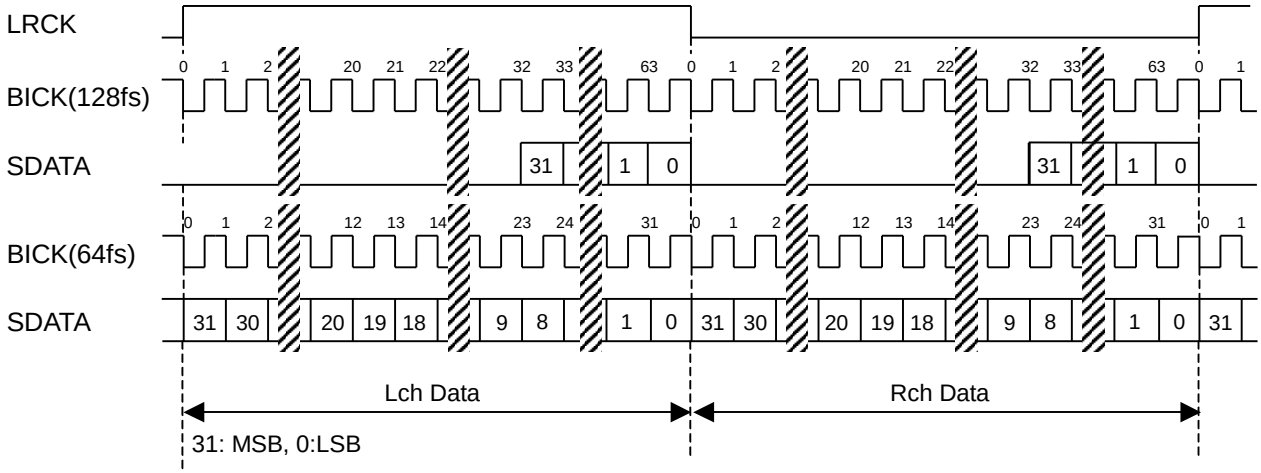



Figure 29. Mode 5 Timing

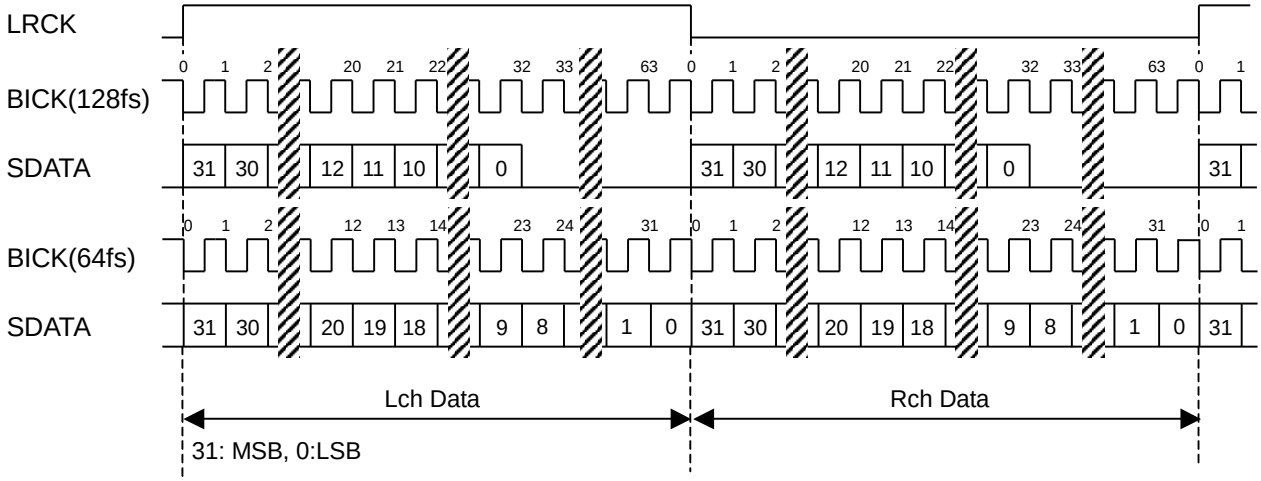



Figure 30. Mode 6 Timing

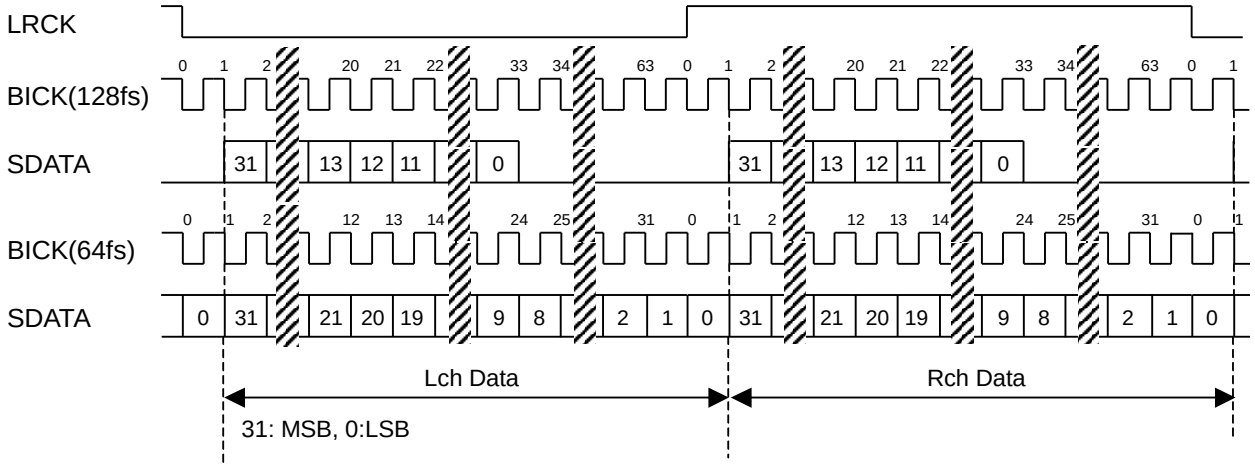



Figure 31. Mode 7 Timing

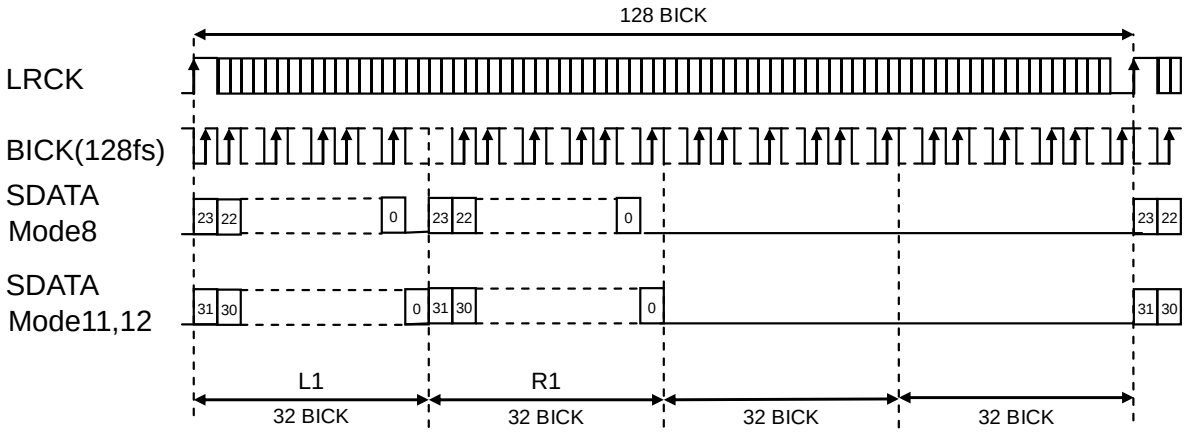



Figure 32. Mode 8/11/12 Timing

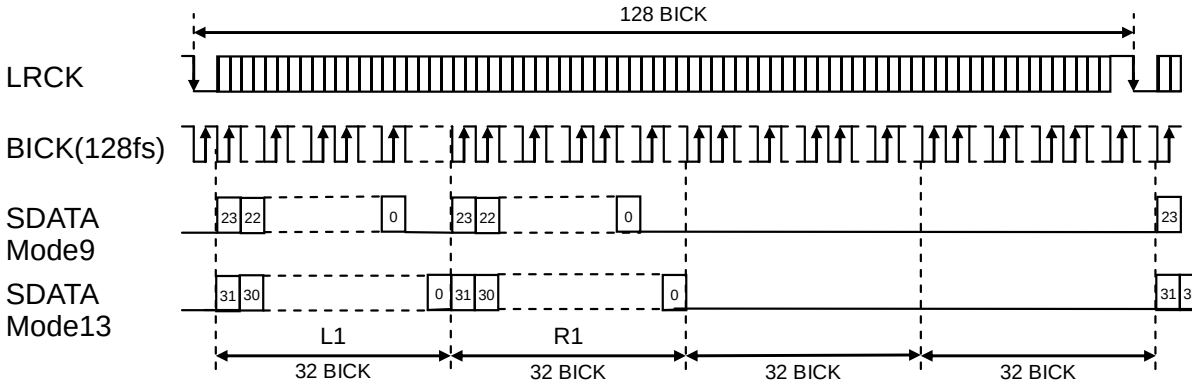



Figure 33. Mode 9/13 Timing

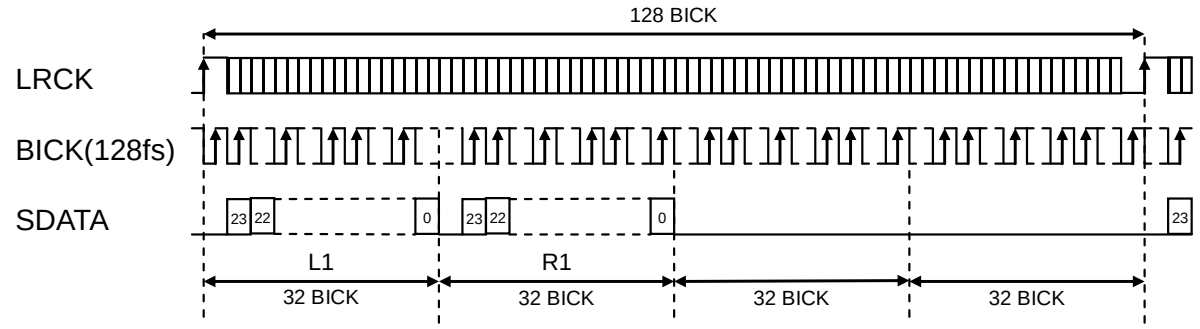



Figure 34. Mode 10 Timing

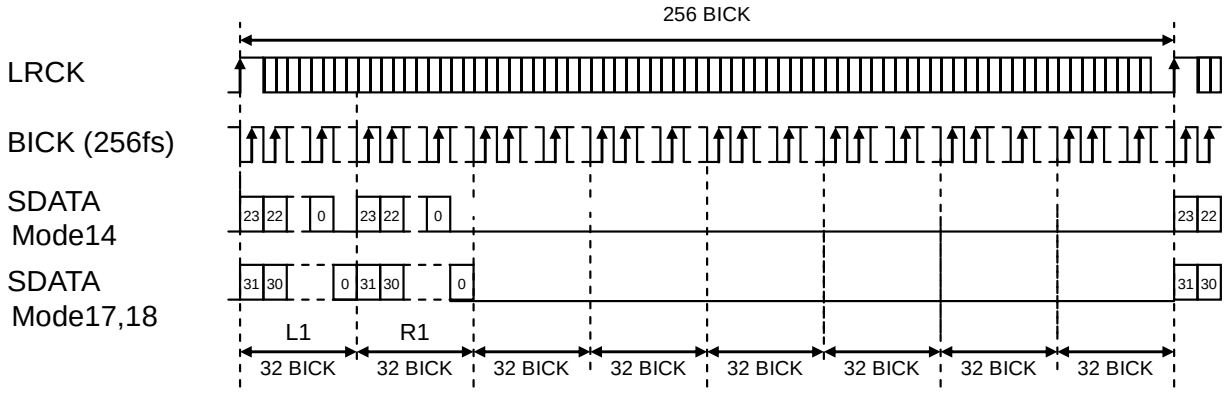



Figure 35. Mode 14/17/18 Timing

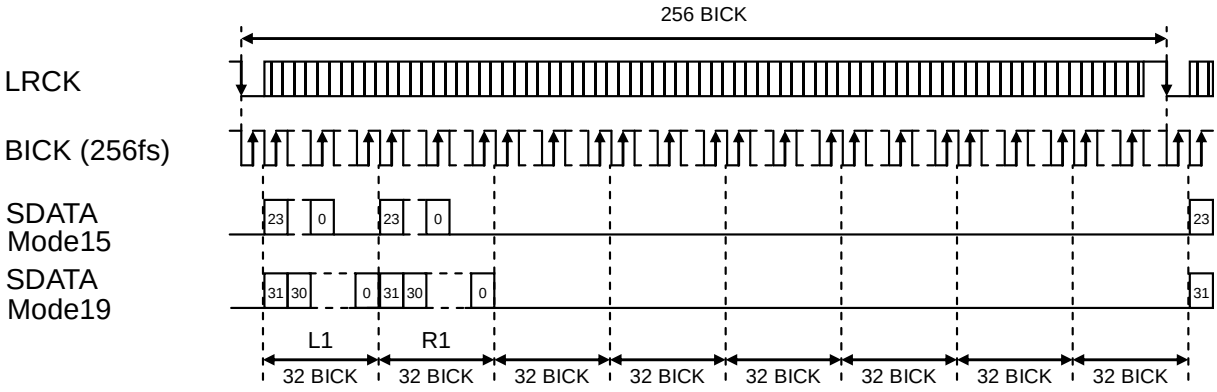



Figure 36. Mode 15/19 Timing

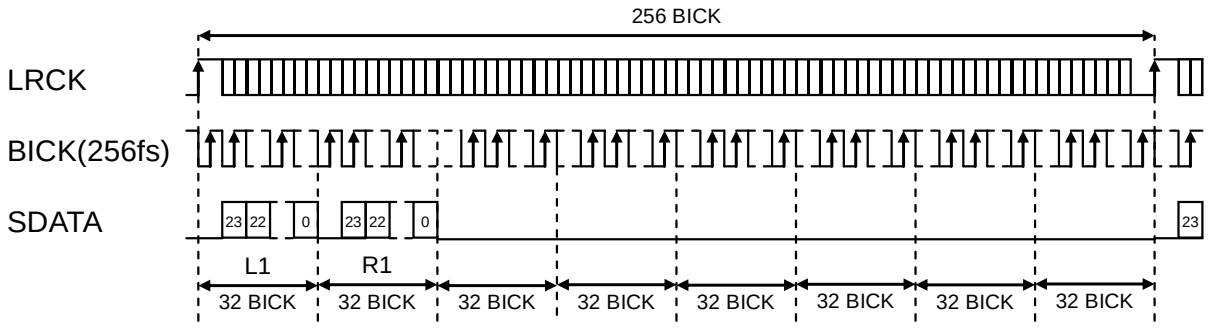



Figure 37. Mode 16 Timing

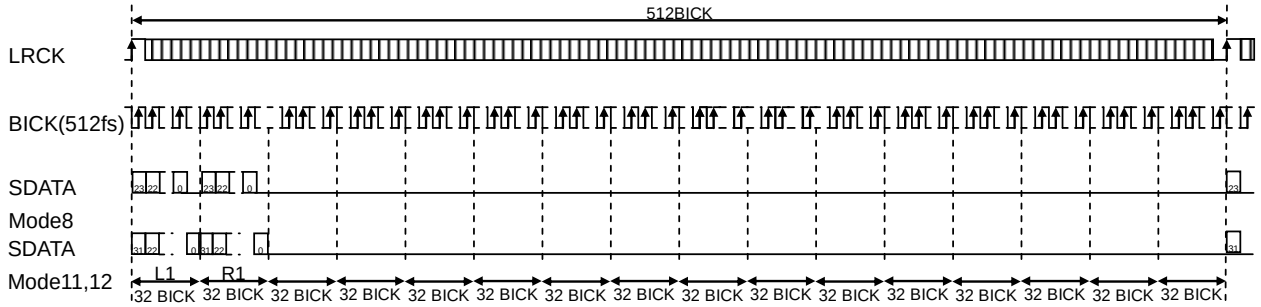



Figure 38. Mode 20/23/24 Timing

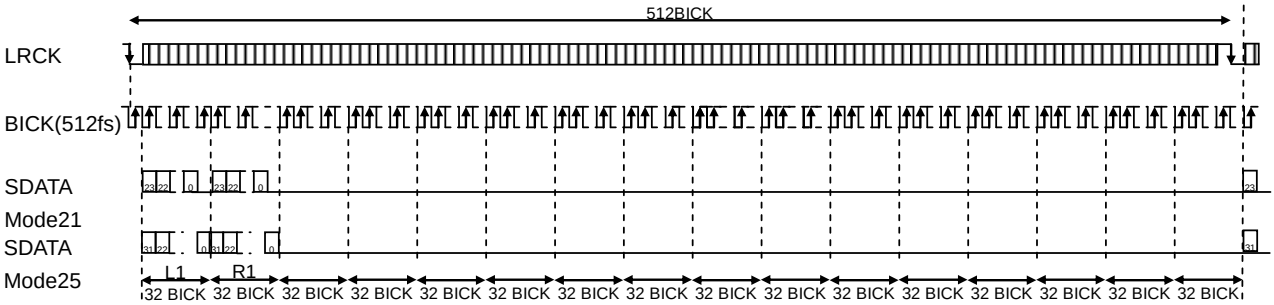



Figure 39. Mode 21/25 Timing

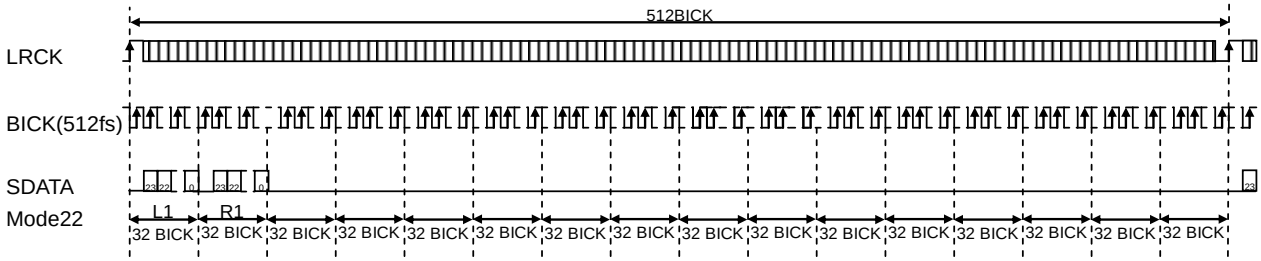



Figure 40. Mode 22 Timing

(2) Data Slot Selection Function

Data slot of 1cycle LRCK for each audio data format is defined as Figure 41 ~ Figure 44. DAC output data can be selected by SDS[2:0] bits as shown in Table 26.

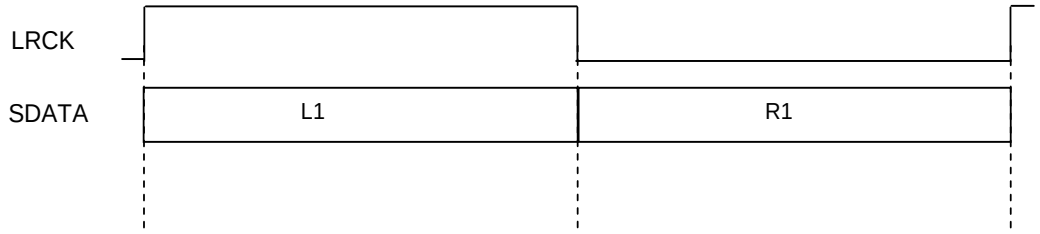



Figure 41. Data Slot in Normal Mode

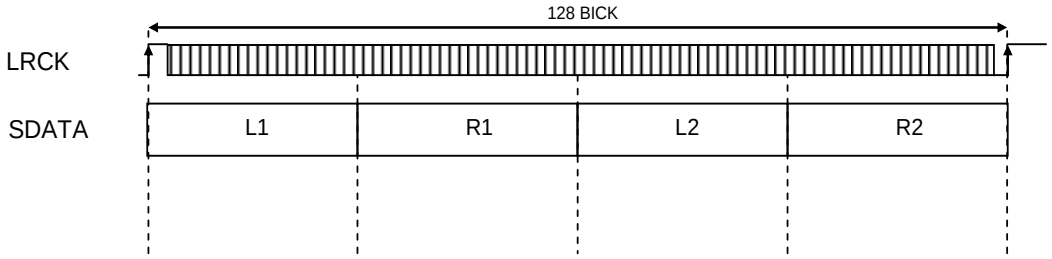



Figure 42. Data Slot in TDM128 Mode

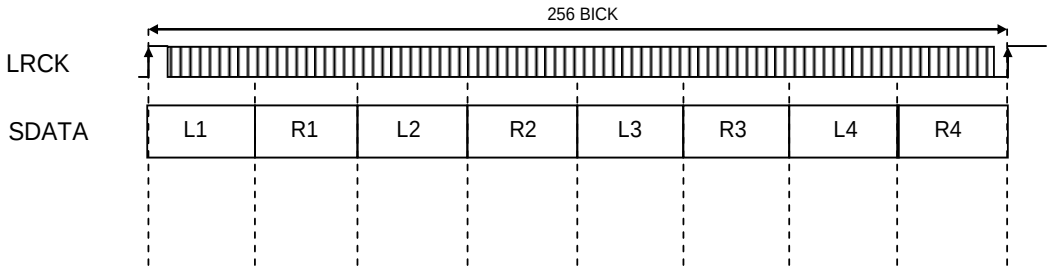



Figure 43. Data Slot in TDM256 Mode

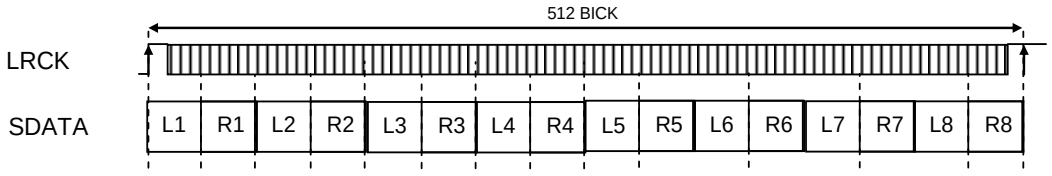



Figure 44. Data Slot in TDM512 Mode

Table 25. Output Data Slot Selection of Each Channel

| | TDM1 | TDM0 | SDS2 | SDS1 | SDS0 | DAC | |
|---|---|---|---|---|---|---|---|
| | | | | | | Lch | Rch |
| Normal | 0 | 0 | x | x | x | L1 | R1 |
| TDM128 | 0 | 1 | x | x | 0 | L1 | R1 |
| | | | x | x | 1 | L2 | R2 |
| TDM256 | 1 | 0 | x | 0 | 0 | L1 | R1 |
| | | | x | 0 | 1 | L2 | R2 |
| | | | x | 1 | 0 | L3 | R3 |
| | | | x | 1 | 1 | L4 | R4 |
| TDM512 | 1 | 1 | 0 | 0 | 0 | L1 | R1 |
| | | | 0 | 0 | 1 | L2 | R2 |
| | | | 0 | 1 | 0 | L3 | R3 |
| | | | 0 | 1 | 1 | L4 | R4 |
| | | | 1 | 0 | 0 | L5 | R5 |
| | | | 1 | 0 | 1 | L6 | R6 |
| | | | 1 | 1 | 0 | L7 | R7 |
| | | | 1 | 1 | 1 | L8 | R8 |

(x: Do not care)

(3) Daisy Chain

The AK4492 supports cascading of multiple devices by daisy chain connection in TDM512/256 mode (TDM[1:0] bits = “10”, “11”). DCHAIN bit or DCHAIN pin controls Daisy Chain mode (Table 26). SDS[2:0] bits setting will be invalid in Daisy Chain mode.

Table 26. Daisy Chain Control

| DCHAIN bit DCHAIN pin | Mode | TDMO pin | |
|---|---|---|---|
| 0 | Normal | L | (default) |
| 1 | Daisy Chain | Data output | |

(3)-1. TDM512 Mode

Figure 45 shows daisy chain connection in TDM512 mode (TDM[1:0] bits = “11”). 16ch data is input to the SDATA pin of the second AK4492 and the TDMO pin of the second AK4492 is connected to the SDATA pin of the first AK4492.

Figure 46 shows data input/output example of daisy chain in TDM512 mode. The second AK4492 receives L8 and R8 data as DAC inputs and outputs the data by shifting 2ch from the TDMO pin. The first AK4492 receives L7 and R7 data as DAC input. Settings of DIF[2:0] bits of the first and second AK4492’s must be the same.

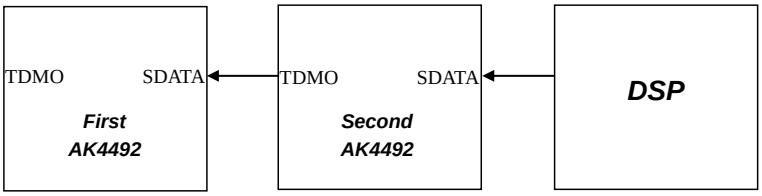



Figure 45. Daisy Chain (TDM512 Mode)

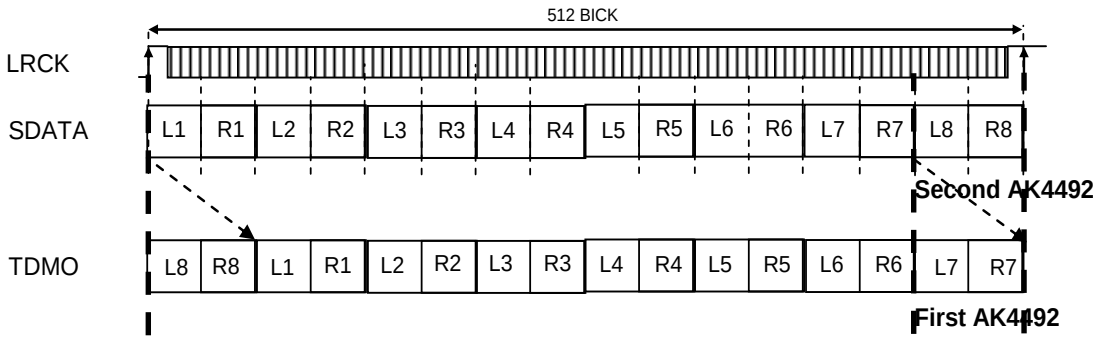



Figure 46. Daisy Chain (TDM512 Mode)

(3)-2. TDM256 Mode
Figure 45 shows daisy chain connection in TDM256 mode (TDM[1:0] bits = “10”). 8ch data is input to the SDATA pin of the second AK4492 and the TDMO pin of the second AK4492 is connected to the SDATA pin of the first AK4492.

Figure 47 shows data input/output example of daisy chain in TDM256 mode. The second AK4492 receives L4 and R4 data as DAC inputs and outputs the data from the TDMO pin by shifting 2ch. The first AK4492 receives L3 and R3 data as DAC input. Settings of DIF[2:0] bits of the first and second AK4492’s must be the same.

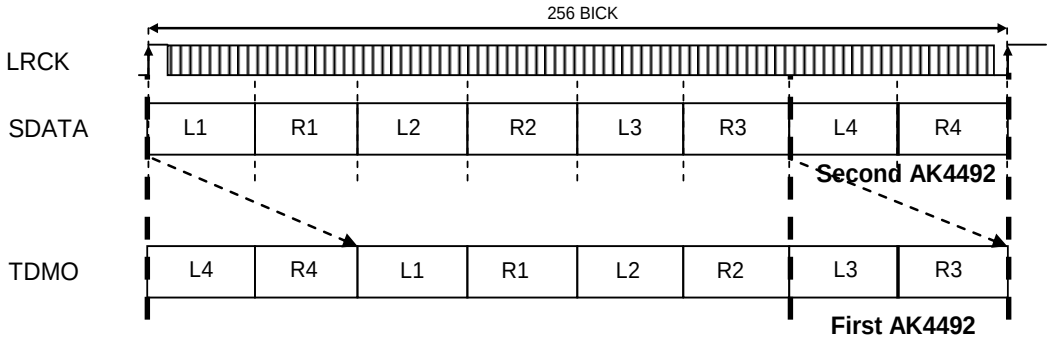



Figure 47. Daisy Chain (TDM256 Mode)

**[2] DSD Mode**
In DSD mode, L channel data and R channel data must be input to the DSDL pin and the DSDR pin, respectively by synchronizing to DCLK. Input pins can be selected by DSDPATH bit. When DSDPATH bit = “0”, the TDM0 pin, the DEM pin and the GAIN pin become DCLK, DSDL and DSDR input pins, respectively. When DSDPATH bit = “1”, the BICK pin, the SDATA pin and the LRCK pin become DCLK, DSDL and DSDR input pins, respectively.

In case of DSD mode, the settings of DIF2-0 pins and DIF[2:0] bits are ignored. The frequency of DCLK is selected between 64fs, 128fs and 256fs by DSDSEL[1:0] bits.
Polarity of DCLK is possible to reverse at DCKB bit.

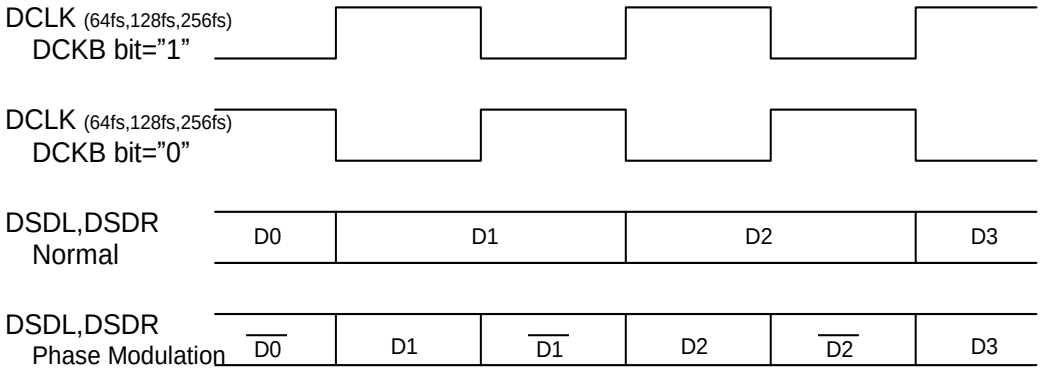



Figure 48. DSD Mode Timing

### [3] External Digital Filter Mode (EXDF Mode)

The audio data is input by BCK and WCK from the DINL and DINR pins. Three formats are available (Table 27) by DIF2-0 bits setting. The data is latched on the rising edge of BCK. The BCK and MCLK clocks must not burst.

Table 27. Audio Interface Format (EXDF Mode)

| Mode | DIF2 | DIF1 | DIF0 | Input Format | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 16-bit LSB justified | |
| 1 | 0 | 0 | 1 | N/A | |
| 2 | 0 | 1 | 0 | 16-bit LSB justified | |
| 3 | 0 | 1 | 1 | N/A | |
| 4 | 1 | 0 | 0 | 24-bit LSB justified | |
| 5 | 1 | 0 | 1 | 32-bit LSB justified | |
| 6 | 1 | 1 | 0 | 24-bit LSB justified | (default) |
| 7 | 1 | 1 | 1 | 32-bit LSB justified | |

(N/A: Not available)

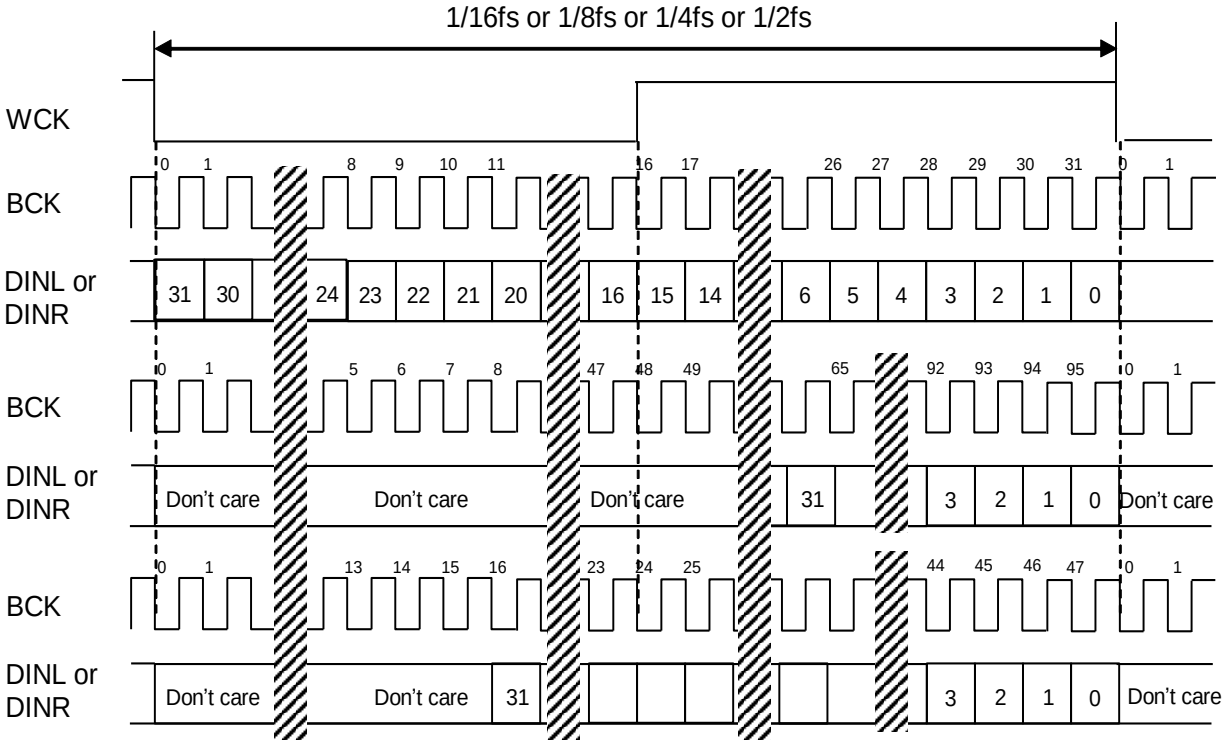



Figure 49. EXDF Mode Timing

## ■ Digital Filter

Six types of digital filter in PCM mode and two types of digital filter in DSD mode are available in the AK4492 for sound color selection of music playback.

In PCM mode, digital filter can be selected by the SD, SLOW and SSLOW pins if the AK4492 is in pin control mode, and digital filter can be selected by SD, SLOW and SSLOW bits in register control mode (Table 28).

Table 28. Digital Filter Setting

| SSLOW | SD | SLOW | Mode | |
|---|---|---|---|---|
| 0 | 0 | 0 | Sharp roll-off filter | |
| 0 | 0 | 1 | Slow roll-off filter | |
| 0 | 1 | 0 | Short delay sharp roll-off filter | (default) |
| 0 | 1 | 1 | Short delay slow roll-off filter | |
| 1 | 0 | 0 | Super slow roll-off filter | |
| 1 | 0 | 1 | Super slow roll-off filter | |
| 1 | 1 | 0 | Low dispersion Shot delay filter) | |
| 1 | 1 | 1 | N/A | |

Note 51. Do not use Reserved mode (SSLOW bit= “1”, SD bit= “1”, SLOW bit= “1”) in PCM mode.

In DSD mode, the cutoff frequency of digital filter can be switched by DSDF bit. Table 29 shows the cutoff frequency of fs = 44.1 kHz. The cutoff frequency tracks the sampling frequency (fs). Do not set GC[2:0] bits to “100” when DSDD bit = “0” and DSDF bit = “1”. Otherwise a pop noise may occur.

Table 29. DSD Filter Select

| DSDF bit | Cut Off Frequency @fs=44.1kHz, | | | |
|---|---|---|---|---|
| | DSD64fs | DSD128fs | DSD256fs | |
| 0 | 39 kHz | 78 kHz | 156 kHz | (default) |
| 1 | 76 kHz | 152 kHz | 304 kHz | |

## ■ De-emphasis Filter (PCM Mode)

A digital de-emphasis filter is available for 32kHz, 44.1kHz or 48kHz sampling rates (tc = 50/15μs) and is enabled or disabled by DEM1-0 pins or DEM1-0 bits. When DSD mode or EXDF mode, DEM1-0 bits are ignored. The setting value is held even if PCM, DSD and EXDF mode is switched.

Table 30. De-emphasis Control (Register Control mode)

| DEM1 | DEM0 | Mode | |
|---|---|---|---|
| 0 | 0 | 44.1kHz | |
| 0 | 1 | OFF | (default) |
| 1 | 0 | 48kHz | |
| 1 | 1 | 32kHz | |

Table 31. De-emphasis Control (Pin Control mode)

| DEM0 Pin | Mode | |
|---|---|---|
| L | 44.1kHz | |
| H | OFF | (default) |

## ■ Output Volume (PCM Mode, DSD Mode, EXDF Mode)

The AK4492 includes channel independent digital output volumes (ATTL/R) with 256 levels at 0.5dB step including MUTE. When changing output levels, it is executed in soft transition thus no switching noise occurs during these transitions. It can attenuate the input data from 0dB to -127dB and mute when assuming the output signal level is 0dB when ATTL/R[7:0] bits = “FFH”.

Table 32. Attenuation level of Digital Attenuator

| ATTL/R[7:0]bits (register 03-04H) | Attenuation Level | |
|---|---|---|
| FFH | +0 dB | (default) |
| FEH | -0.5 dB | |
| FDH | -1.0 dB | |
| : | : | |
| 02H | -126.5 dB | |
| 01H | -127.0 dB | |
| 00H | MUTE (-∞) | |

The transition time of digital output volume is set by ATS[1:0] bits (Table 33). When changing output levels between Mode0-3, it is executed in soft transition thus no switching noise occurs during these transitions. Register setting values will be kept even switching the PCM and DSD modes.

Table 33. Transition Time between Set Values of ATT[7:0] bits

| Mode | ATS1 | ATS0 | ATT speed | | | |
|---|---|---|---|---|---|---|
| | | | EXDF bit = “0”, DP bit = “0” | EXDF bit = “1” DP bit = “0” | DP bit = “1” | |
| 0 | 0 | 0 | 4080/fs | 4080*WCK Cycle | 4080/(2*fs) | (default) |
| 1 | 0 | 1 | 2040/fs | 2040*WCK Cycle | 2040/(2*fs) | |
| 2 | 1 | 0 | 510/fs | 510*WCK Cycle | 510/(2*fs) | |
| 3 | 1 | 1 | 255/fs | 255*WCK Cycle | 255/(2*fs) | |

It takes 4080/fs (92.5ms@fs=44.1kHz) from “FFH” (0dB) to “00H” (MUTE) in Mode 0. The attenuation level is initialized to “FFH” (0dB) by setting the PDN pin = “L”.

If the volume is changed during reset period, the output volume will become a setting value after releasing the reset. It will change to a setting value immediately if the volume is changed within 5/fs after releasing reset.

## ■ Gain Adjustment Function (PCM Mode, DSD Mode, EXDF Mode)

The AK4492 has the gain adjustment function. The analog output amplitude can be adjusted by GC[2:0] bits or the GAIN pin.

Table 34. Output Level between Set Values of GC[2:0] bits

| GC[2] bit | GC[1] bit | GC[0] bit | AOUTLP/LN/RP/RN Output Level | | | |
|---|---|---|---|---|---|---|
| | | | PCM | DSD: Normal Path | DSD: Volume Bypass | |
| 0 | 0 | 0 | 2.8 Vpp | 2.8 Vpp | 2.5 Vpp | (default) |
| 0 | 0 | 1 | 2.8 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 0 | 1 | 0 | 2.5 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 0 | 1 | 1 | 2.5 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 1 | 0 | 0 | 3.75 Vpp | 3.75 Vpp | 2.5 Vpp | |
| 1 | 0 | 1 | 3.75 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 1 | 1 | 0 | 2.5 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 1 | 1 | 1 | 2.5 Vpp | 2.5 Vpp | 2.5 Vpp | |

Table 35. Output Level between Set Values of GAIN pin (Valid Only in PCM Mode)

| GAIN pin | AOUTLP/LN/RP/RN Output Level |
|---|---|
| L | 2.8 Vpp |
| H | 3.75 Vpp |

Note 52. DSDF bit must be set to “0” if GC[2:0] bits are set to “100” when using DSD Normal Path. Click noise may occur if DSDF bit is set to “1”.

## ■ Zero Detection (PCM Mode, DSD Mode, EXDF Mode)

The AK4492 has a channel-independent zero detect function. When the input data at each channel is continuously zeros for 8192 LRCK cycles, the DZF pin of each channel outputs zero detection flag independently. Polarity of the detection flag of the DZFL/R pin can be selected by DZFB bit. The DZFL/R pin goes “H” for zero detection when DZFB bit = “0”, the DZFL/R pin goes “L” when DZFB bit = “1”.

When DZFB bit = “0”, the DZFL/R pin immediately returns to “L” if the input data of each channel is not zero after going to “H”. If the RSTN bit is “0”, the DZF pins of both L and R channels go to “H”. The DZFL/R pin returns to “L” in 4 ~ 5/fs after the input data of each channel becomes “1” when RSTN bit is set to “1”.

If DZFM bit is set to “1” while DZFB bit = “0”, the DZF pins of both L and R channels go to “H” only when the input data for both channels are continuously zeros for 8192 LRCK cycles. The zero detect function can be disabled by setting the DZFE bit. In this case, DZF pins of both channels are always “L”. The zero detect function is also disabled when Volume Bypass is selected in DSD mode (Table 22).

Table 36. Zero Detect Select.

| DZFE | DZFB | RSTN | Data | DZF pin |
|---|---|---|---|---|
| 0 | 0 | - | - | L |
| | 1 | - | - | H |
| 1 | 0 | 0 | - | H |
| | | 1 | not zero | L |
| | | | zero detect | H |
| | 1 | 0 | - | L |
| | | 1 | not zero | H |
| | | | zero detect | L |

(-: Do not care)

## ■ L/R Channel Output Signal Select, Phase Inversion Function (PCM Mode, DSD Mode, EXDF Mode)

In register control mode, input and output combination of the AK4492 can be changed by MONO bit and SELLR bit. In addition, the output signal phase can be inverted by INVL bit and INVR bit. These functions are available on all audio formats. In pin control mode, the phase of R channel output can be inverted by setting the INVR pin.

Table 37. Output Select (Register Control)

| MONO bit | SELLR bit | INVL bit | INVR bit | Lch Out | Rch Out |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Lch In | Rch In |
| | | 0 | 1 | Lch In | Rch In Invert |
| | | 1 | 0 | Lch In Invert | Rch In |
| | | 1 | 1 | Lch In Invert | Rch In Invert |
| 0 | 1 | 0 | 0 | Rch In | Lch In |
| | | 0 | 1 | Rch In | Lch In Invert |
| | | 1 | 0 | Rch In Invert | Lch In |
| | | 1 | 1 | Rch In Invert | Lch In Invert |
| 1 | 0 | 0 | 0 | Lch In | Lch In |
| | | 0 | 1 | Lch In | Lch In Invert |
| | | 1 | 0 | Lch In Invert | Lch In |
| | | 1 | 1 | Lch In Invert | Lch In Invert |
| 1 | 1 | 0 | 0 | Rch In | Rch In |
| | | 0 | 1 | Rch In | Rch In Invert |
| | | 1 | 0 | Rch In Invert | Rch In |
| | | 1 | 1 | Rch In Invert | Rch In Invert |

Table 38. Output Select (Pin Control)

| INVR pin | Lch Out | Rch Out |
|---|---|---|
| 0 | Lch In | Rch In |
| 1 | Lch In | Rch In Invert |

## ■ DSD Signal Full Scale (FS) Detection

The AK4492 has independent full scale detection function for each channel in DSD mode.
The AK4492 detects full scale signal when the DSDL/R input data is continuously "0" (-FS) or "1" (+FS) for 2048 cycles and the detection flag for corresponding channel (DML or DMR bit) becomes "1". DML and DMR bits can be read out at the register address "06H".

When the AK4492 detects full scale signal while DDM bit = "1", the analog output is muted according to Table 39. ATS[2:0] bits control a mute transition time. ATS[2:0] bits and DSDD bit settings are also valid when the AK4492 returns to normal status from full scale detection status.

The recovery timing from full scale detection status and the operation mode of full scale detection are controlled by DDM bit, DMC bit and DMRE bit. RSTN bit must be set to "0" when changing DDM bit setting.

Table 39. DSD Mode and Device Status after Full-Scale Detection (DDM bit= "1")

| DSDD | Mode | Analog Output | Mute Transition Method | |
|---|---|---|---|---|
| 0 | Normal Path | VCML/R (Mute) | Soft Mute | (default) |
| 1 | Volume Bypass | VCML/R (Mute) | Rapid Mute | |

Table 40. Recovery Method to Normal Operation Mode from Full Scale Detection Status

| DDM | DMC | DMRE | Status After Detection | |
|---|---|---|---|---|
| 0 | x | x | When full scale is detected, Mute function is disabled. | (default) |
| 1 | 0 | x | When full scale is detected, Mute function is enabled. The AK4492 returns to normal operation automatically by a normal signal input. | |
| 1 | 1 | 0 | When full scale is detected, Mute function is enabled. The AK4492 keeps mute mode, even if a normal signal is input. | |
| 1 | 1 | 1 (Note 53) | When full scale is detected, Mute function is enabled. The AK4492 returns to normal operation when a normal signal is input and DMRE bit is set to "1". | |

(x: Do not care)

Note 53. DMRE bit returns to "0" automatically after the AK4492 returns to normal operation.

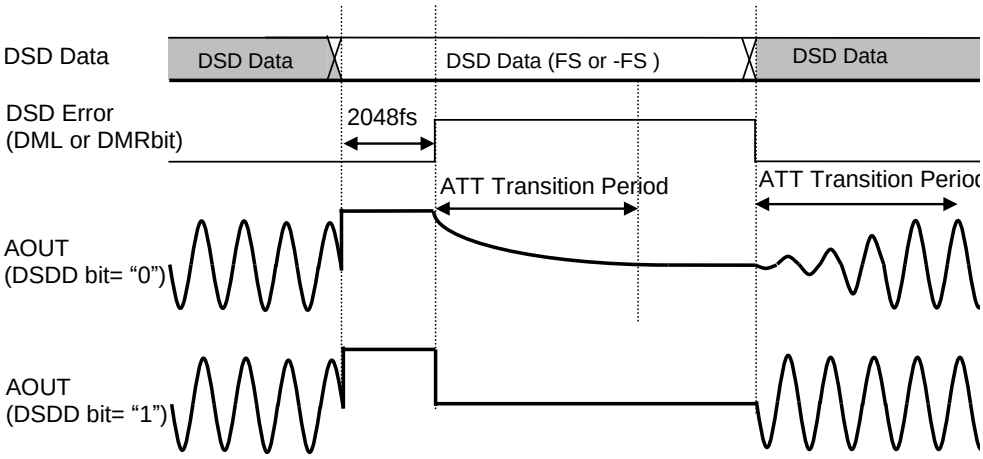



Figure 50. Analog Output Waveform in DSD FS Detection (DMC bit= “0”)

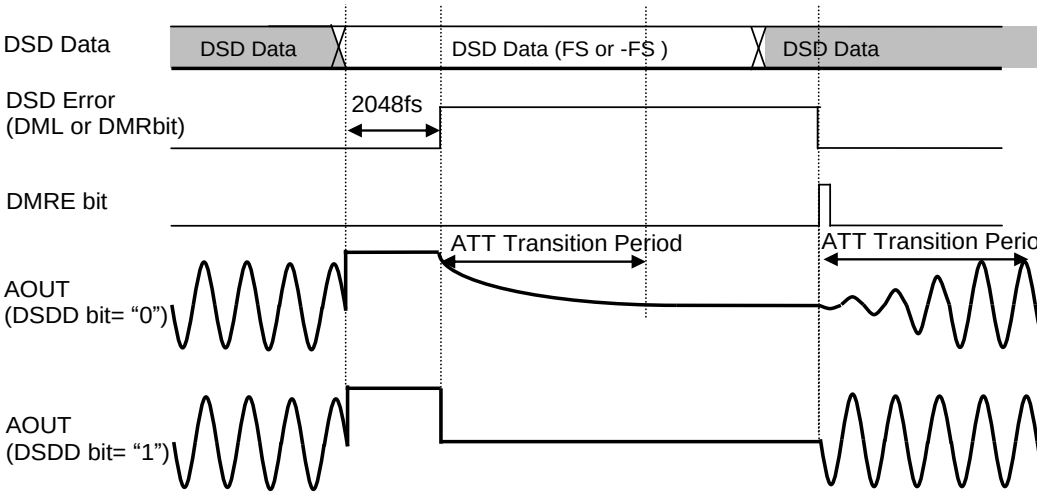



Figure 51. Analog Output Waveform in DSD FS Detection (DMC bit= “1”)

## ■ Soft Mute Operation (PCM Mode, DSD Mode, EXDF Mode)

The soft mute operateion is performed at digital domain. When the SMUTE pin goes to “H” or the SMUTE bit set to “1”, the output signal is attenuated by −∞ during ATT_DATA × ATT transition (1setting per 16/fs) time from the current ATT level.
When the SMUTE pin is returned to “L” or the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time(Refer to Table 33 for ATT). If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

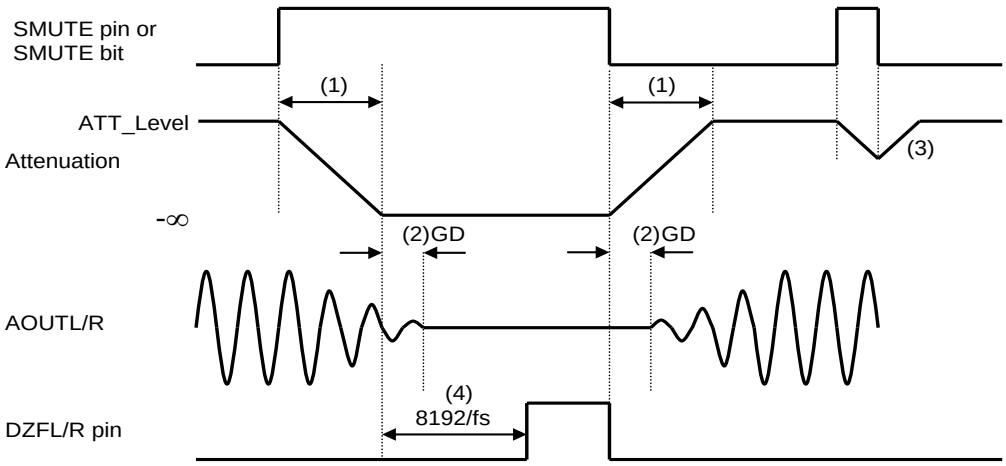



Figure 52. Soft Mute Function

Note:
(1) ATT_DATA × ATT transition time. For example, this time is 4080LRCK cycles at ATT_DATA=255 in PCM Normal Speed Mode.
(2) The analog output corresponding to the digital input has group delay (GD).
(3) If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.
(4) When the input data for each channel is continuously zeros for 8192 LRCK cycles, the DZF pin for each channel goes to “H”. The DZF pin immediately returns to “L” if the input data is not zero.

## ■ LDO

When TVDD = 3.0 ~3.6V, the power for digital core circuit (DVDD) is supplied by the internal LDO by setting the LDOE pin to “H”. Table 41 shows the DVDD pin statuses with the PDN and LDOE pins setting. The internal LDO is powered up by setting the PDN pin from “L” to “H” (power-down release) and it starts supping 1.8V DVDD. It takes 0.1ms (max.) to power-up the internal LDO.

Table 41. LDO Select Mode

| PDN pin | LDOE pin | TVDD | DVDD |
|---|---|---|---|
| X | L | 1.7~3.6 V | LDO OFF: Supply 1.7 ~ 1.98V to the DVDD pin externally |
| L | H | 3.0~3.6 V | 500 ohm Pull Down |
| H | H | 3.0~3.6 V | LDO ON: LDO outputs 1.8V.<br>(Do not connect DVDD with other devices.) |

(X: Do not care)

The AK4492 has error detect function as shown in Table 42 for LDO operation (LDOE pin = “H”). The internal LDO will be powered down and stop supplying the power to the digital core when an error is detected. In this case, the analog signal output becomes unstable. The AK4492 must be reset by setting the PDN pin = “L” → “H” to recover from the error detection status.

Table 42. Error Detection

| No | Error | Error Detection Condition |
|---|---|---|
| 1 | Internal Reference Voltage | Internal reference voltage does not rise. |
| 2 | LDO Over Voltage Detection | Threshold is from 2.2V to 2.5V. |
| 3 | LDO Over Current Detection | LDO current is 40mA or less, or 110mA or more. |

## ■ Shutdown Switch

A shutdown switch is placed between the DVSS pin and VSS for the digital core to prevent SIDD leak of DVDD digital power supply. The on-resistance is maximum 1Ω and the DVDD leak current will be 2uA at the maximum.

When using LDO (LDOE pin = “H”), the shutdown switch is ON after counting by internal oscillator following a power-down release (PDN pin “L” → “H”). It takes 2ms (max.) for the shutdown switch power-up.
When not using LDO (LDOE pin = “L”), the shutdown switch is ON immediately after a power-down release (PDN pin “L” → “H”). It takes 1us (max.) for the shutdown switch power-up.

## ■ Power Up/Down Function

The AK4492 is powered down by setting the PDN pin to “L”. In power-down state, all circuits stop operation and initialized, and the analog output becomes floating (Hi-z) state. The PDN pin must held “L” for more than 150ns for a certain reset. There is a possibility of malfunctions with the “L” pulse less than 150ns. Power-down is released by setting the PDN pin to “H” from “L”. In this time IREF and LDO (if LDOE pin = “H”) are powered up and the analog output becomes floating (Hi-z) state. The Analog common voltage power up after by PDN pin to “H”. The time to be stable voltage is in propotional to the capacitance of the VCML pin and the VCMR pin. For example, when the capacitance is 1uF, the time constant is about 3ms.

(1) Pin Control Mode (PSN pin = “H”)

All circuits will be powered up by inputting MCLK, LRCK and BICK clocks after the PDN pin = “H”. The analog circuit starts operation just after supplying all necessary clocks (MCLK, LRCK and BICK) and the digital circuit starts operation about 4/fs after the clock supply. Figure 53 shows system timing example of power down/up when using the internal LDO (LDOE pin “H”). When power up the AK4492 with the LDOE pin = “H”, 3.3V power supplies (AVDD and TVDD) should be powered up before or at the same time of 5V power supplies (VDDL/R).

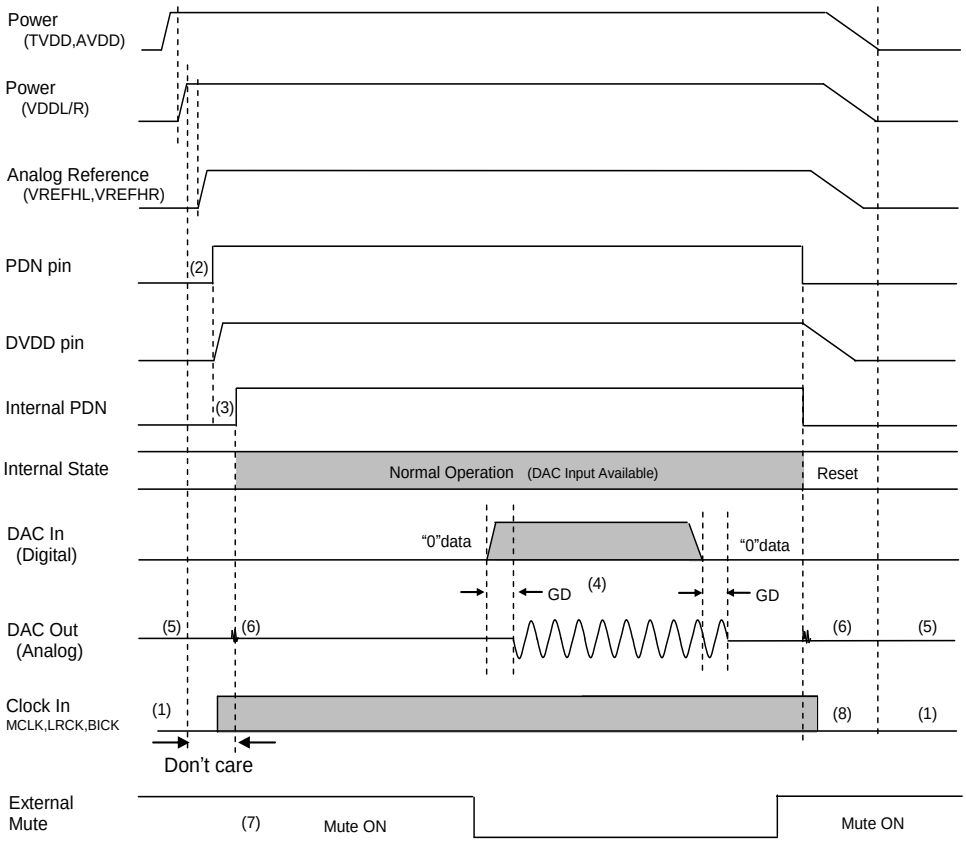



Figure 53. Power-down/up Sequence Example (PinControl Mode, LDOE pin = “H”)

Notes:

(1) Do not input a clock when power supplies are powered down.
(2) The PDN pin must be held “L” for more than 150ns after AVDD, TVDD and VDDL/R reached 90%.
(3) Internal LDO is powered up after the PDN pin = “H” when the LDOE pin= “H”. The internal circuit will starts operation after the shutdown switch is ON (max. 2ms) following the internal oscillator count up.
(4) The analog output corresponding to the digital input has group delay (GD).
(5) Analog outputs are floating (Hi-Z) in power down mode.
(6) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.

(7) Mute the analog output externally if click noise (6) adversely affect system performance.

(8) Clock inputs (MCLK, BICK and LRCK) can be stopped in power down state.

The timing example when not using the internal LDO (LODE pin = “L”) is shown in Figure 54. When the LDOE pin= “L”, 1.8V (DVDD), 3.3V (AVDD, TVDD) and 5V (VDDL, VDDR) power supplies should be powered up at the same time, otherwise power up 3.3V power supplies (AVDD, TVDD) first, the 1.8V power supply (DVDD) next and 5V power supplies (VDDL/R) last.

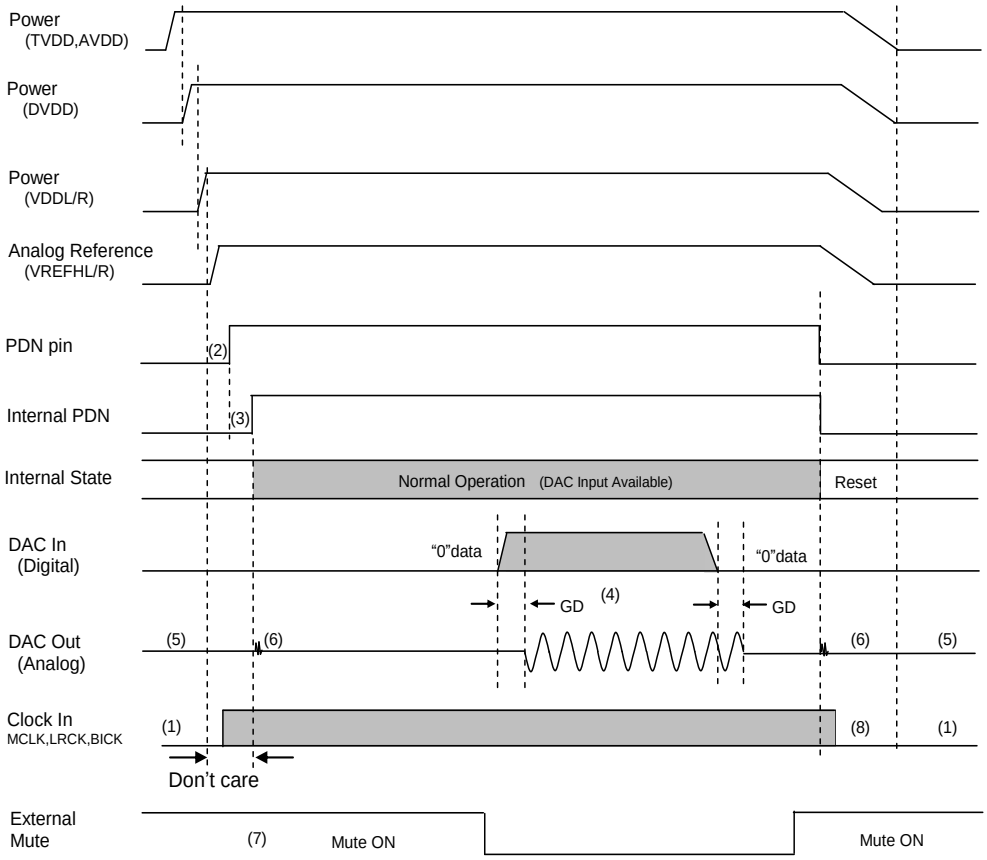



Figure 54. Power-down/up Sequence Example (Pin Control Mode, LDOE pin=“L”)

Notes:

(1) Do not input a clock when power supplies are powered down.
(2) The PDN pin must be held “L” for more than 150ns after AVDD, TVDD, DVDD and VDDL/R reached 90%.
(3) Internal shutdown switch is powered up after the PDN pin = “H” when the LDOE pin= “L”. The internal circuit will start operation after the shutdown switch is ON (max. 1us).
(4) The analog output corresponding to the digital input has group delay (GD).
(5) Analog outputs are floating (Hi-Z) in power down mode.
(6) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(7) Mute the analog output externally if click noise (6) adversely affect system performance.
(8) Clock inputs (MCLK, BICK and LRCK) can be stopped in power down state.

(2) Register Control Mode (PSN pin= “L”)

A register access becomes available after the PDN pin = “H”. The analog circuit starts operation by supplying necessary clocks (MCLK, LRCK and BICK for PCM mode, MCLK and DCLK for DSD mode, MCLK, BCK and WCK for EXDF mode) and the clock divider is powered up about after 4/fs. The analog output pins output analog common voltages (VCML, VCMR) in this time. Then the AK4492 transitions to normal operation by setting RSTN bit = “1”. When power up the AK4492 with the LDOE pin = “H”, 3.3V power supplies (AVDD and TVDD) should be powered up before or at the same time of 5V power supplies (VDDL/R).

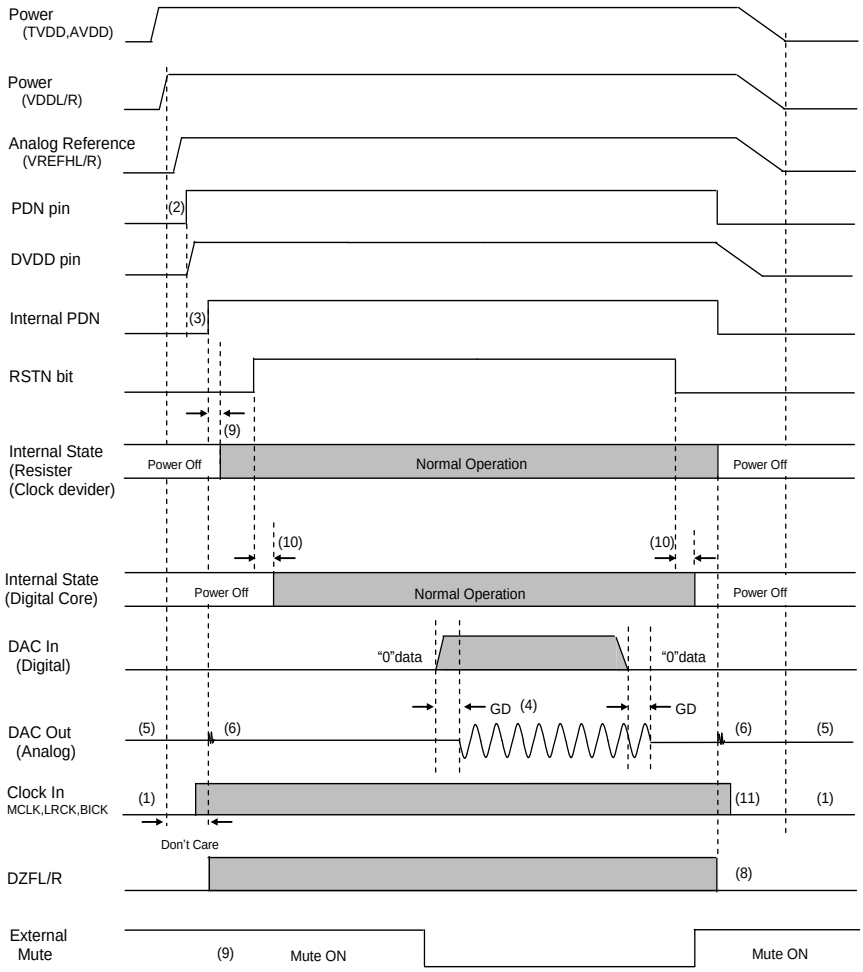



Figure 55. Power-down/up Sequence Example (Resister Control Mode, LDOE pin= “H”)

Notes:

(1) Do not input a clock when power supplies are powered down.
(2) The PDN pin must be held “L” for more than 150ns after AVDD, TVDD and VDDL/R reached 90%.
(3) Internal LDO is powered up after the PDN pin = “H” when the LDOE pin= “H”. The internal circuit will starts operation after the shutdown switch is ON (max. 2ms) following the internal oscillator count up.
(4) The analog output corresponding to the digital input has group delay (GD).
(5) Analog outputs are floating (Hi-Z) in power down mode.
(6) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(7) Mute the analog output externally if click noise (6) adversely affect system performance.
(8) The DZFL/R pin is “L” in power-down mode (PDN pin = “L”).
(9) The clock divider is powered up in about 4/fs after the internal PDN is released.
(10) It takes 3~4/fs until a reset instruction is valid when writing RSTN bit to “0” and it takes 2~3/fs when releasing the reset.
(11) Clock inputs (MCLK, BICK and LRCK) can be stopped in power down state.

The system timing example of power up/down when not using LDO (LODE pin = “L”) is shown in Figure 56. When the LDOE pin= “L”, 1.8V (DVDD), 3.3V (AVDD, TVDD) and 5V (VDDL, VDDR) power supplies should be powered up at the same time, otherwise power up the 3.3V power supplies (AVDD, TVDD) first, 1.8V power supply (DVDD) next and 5V power supplies (VDDL/R) last.

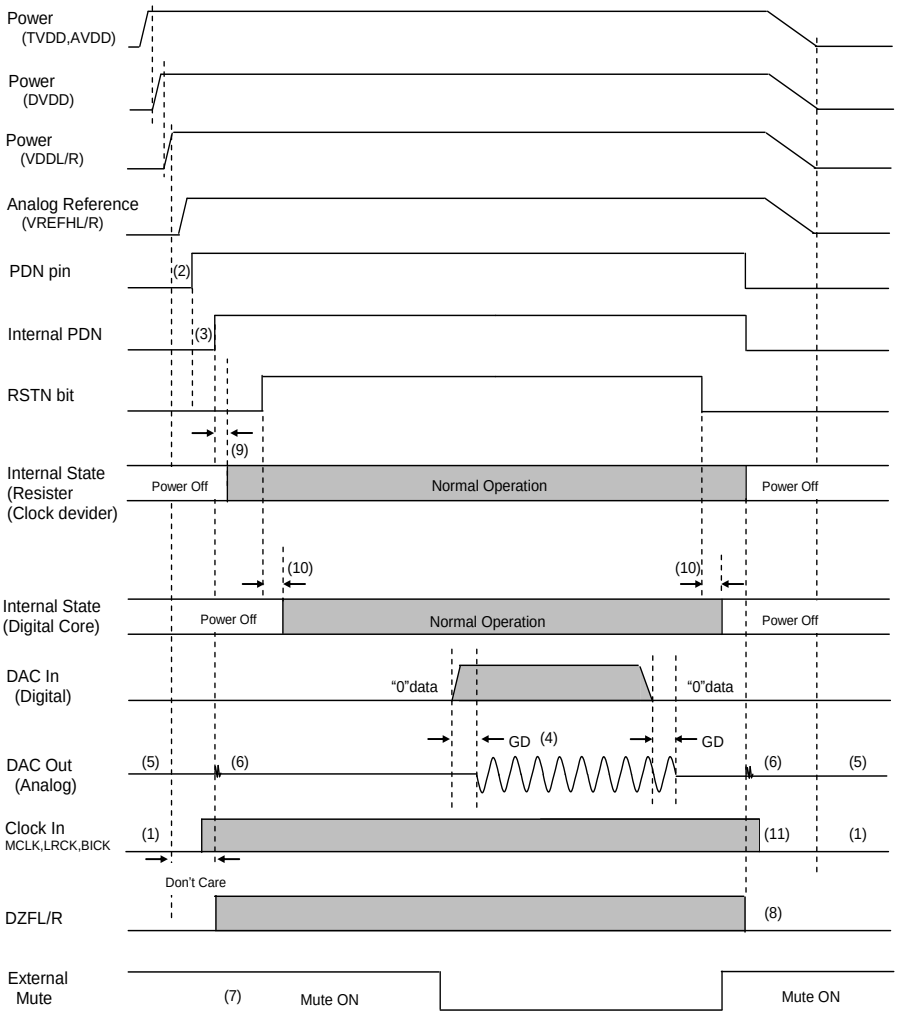



Figure 56. Power-down/up Sequence Example (Resister Control Mode, LDOE pin = “L”)

Notes:

(1) Do not input a clock when power supplies are powered down.
(2) The PDN pin must be held “L” for more than 150ns after AVDD, TVDD and VDDL/R reached 90%.
(3) Internal shutdown switch is powered up after the PDN pin = “H” when the LDOE pin= “L”. The internal circuit will start operation after the shutdown switch is ON (max. 1us).
(4) The analog output corresponding to the digital input has group delay (GD).
(5) Analog outputs are floating (Hi-Z) in power down mode.
(6) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(7) Mute the analog output externally if click noise (6) adversely affect system performance.
(8) The DZFL/R pin is “L” in power-down mode (PDN pin = “L”).
(9) The clock divider is powered up in about 4/fs after the internal PDN is released.
(10) It takes 3~4/fs until the internal RSTN is changed when changing RSTN bit to “0” and it takes 2~3/fs when changing RSTN bit to “1”.
(11) Clock inputs (MCLK, BICK and LRCK) can be stopped in power down state.

## ■ Power-OFF/Reset Function

Power-off and Reset function of the AK4492 are controlled by PW bit, RSTN bit and MCLK (Table 43).

Table 43. Power Off, Reset Function

| Mode | PDN Pin | MCLK Supply | PW bit | RSTN bit | DIGITAL Block | ANALOG Block | LDO Register | Analog Output |
|---|---|---|---|---|---|---|---|---|
| Power Down | L | – | – | – | OFF | OFF | OFF | Hi-Z |
| MCLK Stop | H | No | – | – | OFF | OFF | ON | Hi-Z |
| Power OFF | H | Yes | 0 | – | OFF | OFF | ON | Hi-Z |
| Reset | H | Yes | 1 | 0 | OFF | ON | ON | VCML/R |
| Normal Operation | H | Yes | 1 | 1 | ON | ON | ON | Signal output |

(- : Do not care)

### [1] Power ON/OFF by MCLK Clock

The AK4492 detects a clock stop and all circuits including MCLK stop detection circuit, control register and IREF (except LDO when the LDOE pin = "H") stop operation if MCLK is not input for 1us (min.) during operation (PDN pin = "H"). In this case, the analog output goes floating state (Hi-Z). The AK4492 returns to normal operation if PW bit and RSTN bit are "1" after starting to supply MCLK again. The zero detect function is disabled when MCLK is stopped.

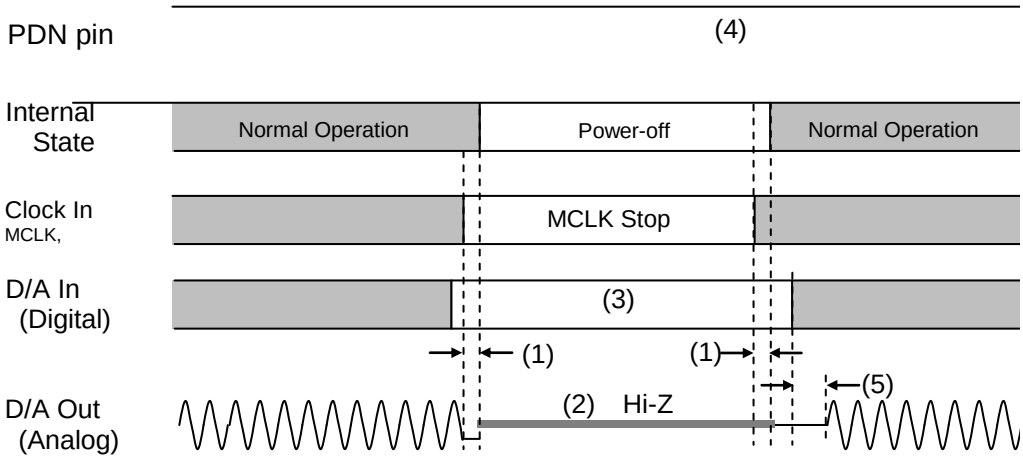



Figure 57. Power ON/OFF by MCLK Clock

Notes:

(1) The AK4492 detects MCLK stop and becomes power off state when MCLK edge is not detected for 1us (min.) during operation.
(2) The analog output goes to floating state (Hi-Z).
(3) Click noise can be reduced by inputting "0" data when stopping and resuming MCLK supply.
(4) Resume MCLK input to release the power-off state by MCLK. In this case, power-up sequence by the PDN pin or power-on sequence by PW bit is not necessary.
(5) The analog output corresponding to the digital input has group delay (GD).

**[2] Power ON/OFF by PW bit**

All circuits including control register and IREF (except LDO when the LDOE pin = “H”) stop operation by setting PW bit to “0”. In this case, control register access is available. The analog output goes to floating state (Hi-Z). Figure 58 shows power ON/OFF sequence by PW bit.

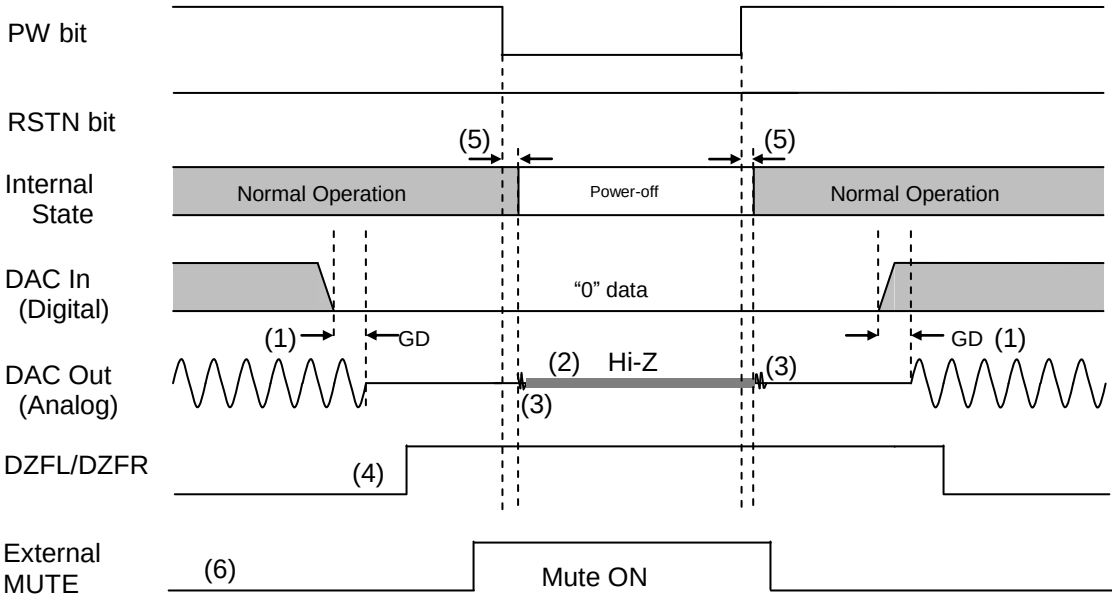



Figure 58. Power ON/OFF Timing Example

Notes:
(1) The analog output corresponding to the digital input has group delay (GD).
(2) The analog output is floating (Hi-Z) state when PW bit = “0”.
(3) Click noise occurs at the edge of PW bit. This noise is output even if “0” data is input.
(4) The zero detect function is enable when the AK4492 is power off (PW bit= “0”). This figure shows the seuqnece when DZFE bit= “1”, DZFB bit = “0” and DZFM bit= “0”.
(5) It takes 4~5/fs until a power down instruction is valid when writing PW bit and it takes 1~2/fs when releasing the power down.
(6) Mute the analog output externally if click noise (3) or Hi-z output (2) adversely affect system performance.

### [3] Reset by RSTN bit

Digital circuits except control registers and clock divider are reset by setting RSTN bit to “0”. In this case, control register settings are held, the analog output becomes VCML/R voltage and the DZFL/R pin outputs “H”. Figure 59 shows power ON/OFF sequence by RSTN bit.

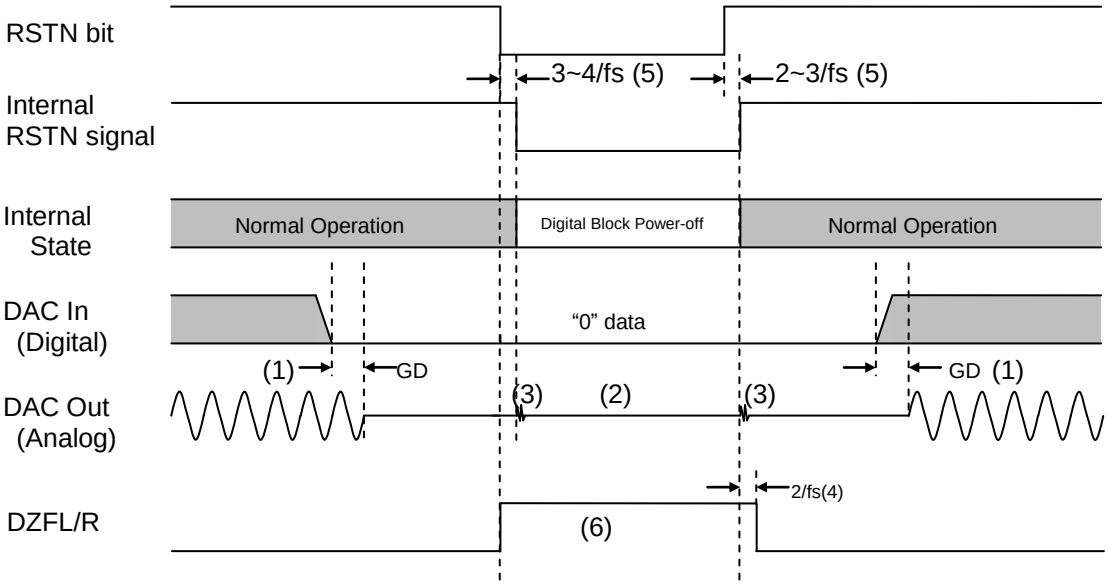



Figure 59. Reset Timing Example

Notes：

(1) The analog output corresponding to the digital input has group delay (GD).
(2) The analog output is VCOM voltage when RSTN bit = “0”.
(3) Click noise occurs at the edge of PW bit. This noise is output even if “0” data is input.
(4) This figure shows the seuqnece when DZFE bit= “1”, DZFB bit = “0” and DZFM bit= “0”. The DZFL/R pin goes “H” on a falling edge of RSTN bit and goes “L” 2/fs after a rising edge of internal RSTN bit.
(5) It takes 3~4/fs until the internal RSTN is changed when changing RSTN bit to “0” and it takes 2~3/fs when changing RSTN bit to “1”.
(6) Mute the analog output externally if click noise (3) adversely affect system performance.

## ■ Synchronize Function (PCM Mode, EXDF Mode)

The AK4492 has a function that resets the internal counter to keep the timing of falling edge of the internal clock CLK1 and the external clock edge in a certain range. With this synchronize function, group delays between each device can be kept within 4/256fs when using multiple AK4492's.
Clock synchronize function becomes valid when input data of both L and R channels are "0" for 8192 times continuously in PCM mode or EXDF mode, when both L and R channels become "0" and kept for 8192 times continuously by attenuation or when RSTN bit = "0". In PCM mode, the internal counter is synchronized with a rising edged of LRCK (falling edge of LRCK in I2C mode), and it is synchronized with a rising edge of WCK in EXDF mode. In this case, the analog output has the same voltage as VCML/R. This function is disabled by setting SYNCE bit = "0" in register control mode. Figure 60 shows a synchronizing sequence when the input data is "0" for 8192 times continuously. Figure 61 shows a synchronizing sequence by RSTN bit.

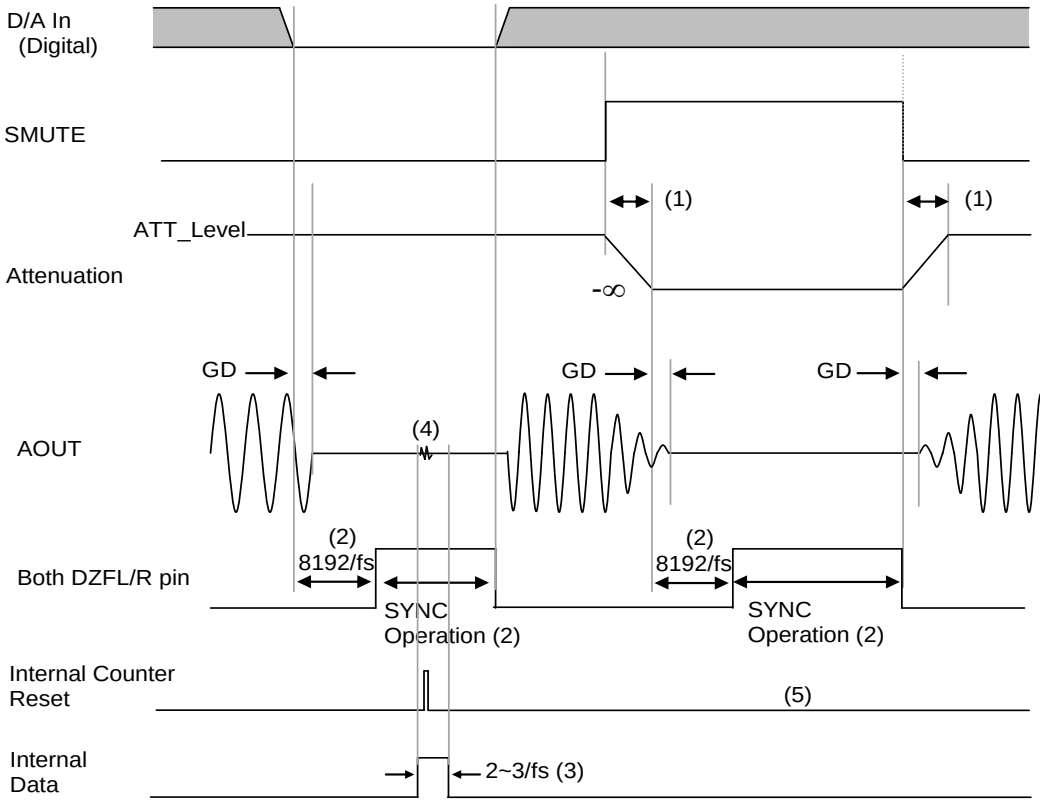



Figure 60. Synchronizing Sequenc by Continuous "0" Data Input for 8192 Times

Notes:

(1) Regarding ATT Transition time, refer to "■ Output Volume (PCM Mode, DSD Mode, EXDF Mode)".
(2) When both L and R channels data are "0" for 8192 times continuously, the DZFL and DZFR pins become "H" and the synchronize function is valid.
(3) Internal data is fixed to "0" forcibly for 2 to 3/fs when internal counter is reset.
(4) A click noise may occur when the internal counter is reset. This noise is output even if a "0" data is input. Mute the analog output externally if this click noise affects the system performance.
(5) When the internal clock and external clock are in synchronization, the internal counter is not reset even if the synchronize function is valid.

If RSTN bit is set to “0”, the output signal of the DZFL/R pin becomes “H”. Then, the DAC is reset after 3~4/fs and the analog output becomes the same voltage as VCML/R. The synchronize function becomes valid when both of the DZFL and the DZFR pins output “H”.

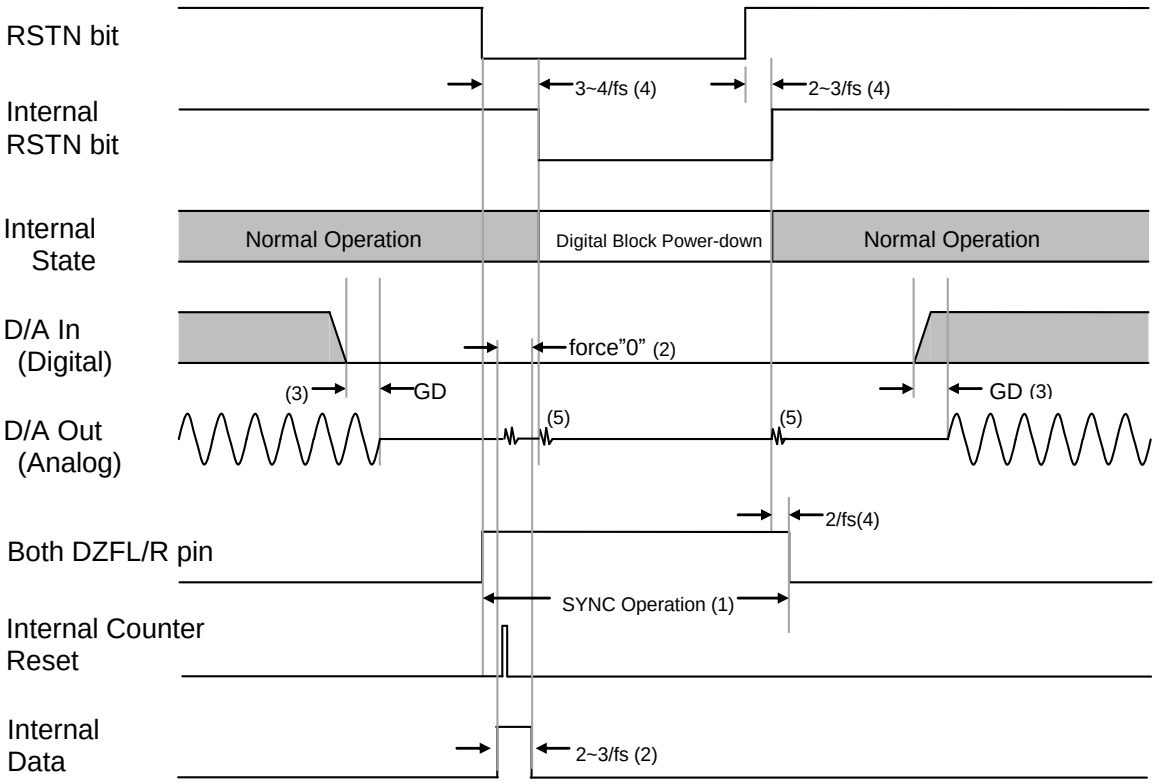



Figure 61. Synchronizing Sequence by RSTN Bit

Notes:

(1) The DZFL and the DZFR pins become “H” by a falling edge of RSTN bit, and becomes “L” 2/fs after a rising edge of internal signal of RSTN bit. The synchronize function is valid During the DZFL/R pin = “H”.

(2) Internal data is fixed to “0” forcibly for 2 to 3/fs when the internal counter is reset.

(3) Since the analog output corresponding to digital input has group delay (GD), it is recommended to have a no-input period longer than the group delay before writing “0” to RSTN bit.

(4) It takes 3 to 4/fs when falling to change the internal RSTN signal of the LSI after writing to RSTN bit. It also takes 2 to 3/fs when rising to change the internal RSTN signal of the LSI. The synchronize function becomes valid immediately when “0” is written to RSTN bit. Therefore, there is a case that the internal counter is reset before internal RSTN signal of the LSI is changed.

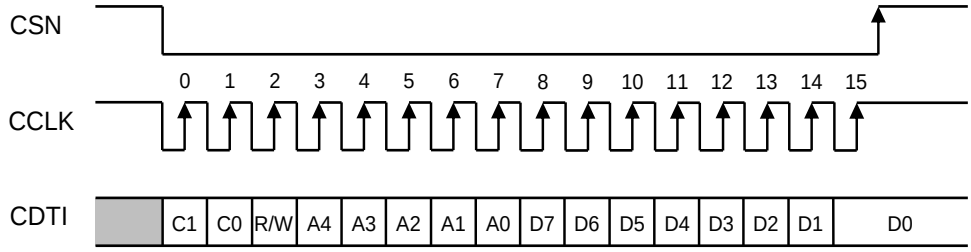
(5) A click noise occurs on the rising or falling edge of the internal RSTN signal and when the internal counter is reset. This noise is output even if a “0” data is input. Mute the analog output externally if this click noise affects the system performance.

## ■ Register Control Interface

### [1] 3-wire Serial Control Mode (I2C pin = "L")

Pins (pin control mode) or registers (register control mode) can control the functions of the AK4492. In pin control mode, the register setting is ignored, and in register control mode the pin settings are ignored. When the state of the PSN pin is changed, the AK4492 should be powered down by the PDN pin. Otherwise, malfunctions may occur since previous settings are not initialized. The register control interface is enabled by the PSN pin = "L". Internal registers may be written to through 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2-bits, C1/0), Read/Write (1-bit; fixed to "1", write only), Register address (MSB first, 5-bits) and Control data (MSB first, 8-bits). The data is output on a falling edge of CCLK and the data is received on a rising edge of CCLK. The writing of data is valid when CSN "↑". The clock speed of CCLK is 5MHz (max).

Setting the PDN pin to "L" resets the registers to their default values. In register control mode, the digital block except control registers and clock divider is reset by setting RSTN bit to "0". In this case, the register values are not initialized.




C1-C0: Chip Address (C1 bit = CAD1 pin, C0 bit = CAD0 pin)
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 62. Control I/F Timing

* The AK4492 does not support read commands in 3-wire serial control mode.
* When the AK4492 is in power down mode (PDN pin = "L"), writing into control registers is prohibited.
* The control data cannot be written when the CCLK rising edge is 15 times or less, or 17 times or more during CSN is "L".
* The CDTI pin must not fall during the CCLK pin is "H". Writing into registers may not be valid when it is happened.

Precautions when using the 3-wire serial interface

The I²C interface block continues to run, even when the 3-wire serial interface is selected. Therefore, if CDTI (SDA) transitions from "H" to "L" while CCLK (SCL) is "H", the I²C interface recognizes this as a start condition and receives subsequent data. If this data string matches the slave address, the I²C interface outputs the ACK signal and data to the CDTI (SDA) pin. As a result, the CDTI (SDA) pin would experience a drive conflict resulting from the I2C block's output and the 3-wire serial interface's input. In this scenario, the data cannot be reliably written to the register.

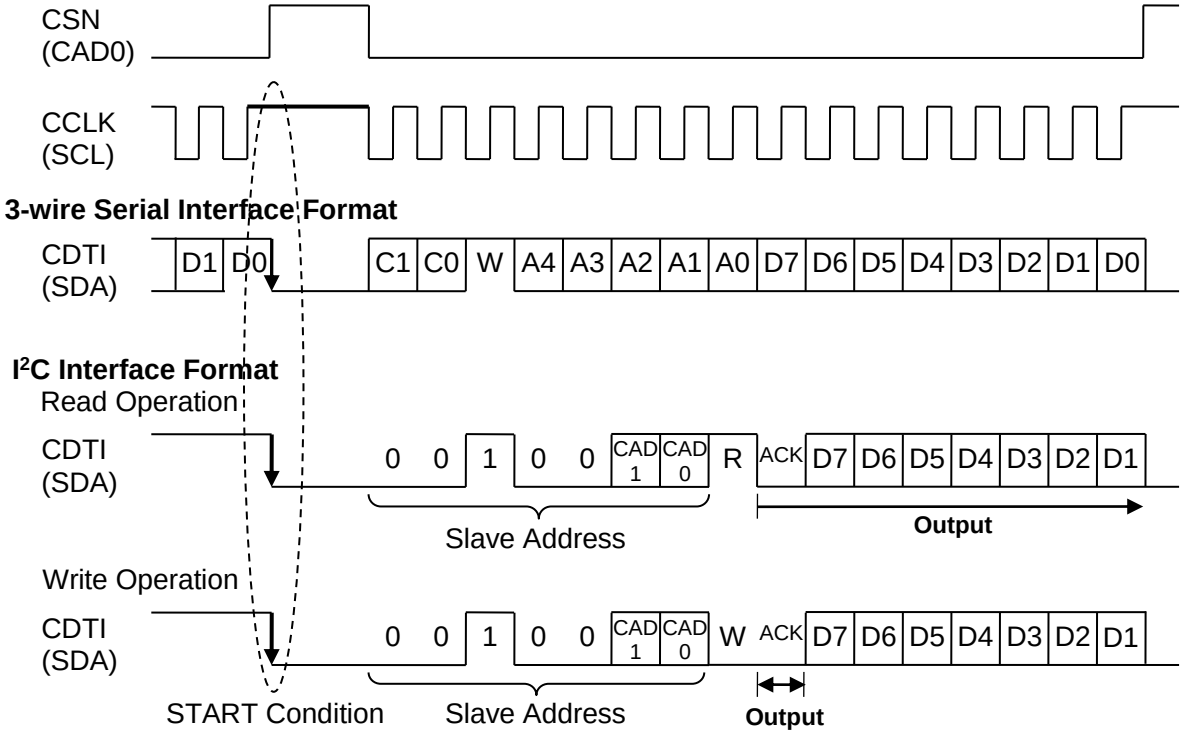



Figure 63. Comparison of 3-wire Serial and I²C Interface Timing

To prevent the above situation when using the 3-wire serial interface, change CDTI only at the falling edge of CCLK in order to avoid generation of a start condition.

Example 1) When CCLK is not stopped while CSN is "H"

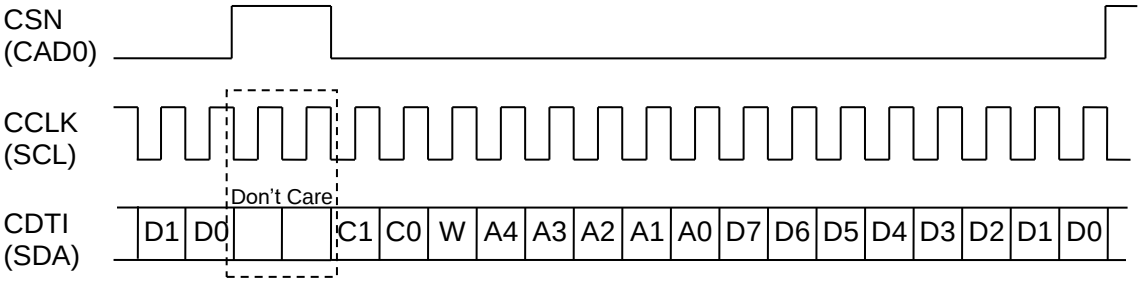



Figure 64. CDTI Change Timing Example 1

Example 2) When CCLK is stopped while CSN is "H"

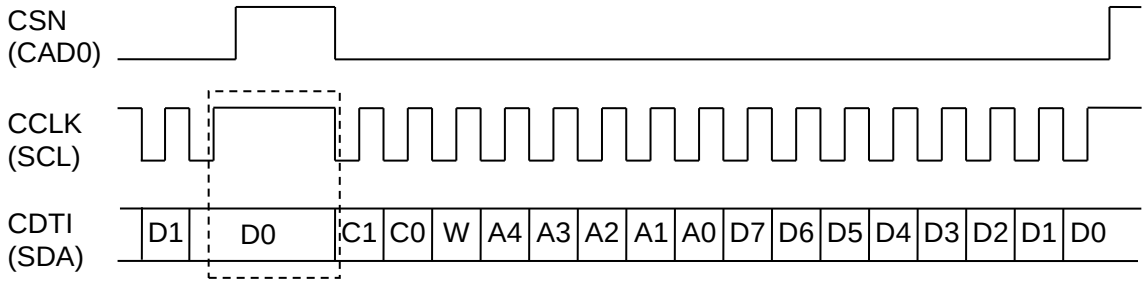



Figure 65. CDTI Change Timing Example 2

### [2] I²C-bus Control Mode (I2C pin = "H")

The AK4492 supports the fast-mode I²C-bus (max: 400kHz, Ver. 1.0).

(1) WRITE Operations

Figure 66 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 72). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bits). This bit identifies the specific device on the bus. The hard-wired input pin (CAD1 pin, CAD0 pin) sets these device address bits (Figure 67). If the slave address matches that of the AK4492, the AK4492 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 73). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4492 and the format is MSB first. (Figure 68). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 69). The AK4492 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 72).

The AK4492 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4492 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "15H" prior to generating a stop condition, the address counter will "roll over" to "00H" and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 74) except for the START and STOP conditions.

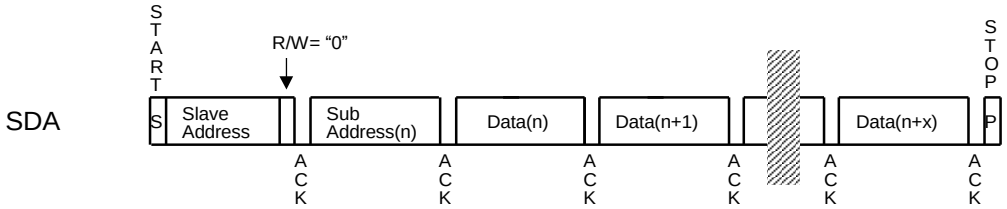



Figure 66. Data Transfer Sequence at I²C Bus Mode

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | CAD1 | CAD0 | R/W |

Figure 67. The First Byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | A4 | A3 | A2 | A1 | A0 |

Figure 68. The Second Byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Figure 69. The Third Byte and After The Third Byte

(2) READ Operation

Set the R/W bit = “1” for the READ operation of the AK4492. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “15H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK4492 supports two basic read operations: Current Address Read and Random Address Read.

(2)-1. Current Address Read
The AK4492 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4492 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4492 ceases the transmission.

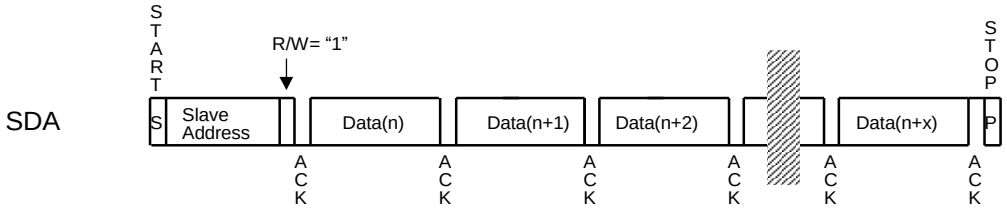



Figure 70. Current Address Read

(2)-2. Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4492 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4492 ceases the transmission.

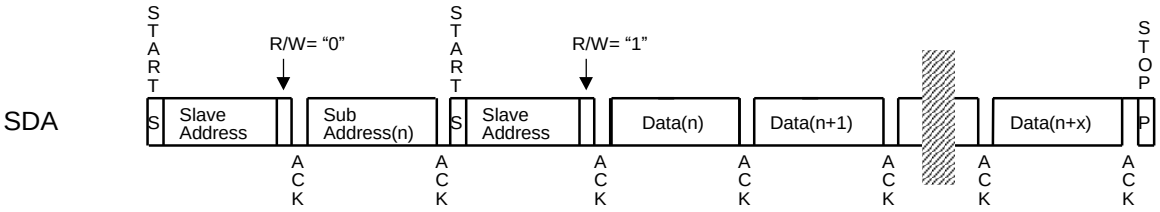



Figure 71. Random Address Read

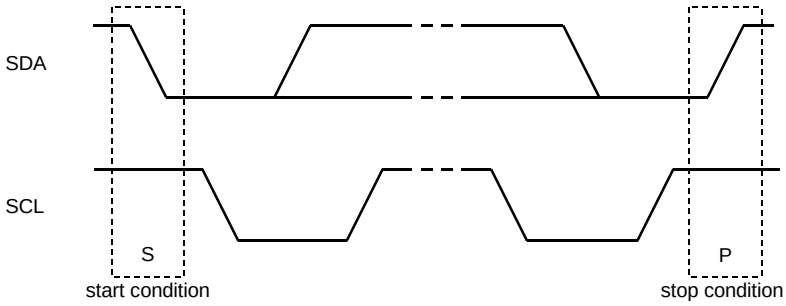



Figure 72. Start Condition and Stop Condition

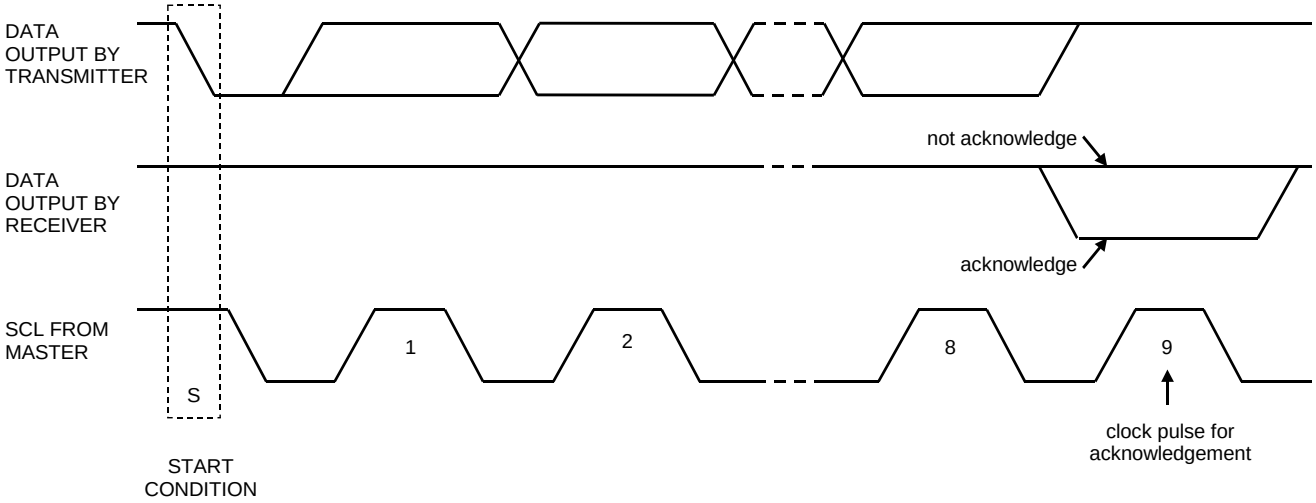



Figure 73. Acknowledge ($I^2C$ Bus)

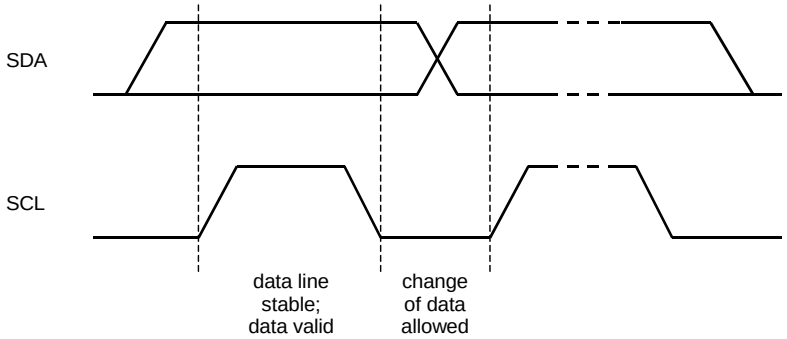



Figure 74. Bit Transfer ($I^2C$ Bus)

## ■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | ACKS | EXDF | ECS | AFSD | DIF2 | DIF1 | DIF0 | RSTN |
| 01H | Control 2 | DZFE | DZFM | SD | DFS1 | DFS0 | DEM1 | DEM0 | SMUTE |
| 02H | Control 3 | DP | 0 | DCKS | DCKB | MONO | DZFB | SELLR | SLOW |
| 03H | Lch ATT | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 04H | Rch ATT | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 05H | Control4 | INVL | INVR | 0 | 0 | 0 | 0 | DFS2 | SSLOW |
| 06H | DSD1 | DDM | DML | DMR | DMC | DMRE | 0 | DSDD | DSDSEL0 |
| 07H | Control5 | 0 | 0 | 0 | 0 | GC2 | GC1 | GC0 | SYNCE |
| 08H | Sound Control | 0 | 0 | 0 | 0 | HLOAD | 0 | 0 | 0 |
| 09H | DSD2 | 0 | 0 | 0 | 0 | 0 | DSDPATH | DSDF | DSDSEL1 |
| 0AH | Control 7 | TDM1 | TDM0 | SDS1 | SDS2 | 0 | PW | 0 | 0 |
| 0BH | Control 8 | ATS1 | ATS0 | 0 | SDS0 | 0 | 0 | DCHAIN | 0 |
| 0CH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0DH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0EH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0FH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15H | DFS read | 0 | 0 | 0 | 0 | 0 | ADFS2 | ADFS1 | ADFS0 |

Notes:

- In 3-wire serial control mode, the AK4492 does not support read commands.
- The AK4492 supports read command in $I^2C$-bus control mode.
- If the address exceeds “15H”, the address counter will “roll over” to “00H” and the next write/read address will be “00H” by automatic increment function in $I^2C$-Bus mode.
- Bits indicated as 0 in each address must contain a “0” value. Writing after 16H is also forbidden. Malfunctions may occur by these actions.
- When the PDN pin goes to “L”, the registers are initialized to their default values.
- When RSTN bit is set to “0”, the digital block except control registers and clock divider is reset, and the registers are not initialized to their default values.
- When the state of the PSN pin is changed, the AK4492 should be reset by the PDN pin.

## ■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | ACKS | EXDF | ECS | AFSD | DIF2 | DIF1 | DIF0 | RSTN |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

RSTN: Internal Timing Reset
0: Reset. All registers are not initialized. (default)
1: Normal Operation

DIF[2:0]: Audio Interface Format (Table 24)
Initial value is “110” (Mode6: 32bit MSB justified).

AFSD: Sampling Frequency Auto Detect Mode Enable (PCM & EXDF mode only). (Table 5)
0: Disable: Manual or Auto Setting Mode (default)
1: Enable: Auto Detect Mode
When AFSD bit = “1”, DFS[2:0] bits are ignored.

ECS: EXDF mode clock setting (Table 23)
0: WCK = 768kHz mode(default)
1: WCK = 384kHz mode

EXDF: External Digital Filter I/F Mode (Register Control mode only)
0: Disable: Internal Digital Filter mode (default)
1: Enable: External Digital Filter mode

ACKS: Master Clock Frequency Auto Setting Mode Enable (PCM & EXDF mode only) (Table 14, Table 5)
0: Disable: Manual Setting Mode (default)
1: Enable: Auto Setting Mode

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | Control 2 | DZFE | DZFM | SD | DFS1 | DFS0 | DEM1 | DEM0 | SMUTE |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: DAC outputs soft-muted.

DEM[1:0]: De-emphasis Control (Table 30)
Initial value is “01” (OFF).

DFS[1:0]: Sampling Speed Control. (Table 7, Table 11)
Initial value is “000” (Normal Speed). Click noise occurs when DFS[2:0] bits are changed.

SD: Minimum delay Filter Enable. (Table 28)
0: Traditional filter
1: Short delay filter (default)

DZFM: Data Zero Detect Mode
0: Channel Separated Mode (default)
1: Channel ANDed Mode
If the DZFM bit is set to “1”, the DZF pins of both L and R channels go to “H” only when the input data at both channels are continuously zeros for 8192 LRCK cycles.

DZFE: Data Zero Detect Enable
0: Disable (default)
1: Enable
Zero detect function can be disabled by DZFE bit “0”. In this case, the DZF pins of both channels are always “L”.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02H | Control 3 | DP | 0 | DCKS | DCKB | MONO | DZFB | SELLR | SLOW |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SLOW: Slow Roll-off Filter Enable. (Table 28)
0: Slow roll-off filter disable (default)
1: Slow roll-off filter

SELLR: The data selection of L channel and R channel, when MONO mode
0: All channel output L channel data, when MONO mode. (default)
L channel output L channel data, R channel data output R channel data(default)
1: All channel output R channel data, when MONO mode.
L channel output R channel data, R channel data output L channel data

DZFB: Inverting Enable of DZF. (Table 36)
0: DZF pin goes “H” at Zero Detection (default)
1: DZF pin goes “L” at Zero Detection

MONO: MONO mode Stereo mode select
0: Stereo mode (default)
1: MONO mode

DCKB: Polarity of DCLK (DSD Only)
0: DSD data is output from DCLK falling edge. (default)
1: DSD data is output from DCLK rising edge.

DCKS: Master Clock Frequency Select at DSD mode (DSD only)
0: 512fs (default)
1: 768fs

DP: DSD/PCM Mode Select
0: PCM Mode (default)
1: DSD Mode
When DP bit is changed, the AK4492 should be reset by RSTN bit.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 03H | Lch ATT | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 04H | Rch ATT | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

ATT[7:0]: Attenuation Level
255 levels 0.5 dB step + mute

| Data | Attenuation |
|---|---|
| FFH | 0 dB (default) |
| FEH | -0.5 dB |
| FDH | -1.0 dB |
| : | : |
| : | : |
| 02H | -126.5 dB |
| 01H | -127.0 dB |
| 00H | MUTE (-∞) |

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 05H | Control 4 | INVL | INVR | 0 | 0 | 0 | 0 | DFS2 | SSLOW |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SSLOW: Super Slow Roll Off (Digital Filter bypass mode) Enable. (Table 28)
0: Disable (default)
1: Enable

DFS2: Sampling Speed Control. (Table 7, Table 11)

INVR: AOUTR Output Phase Inverting
0: Disable (default)
1: Enable

INVL: AOUTL Output Phase Inverting
0: Disable (default)
1: Enable

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 06H | DSD1 | DDM | DML | DMR | DMC | DMRE | 0 | DSDD | DSDSEL0 |
| R/W | | R/W | R | R | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DSDSEL[1:0]: DSD data stream select

Table 21. DSD Data Stream Select

| DSDSEL1 | DSDSEL0 | DSD Data Stream | | | |
|---|---|---|---|---|---|
| | | fs = 32 kHz | fs = 44.1 kHz | fs = 48 kHz | |
| 0 | 0 | 2.048 MHz | 2.8224 MHz | 3.072 MHz | (default) |
| 0 | 1 | 4.096 MHz | 5.6448 MHz | 6.144 MHz | |
| 1 | 0 | 8.192 MHz | 11.2896 MHz | 12.288 MHz | |
| 1 | 1 | N/A | N/A | N/A | |

DSDD: DSD Playback Path Select

Table 22. DSD Playback Path Select

| DSDD | Mode | |
|---|---|---|
| 0 | Normal Path | (default) |
| 1 | Volume Bypass | |

DMRE: DSD Mute Release

0: Hold (default)

1: Release Mute

This register is only valid when DDM bit = “1” and DMC bit = “1”. When the AK4492 mutes DSD data by DDM and DMC bits settings, the mute is released by setting DMRE bit to “1”.

Table 40. Recovery Method to Normal Operation Mode from Full Scale Detection Status

| DDM | DMC | DMRE | Status After Detection | |
|---|---|---|---|---|
| 0 | x | x | When full scale is detected, Mute function is disabled. | (default) |
| 1 | 0 | x | When full scale is detected, Mute function is enabled. The AK4492 returns to normal operation automatically by a normal signal input. | |
| 1 | 1 | 0 | When full scale is detected, Mute function is enabled. The AK4492 keeps mute mode, even if a normal signal is input. | |
| 1 | 1 | 1 (Note 53) | When full scale is detected, Mute function is enabled. The AK4492 returns to normal operation when a normal signal is input and DMRE bit is set to “1”. | |

(x: Don not care)

Note 53. DMRE bit returns to “0” automatically after the AK4492 returns to normal operation.

DMC: DSD Mute Control

0: Auto Return (default)

1: Mute Hold (manual return)

This register is only valid when DDM bit = “1”. It selects the mute releasing mode of when the DSD data level becomes under full-scale after the AK4492 mutes DSD data by DDM bit setting.

DMR/DML

This register outputs detection flag when a full scale signal is detected at DSDR/L channel.

DDM: DSD Data Mute

The AK4492 has an internal mute function that mutes the output when DSD audio data becomes all “1” or all “0” for 2048 Samples (DCLK cycle). DDM bit controls this function.

0: Disable (default)

1: Enable

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 07H | Control 5 | 0 | 0 | 0 | 0 | GC2 | GC1 | GC0 | SYNCE |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

SYNCE: SYNC Mode Enable
0: SYNC Mode Disable
1: SYNC Mode Enable (default)

GC[2:0]: PCM, DSD Mode Gain Control

Table 34. Output Level between Set Values of GC[2:0] bit

| GC[2] bit | GC[1] bit | GC[0] bit | AOUTLP/LN/RP/RN Ouput Level | | | |
|---|---|---|---|---|---|---|
| | | | PCM | DSD: Normal Path | DSD: Volume Bypass | |
| 0 | 0 | 0 | 2.8 Vpp | 2.8 Vpp | 2.5 Vpp | (default) |
| 0 | 0 | 1 | 2.8 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 0 | 1 | 0 | 2.5 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 0 | 1 | 1 | 2.5 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 1 | 0 | 0 | 3.75 Vpp | 3.75 Vpp | 2.5 Vpp | |
| 1 | 0 | 1 | 3.75 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 1 | 1 | 0 | 2.5 Vpp | 2.5 Vpp | 2.5 Vpp | |
| 1 | 1 | 1 | 2.5 Vpp | 2.5 Vpp | 2.5 Vpp | |

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 08H | Sound Control | 0 | 0 | 0 | 0 | HLOAD | 0 | 0 | 0 |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

HLOAD: Heavy Load Mode Enable
0: Heavy Load Mode Disable (default)
1: Heavy Load Mode Enable

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 09H | DSD2 | 0 | 0 | 0 | 0 | 0 | DSDPATH | DSDF | DSDSEL1 |
| R/W | | R | R | R | R | R | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DSDSEL[1:0]: DSD data stream select

Table 21. DSD data stream select

| DSDSEL1 | DSDSEL0 | DSD data stream | | | |
|---|---|---|---|---|---|
| | | fs = 32 kHz | fs = 44.1 kHz | fs = 48 kHz | |
| 0 | 0 | 2.048 MHz | 2.8224 MHz | 3.072 MHz | (default) |
| 0 | 1 | 4.096 MHz | 5.6448 MHz | 6.144 MHz | |
| 1 | 0 | 8.192 MHz | 11.2896 MHz | 12.288 MHz | |
| 1 | 1 | N/A | N/A | N/A | |

DSDF: Cut-off frequency of DSD Filter Control

Table 29. DSD Filter Select

| DSDF bit | Cut Off Frequency @fs = 44.1 kHz, | | | |
|---|---|---|---|---|
| | DSD64fs | DSD128fs | DSD256fs | |
| 0 | 39 kHz | 78 kHz | 156 kHz | (default) |
| 1 | 76 kHz | 152 kHz | 304 kHz | |

DSDPATH: DSD Data Input Pin Select

0: A3, B1, B2 (default)

1: J1, H1, G1

Table 4. PCM/DSD/EXDF Mode Control

| DP bit | EXDF bit | DSDPATH bit | D/A Conv. Mode | Pin Assignment | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | J1 pin | H1 pin | G1 pin | A3 pin | B1 pin | B2 pin |
| 0 (default) | 0 (default) | x | PCM | BICK | SDATA | LRCK | Not Use | Not Use | Not Use |
| 1 | x | 0 (default) | DSD | Not Use | Not Use | Not Use | DCLK | DSDL | DSDR |
| 1 | x | 1 | DSD | DCLK | DSDL | DSDR | Not Use | Not Use | Not Use |
| 0 | 1 | x | EXDF | BCK | DINL | DINR | Not Use | Not Use | Not Use |

(x: Do not care)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0AH | Control 7 | TDM1 | TDM0 | SDS1 | SDS2 | 0 | PW | 0 | 0 |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

PW: Power ON/OFF control
0: Power off
1: Power on (default)

SDS[2:0]: Output Data Slot Selection of Each Channel (Table 25)

Table 25. Output Data Slot Selection of Each Channel

| | TDM1 | TDM0 | SDS2 | SDS1 | SDS0 | DAC | |
|---|---|---|---|---|---|---|---|
| | | | | | | Lch | Rch |
| Normal | 0 | 0 | x | x | x | L1 | R1 |
| TDM128 | 0 | 1 | x | x | 0 | L1 | R1 |
| | | | x | x | 1 | L2 | R2 |
| TDM256 | 1 | 0 | x | 0 | 0 | L1 | R1 |
| | | | x | 0 | 1 | L2 | R2 |
| | | | x | 1 | 0 | L3 | R3 |
| | | | x | 1 | 1 | L4 | R4 |
| TDM512 | 1 | 1 | 0 | 0 | 0 | L1 | R1 |
| | | | 0 | 0 | 1 | L2 | R2 |
| | | | 0 | 1 | 0 | L3 | R3 |
| | | | 0 | 1 | 1 | L4 | R4 |
| | | | 1 | 0 | 0 | L5 | R5 |
| | | | 1 | 0 | 1 | L6 | R6 |
| | | | 1 | 1 | 0 | L7 | R7 |
| | | | 1 | 1 | 1 | L8 | R8 |

(x: Do not care)

TDM[1:0]: TDM Mode Select
00: Normal (default)
01: TDM128
10: TDM256
11: TDM512

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0BH | Control 8 | ATS1 | ATS0 | 0 | SDS0 | 0 | 0 | DCHAIN | 0 |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DCHAIN: Daisy Chain Mode Enable
0: Daisy Chain Mode Disable (default)
1: Daisy Chain Mode Enable

SDS[2:0]: Output Data Slot Selection of Each Channel
0: Normal Operation
1: Changing Data Slot (Table 25)
Default value is “00”.

ATS[1:0]: Transition Time between Set Values of ATT[7:0] bits (Table 33)
Default value is “00”.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0CH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0DH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0EH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0FH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0CH: Reserved

0DH: Reserved

0EH: Reserved

0FH: Reserved

10H: Reserved

11H: Reserved

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 12H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | | R | R | R | R | R | R | R | R |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

12H: Reserved

13H: Reserved

14H: Reserved

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 15H | ADFS read | 0 | 0 | 0 | 0 | 0 | ADFS2 | ADFS1 | ADFS0 |
| R/W | | R | R | R | R | R | R | R | R |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ADFS[2:0]: Mode Detection Result in FS Auto Detect Mode

Table 44. Jugdement result of Mode and ADFS[2:0]

| ADFS2 bit | ADFS1 bit | ADFS0 bit | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Normal Speed Mode |
| 0 | 0 | 1 | Double Speed Mode |
| 0 | 1 | 0 | Quad Speed Mode |
| 0 | 1 | 1 | Quad Speed Mode |
| 1 | 0 | 0 | Oct Speed Mode |
| 1 | 0 | 1 | Hex Speed Mode |
| 1 | 1 | 0 | Oct Speed Mode |
| 1 | 1 | 1 | Hex Speed Mode |

## 10. Recommended External Circuits

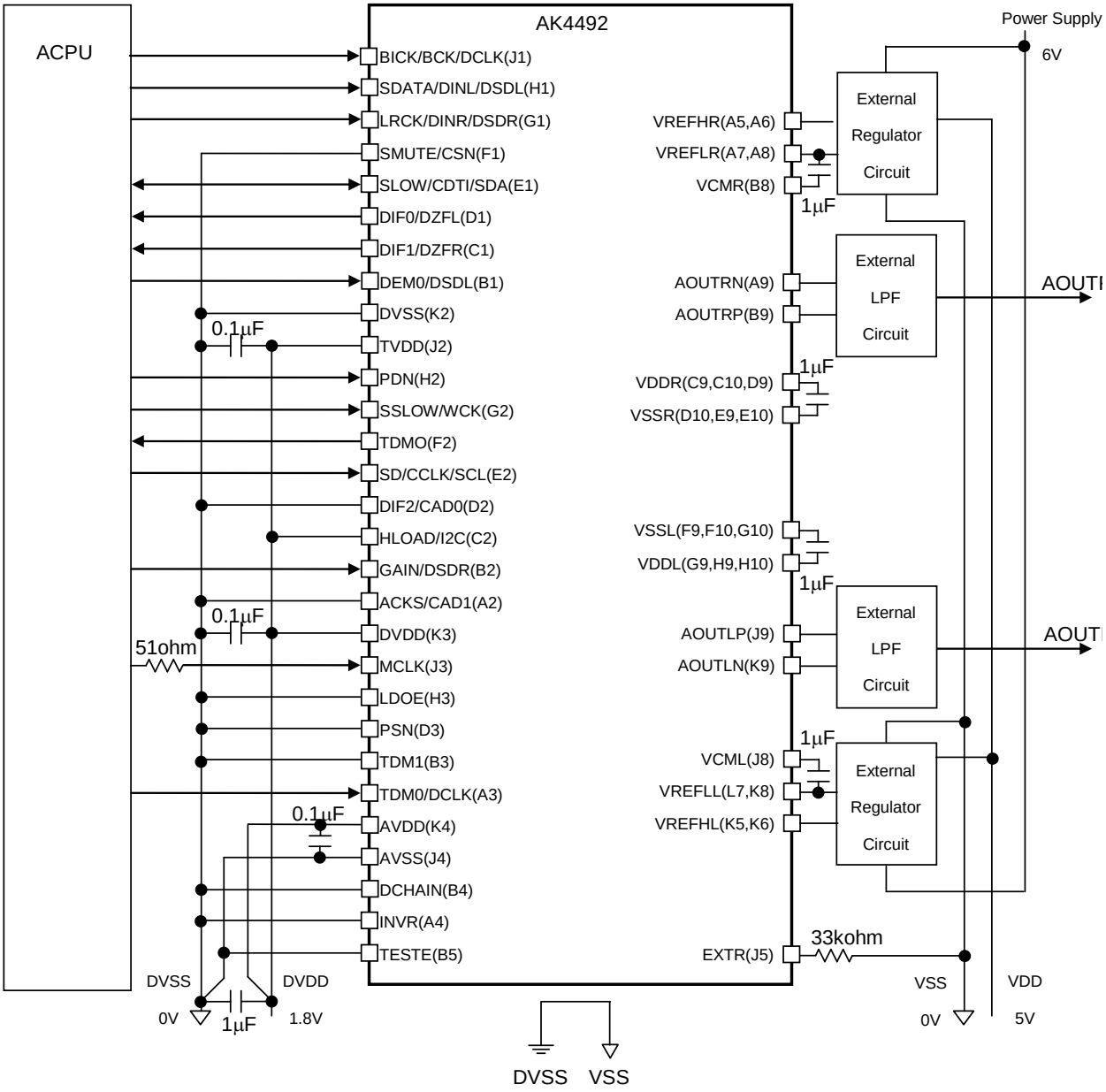



Figure 75. Typical Connection Diagram
(AVDD = TVDD = DVDD = 1.8 V, VDDL/R = 5.0 V, LDOE pin = “L”, Register control mode)

Note:
- Chip Address = “00”. BICK = 64fs, LRCK = fs
- Power lines of AVDD, TVDD, VDDL and VDDR should be distributed separately from the point with low impedance of regulator etc.
- AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane. (Analog ground should has low impedance as a solid pattern. THD+N characteristics will degrade if there are impedances between each VSS.)
- It is recommended to input MCLK via a dumping resistor of 51ohm. Without the resistor, there is a possibilrty that THD+N characteristic degrades because of high-frequency noise of MCLK.
- All input pins except pull-down/pull-up pins should not be allowed to float.

### 1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD, TVDD, DVDD, VDDL and VDDR. AVDD and VDDL/R are supplied from analog supply in system, and TVDD and DVDD are supplied from digital supply in system. Power lines of VDDL/R should be distributed separately from the point with low impedance of regulator etc.
When not using the LDO (LDOE pin = "L"), all power supplies (DVDD (1.8V), TVDD and AVDD (3.3V) and VDDL/R (5V)) should be powered up at the same time or sequentially in the order of 3.3V (TVDD, AVDD), 1.8V (DVDD) and 5V (VDDL/R).
The internal LDO outputs DVDD (1.8V) when the LDOE pin = "H". 3.3V (TVDD and AVDD) power supplies must be powered up before or at the same time with 5V (VDDL/R) power supplies when the LDOE pin = "H".
**AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.** Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

### 2. Voltage Reference

The differential voltage between VREFHL/R and VREFLL/R sets the full scale of the analog output range. The VREFHL/R pin is normally connected to VDD, and the VREFLL/R pin is normally connected to the VSS. The VREFH, VREFL pin should be connected to the noiseless power supply. If not, it is recommended to connect these pin to an external regulator circuit as shown in Figure 76. In this case, a tantalum or an electrolytic capacitor (6.8u) should be used between each of the VREFHL and VREFHR pins, and the VREFLL and VREFLR pins. Digital signal and clock lines should be kept away from the VREFHL/R and VREFLL/R pins in order to avoid unwanted coupling into the AK4492.
Low noise 5V (typ.) should be input to the external regulator circuit. If this input voltage has a noise, attenuate the noise by a 1st order LPF as shown in Figure 76.
No load current may be drawn from the VCML/R pin since VCML/R is a common voltage of analog signals.

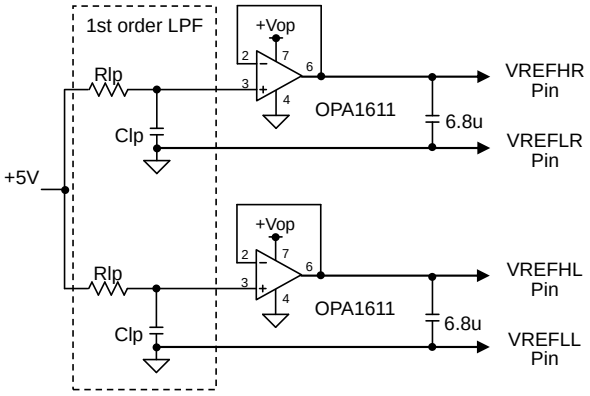



Figure 76. External Regulator Circuit Example

### 3. Analog Output

The analog outputs are full differential outputs. The differential outputs are summed externally, $V_{AOUT}$ = (AOUT+) – (AOUT–) between AOUT+ and AOUT–. If the summing gain is 1, the output range of the setting the GAIN pin = "L" or GC[2] bit = "0" is 2.8Vpp (typ, VREFHL/R – VREFLL/R = 5V) centered around VCML and VCMR voltages. In this case, the output range after summing will be 5.6V (typ.). The output range of the setting the GAIN pin = "H" or GC[2] bit = "1" is 3.75Vpp (typ.) centered around VCML and VCMR voltages. In this case, the output range after summing will be 7.5Vpp (typ.). The bias voltage of the external summing circuit is supplied externally.
The input data format is 2's complement. The output voltage ($V_{AOUT}$) is a positive full scale for 7FFFFFFFH (@32bit) and a negative full scale for 80000000H (@32bit). The ideal $V_{AOUT}$ is 0V for 00000000H (@32bit). The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond

the audio passband. Figure 77 shows examples of external LPF circuit summing the differential outputs by a single op-amp. Load resistances of the analog output of the AK4492 are 1360 ohm for AOUT+ and 453 ohm for AOUT-, and the external LPF circuit can be driven regardless of the HLOAD pin or HLOAD bit setting. The HLOAD pin/bit should be set to “H/1” when driving the LPF circuit if the AOUT- load resistance is 300 ~ 400 ohm. The analog output will be 5.6 Vpp (typ.) after a single conversion with this circuit by setting the GAIN pin = “L” or GC[2] bit = “0”. It will be 7.5 Vpp if setting the GAIN pin = “H” or GC[2] bit = “1”. A resistor that has 0.1% or less absolute error must be used for external LPFs.

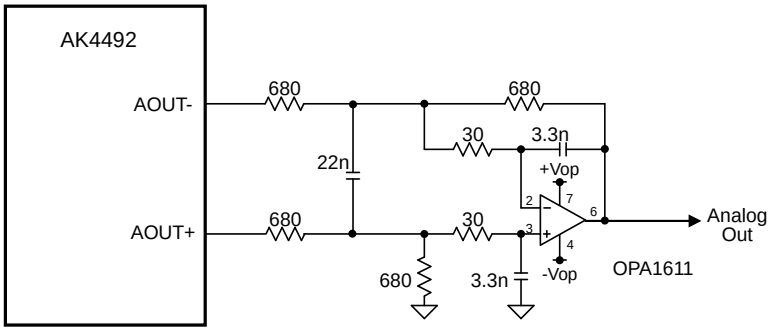



Figure 77. External LPF Circuit Example 1 (fc = 90 kHz(typ), Q = 0.705(typ))

Table 44. Frequency Response of External LPF Circuit Example 1

| Gain(1 kHz,typ) | | 0 dB |
|---|---|---|
| Frequency Response (ref:1 kHz,typ) | 20 kHz | -0.04 dB |
| | 40 kHz | -0.22 dB |
| | 80 kHz | -2.08 dB |

## 4. Connection Example with the AK8157A

The AK8157A is the multi clock generater for the audio product with low RMS gitter. MCLK, BCLK and LRCK are generated by the AK8157A. Connection example of the AK4492 and the external device is as follows.

e.g. AK8157: Master / External DSP: Slave
MCLK, BCLK and LRCK are generated by the AK8157A.
SDATA for the AK4492 is output from the external DSP in synchronization with BCLK and LRCK.
System rayout should be designed so that a noise interference between VSS and DVSS does not occure.

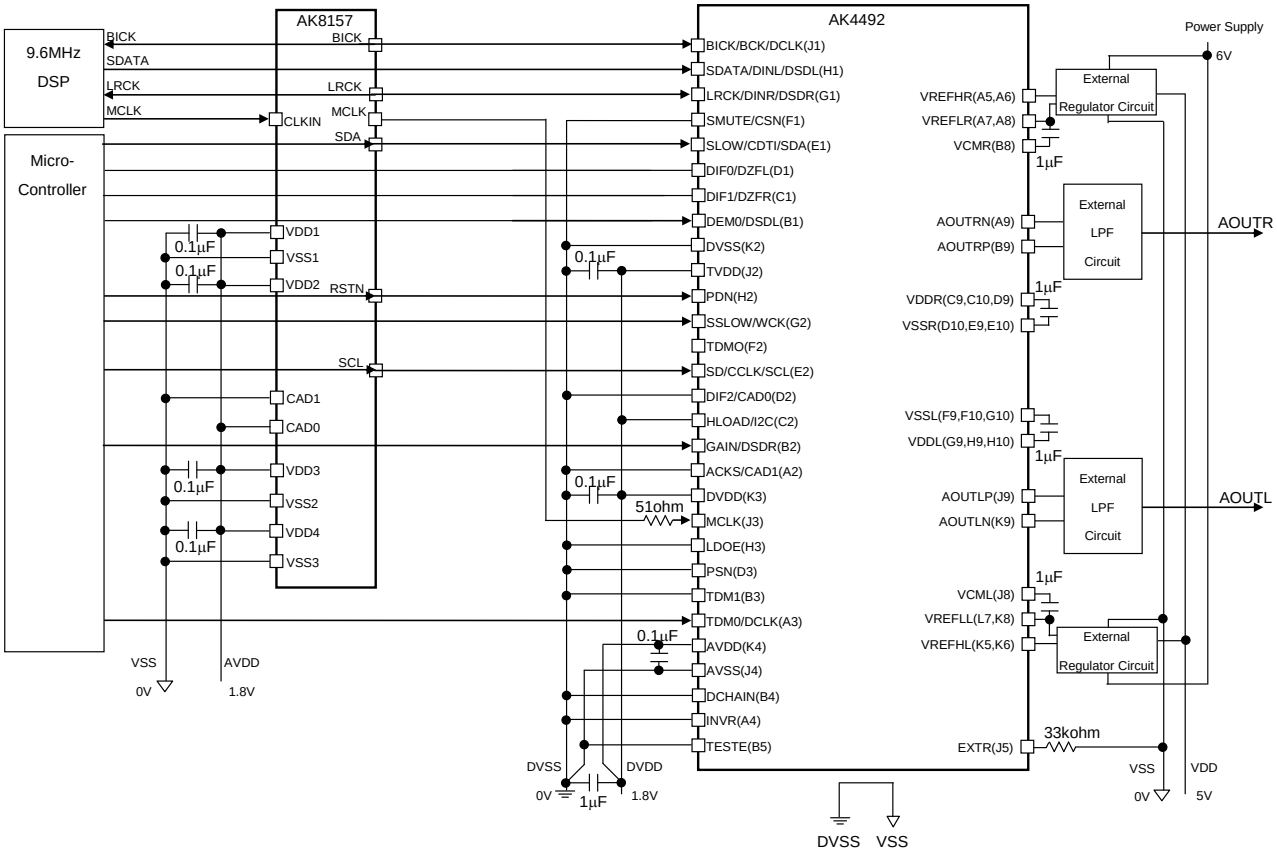



Figure 78. Circuit Example with AK8157A

## 5. Connection Example with the AK4205

The AK4205 is a low-distorsion stereo headphone amplifier with an analog switch for Hi-Fi mobile aplications. It integrates a gain setting resistor and a LPF, saving mounting area of the printing circuit board. A connection example of the AK4492 and the AK44205 is shown below. Exposed pad (TAB) on the bottom surface of the package should be connected to the gorund. System rayout should be designed so that a noise interference between VSS and DVSS does not occure.
The AK8175A can be connected at the input stage of the AK4492 (Figure 78).

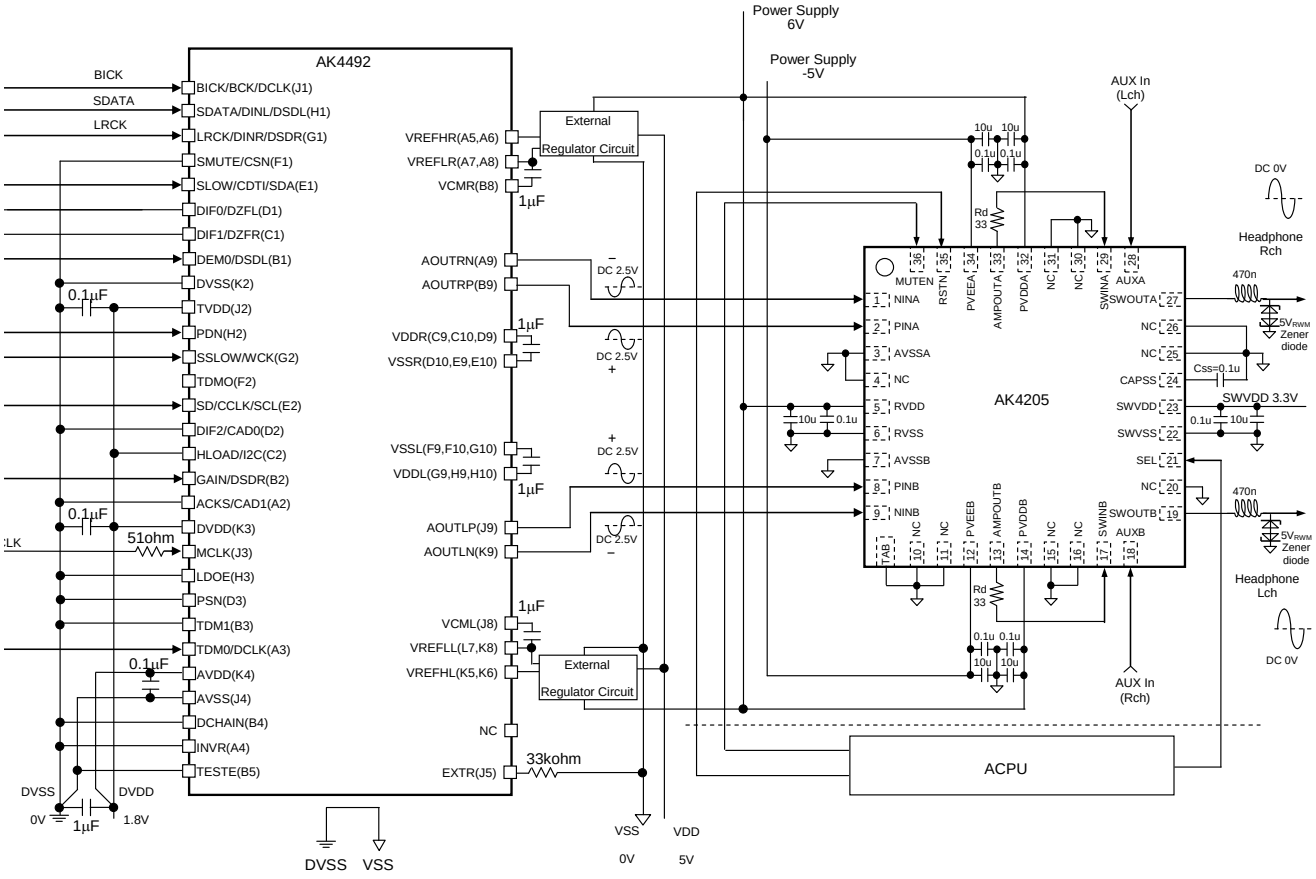
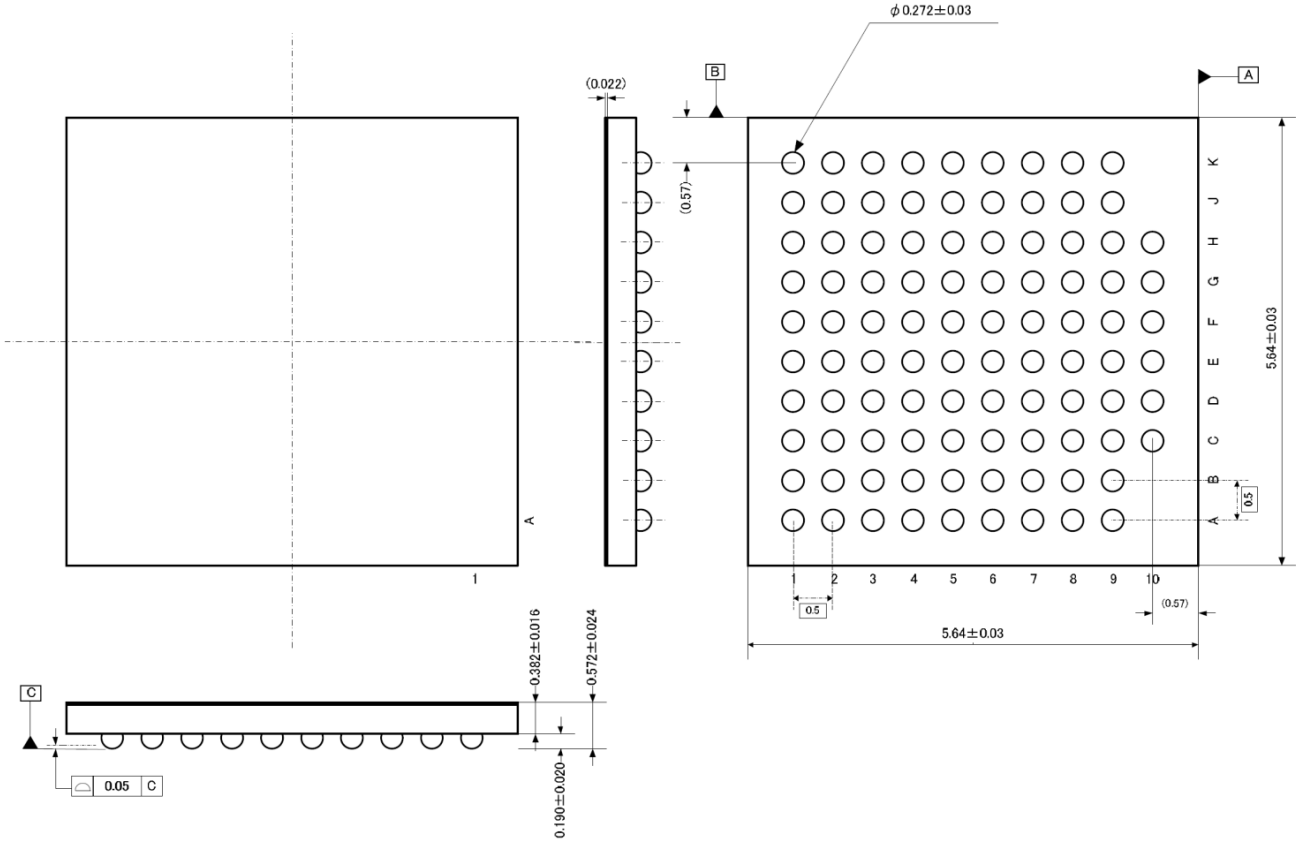



Figure 79. Circuit Example with AK4205

## 11. Package

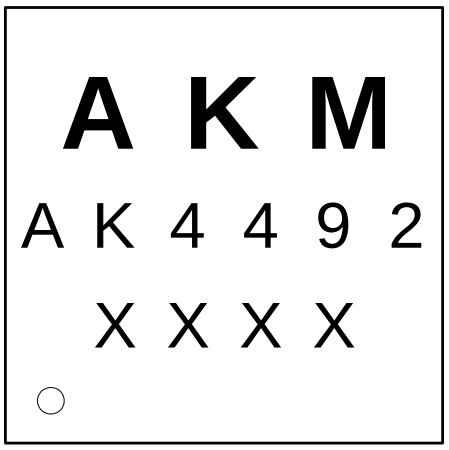
### ■ Outline Dimensions (96-pin WLCSP)




### ■ Material & Lead Finish

Package molding compound: Halogen free
Solder ball material: SAC-405 (Sn/Ag/Cu)

### ■ Marking




1) AKM Logo
2) Pin #A1 indication
3) Date Code: XXXX (4 digits)
4) Marking Code: AK4492

## 12. Ordering Guide

### ■ Ordering Guide

| | |
|---|---|
| AK4492ECB | −40 ~ +85°C 96-pin WLCSP |
| AKD4492 | AK4492 Evaluation Board |

## 13. Revesion History

| Date (Y/M/D) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 16/12/1 | 00 | First Edition | | |
| 20/09/25 | 02 | Specification Change | 26 | ■ **Switching Characteristics**<br>**LRCK Clock Timing**<br>**Normal Mode (TDM[1:0] bits = "00")**<br>fso; Typ 384 → Min 216, Max 388<br>fsh; Typ 768 → Min 388, Max 776 |
| | | Specification Change | 27 | ■ **Switching Characteristics**<br>**LRCK Clock Timing**<br>**Normal Mode (TDM[1:0] bits = "00")**<br>fsd; Min 88.2 → 87<br>fsq; Min 176.4 → 174<br>fso; Typ 384 → Min 348, Max 388<br>fsh; Typ 768 → Min 696, Max 776<br>**TDM128 mode (TDM[1:0] bits = "01")**<br>fsd; Min 88.2 → 87<br>fsq; Min 176.4 → 174<br>**TDM256 mode (TDM[1:0] bits = "10")**<br>fsd; Min 88.2 → 87 |
| | | Error Correction | 33 | ■ **Timing Diagram**<br>Figure 16 is corrected. |
| | | Description Change | 34 | ■ **Timing Diagram**<br>Figure 18 is changed. |
| | | Error Correction | 35 | ■ **Timing Diagram**<br>Figure 20 is corrected. |
| | | Description Change | 43 | Table 11 is changed. |
| | | Description Added | 47 | DSD Mode : Added the following description.<br>DSDSEL [1:0] bits are changed during RSTN bit = "0". |
| | | Description Change | 62 | Table 30, 31 are changed. |
| | | Description Change | 79 | Figure 62 is changed. |
| | | Description Added | 80~81 | Precautions when using the 3-wire serial interface added. |

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