ISOFACE™

Galvanic Isolated Interfaces

ISO2H823V2 Evaluation Board Guide

ISO2H823V2 Evaluation Board Revision 1.1

EVAL ISO2H823V2.5

SP001328752

Application Note

About this document

Scope and purpose

This document describes the features and hardware details of the ISO2H823V2.5 Evaluation Board to experience the features of the innovative isolated 8 channel high side driver ISO2H823V2.5.

Abstract

The Evaluation Board Revision 1.1 houses the ISOFACE™ ISO2H823V2.5 and a 40 pin header for an easy Microcontroller or BUS-ASIC connection either per parallel or serial interface. At the process or factory side different kind of loads can be connected at a 2 row 8 output terminal connector. The board is intended to demonstrate the capabilities of the ISO2H823V2.5.

Internet Presence

http://www.infineon.com/isoface

Order Information

EVAL ISO2H823V2.5

Attention: The focus is safe operation under evaluation conditions. The board is neither cost nor size optimized and does not serve as a reference design.

1 Overview

The ISO2H823V2.5 is a galvanically isolated 8-bit data interface in PG-VQFN70-2 package that provides 8 fully protected high-side power switches that are able to handle currents up to 730 mA per channel.

An 8-bit parallel µController compatible interface or a serial SPI-interface allows to connect the IC directly to a µController system. The input interface supports also a direct control mode for writing driver information and is designed to operate with 3.3 V CMOS compatible levels.

This product is the second generation of isolated 8 channel digital output device (ISO2H823V2.5) and provides a robust integrated diagnosis for switches with low $R_{DS(on)}$ as well as an upgraded µController interface.

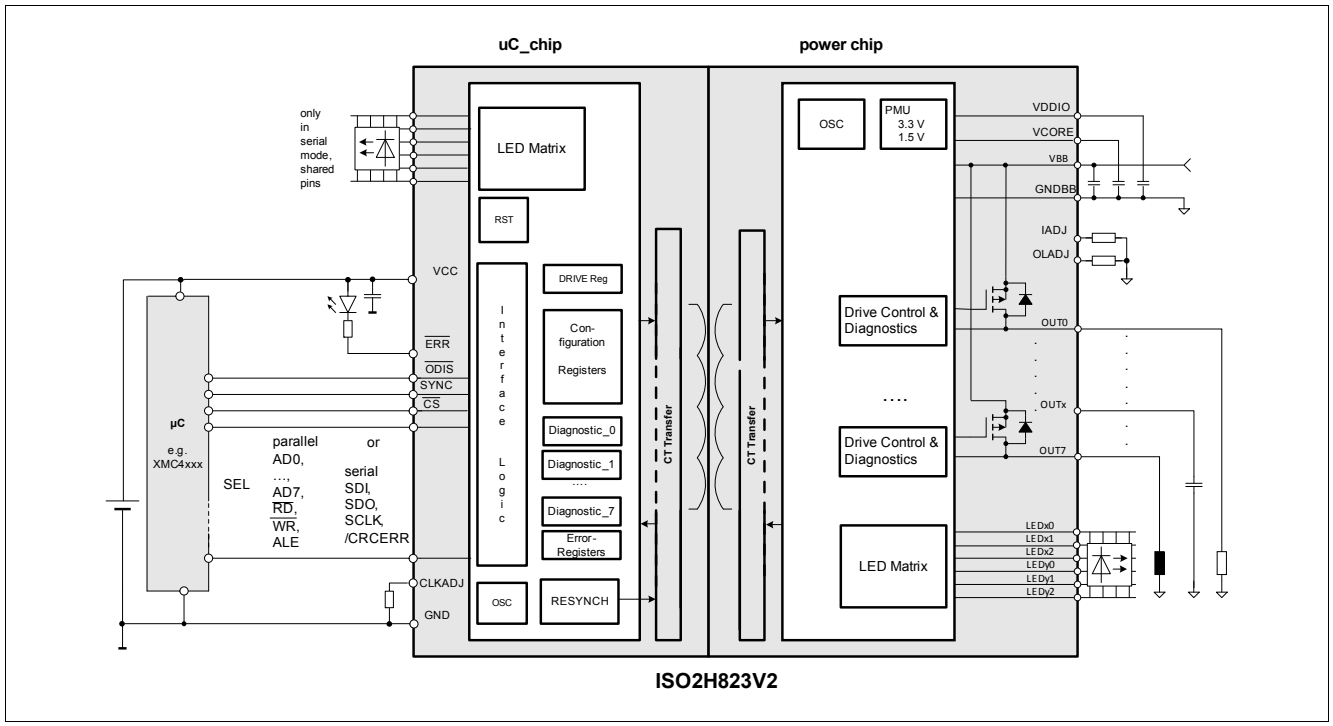


Figure 1 Typical Application

The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.

The IC contains 2 galvanic isolated voltage domains that are independent from each other. The input interface (µC-chip) is supplied at V_{CC} and the output stage (power chip) is supplied at V_{BB}. The different voltage domains can be switched on at different time. The output stage is only enabled once the input stage enters a stable state. The power chip generates out of V_{BB} two internal voltages V_{DDIO} = 3.3 V (± 10%) and V_{CORE} = 1.5 V (± 10%) which have to be buffered externally.

The ISOFACE ISO2H823V2.5 includes 8 high-side power switches that are controlled by means of the integrated parallel/serial interface. The interface is 8-bit µController compatible. Furthermore a direct control mode can be selected that allows the direct control of the outputs OUT0 … OUT7 (power chip) by means of the inputs AD0 … AD7 (µC-chip) without any additional logic signal. The IC can replace 8 optocouplers and the 8 high-side switches in conventional I/O-Applications as a galvanic isolation is implemented by means of the integrated coreless transformer technology. The µController compatible interface allows a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against overload, overtemperature and against overvoltage by an active zener clamp.

1.1 Board Overview

Figure 2 shows the main components of the ISO2H823V2.5 Evaluation Board and their interconnections. There are the following main building blocks:

- ISO2H823V2.5 in a 12x12 mm PG-VQFN70-2 package
- Supply connector 3V3 V_{DD}
- 40 pin connector for microcontroller connection
- $\overline{\text{ERR}}$ LED for fault indication
- Supply connector 24V V_{BB}
- 2x8 pin terminal for load connection
- LED Matrix indicating the output status

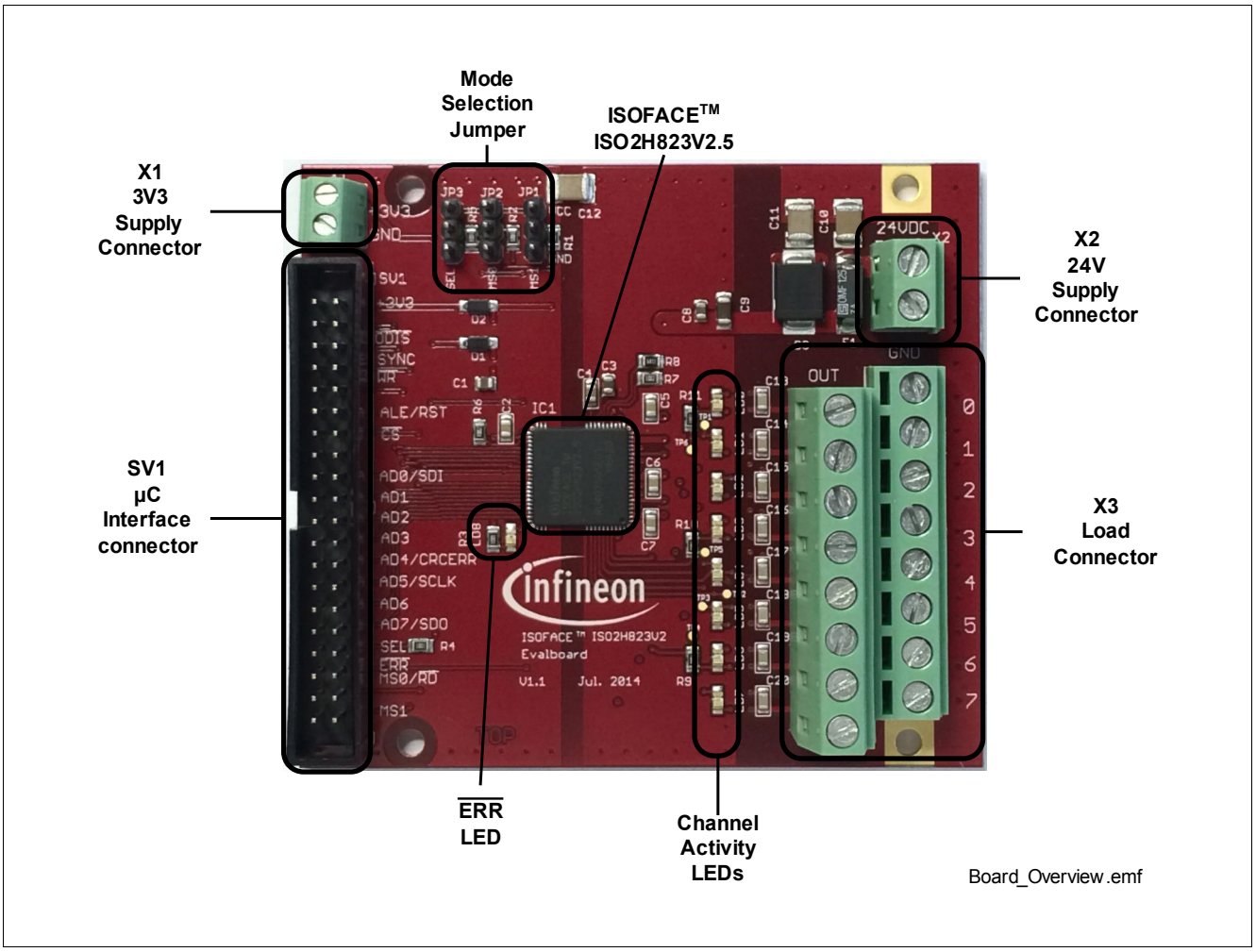


Figure 2 ISO2H823V2.5 Evaluation Board Revision 1.1

Table 1 Board Characteristics

Parameter	Min.	Max.	Unit	Remarks
V_{DD} 3V3 Input Voltage	3.0	3.8	V	Supply for the control side of the IC either supplied via connector X1 or connector pin 2 of connector SV1
V_{BB} 24V Input Voltage	11	35	V	

2 Functional Description

This board has been developed to experience the features of the innovative isolated 8 channel high side driver ISO2H823V2.5. The following sub chapters will explain the features and setup possibilities of the evaluation board and the ISO2H823V2.5.

The boards provided by Infineon have been subjected to functional testing only.

Due to their purpose, evaluation boards are not subjected to the same procedures regarding Returned Material Analysis (RMA), Process Change Notification (PCN) and Product Discontinuation (PD) as regular products. The boards are intended for development support only and should not be used directly as reference designs for volume production.

See Legal Disclaimer and Warnings for further restrictions on Infineon's warranty and liability.

2.1 Power Supply

The Evaluation board can be powered on the connector X1 or via the connector SV1 with 3.3V. The process side can be powered via the 2 pin terminal X2 with 24V nominal.

2.2 Microcontroller Interface

The ISO2H823V2.5 contains a microcontroller interface, which can be configured as a parallel or serial interface via the SEL pin.

Table 2 Interface Setting

Mode	JP3 SEL[1)]	JP2 MS0	JP1 MS1	Comment
Parallel				
	2-3 GND	open	open	
Serial				
Serial mode select per µC[2)]	1-2 V_{CC}	open	open	
Serial mode select per JP1 and JP2				
Serial mode 0: Drive mode without CRC	1-2 V_{CC}	2-3 GND	2-3 GND	
Serial mode 1: Drive mode with CRC		1-2 V_{CC}	2-3 GND	
Serial mode 2: Register access without CRC		2-3 GND	1-2 V_{CC}	
Serial mode 3: Register access with CRC		1-2 V_{CC}	1-2 V_{CC}	

1) The SEL pin has to be configured before powering up the device
2) The serial mode will be set via the logic level at the SV1 connector

SEL (Serial or Parallel Mode Select)

When this pin is in a logic Low state, the IC operates in parallel mode. For serial mode operation the pin has to be pulled into logic High state. This pin has an internal Pull-Down resistor.

$\overline{CS}$ (Chip Select)

When this pin is in a logic Low state, the IC interface is enabled and data can be transferred. This pin has an internal Pull-Up resistor.

$\overline{\text{ODIS}}$ (Output Disable)

The low active $\overline{\text{ODIS}}$ signal immediately switches off the output channels OUT0-OUT7. This pin has an internal Pull-Down resistor. In normal operation the signal $\overline{\text{ODIS}}$ is high. Setting $\overline{\text{ODIS}}$ to Low clears the DRIVE register as well. The minimum width of the $\overline{\text{ODIS}}$ signal is 5 µs.

SYNC

This pin can be used for synchronisation purpose, for normal operation pull this pin up. For details refer to the ISO2H823V2.5 datasheet. This pin has an internal Pull-Up resistor.

$\overline{\text{ERR}}$ (Fault Indication)

The low active $\overline{\text{ERR}}$ signal contains the OR-wired diagnostic information depending on chosen serial or parallel mode (V_{BB} undervoltage or missing voltage detection, the internal data transmission failure detection unit and the fault(s) of the output switch).The output pin $\overline{\text{ERR}}$ provides an open drain functionality.This pin has an internal Pull-Up resistor. In normal operation the signal $\overline{\text{ERR}}$ is high.

2.2.1 Parallel Interface Mode

$\overline{\text{WR}}$ (Write)

By pulling this pin down, a write transaction is initiated on the AddressData bus and the data has to be valid on the rising edge of $\overline{\text{WR}}$. The AD7-bit of the register address has to be set to ‘1’. This pin has an internal Pull-Up resistor.

$\overline{\text{RD}}$ (Read)

By pulling this pin down, a read transaction is initiated on the AddressData bus and the data are driven by the falling edge of $\overline{\text{RD}}$. The AD7-bit of the register address has to be set to ‘0’. This pin has an internal Pull-Up resistor.

ALE (Address Latch Enable)

The pin ALE is used to select between address (ALE is in a logic High state) or data (ALE is in a logic Low state). Furthermore, a read or write transaction can be selected with the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pin. When ALE is pulled high, address is transferred and latched over the bit AD0 to AD7. During the time interval where ALE = High RD or $\overline{\text{WR}}$ have to be pulled to High. During the Low State of ALE all transactions hit the same address. This pin has an internal Pull-Down resistor.

AD7:AD0 (AddressData input / output bit7 ... bit0)

The pins AD0 .. AD7 are the bidirectional input / outputs for data write and read. Depending on the state of the ALE pin and the AD7 pin, register addresses or data can be transferred between the internal registers and e.g. the micro-controller. By connecting $\overline{\text{CS}}$ and $\overline{\text{WR}}$ and ALE/RST pins to GND and $\overline{\text{RD}}$ to V_{CC}, the parallel direct mode is activated.The interface can be directly controlled by the µController output ports (see Figure 3). The output pins AD7:AD0 are in state “Z” as long as $\overline{\text{CS}}$=1, $\overline{\text{RD}}$=1 and $\overline{\text{WR}}$=1.

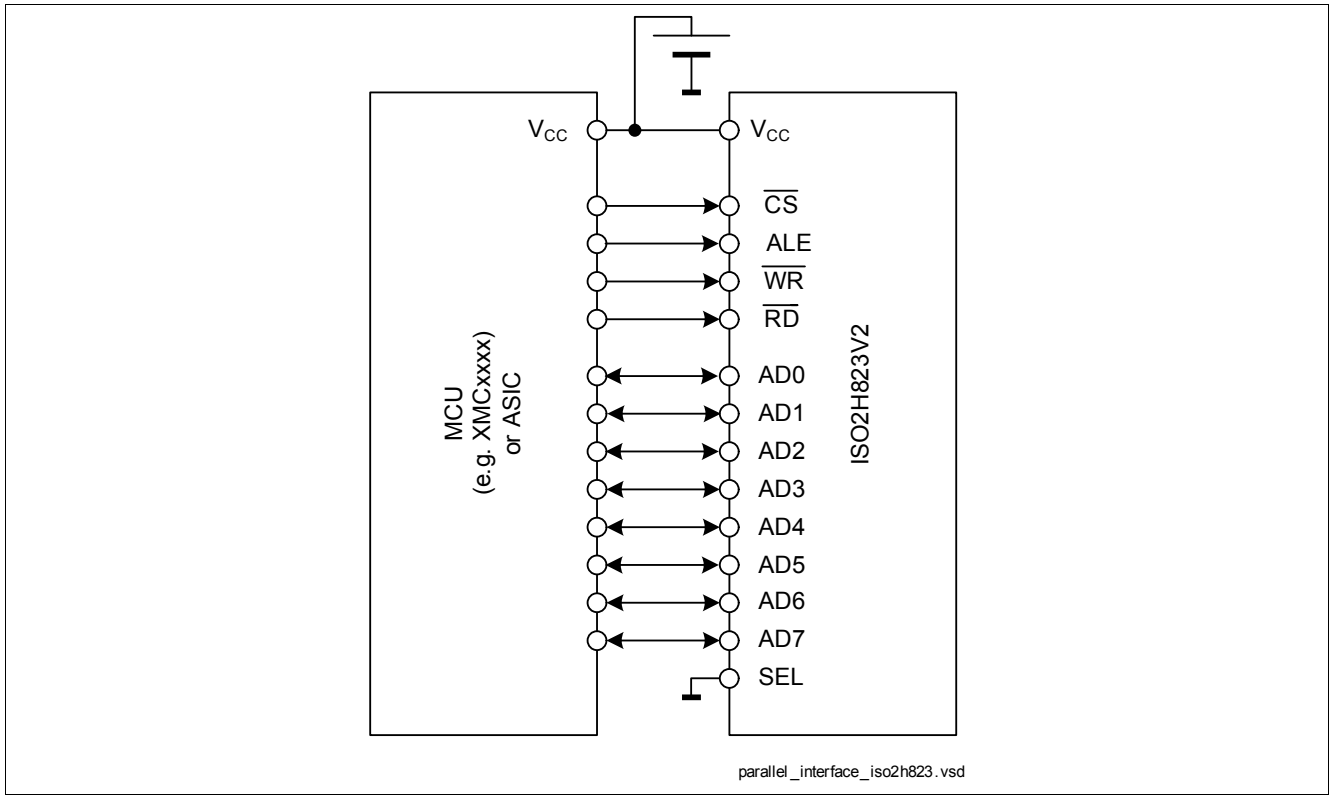


Figure 3 Bus Configuration for parallel mode

The timing requirements for the parallel interface are shown in Figure 4 (Read), Figure 5 (Write) and inside the chapter electrical characteristics in the ISO2H823V2.5 datasheet.

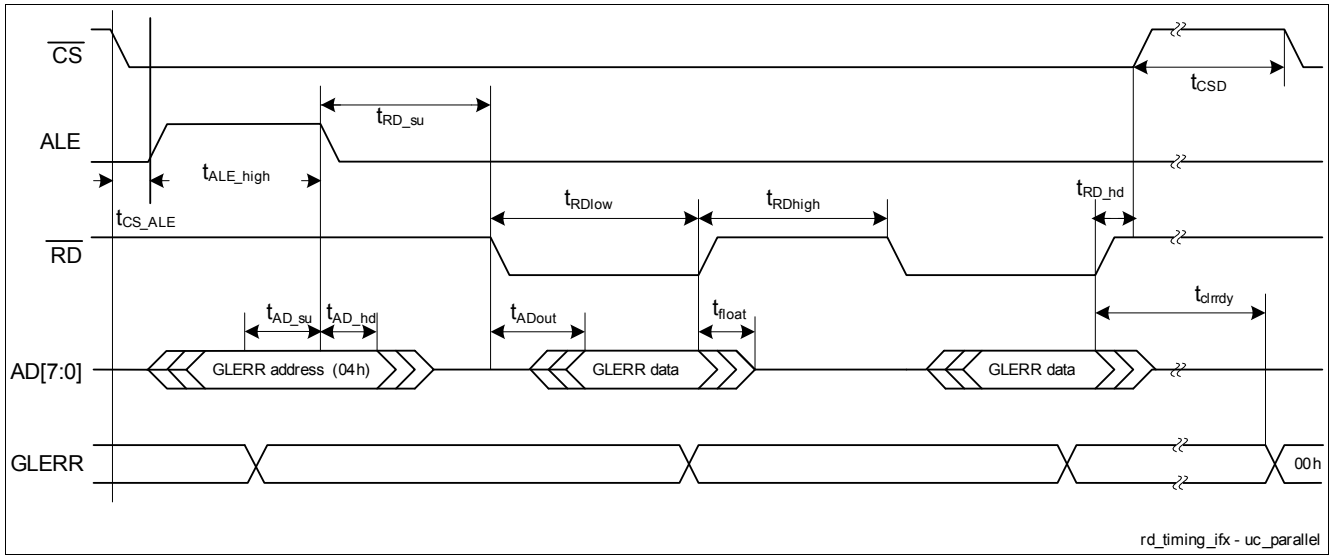


Figure 4 Timing by Parallel Read Access (e.g. GLERR Register)

For a reading access to internal registers the MSB of the address register has to be set to “0”.

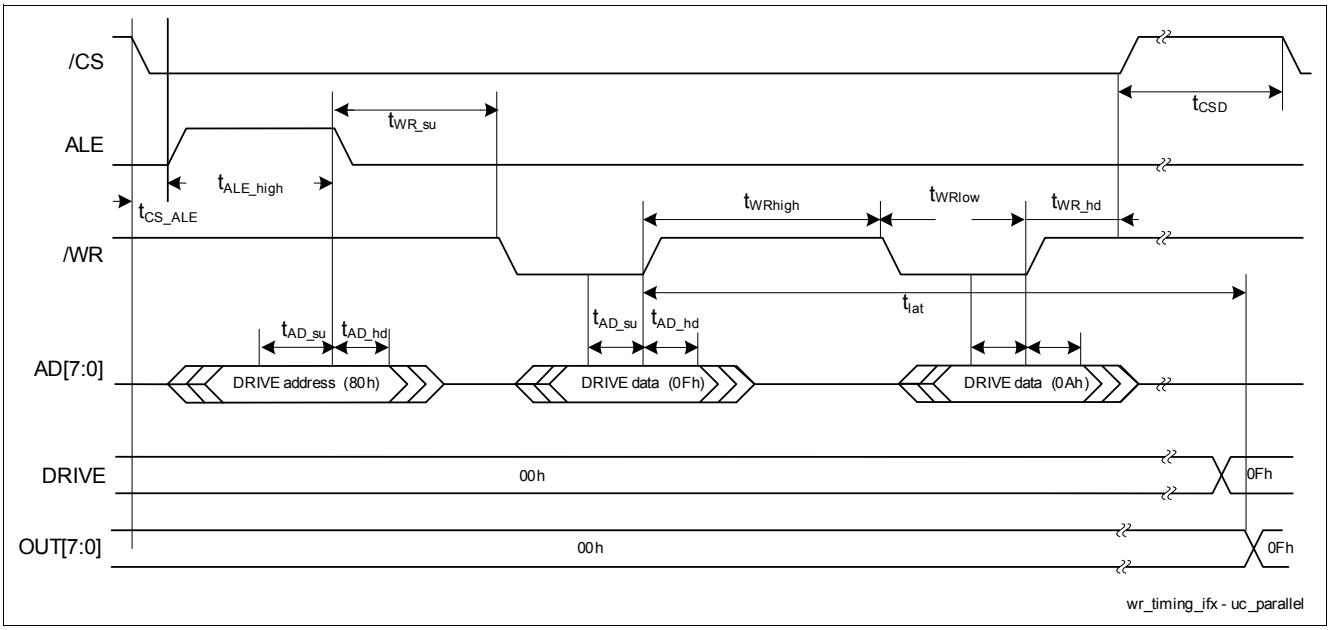


Figure 5 Timing by Parallel Write Access (e.g. DRIVE Register)

For a writing access to internal registers the MSB of the address register has to be set to “1”.

2.2.1.1 Parallel Direct Mode

The parallel interface can be also used in a direct mode that allows direct changes of the output OUT0...OUT7 by means of the corresponding inputs AD0-AD7 without additional logic signals. To activate the parallel direct mode $\overline{CS}$, $\overline{WR}$ and ALE pins have to be wired to ground and $\overline{RD}$ has to be wired to V_{CC} as shown in the Figure 6. The asynchronous output disable $\overline{ODIS}$ has to be tied high, because this safety function will otherwise override the drive information. Although the diagnostics cannot be read in this operation mode, W4P (Wait for power) and OTC over temperature faults are reported at the $\overline{ERR}$ pin (volatile).

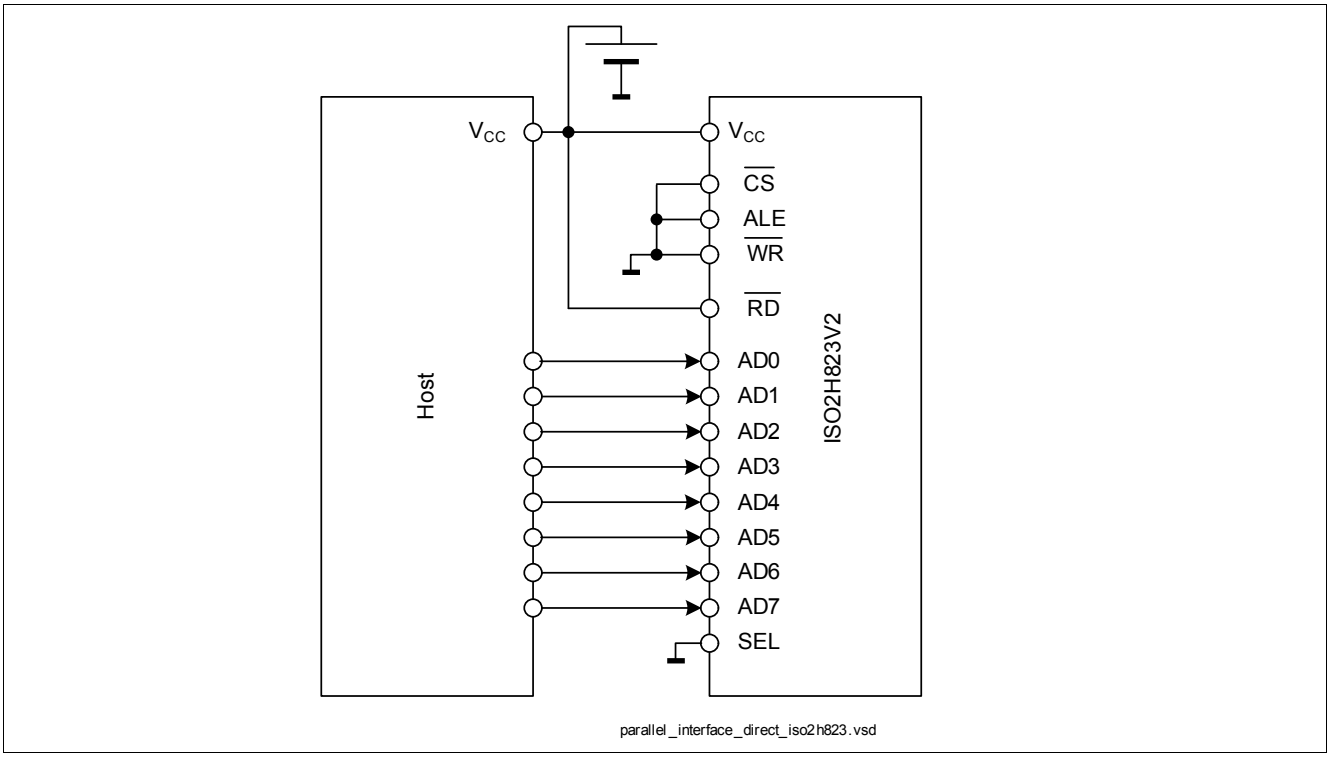


Figure 6 Parallel Direct Mode

The direct mode is intended to be an additional parallel mode which is invoked directly after reset. In this case internal settings have already been realized (f.e. MSB of the address register is set to “1”).

2.2.2 Serial Interface Mode

The ISO2H823V2.5 device contains a serial interface that can be activated by pulling the SEL pin to logic high state. The interface can be directly controlled by the µController output ports. The output pin SDO is in state “Z” as long as $\overline{CS}$=1. Otherwise, the bits at the SDI input are sampled with the rising edge of SCLK and registered into the input FIFO buffer of length dependent on the selected SPI-mode (8, 16, 24 bits, Figure 8, Figure 9, Figure 10, Figure 11). With every falling edge of SCLK the bits to be read are provided serially to the pin SDO.

The timing requirements for the serial interface are shown in Figure 7 and inside the chapter electrical characteristics in the ISO2H823V2.5 datasheet.

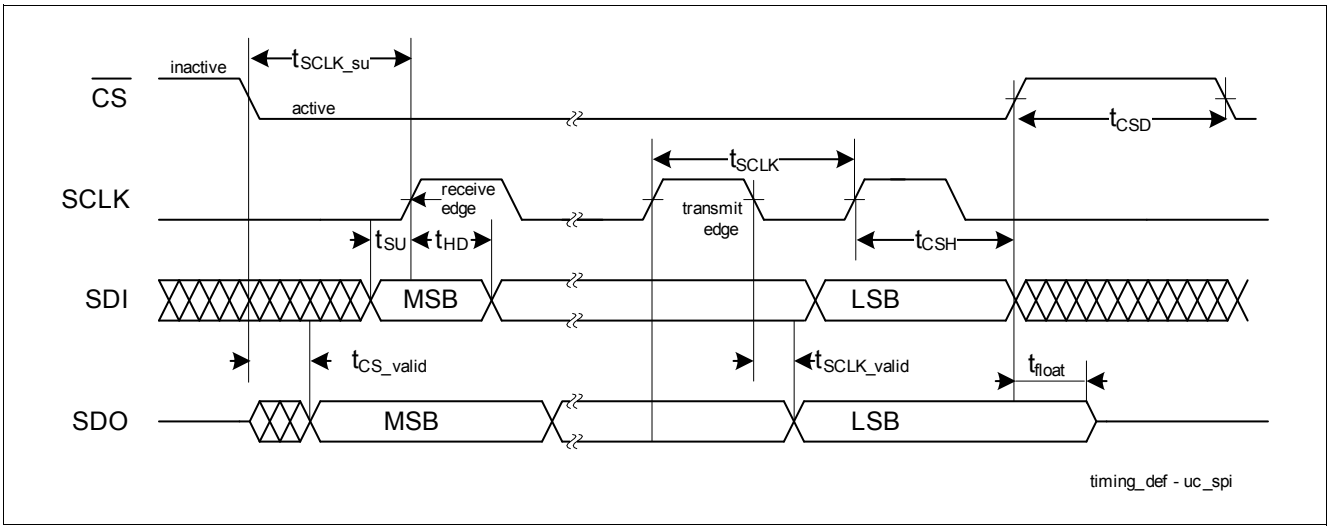


Figure 7 Serial Bus Timing

2.2.2.1 SPI Modes

Four different SPI-modes can be distinguished (Figure 8 - Figure 11).

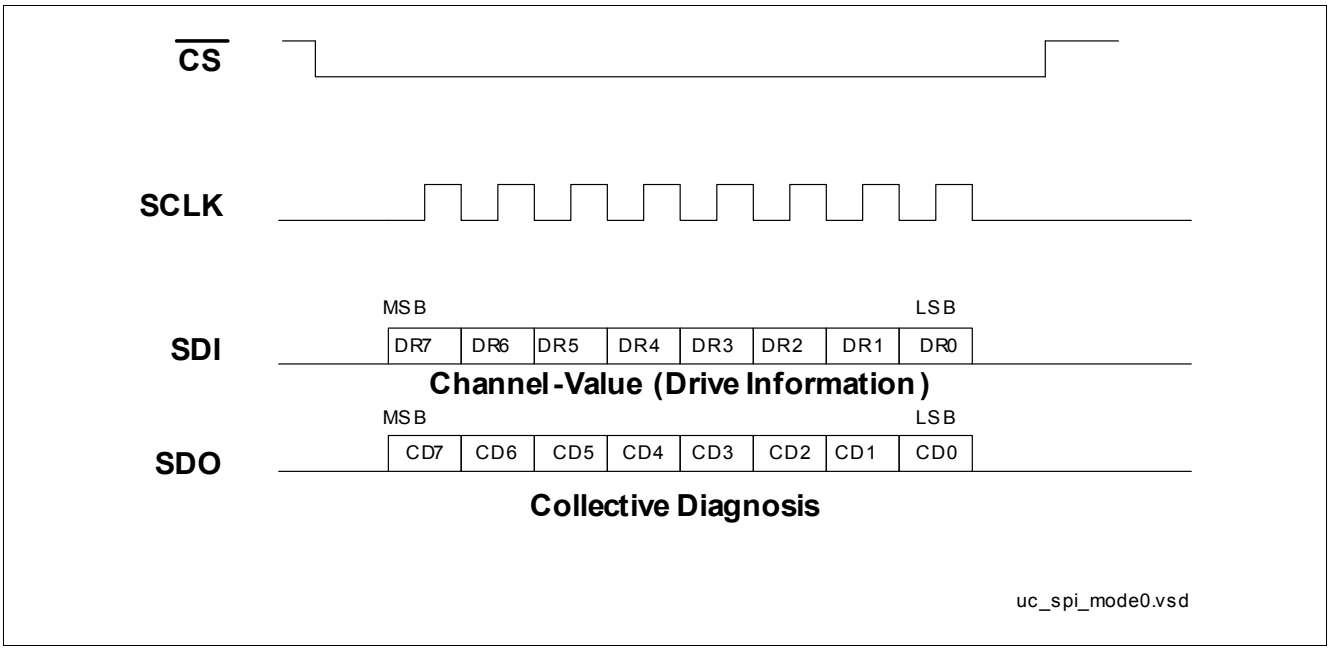


Figure 8 SPI Mode 0, MS0 = 0, MS1 = 0, Daisy Chain Supported

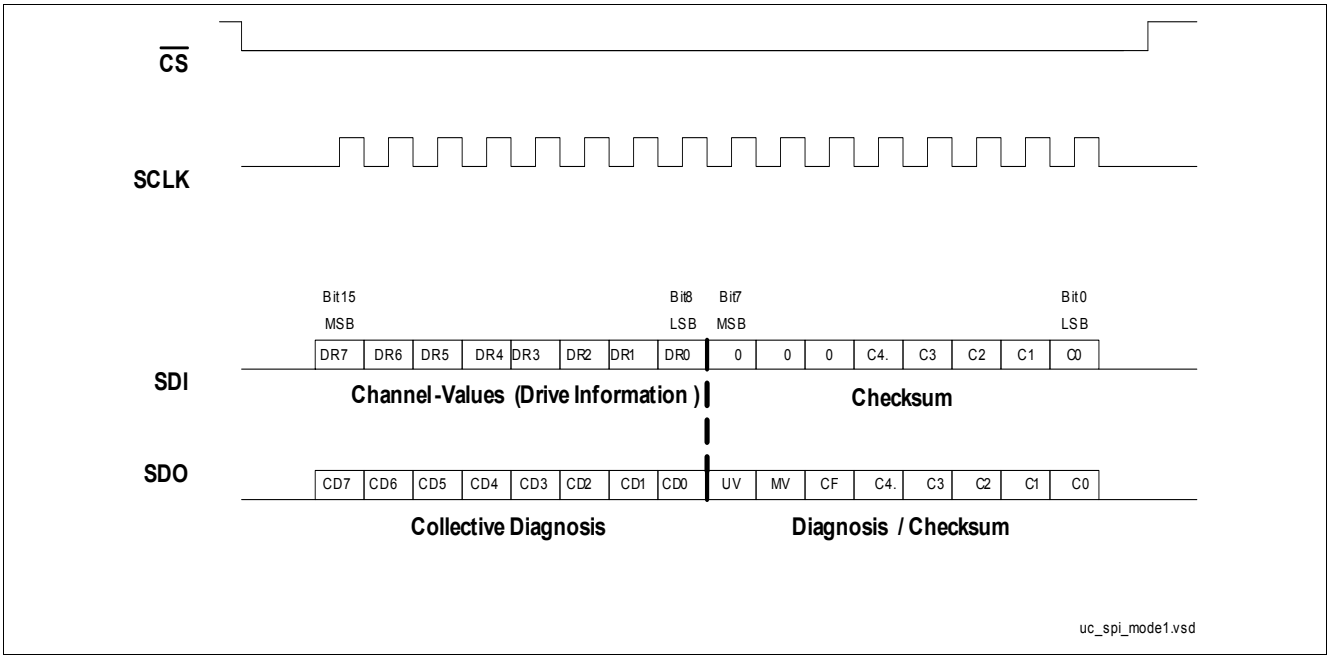


Figure 9 SPI Mode 1, MS0 = 1, MS1 = 0, Daisy Chain Supported

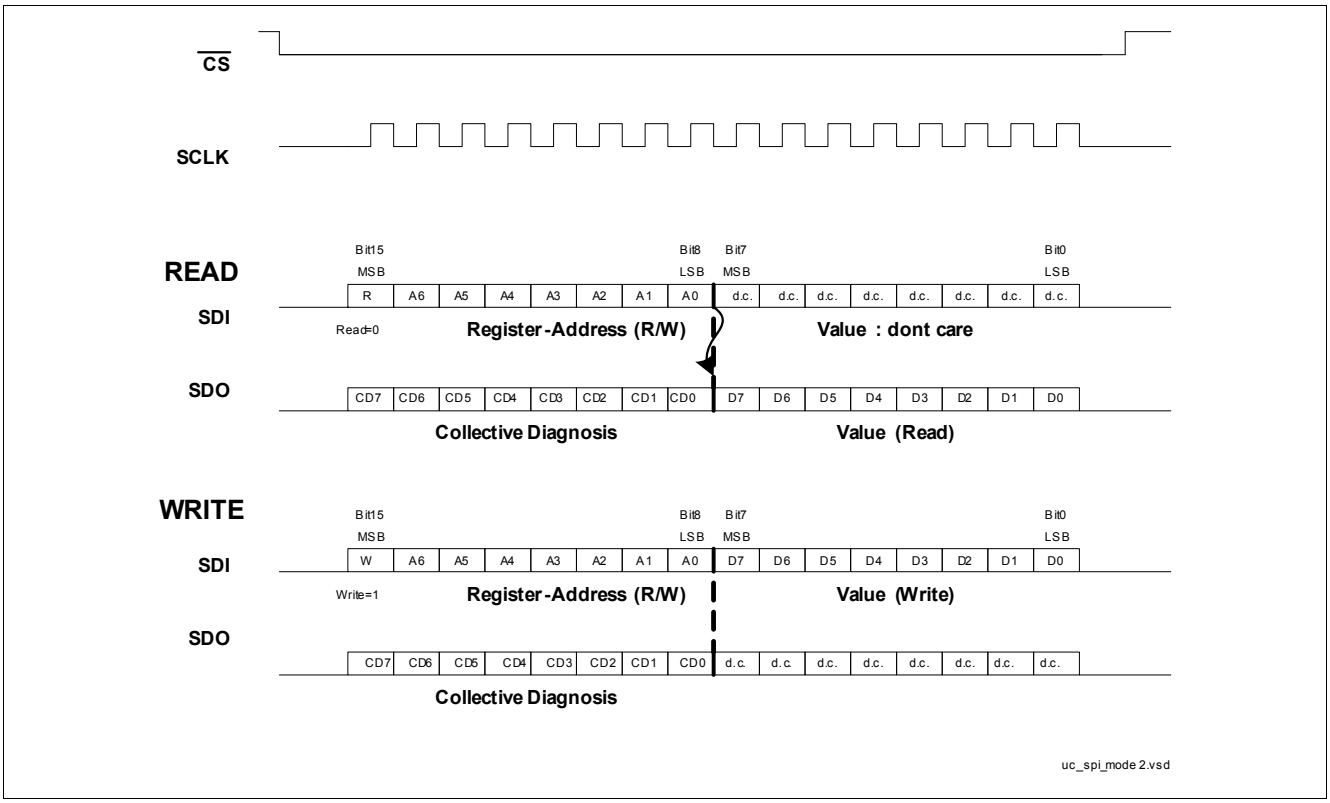


Figure 10 SPI Mode 2, MS0 = 0, MS1 = 1

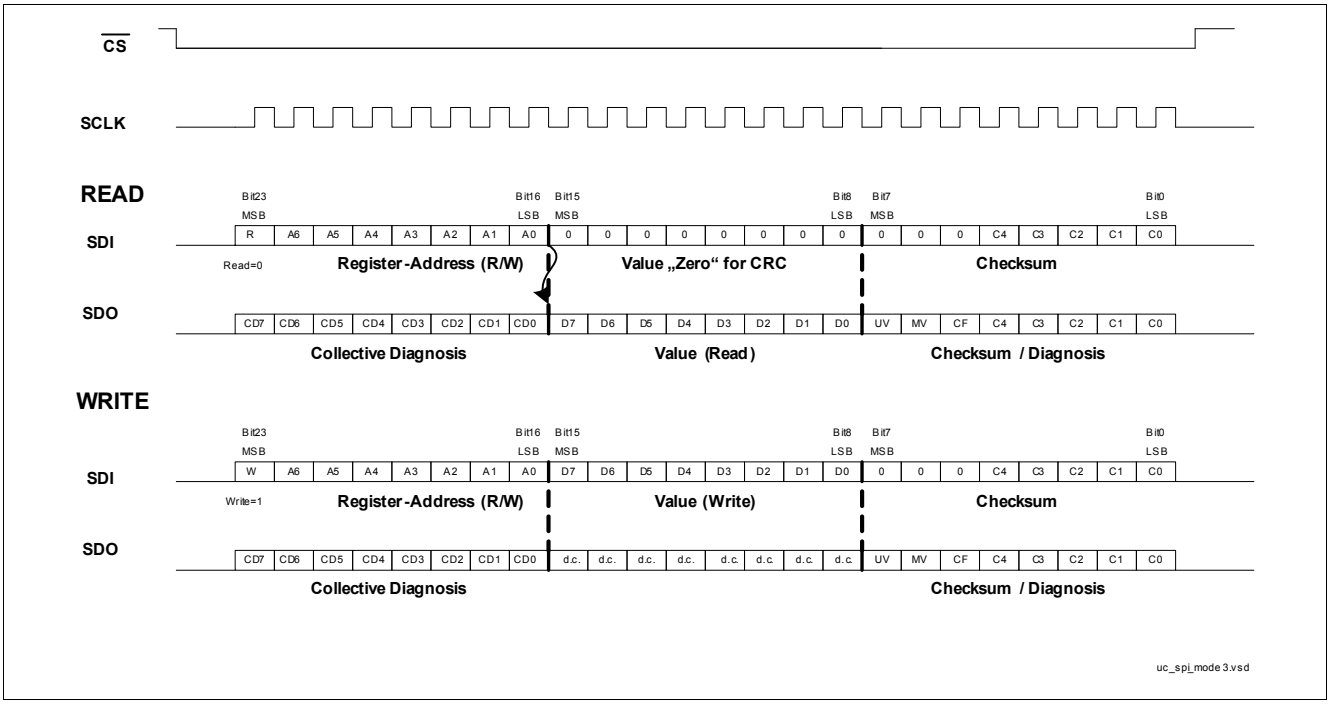


Figure 11 SPI Mode 3, MS0 = 1, MS1 = 1

2.3 Process Side

2.3.1 Output Stage

Each channel contains a high-side power FET that is protected by embedded protection functions. The continuous current for each channel is 600 mA nominal, which depends on the cooling conditions and the total power dissipation.

2.3.1.1 Output Stage Control

Each output is independently controlled by an output latch and a common reset line via the pin $\overline{\text{ODIS}}$ that disables all eight outputs and resets the latches.

2.3.1.2 Protection Functionality

Power Transistor Overvoltage Protection

Each of the eight output stages has it’s own zener clamp that causes a voltage limitation at the power transistor when solenoid loads are switched off. V_{ONCL} is then clamped to 52 V (typ.).

Power Transistor Overload Protection

The outputs are provided with a linear current limitation, which regulates the output current to the current limit value in case of overload. The electrical operation point does not lead to a shutdown.

The excess power dissipation in the power transistor during current limitation will lead to a rapid increase of the junction temperature. When the junction temperature exceeds 150°C (typ.) the output will switch off and will switch on again when the junction temperature has cooled down by a temperature hysteresis of 15K (typ.). Therefore during overload a thermal on-off toggling may occur.

The thermal hysteresis is reset during inactive mode. Therefore when switching to the active mode the power transistor is first switched on if the junction temperature is below 150°C.

Current Sense and Limitation

To achieve an excellent accuracy for the current limitation and current referred diagnostic (OCLx) an external reference resistor is used. The nominal resistor value is 6.81 kΩ , the tolerance should be within 2% to meet an overall current limit tolerance from 0.73 A to 1.3 A.

To offer open load diagnostics in active mode, a part of the power transistor is driven down when the drain-source-voltage drops below a certain limit (low load condition). The voltage drop across the remaining part is used to evaluate an open load diagnostic.

Diagnostic Functions

For each of the output stages 5 different types of diagnostics are available. Table 3 specifies the diagnostics.

Some of the diagnostics are available only in active mode, others only in inactive mode. The diagnostics OLIx, OLAx, SCVx can be prolonged within the complementary mode. Overtemperature in inactive mode is not reported (set to zero).

Table 3 Diagnostic

Item	Diagnostic Type	Inactive Mode	Active Mode
OTx	Overtemperature	no	yes (OTx Active)
OLIx	Open Load/Wire Break, “inactive”	yes	no
OLAx	Open Load/Wire Break, “active”	no	yes
OCLx	Current Sense, Overload Detection	no	yes
SCVx	Short Circuit to V_{BB}	yes	not distinguishable from OLAx

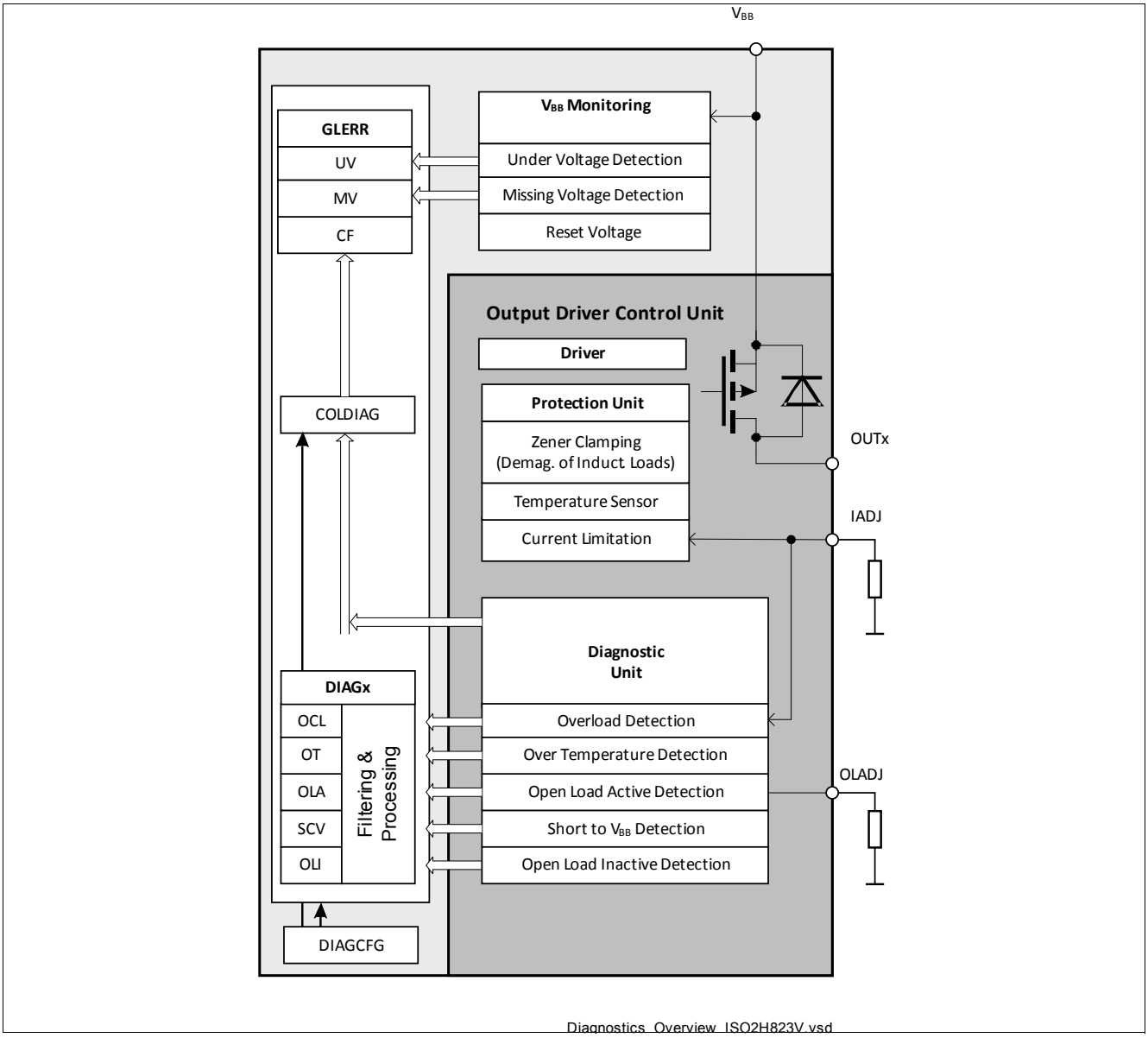


Figure 12 Diagnostics Overview

Global Diagnostics

The global diagnostics include:

- **UV:** undervoltage supply condition when VBB is below 16 V with 0.5 V hysteresis,
- **MV :** missing voltage supply condition when VBB is below 13 V with 0.5 V hysteresis,
- **OTP:** global over temperature (chip temperature outside the switch area triggers above 125°C), the global over temperature does not lead to thermal shutdown,
- **ALLOFF:** all drivers in the power chip are disabled (by DRIVE-programming, $\overline{\text{ODIS}}$-setting or temperature shutdown of all channels),
- LAMP: the load of one of the drivers behaves like a cold lamp

2.3.1.3 Power Supply

The startup procedure of the power chip is explained in Figure 13.

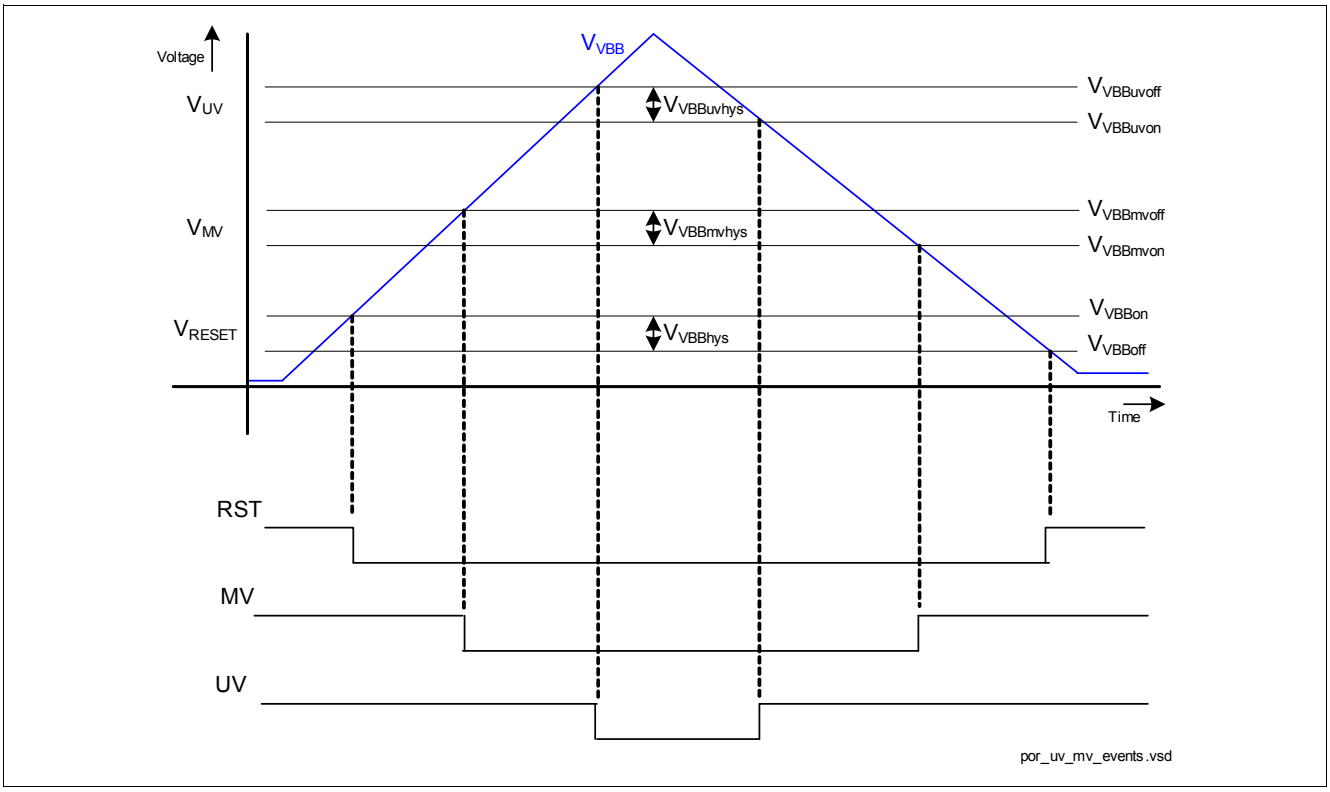


Figure 13 Start Up Procedure of the Power Chip

During UVLO, all registers of the power chip are reset to their reset values as specified in the register description (Chapter 6 inside the datasheet). As a result, the flags TE, UV as well as MV are High and the $\overline{\text{ERR}}$ pin is Low (error condition). Immediately after the reset is released, the chip is first configured by “reading“ the logic level of the SEL, MS1, MS0 - pins. The IC powers up as a parallel device i.e. the AD0-7 pins are high-impedance until the IC configuration is over.

The supply voltage V_{BB} is monitored during operation by two internal comparators (with typ. 2 ms blanking time) detecting:

- V_{BB} Undervoltage: If the voltage drops below the UV threshold, the UV-bit in the GLERR register is set High. The IC operates normally.
- V_{BB} Missing Voltage: If the voltage further drops below the MV threshold, lower than the previous threshold, the MV-bit in the GLERR register is set, the Power Side of the IC is turned off when reaching the VReset-threshold whereas the Micro-Controller Side remains active.

Note: The driver stage is self protected in overload condition: the internal switches will be turned off as long as the overcurrent condition is detected and the IC will automatically restart once the overload condition disappears.

Important: Since the UV and MV (as well as the TE) bits used for generating the $\overline{\text{ERR}}$ signal are preset to High during UVLO, the $\overline{\text{ERR}}$ pin is Low after power up. Therefore the $\overline{\text{ERR}}$ requires to be explicitly cleared after power up. At least one read access to the GLERR and INTERR registers or one default read access in certain access-modes (see Chapter 4 of the datasheet) is needed to update those status bits and thus release the $\overline{\text{ERR}}$ pin.

3 Getting Started

In general to have a quick start, it is recommended either to use the parallel setup, serial mode 0 or serial mode 2. For a quick check of the switching perfomance the parallel direct mode will be the first choice.

3.1 Setting up the board for the parallel mode

Follow the steps before powering up the board

- Connect Jumper JP3 to GND (Connection 2-3).
- Remove Jumper on JP1 and JP2, if present
- Ensure that the following signal levels are present at connector SV1 from your control board:
  - $\overline{CS}$
  - $\overline{WR}$
  - $\overline{RD}$
  - $\overline{ODIS}$
  - SYNC
  - AD0..AD7

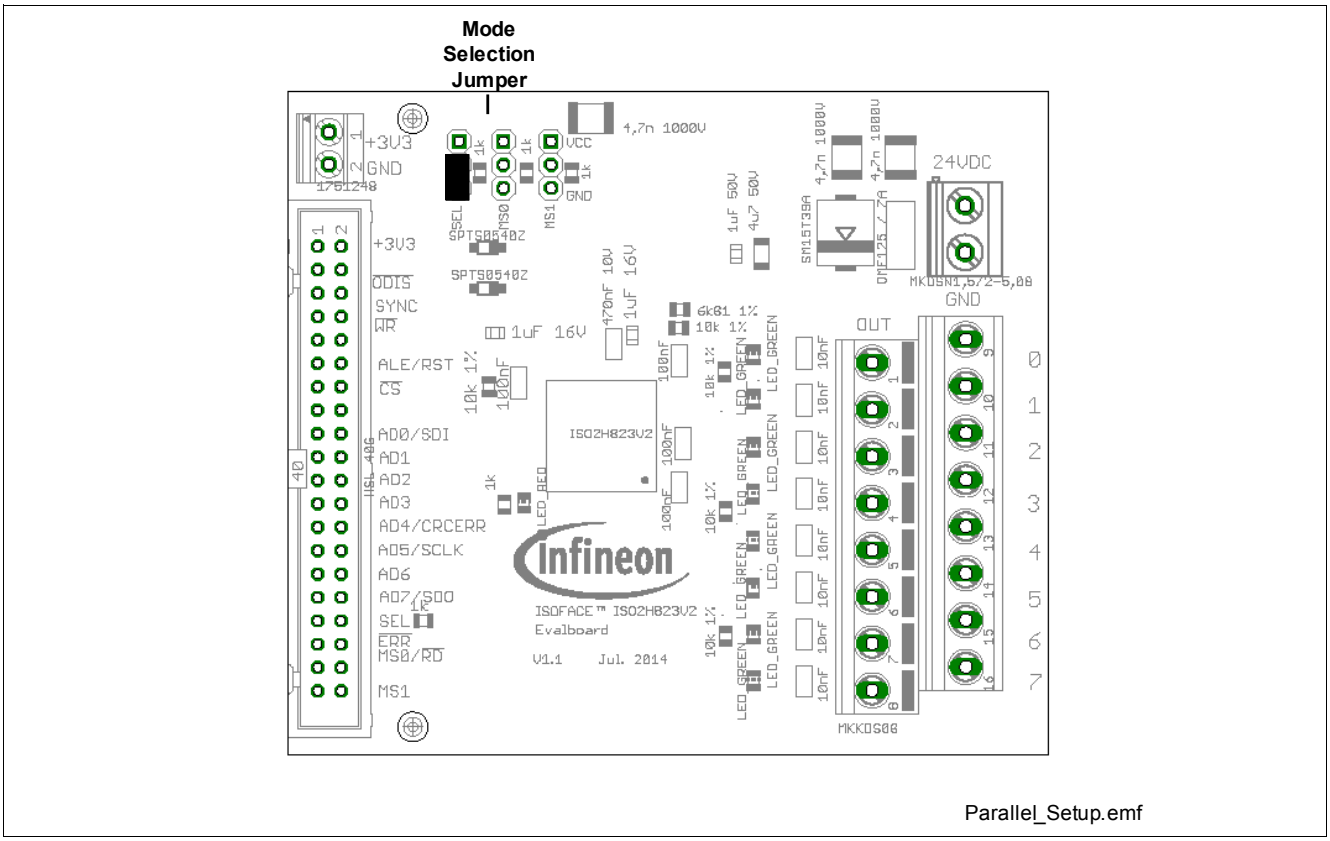


Figure 14 Jumper setting for parallel mode

3.2 Setting up the board for the parallel direct mode

Follow the steps before powering up the board

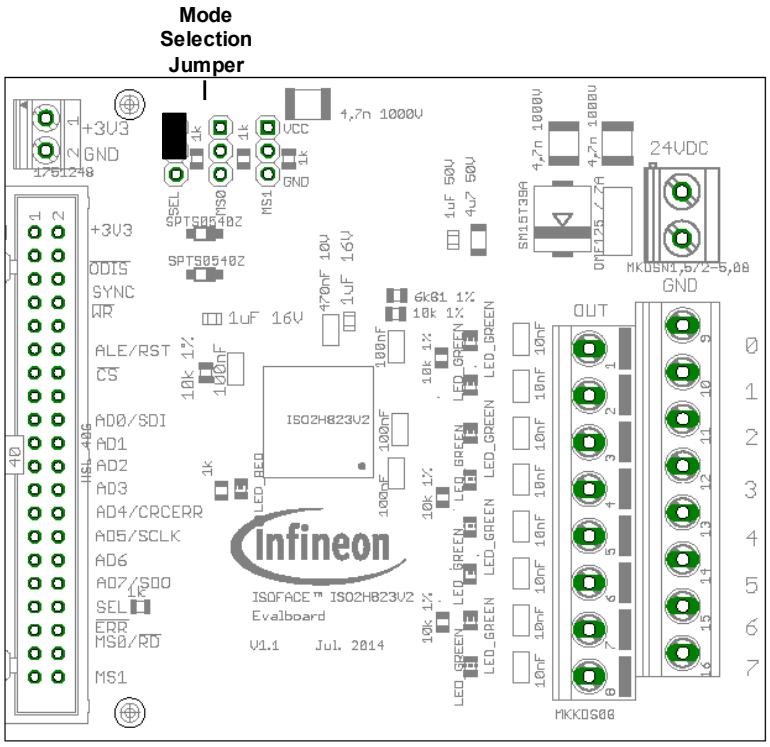
- Connect Jumper JP3 to GND (Connection 2-3).
- Remove Jumper on JP1 and JP2, if present.
- Connect your controller to connector SV1
- Ensure that the following signal levels are present at SV1
  - $\overline{CS}$ set to LOW
  - $\overline{WR}$ set to LOW
  - $\overline{RD}$ set to HIGH
  - ALE set to LOW
  - $\overline{ODIS}$ set to HIGH
  - SYNC set to HIGH

After applying V_{DD} and V_{BB} to the board, the $\overline{ERR}$ LED will be turned off. The outputs OUT0 ..OUT7 will be directly controlled via the signals connected to AD0 .. AD7 on the connector SV1.

3.3 Setting up the board for the serial mode

Follow the steps before powering up the board

- Connect Jumper JP3 to VCC (Connection 2-3).
- Remove Jumper on JP1 and JP2, if you are planing to externally control the serial mode.
- Ensure that the following signal levels are present from your control board:
  - $\overline{CS}$
  - MS0, MS1
  - $\overline{ODIS}$
  - SYNC
  - SDI
  - SDO
  - SCLK
  - $\overline{CRCERR}$



Serial_Setup.emf

Figure 15 Jumper setting for serial access

If it is not intended to change the used SPI transfer mode by the attached controller, the SPI Mode can be set by placing jumpers JP1 and JP2 according Table 2. As an example the setup for SPI mode 2 is shown in Figure 16.

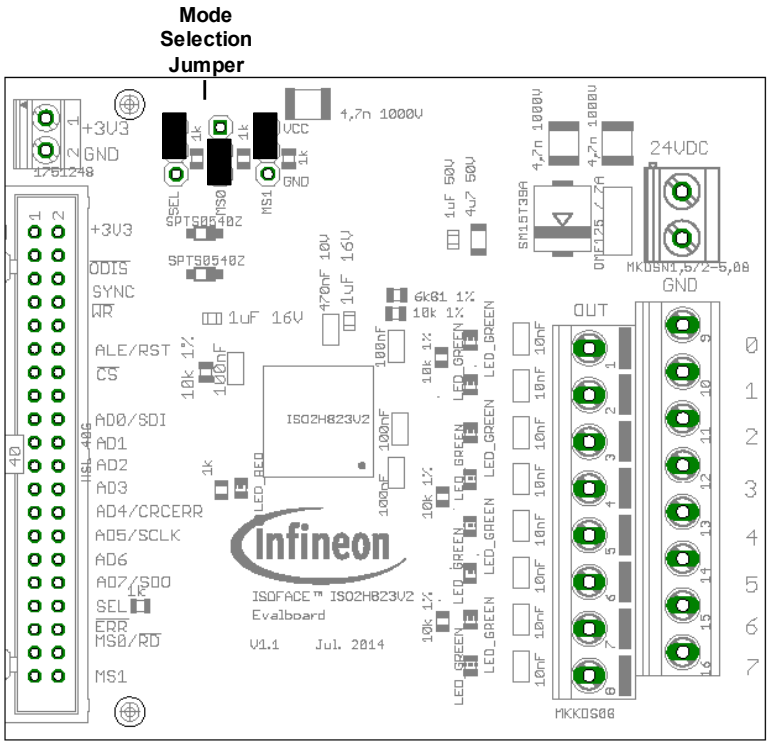


Figure 16 Jumper setting for serial mode 2

4 Connectors

Connector SV1

	1	2	
	GND	V_{DD}	
3	GND	!ODIS	4
5	GND	SYNC	6
7	GND	!WR	8
9	GND	ALE / RST	10
11	GND	n.c.	12
13	GND	!CS	14
15	GND	n.c.	16
17	GND	AD0	18
19	GND	AD1	20
21	GND	AD2	22
23	GND	AD3	24
25	GND	AD4	26
27	GND	AD5	28
29	GND	AD6	30
31	n.c.	AD7	32
33	n.c.	SEL	34
35	n.c.	!ERR	36
37	GND	MS0 / !RD	38
39	GND	MS1	40

(Top View)

Figure 17 Connector SV1 Signal Mapping Top View

Table 4 Connector SV1 Mapping per Mode

No.	Serial Mode	Parallel Mode	Comment
2	V_{DD}	V_{DD}	
4	$\overline{ODIS}$	$\overline{ODIS}$	
6	SYNC	SYNC	
8		$\overline{WR}$	
10	RST	ALE	
12			
14	$\overline{CS}$	$\overline{CS}$	
16			
18	SDI	AD0	
20		AD1	
22		AD2	
24		AD3	
26	$\overline{CRCERR}$	AD4	
28	SCLK	AD5	
30		AD6	
32	SDO	AD7	
34	SEL	SEL	
36	$\overline{ERR}$	$\overline{ERR}$	
38	MSO	$\overline{RD}$	
40	MS1		

Table 5 Connector X3 Mapping

No.	Top Row	No.	Lower Row	Comment
1	OUT0	9	GND_{BB}	
2	OUT1	10	GND_{BB}	
3	OUT2	11	GND_{BB}	
4	OUT3	12	GND_{BB}	
5	OUT4	13	GND_{BB}	
6	OUT5	14	GND_{BB}	
7	OUT6	15	GND_{BB}	
8	OUT7	16	GND_{BB}	

5 Production Data

5.1 Schematic

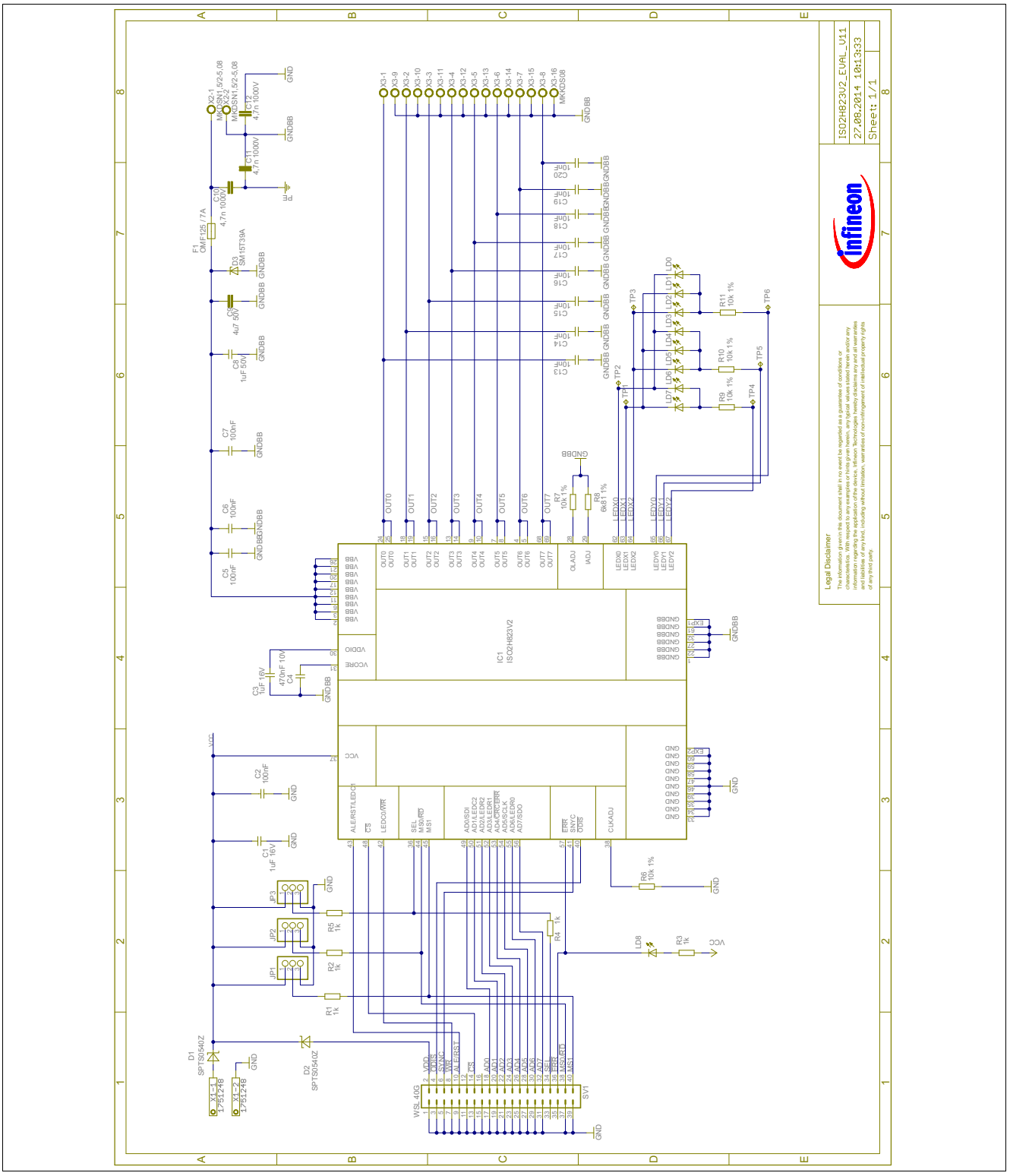


Figure 18 Schematic

5.2 Components Placement

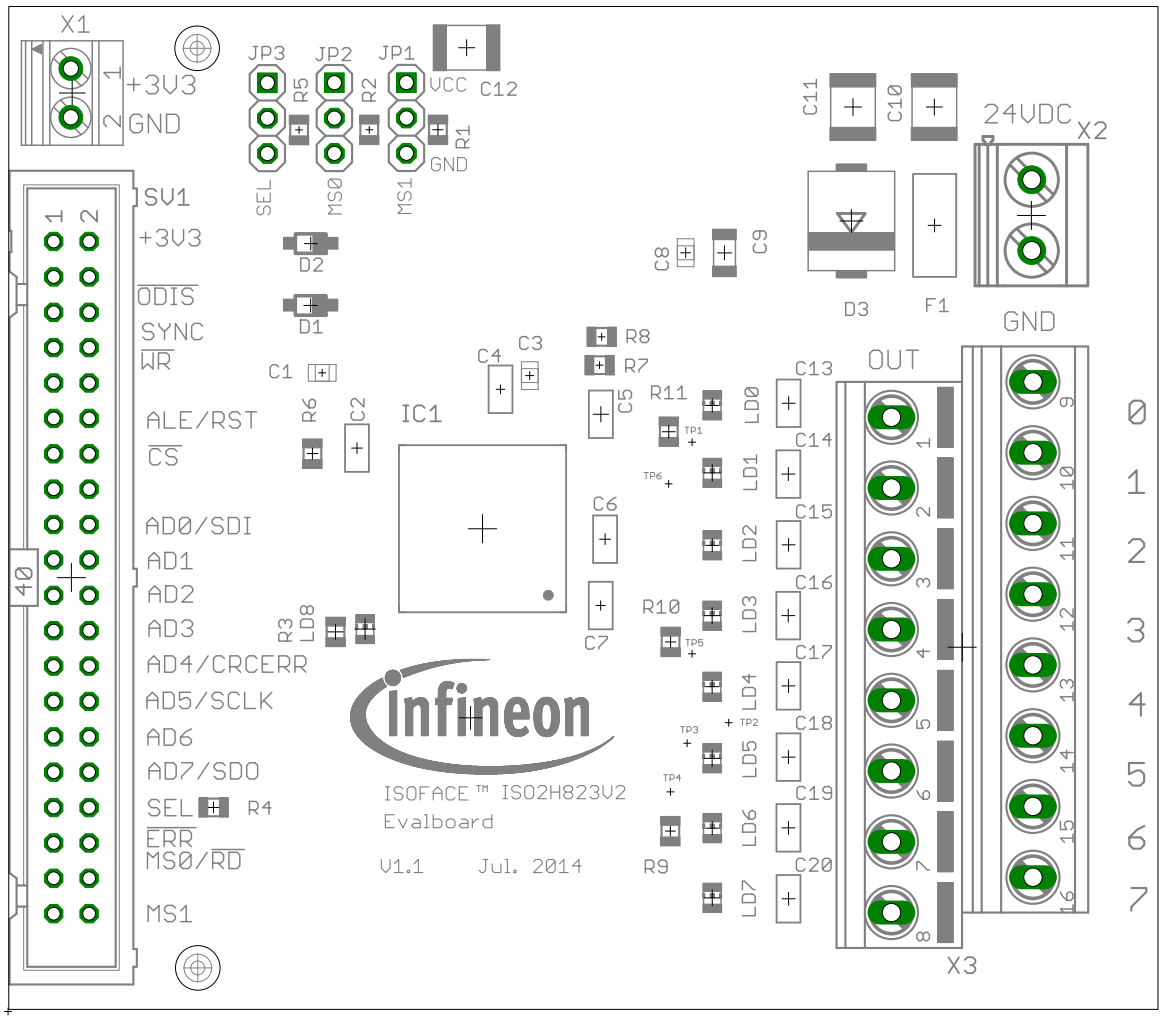


Figure 19 Component Placement

5.3 Layout

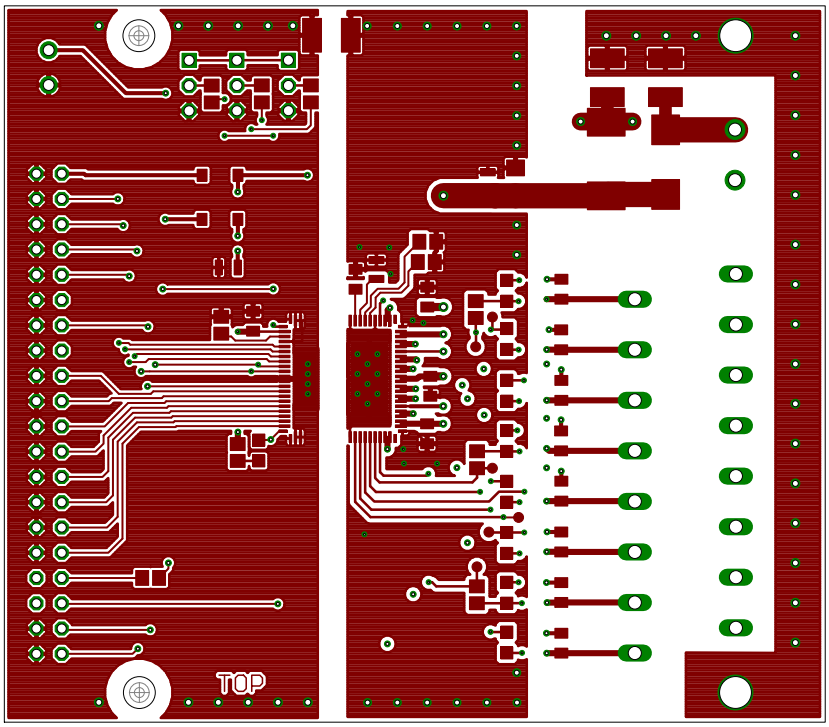


Figure 20 Top Layer L1

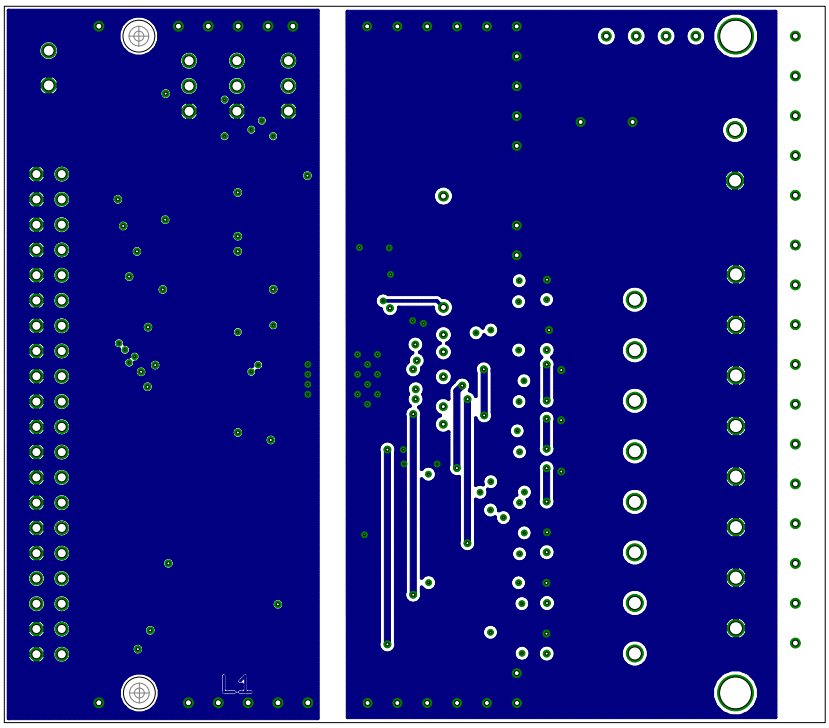


Figure 21 Inner Layer L2

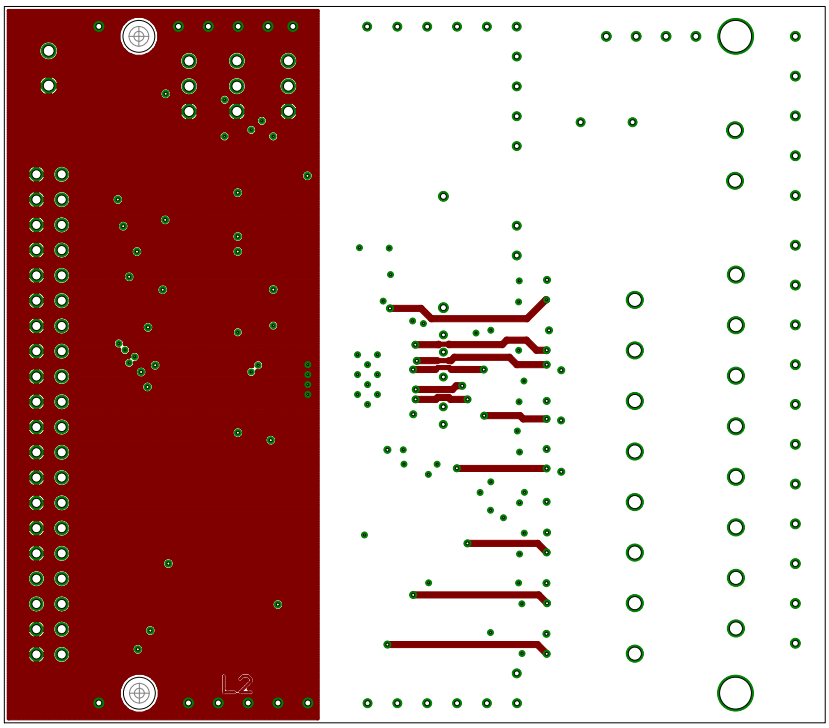


Figure 22 Inner Layer L3

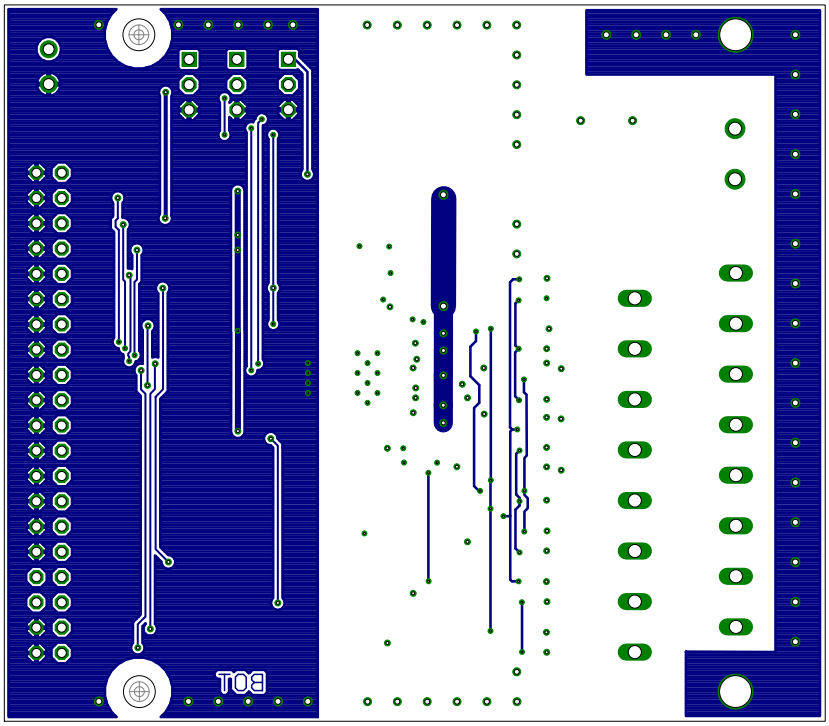


Figure 23 Bottom Layer L4

5.4 Bill of Material

The list of material is valid for the ISOFACE ISO2H823V2 Board V1.1 Revision July 2014.

Table 6 Bill of Material

Pos	Reference Designator	Value	Device	Package	Qty
1	C1, C3	1uF/ 16V	C0805	0805	2
2	C10, C11, C12	4.7nF/ 1000V	C1812	1812	3
3	C13, C14, C15, C16, C17, C18, C19, C20	10nF/ 50V	C0805	0805	8
4	C2, C5, C6, C7	100nF/ 50V	C0805	0805	4
5	C4	470nF/ 16V	C0805	0805	1
6	C8	1uF/ 50V	C0805	0805	1
7	C9	4.7uF/ 50V	C1206	1206	1
8	D1, D2	SPTS0540Z	SPTS0540Z	SOD123	2
9	D3	SM15T39A	TVS,39V,1500W,SMC	SMC	1
10	F1	OMF125 / 7A	3404.0019.11	FUSE7,	1
11	IC1	ISO2H823V2	ISO2H823V2	PG-VQFN-70-2	1
12	JP1, JP2, JP3	Connector 1x3 2,54mm	PINHD-1X03_2.54, SL 11/112/ 36/S	1X03-S	3
13	LD0, LD1, LD2, LD3, LD4, LD5, LD6, LD7	LED_GREEN	LED-SMD, GREEN, 3.3V, 20mA	CHIP-LED0805	8
14	LD8	LED_RED	LED_RED	CHIP-LED0805	1
15	R1, R2, R3, R4, R5	1k Ohm/ 1%	R-EU_R0805	0805	5
16	R6, R7, R9, R10, R11	10k Ohm/ 1%	R-EU_R0805	0805	5
17	R8	6.81k Ohm/ 1%	R-EU_R0805	0805	1
18	SV1	WSL 40W	ML40	ML40	1
19	X1	MKDS 1/ 2-3,5	Terminal, 2Pin, RM3.5	1x2, pitch3,5	1
20	X2	MKDSN 1,5/2-5,08	Terminal, 2Pin, RM5.08	1x2, pitch5.08	1
21	X3	MKKDSN 1,5/ 8-5,08	Terminal, 2x8pin, RM5.08	2x8-ZIP, pitch5.08	1

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