DEMO MANUAL DC1282A

LTC2209/LTC2209#3BC/ LTC2209#3CD 16-Bit, 160Msps to 185Msps ADCs

DESCRIPTION

Demonstration circuit 1282A supports a family of 16-bit 160Msps to 185Msps ADCs. Each assembly features one of the following devices: LTC®2209, LTC2209#3BC, or LTC2209#3CD high speed, high dynamic range ADCs.

Other members of this family include the LTC2208 which is a 130Msps 16-bit version of this device. The LTC2208 is supported on the DC854 (CMOS outputs) and the DC996 (LVDS outputs). Lower speed versions are also supported on the DC918 and DC919 for single-ended clock input.

Several versions of the DC1282A demo board supporting the LTC2209 16-bit series of A/D converters are listed in Table 1. Depending on the sample rate, the DC1282A is supplied with the appropriate ADC and with an optimized input circuit. The circuitry on the analog inputs is optimized for analog input frequencies above 160MHz. For lower input frequencies, use a DC1281A demonstration circuit.

Design files for this circuit board are available at http://www.linear.com/demo

Table 1. DC1282A Variants

DC1282A VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY	SUPPLY VOLTAGE
1282A-A	LTC2209	16-Bit	160Msps	f_{IN} > 160MHz	3.3V
1282A-C	LTC2209#3BCPBF	16-Bit	180Msps	f_{IN} > 160MHz	3.6V
1282A-D	LTC2209#3CDPBF	16-Bit	185Msps	f_{IN} > 160MHz	3.6V

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage – LTC2209	Depending on Sampling Rate and the A/D Converter Provided, This Supply Must Provide Up to 700mA.	Optimized for 3.3V [3.15V⇔3.45V min/max]
Supply Voltage – LTC2209#3BC or LTC2209#3CD	Depending on Sampling Rate and the A/D Converter Provided, This Supply Must Provide Up to 700mA.	Optimized for 3.6V [3.5V⇔3.78V min/max]
Analog Input Range	Depending on PGA Pin Voltage	1.5V_{P-P} to 2.25V_{P-P}
Logic Input Voltages	Minimum Logic High Maximum Logic Low	2V 0.8V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load) Minimum Logic Levels (100Ω Load)	350mV/2.1V Common Mode 247mV/2.1V Common Mode
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	50Ω Source Impedance, AC-coupled or Ground Referenced (Convert Clock Input is Capacitor Coupled on Board and Terminated with 50Ω).	2V_{P-P}⇔2.5V_{P-P} Sine Wave or Square Wave
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 1282A is easy to set up to evaluate the performance of the LTC2209 A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

Setup

If a DC890 QuikEval™ II Data Acquisition and Collection System was supplied with the DC1282A demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1282A and to a PC.

DC1282A Demonstration Circuit Board Jumpers

The DC1282A demonstration circuit board should have the following jumper settings as default: (as per Figure 1)

J2: Mode (VCC) 2's Complement DCS Off

J3: SHDN: (Run) Dither (Off)

J4: RAND (Off) PGA 1x

J9: Unused Power Connector

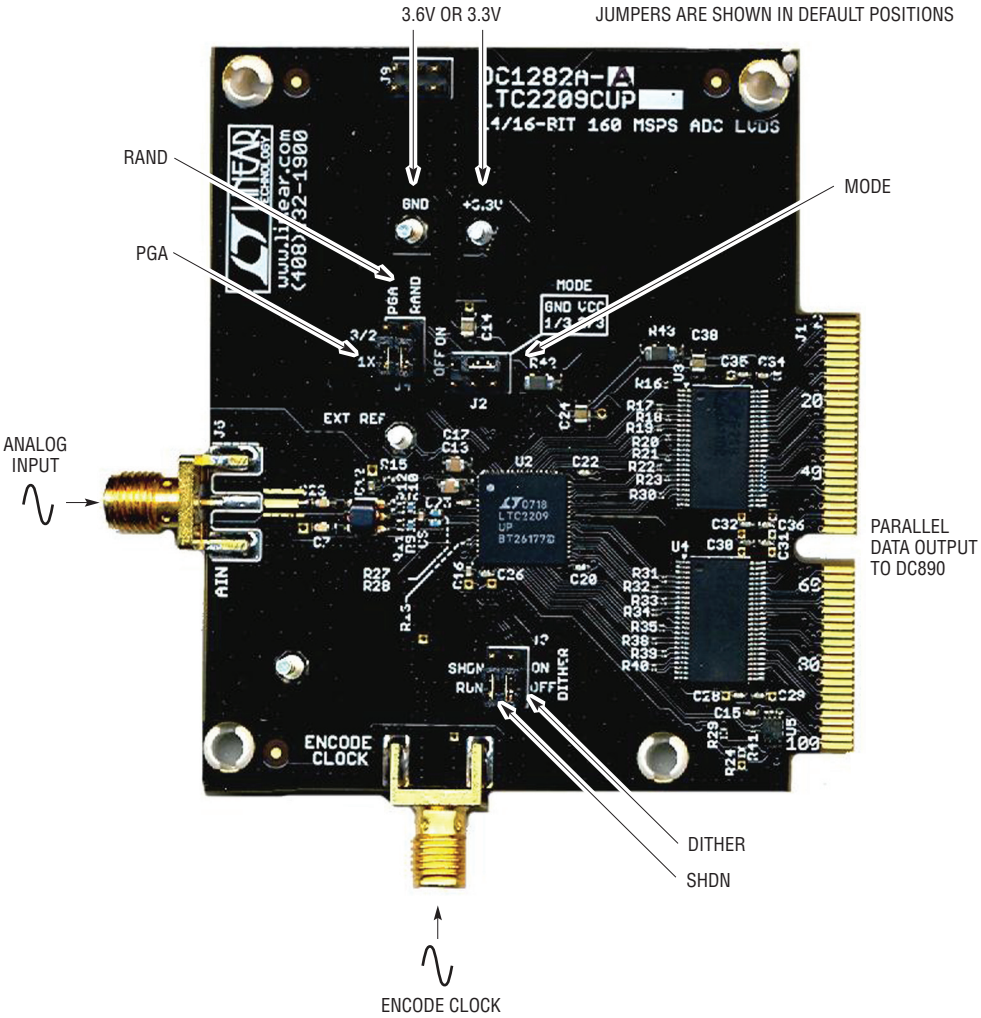


Figure 1. DC1282A Setup (Zoom for Detail)

QUICK START PROCEDURE

Applying Power and Signals to the DC1282A Demonstration Circuit

If a DC890 is used to acquire data from the DC1282, the DC890 must *first* be connected to a powered USB port or provided an external 6V to 9V *before* applying 3.3V or 3.6V across the pins marked +3.3V and PWR GND on the DC1282. The LTC2209#3BC and LTC2209#3CD require 3.6V for proper operation. The DC1282 demonstration circuit requires up to 700mA depending on the sampling rate and the A/D converter supplied.

The DC890 data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an unpowered hub in which case it must be supplied an external 6-9V on turrets G7(+) and G1(–) or the adjacent 2.1mm power jack.

Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies less than 160MHz, other input networks may be more appropriate. For input frequencies less that 160MHz, use demonstration circuit 1281A.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC-based operational amplifiers may be unable to deliver the combination of low noise figure and high IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Encode Clock

Note: This is not a logic-compatible input. It is terminated with 50Ω. Apply an encode clock to the SMA connector on the DC1282A demonstration circuit board marked J7 ENCODE INPUT. This is a transformer-coupled input, terminated on the secondary side in two steps, 100Ω at the transformer with final termination at the ADC at 100Ω.

QUICK START PROCEDURE

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should often be as large as possible, up to $3V_{P-P}$ or 15dBm. Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10-pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE bandpass filters for both the clock input and the analog input.

Apply the analog input signal of interest to the SMA connectors on the DC1282A marked J5 ANALOG INPUT. These inputs are capacitive coupled to Balun transformers ETC1-1-13, or directly coupled through Flux-coupled transformers ETC1-1T.

An internally generated conversion clock output is available on J1 which could be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 QuikEval II Data Acquisition Board using PScope™ software.

Software

The DC890 is controlled by the PScope system software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

QUICK START PROCEDURE

To start the data collection software if PScope.exe is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1282 demonstration circuit is properly connected to the DC890, PScope should automatically detect the DC1282, and configure itself accordingly. If necessary the procedure below explains how to manually configure PSCOPE.

Under the Configure menu, go to ADC Configuration. Check the Config Manually box and use the following configuration options, see Figure 2:

Manual Configuration settings:

Bits: 16

Alignment: 16

FPGA Ld: LVDS

Channs: 1

Bipolar: Checked

Positive-Edge Clk: Checked

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890 Quick Start Guide and in the online help available within the PScope program itself.

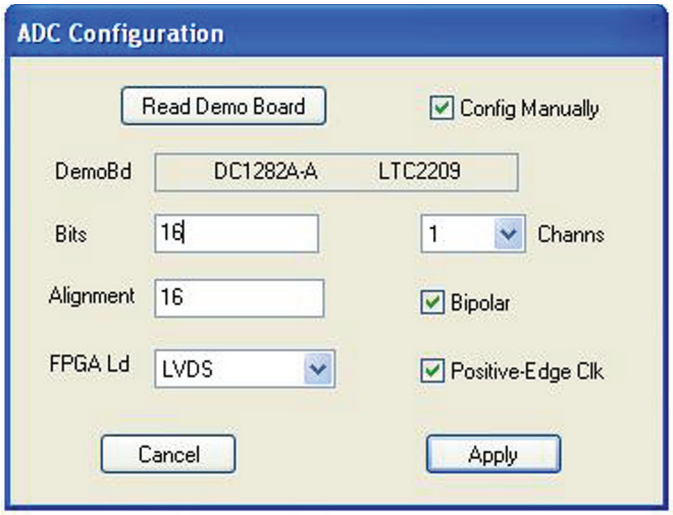
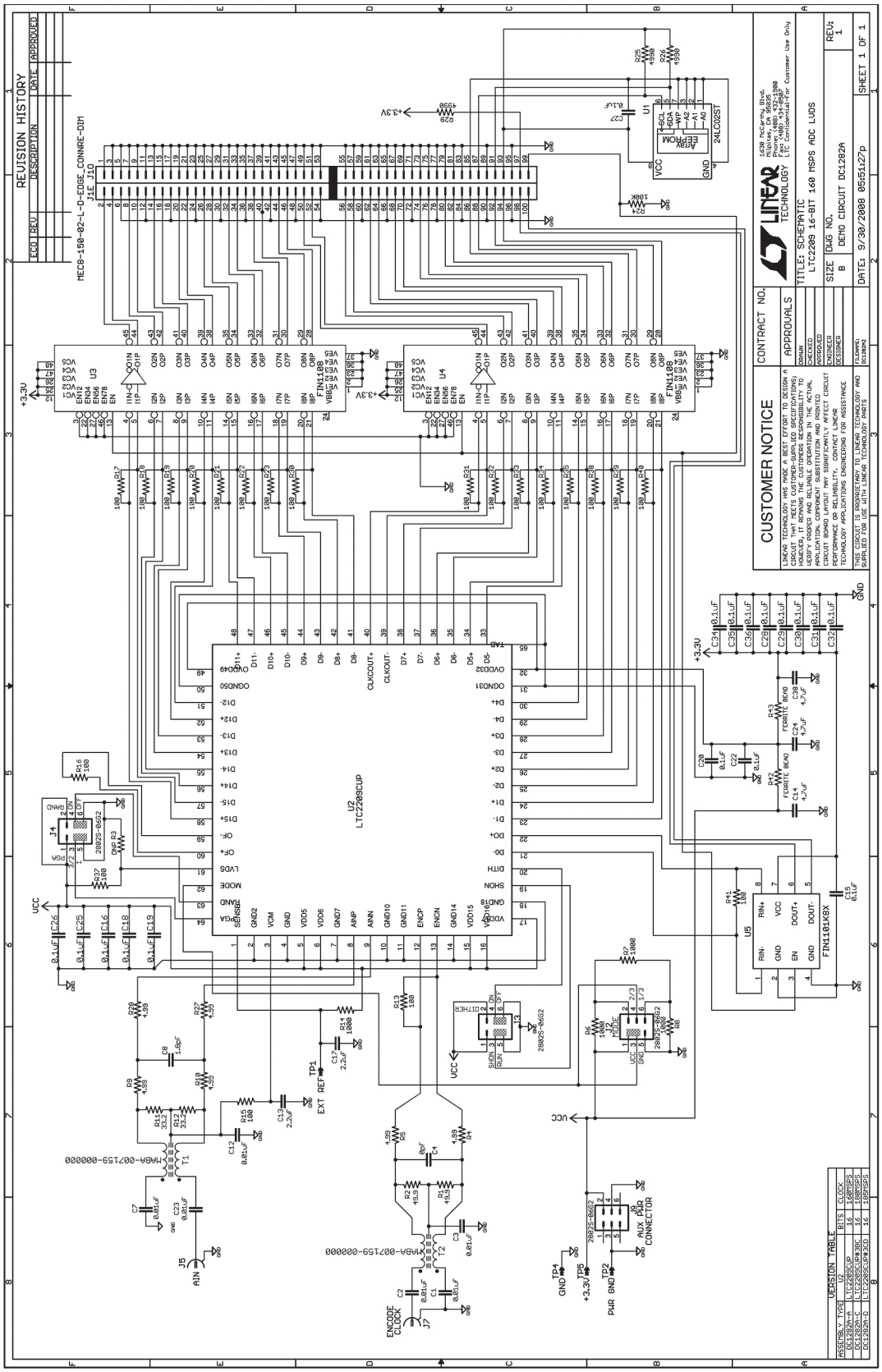


Figure 2: ADC Configuration

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	0	C4 (Option)	CAP~NPO~1.8pF~50V~0.25pF~0402	AVX/04025A1R8CAT2A
2	1	C8	CAP~NPO~1.8pF~50V~0.25pF~0402	AVX/04025A1R8CAT2A
3	1	C12	CAP~X5R~0.01µF~16V~10%~0402	AVX/0402YC103KAT
4	15	C15-C16, C20, C22, C25-C32, C34-C36	CAP~X5R~0.1µF~10V~10%~0402	AVX/0402ZD104KAT
5	5	C1-C3, C7, C23	CAP~X7R~0.01µF~16V~10%~0603	AVX/0603YC103KAT
6	2	C18, C19	CAP~X7R~0.1µF~16V~10%~0603	AVX/0603YC104KAT
7	2	C13, C17	CAP~X5R~2.2µF~10V~20%~0805	AVX/0805ZD225MAT
8	3	C14, C24, C38	CAP~X5R~4.7µF~10V~20%~0805	AVX/0805ZD475MAT
9	4	J2, J3, J4, J9	HEADER~3 × 2~2mm	Samtec, TMM-103-02-L-D
10	2	J5, J7	CONN~SMA 50Ω EDGE-LAUNCH	E.F. Johnson, 142-0701-851
11	19	R13, R16-R23, R30-R35, R38-R41	RES~100Ω~5%~1/20~0201	VISHAY, CRCW0201100RJNED
12	1	R15	RES~100Ω~1%~1/16~0402	VISHAY, CRCW0402100RFKED
13	1	R24	RES~100k~1%~1/16~0402	VISHAY, CRCW0402100KFKED
14	2	R11-R12	RES~33.2Ω~1%~1/16~0402	VISHAY, CRCW040233R2FKED
15	2	R1, R2	RES~49.9Ω~1%~1/16~0402	VISHAY, CRCW040249R9FKEA
16	6	R4, R5, R9, R10, R27, R28	RES~4.99Ω~1%~1/16W~0402	VISHAY/CRCW04024R99FKED
17	3	R25, R26, R29	RES~4990Ω~1%~1/16~0402	VISHAY, CRCW04024K99FKED
18	0	R3 (OPTION)		
19	2	R14, R37	RES~100Ω~1%~1/16W~0603	VISHAY, CRCW0603100RFKED
20	3	R6-R8	RES~1k~1%~1/16W~0603	VISHAY, CRCW06031K00FKEB
21	2	R42, R43	FERRITE BEAD~SMT~1206	MURATA/BLM31PG330SN1L
22	2	T1, T2	XFRM~RF~SMT~1:1 BALUN	MACOM/MABA-007159-000000
23	1	U1	IC~SERIAL_EEPROM~TSSOP8	MICROCHIP/24LC025-I /ST
24	2	U3, U4	BUFFER~LVDS~OCTAL	FAIRCHILD/FIN1108MTD
25	1	U5	BUFFER~LVDS~SINGLE	FAIRCHILD/FIN1101K8X
26	4	TP1, TP2, TP4, TP5	TURRET	MILL_MAX/2308-2
27	4	Z (STAND-OFF)	STAND-OFF, NYLON 0.25" TALL	KEYSTONE, 8831(SNAP ON)
28	5		SHUNT, 0.079" Center	SAMTEC, 2SN-BK-G
29	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1282A
30	2		STENCIL, 20 × 20	STENCIL 1282A, 20 × 20
DC1282A-A				
1	1	DC1282A	GENERAL BOM	
2	1	U2	IC~ADC~160MSPS~16-BIT~QFN-64	LINEAR_TECH/LTC2209CUP#PBF
DC1282A-C				
1	1	DC1282A	GENERAL BOM	
2	1	U2	IC~ADC~180MSPS~16-BIT~QFN-64	LINEAR_TECH/LTC2209CUP#3BCPBF
DC1282A-D				
1	1	DC1282A	GENERAL BOM	
2	1	U2	IC~ADC~185MSPS~16-BIT~QFN-64	LINEAR_TECH/LTC2209CUP#3CDPBF

SCHEMATIC DIAGRAM



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