MAX20034

High-Efficiency 2.2MHz, 36V, Dual Buck Controller with 17µA Quiescent Current

General Description

The MAX20034 is an automotive 2.2MHz, dual synchronous step-down controller IC that provides two high-voltage, synchronous step-down controllers that operate 180° out-of-phase. The IC operates with a 3.5V to 42V input-voltage supply and can function in dropout condition by running at 99% duty cycle. It is intended for applications with mid- to high-power requirements that perform at a wide input voltage range, such as during automotive cold-crank or engine stop-start conditions.

The IC's step-down controllers operate at up to 2.2MHz frequency to allow small external components, reduced output ripple, and to guarantee no AM band interference. The switching frequency is resistor adjustable (220kHz to 2.2MHz). SYNC input programmability enables three frequency modes for optimized performance: forced fixed-frequency operation, skip mode with ultra-low quiescent current, and synchronization to an external clock. The IC is also available with spread-spectrum frequency modulation to minimize EMI interference.

The IC features a power-OK monitor, overvoltage lockout, and undervoltage lockout. Protection features include cycle-by-cycle current limit and thermal shutdown. The MAX20034 is specified for operation over the -40°C to +125°C automotive temperature range.

Applications

- POL Applications for Automotive Power
- Distributed DC Power Systems
- Navigation and Radio Head Units

Benefits and Features

- Meets Stringent OEM Module Power-Consumption and Performance Specifications
  - 17µA Quiescent Current in Skip Mode
  - ±1.5% Output-Voltage Accuracy: 5.0V/3.3V Fixed, or Adjustable Between 1V and 10V
- Enables Crank-Ready Designs
  - Wide 3.5V to 36V Input Supply Range
- EMI Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range
  - 50ns (typ) Minimum On-Time Guarantees Skip-Free Operation for 3.3V Output from a Car Battery at 2.2MHz
  - Spread-Spectrum Option
  - Frequency-Synchronization Input
  - Resistor-Programmable Frequency Between 220kHz and 2.2MHz
- Integration and Thermally Enhanced Packages Save Board Space and Cost
  - Dual, Up to 2.2MHz Step-Down Controllers
  - 180° Out-of-Phase Operation
  - Current-Mode Controllers with Forced-PWM (FPWM) and Skip Modes
  - Thermally Enhanced, 28-Pin TQFN-EP Package
- Protection Features Improve System Reliability
  - Supply Overvoltage and Undervoltage Lockout
  - Overtemperature and Short-Circuit Protection

Ordering Information appears at end of data sheet.

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Simplified Block Diagram
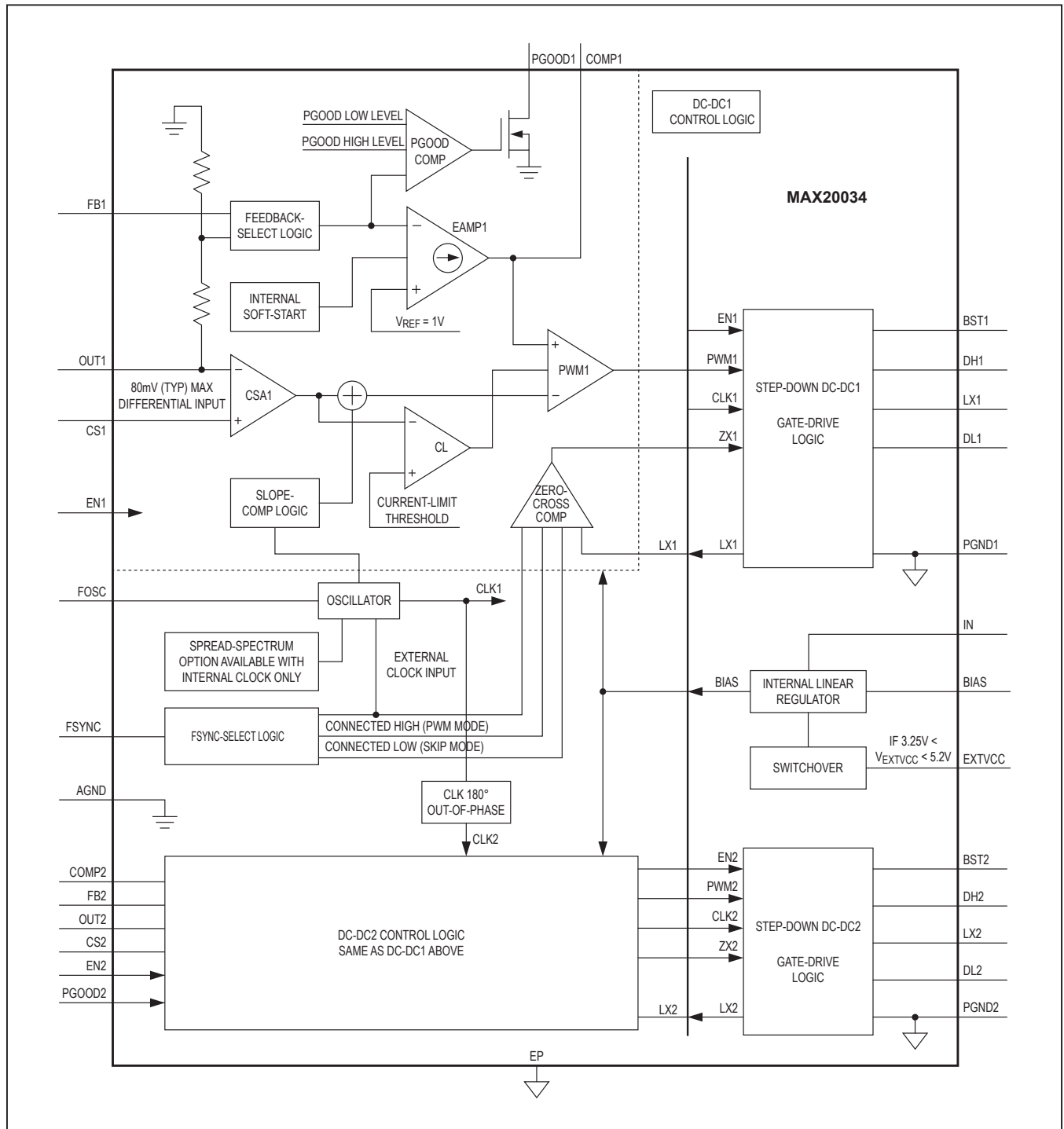
Absolute Maximum Ratings

IN, EN1, EN2, LX_ to PGND.................................-0.3V to +42V
OUT1, OUT2 to AGND...-0.3V to +12V
CS1 to OUT1...-0.3V to +0.3V
CS2 to OUT2...-0.3V to +0.3V
BIAS, FSYNC, PGOOD_, FB_,
    EXTVCC to AGND..-0.3V to +6V
COMP_, FOSC to PGND_ ....-0.3V to V_{BIAS} + 0.3V
DL_ to PGND_ (Note 1) ....-0.3V to V_{BIAS} + 0.3V
BST_ to LX_ (Note 1)..-0.3V to +6V

DH_ to LX_ (Note 1)...............................-0.3V to $V_{BST\_}$ + 0.3V
PGND_ to AGND..-0.3V to +0.3V
Continous Power Dissipation (T_A = +70°C)
    28 TQFN (derate 37mW/°C above +70°C)...............2285mW
Operating Temperature Range......................... -40°C to +125°C
Junction Temperature...+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow).....................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Package Information

PACKAGE TYPE: 28-PIN TQFN	
Package Code	T2855Y-5C
Outline Number	**21-100130**
Land Pattern Number	**90-0027**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient ($θ_{JA}$)	35°C/W
Junction to Case ($θ_{JC}$)	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 14V, C_{BIAS} = 6.8µF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}	Normal operation	3.5		36	V
		t < 1s			42	
Supply Current	I_{IN}	V_{EN1} = V_{EN2} = 0V		6.5	10	µA
		V_{EN1} = 5V, V_{OUT1} = 5V, V_{EN2} = 0V, V_{EXTVCC} = 5V (no switching)		25	40	
		V_{EN2} = 5V, V_{OUT2} = 3.3V, V_{EN1} = 0V, V_{EXTVCC} = 3.3V (no switching)		17	28	
Buck 1 Fixed-Output Voltage	V_{OUT1}	V_{FB1} = V_{BIAS}, V_{OUT1} = 5V, PWM mode	4.925	5	5.075	V
Buck 2 Fixed-Output Voltage	V_{OUT2}	V_{FB2} = V_{BIAS}, V_{OUT2} = 3.3V, PWM mode	3.25	3.3	3.35	V

Electrical Characteristics (continued)

(V_{IN} = 14V, C_{BIAS} = 6.8µF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage-Adjustable Range		Buck 1, Buck 2	1		10	V
Regulated Feedback Voltage	V_{FB1}, V_{FB2}	PWM	0.995	1.005	1.015	V
Feedback Leakage Current	I_{FB1}, I_{FB2}	T_A = +25°C		0.01	1	µA
Feedback Line-Regulation Error		V_{IN} = 3.5V to 36V, $V_{FB\_}$ = 1V		0.01		%/V
Transconductance (from FB1, 2 to COMP1, 2)	g_m	$V_{FB\_}$ = 1V, V_{BIAS} = 5V	300	470	700	µS
Dead Time		DL_ low to DH_ high		15		ns
		DH_ low to DL_ high		15		
Maximum Duty Cycle		Buck 1, Buck 2	97	99		%
Minimum On-Time	$t_{ON,MIN}$	Buck 1, Buck 2		50		ns
PWM Switching-Frequency Range	f_{SW}	Programmable	0.22		2.2	MHz
Switching-Frequency Accuracy		R_{FOSC} = 12kΩ, V_{BIAS} = 5V, 3.3V	2	2.2	2.4	MHz
CS_ Current-Limit Voltage Threshold	V_{LIMIT1}, V_{LIMIT2}	$V_{CS\_}$ - V_{OUT}; V_{BIAS} = 5V, V_{OUT} ≥ 2.5V	68	80	92	mV
Soft-Start Ramp Time		Buck 1 and Buck 2	3	5	8	ms
Phase Shift Between Buck 1 and Buck 2		PWM operation (Note 2)		180		deg
LX1, LX2 Leakage Current		$V_{LX\_}$ = $V_{PGND\_}$ or V_{IN}, T_A = +25°C		0.001	1	µA
DH1, DH2 Pullup Resistance		V_{BIAS} = 5V, I_{DH} = -100mA		3	6	Ω
DH1, DH2 Pulldown Resistance		V_{BIAS} = 5V, I_{DH} = 100mA		1.5	3	Ω
DL1,2 Pullup Resistance		V_{BIAS} = 5V, I_{DL} = -100mA		3	6	Ω
DL1, DL2 Pulldown Resistance		V_{BIAS} = 5V, I_{DL} = 100mA		1.5	3	Ω
Output Overvoltage Threshold		Detected with respect to $V_{FB\_}$ rising	105	108	112	%
Output Overvoltage Hysteresis				3		%

Electrical Characteristics (continued)

(V_{IN} = 14V, C_{BIAS} = 6.8µF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Threshold	PGOOD_R	Percentage of $V_{OUT\_}$, rising	92	94	97	%
	PGOOD_F	Percentage of $V_{OUT\_}$, falling	90	92	95	
Leakage Current		$V_{PGOOD\_}$ = 5V, T_A = +25°C		0.01	1	µA
Output Low Voltage		I_{SINK} = 1mA			0.2	V
Debounce Time		Fault detection, rising and falling		20		µs
FSYNC INPUT						
FSYNC Frequency Range		Minimum sync pulse > (1/FSYNC - 1/FOSC) R_{FOSC} = 12kΩ	1.8		2.6	MHz
		Minimum sync pulse > (1/FSYNC - 1/FOSC) R_{FOSC} = 70kΩ	250		550	kHz
FSYNC Switching Thresholds		High threshold	1.4			V
		Low threshold			0.4	
INTERNAL LDO BIAS						
Internal BIAS Voltage		V_{IN} > 6V, no load		5		V
BIAS UVLO Threshold		V_{BIAS} rising		3.1	3.25	V
		V_{BIAS} falling	2.35	2.6		
EXTVCC Operating Range			3.25		5.5	V
EXTVCC Threshold	$V_{TH,EXTVCC}$	EXTVCC rising, hysteresis = 110mV	2.85	3	3.25	V
THERMAL OVERLOAD						
Thermal-Shutdown Temperature		(Note 2)		170		°C
Thermal-Shutdown Hysteresis		(Note 2)		20		°C
ENABLE LOGIC INPUT						
High Threshold		EN1, EN2	1.8			V
Low Threshold		EN1, EN2			0.8	V
EN_ Input Bias Current		EN1, EN2 logic inputs only, T_A = +25°C		0.01	1	µA

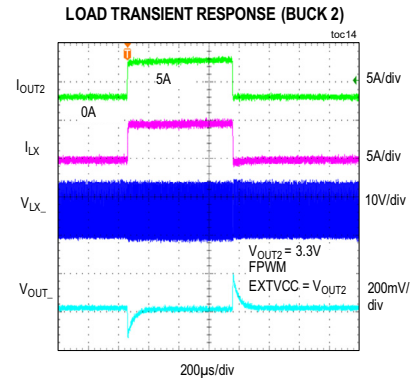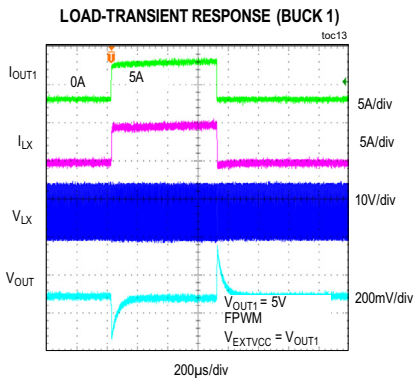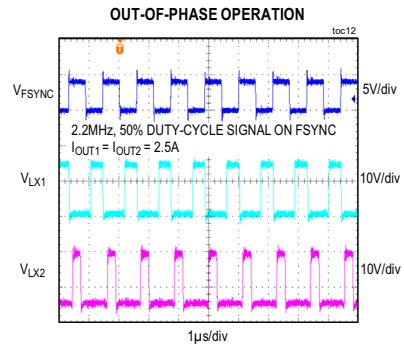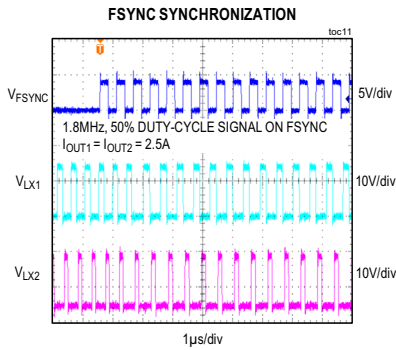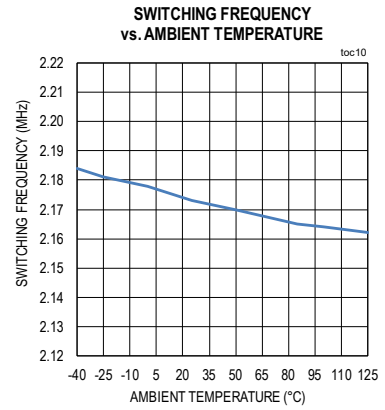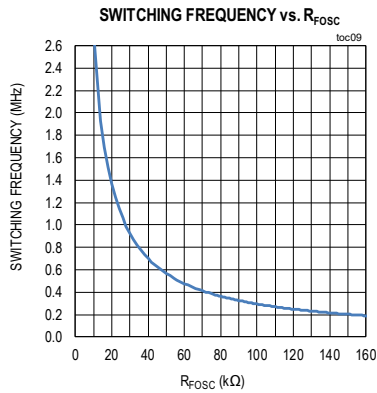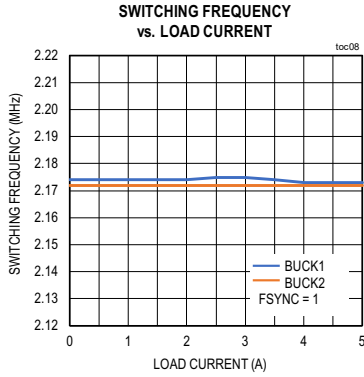**Note 2:** Guaranteed by design, not production tested.

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

STARTUP INTO NO-LOAD

$V_{EN\_}$
V_{OUT1}
V_{PGOOD1}
V_{OUT2}
V_{PGOOD2}

5V/div
2V/div
5V/div
2V/div
5V/div

EN1 = EN2
FSYNC = 0
V_{EXTVCC} = V_{OUT1}
I_{OUT1} = I_{OUT2} = 0A

2ms/div

toc01

STARTUP INTO LOAD

$V_{EN\_}$
V_{OUT1}
V_{PGOOD1}
V_{OUT2}
V_{PGOOD2}

5V/div
2V/div
5V/div
2V/div
5V/div

EN1 = EN2
FSYNC = 0
I_{OUT1} = I_{OUT2} = 3A
V_{EXTVCC} = V_{OUT1}

2ms/div

toc02

SHUTDOWN SUPPLY CURRENT
vs. SUPPLY VOLTAGE

toc03

QUIESCENT CURRENT
vs. SUPPLY VOLTAGE

toc04

ONLY BUCK 1 ON, V_{EXTVCC} = V_{OUT1}
ONLY BUCK 2 ON, V_{EXTVCC} = V_{OUT2}
BOTH BUCKS ON, V_{EXTVCC} = V_{OUT1}

BUCK 1 EFFICIENCY vs. OUTPUT CURRENT
(f_{SW} = 2.2MHz)

toc05

SKIP ENABLED
FPWM

EN1 = HIGH
EN2 = LOW
V_{EXTVCC} = V_{OUT1}
V_{OUT1} = 5V

BUCK 1 EFFICIENCY vs. OUTPUT CURRENT
(f_{SW} = 400kHz)

toc06

SKIP ENABLED
FPWM

EN1 = HIGH
EN2 = LOW
V_{EXTVCC} = V_{OUT1}
V_{OUT1} = 5V

BUCK 2 EFFICIENCY vs. OUTPUT CURRENT
(f_{SW} = 400kHz)

toc07

SKIP ENABLED
FPWM

EN1 = HIGH
EN2 = HIGH
V_{EXTVCC} = V_{OUT1}
V_{OUT2} = 3.3V

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

SWITCHING FREQUENCY vs. LOAD CURRENT

toc08

SWITCHING FREQUENCY vs. R_{FOSC}

toc09

SWITCHING FREQUENCY vs. AMBIENT TEMPERATURE

toc10

FSYNC SYNCHRONIZATION

toc11

1µs/div

OUT-OF-PHASE OPERATION

toc12

1µs/div

LOAD-TRANSIENT RESPONSE (BUCK 1)

toc13

200µs/div

LOAD TRANSIENT RESPONSE (BUCK 2)

toc14

200µs/div

Typical Operating Characteristics (continued)
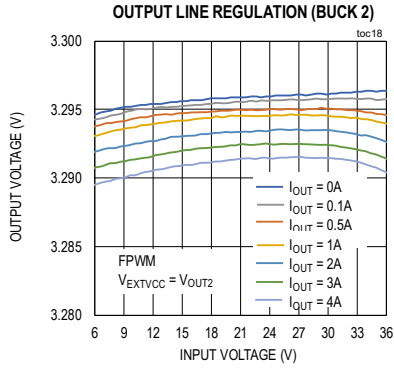
(T_A = +25°C, unless otherwise noted.)

OUTPUT LOAD REGULATION (BUCK 1)

toc15

- SKIP
- FPWM

$V_{EXTVCC} = V_{OUT1}$

Y-axis: OUTPUT VOLTAGE (V) — 4.90, 4.95, 5.00, 5.05, 5.10
X-axis: OUTPUT CURRENT (A) — 0.001, 0.01, 0.1, 1, 10

OUTPUT LOAD REGULATION (BUCK 2)

toc16

- SKIP
- FPWM

$V_{EXTVCC} = V_{OUT1}$

Y-axis: OUTPUT VOLTAGE (V) — 3.234, 3.267, 3.300, 3.333, 3.366
X-axis: OUTPUT CURRENT (A) — 0.001, 0.01, 0.1, 1, 10

OUTPUT LINE REGULATION (BUCK 1)

toc17

- I_{OUT} = 0A
- I_{OUT} = 0.1A
- I_{OUT} = 0.5A
- I_{OUT} = 1A
- I_{OUT} = 2A
- I_{OUT} = 3A
- I_{OUT} = 4A

FPWM
$V_{EXTVCC} = V_{OUT1}$

Y-axis: OUTPUT VOLTAGE (V) — 4.96, 4.97, 4.98, 4.99, 5.00, 5.01, 5.02
X-axis: INPUT VOLTAGE (V) — 6, 9, 12, 15, 18, 21, 24, 27, 30, 33, 36

OUTPUT LINE REGULATION (BUCK 2)

toc18

- I_{OUT} = 0A
- I_{OUT} = 0.1A
- I_{OUT} = 0.5A
- I_{OUT} = 1A
- I_{OUT} = 2A
- I_{OUT} = 3A
- I_{OUT} = 4A

FPWM
$V_{EXTVCC} = V_{OUT2}$

Y-axis: OUTPUT VOLTAGE (V) — 3.280, 3.285, 3.290, 3.295, 3.300
X-axis: INPUT VOLTAGE (V) — 6, 9, 12, 15, 18, 21, 24, 27, 30, 33, 36

COLD CRANK (BUCK 1)

toc19

V_{IN} — 3V/div
V_{OUT} — 1V/div
I_{LX} — 2A/div
V_{PGOOD1} — 5V/div

V_{IN} = 14V TO 3.5V TO 5V TO 14V
FPWM, I_{OUT} = 4A, $V_{EXTVCC} = V_{OUT1}$

100ms/div

COLD CRANK (BUCK 2)

toc20

V_{IN} — 3V/div
V_{OUT} — 1V/div
I_{LX} — 2A/div
V_{PGOOD} — 5V/div

V_{IN} = 14V TO 3.5V TO 5V TO 14V
FPWM, I_{OUT} = 4A, $V_{EXTVCC} = V_{OUT2}$

100ms/div

LOAD DUMP (BUCK 1)

toc21

V_{IN} — 10V/div
V_{OUT} — 1V/div
I_{LX} — 2A/div
V_{PGOOD} — 5V/div

FPWM, I_{OUT} = 4A, $V_{EXTVCC} = V_{OUT1}$

50ms/div

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

LOAD DUMP (BUCK 2)
toc22

FPWM, I_{OUT} = 4A, V_{EXTVCC} = V_{OUT1}

50ms/div

SLOW INPUT-VOLTAGE RISING (BUCK 1)
toc23

V_{IN} = 0 TO 14V
FPWM, I_{OUT} = 4A
V_{EXTVCC} = V_{OUT1}

5s/div

SLOW INPUT-VOLTAGE RISING (BUCK 2)
toc24

V_{IN} = 0 TO 14V
FPWM, I_{OUT} = 4A
V_{EXTVCC} = V_{OUT1}

5s/div

LINE TRANSIENT OUT OF DROPOUT
(BUCK 1)
toc25

V_{IN} = 5V TO 14V
FPWM, NO LOAD

5.13V

50μs/div

LINE TRANSIENT OUT OF DROPOUT
(BUCK 2)
toc26

3.42V

V_{IN} = 5V TO 14V
FPWM, NO LOAD

50μs/div

SHORT CIRCUIT AFTER REGULATION
(BUCK 1)
toc27

400μs/div

SHORT CIRCUIT AFTER REGULATION
(BUCK 2)
toc28

400μs/div

Pin Configuration

TOP VIEW

MAX20034

TQFN
(5mm x 5mm)

Pin Description

PIN	NAME	FUNCTION
1	LX1	Inductor Connection for Buck 1. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
2	DL1	Low-Side Gate-Driver Output for Buck 1. DL1 output voltage swings from V_{PGND1} to V_{BIAS}.
3	PGND1	Power Ground for Buck 1
4	CS1	Positive Current-Sense Input for Buck 1. Connect CS1 to the positive terminal of the current-sense element. See the *Current Limiting and Current-Sense Inputs (OUT_ and CS_)* and *Current-Sense Measurement* sections.
5	OUT1	Output Sense and Negative Current-Sense Input for Buck 1. When using the internal preset 5V feedback-divider (FB1 = BIAS), the controller uses OUT1 to sense the output voltage. Connect OUT1 to the negative terminal of the current-sense element. See the *Current Limiting and Current-Sense Inputs (OUT_ and CS_)* and *Current-Sense Measurement* sections.
6	FB1	Feedback Input for Buck 1. Connect FB1 to BIAS for the 5V fixed output or to a resistive divider between OUT1 and AGND to adjust the output voltage between 1V and 10V. In adjustable version, FB1 regulates to 1V (typ). See the *Setting the Output Voltage in Buck Converters* section.
7	COMP1	Buck 1 Error-Amplifier Output. Connect an RC network to COMP1 to compensate.
8	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to PGND with a low-ESR ceramic capacitor of 2.2µF minimum value. BIAS provides the power to the internal circuitry and external loads. See the *Fixed 5V Linear Regulator (BIAS)* section.
9	AGND	Signal Ground for IC
10	EXTVCC	Switchover Comparator Input. Connect a voltage between 3.25V and 5.5V to EXTVCC to power the IC and bypass the internal bias LDO.

Pin Description (continued)

PIN	NAME	FUNCTION
11	IN	Supply Input. Bypass IN with enough capacitors to supply the two out-of-phase buck converters.
12	PGOOD1	Open-Drain Power-Good Output for Buck 1. PGOOD1 is low if OUT1 is more than 92% (typ) below the normal regulation point. PGOOD1 asserts low during soft-start and in shutdown. PGOOD1 becomes high impedance when OUT1 is in regulation. To obtain a logic signal, pull PGOOD1 up with an external resistor connected to a positive voltage lower than 5.5V.
13	PGOOD2	Open-Drain Power-Good Output for Buck 2. PGOOD2 is low if OUT2 is more than 92% (typ) below the normal regulation point. PGOOD2 asserts low during soft-start and in shutdown. PGOOD2 becomes high impedance when OUT2 is in regulation. To obtain a logic signal, pull PGOOD2 up with an external resistor connected to a positive voltage lower than 5.5V.
14	FSYNC	External Clock-Synchronization Input. Synchronization to the controller operating-frequency ratio is 1. See the _Switching Frequency/External Synchronization_ section. For FSYNC high, and T_{ON} < $T_{ON,MIN}$, ensure there is at least 50µA (including the resistor-divider current on $V_{OUT1,2}$) of load current if V_{BIAS} - V_{OUT} > 1.3V.
15	FOSC	Frequency-Setting Input. Connect a resistor from FOSC to AGND to set the switching frequency of the DC-DC converters.
16	COMP2	Buck 2 Error-Amplifier Output. Connect an RC network to COMP2 to compensate buck converter 2.
17	FB2	Feedback Input for Buck 2. Connect FB2 to BIAS for the 3.3V fixed output or to a resistive divider between OUT2 and AGND to adjust the output voltage between 1V and 10V. In adjustable version, FB2 regulates to 1V (typ). See the _Setting the Output Voltage in Buck Converters_ section.
18	OUT2	Output Sense and Negative Current-Sense Input for Buck 2. When using the internal preset 3.3V feedback-divider (FB2 = BIAS), the buck uses OUT2 to sense the output voltage. Connect OUT2 to the negative terminal of the current-sense element. See the _Current Limiting and Current-Sense Inputs (OUT_ and CS_)_ and _Current-Sense Measurement_ sections.
19	CS2	Positive Current-Sense Input for Buck 2. Connect CS2 to the positive terminal of the current-sense element. See _Current Limiting and Current-Sense Inputs (OUT_ and CS_)_ and _Current-Sense Measurement_ sections.
20	PGND2	Power Ground for Buck 2
21	DL2	Low-Side Gate-Driver Output for Buck 2. DL2 output voltage swings from V_{PGND2} to V_{BIAS}.
22	LX2	Inductor Connection for Buck 2. Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
23	DH2	High-Side Gate-Driver Output for Buck 2. DH2 output voltage swings from V_{LX2} to V_{BST2}.
24	BST2	Boost Flying-Capacitor Connection for High-Side Gate Voltage of Buck 2. Connect a high-voltage diode between BIAS and BST2. Connect a ceramic capacitor between BST2 and LX2. See the _High-Side Gate-Driver Supply (BST_)_ section.
25	EN2	High-Voltage-Tolerant, Active-High Digital Enable Input for Buck 2. Driving EN2 high enables Buck 2.
26	EN1	High-Voltage-Tolerant, Active-High Digital Enable Input for Buck 1. Driving EN1 high enables Buck 1.
27	BST1	Boost Flying-Capacitor Connection for High-Side Gate Voltage of Buck 1. Connect a high-voltage diode between BIAS and BST2. Connect a ceramic capacitor between BST1 and LX1. See the _High-Side Gate-Driver Supply (BST_)_ section.
28	DH1	High-Side Gate-Driver Output for Buck 2. DH1 output voltage swings from V_{LX1} to V_{BST1}.
—	EP	Exposed Pad. Connect EP to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND1, PGND2, and AGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX20034 is an automotive-rated dual-output switching power-supply IC. The IC integrates two synchronous step-down controllers and can provide two independent-controlled power rails as follows:

● Buck controller with a fixed 5V output voltage, or an adjustable 1V to 10V output voltage.

● Buck controller with a fixed 3.3V output voltage, or an adjustable 1V to 10V output voltage.

EN1 and EN2 enable the respective buck controllers. Connect EN1 and EN2 directly to V_{BAT}, or to power-supply sequencing logic.

In skip mode, the total supply current is reduced to 17µA (typ) with Buck 1 disabled and Buck 2 enabled. When both controllers are disabled, the total current drawn is further reduced to 6.5µA (typ).

Fixed 5V Linear Regulator (BIAS)

The internal circuitry of the IC requires a 5V bias supply. An internal 5V linear regulator (BIAS) generates this bias supply. Bypass BIAS with a ≥ 6.8µF ceramic capacitor to guarantee stability under the full-load condition.

The internal linear regulator can source up to 100mA (150mA under EXTVCC switchover; see the *EXTVCC Switchover* section). Use the following equation to estimate the internal current requirements for the IC:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G\_DH1} + Q_{G\_DL1} + Q_{G\_DH2} + Q_{G\_DL2}) = 10mA \text{ to } 50mA \text{ (typ)}$$

where I_{CC} is the internal 5mA (typ) supply current, f_{SW} is the switching frequency, and $Q_{G\_}$ is the MOSFET's total gate charge (specification limits at V_{GS} = 5V). To minimize the internal power dissipation, bypass BIAS to an external 5V rail.

EXTVCC Switchover

The internal linear regulator can be bypassed by connecting an external supply (3.25V to 5.2V) or one of the buck converter outputs to EXTVCC. BIAS internally switches to EXTVCC and the internal linear regulator turns off. This configuration has several advantages:

● It reduces the internal power dissipation of the device.

● The low-load efficiency improves as the internal supply current is scaled down proportionally to the duty cycle.

If V_{EXTVCC} drops below 3.25V, the internal regulator is enabled and BIAS switches back to the internal regulator.

Undervoltage Lockout (UVLO)

The BIAS input undervoltage-lockout (UVLO) circuitry inhibits switching if the 5V bias supply (BIAS) is below its 2.6V (typ) UVLO falling threshold. Once BIAS rises above its UVLO rising threshold and EN1 and EN2 enable the buck controllers, the controllers start switching and the output voltages begin to ramp up using soft-start.

Buck Controllers

The IC provides two buck controllers with synchronous rectification. The step-down controllers use a pulse-width modulation (PWM) current-mode control scheme. External MOSFETs allow for optimized load-current design. Fixed-frequency operation with optimal interleaving minimizes input ripple current from the minimum to the maximum input voltages. Output-current sensing provides an accurate current limit with a sense resistor, or power dissipation can be reduced using lossless current sensing across the inductor.

Soft-Start

Once a buck converter is enabled by driving the corresponding EN_ high, the soft-start circuitry gradually ramps up the reference voltage during soft-start time (t_{SSTART} = 5ms (typ)) to reduce the input surge currents during startup. Before the IC can begin the soft-start, the following conditions must be met:

1) V_{BIAS} exceeds the 3.25V (max) undervoltage-lockout threshold.

2) $V_{EN\_}$ is logic-high.

Switching Frequency/External Synchronization

The IC provides an internal oscillator, adjustable from 220kHz to 2.2MHz. High-frequency operation optimizes the application for the smallest component size, trading off efficiency to higher switching losses. Low-frequency operation offers the best overall efficiency at the expense of component size and board space. To set the switching frequency, connect a resistor (R_{FOSC}) from FOSC to AGND:

$$f\_SW = \frac{\left(25.5 + \sqrt{\left(\frac{R\_FOSC}{6}\right)}\right)}{R\_FOSC}$$

See the *Typical Operating Characteristics* to determine the relationship between switching frequency and R_{FOSC}.

The IC can be synchronized to an external clock by connecting the external clock signal to FSYNC. A rising edge on FSYNC resets the internal clock. The FSYNC clock should have a minimum 150ns high pulse width.

Light-Load Efficiency Skip Mode (V_FSYNC = 0V)

Drive FSYNC low to enable skip mode. In skip mode, the IC stops switching until the FB_ voltage drops below the reference voltage. Once the FB_ voltage has dropped below the reference voltage, the IC begins switching until the inductor current reaches 30% (skip threshold) of the maximum current defined by the inductor DCR or output shunt resistor.

Forced-PWM Mode (V_FSYNC = High)

Driving FSYNC high prevents the IC from entering skip mode by disabling the zero-crossing detection of the inductor current. This forces the low-side gate-driver waveform to constantly be the complement of the high-side gate-driver waveform, so the inductor current reverses at light loads and discharges the output capacitor. The benefit of forced-PWM (FPWM) mode is to keep the switching frequency constant under all load conditions; however, forced-frequency operation diverts a considerable amount of the output current to PGND, reducing the efficiency under light-load conditions.

FPWM mode is useful for improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands.

Maximum Duty-Cycle Operation

The IC has a maximum duty cycle of 97% (min). The internal logic of the IC looks for approximately 10 consecutive high-side FET-on pulses and decides to turn on the low-side FET for 150ns (typ) every 12µs. The input voltage at which the IC enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design. The input voltage at which the IC enters dropout can be approximated as:

$$V_{OUT\_} = [V_{OUT\_} + (I_{OUT\_} \times R_{ON\_H})]/0.97$$

Note: The above equation does not take into account the efficiency and switching frequency, but is a good first-order approximation. Use the R_{ON_H} (max) number from the data sheet of the high-side MOSFET used.

Spread Spectrum

The IC features enhanced EMI performance, which performs ±6% dithering of the switching frequency to reduce peak emission noise at the clock frequency and its harmonics, making it easier to meet stringent emission limits.

When using an external clock source (i.e., driving the FSYNC input with an external clock), spread spectrum is disabled.

MOSFET Gate Drivers (DH_ and DL_)

The DH_ high-side n-channel MOSFET drivers are powered from capacitors at BST_, while the low-side drivers (DL_) are powered by the 5V linear regulator (BIAS). On each channel, a shoot-through protection circuit monitors the gate-to-source voltage of the external MOSFETs to prevent a MOSFET from turning on until the complementary switch is fully off. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the protection circuits to work properly. Follow the instructions listed to provide the necessary low-resistance and low-inductance path:

- Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

- It may be necessary to decrease the slew rate for the gate drivers to reduce switching noise or to compensate for low-gate-charge capacitors. For the low-side drivers, use 1nF to 5nF gate capacitors from DL_ to PGND, and for the high-side drivers, connect a small 5Ω to 10Ω resistor between BST_ and the bootstrap capacitor.

Note: Gate drivers must be protected during shutdown, at the absence of the supply voltage (V_{BIAS} = 0V) when the gate is pulled high either capacitively or by the leakage path on the PCB; therefore, external-gate pulldown resistors are needed to prevent making a direct path from V_{BAT} to PGND.

High-Side Gate-Driver Supply (BST_)

The high-side MOSFET is turned on by closing an internal switch between BST_ and DH_ and transferring the bootstrap capacitor's (at BST_) charge to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX_ voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor.

The selected n-channel high-side MOSFET determines the appropriate boost capacitance values ($C_{BST\_}$ in the *Typical Operating Circuit*) according to the following equation:

$$C_{BST\_} = \frac{Q_G}{\Delta V_{BST\_}}$$

where Q_G is the total gate charge of the high-side MOSFET and $\Delta V_{BST\_}$ is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose $\Delta V_{BST\_}$ such that the available gate-drive voltage is not significantly degraded (e.g., $\Delta V_{BST\_}$ = 100mV to 300mV) when determining $C_{BST\_}$.

The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF works in most cases.

Current Limiting and Current-Sense Inputs (OUT_ and CS_)

The current-limit circuit uses differential current-sense inputs (OUT_ and CS_) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold ($V_{LIMIT1,2}$ = 80mV (typ)), the PWM controller turns off the high-side MOSFET. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half the inductor ripple current; therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle ($V_{OUT\_}/V_{IN}$).

For the most accurate current sensing, use a current-sense shunt resistor (R_{SH}) between the inductor and the output capacitor. Connect CS_ to the inductor side of R_{SH} and OUT_ to the capacitor side. Dimension R_{SH} such that the maximum inductor current ($I_{L,MAX} = I_{LOAD,MAX} + 1/2$ $I_{RIPPLE,PP}$) induces a voltage of $V_{LIMIT1,2}$ across R_{SH}, including all tolerances.

For higher efficiency, the current can also be measured directly across the inductor. This method could cause up to 30% error over the entire temperature range and requires a filter network in the current-sense circuit. See the *Current-Sense Measurement* section.

Voltage Monitoring (PGOOD_)

The IC includes several power-monitoring signals to facilitate power-supply sequencing and supervision. PGOOD_ can be used to enable circuits that are supplied by the corresponding voltage rail, or to turn on subsequent supplies.

Each PGOOD_ goes high (high impedance) when the corresponding regulator output voltage is in regulation. Each PGOOD_ goes low when the corresponding regulator output voltage drops below 92% (typ) or rises above 95% (typ) of its nominal regulated voltage. Connect a 10kΩ (typ) pullup resistor from PGOOD_ to the relevant logic rail to level-shift the signal.

PGOOD_ asserts low during soft-start, soft-discharge, and when either buck converter is disabled (either EN1 or EN2 is low).

Thermal-Overload, Overcurrent, and Overvoltage/Undervoltage Behavior

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the IC. When the junction temperature exceeds +170°C, an internal thermal sensor shuts down the device, allowing it to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C.

Overcurrent Protection

If the inductor current in the IC exceeds the maximum current limit programmed at CS_ and OUT_, the respective driver turns off. In an overcurrent mode, this results in shorter and shorter high-side pulses.

A hard short results in a minimum on-time pulse every clock cycle. Choose the components so they can withstand the short-circuit current if required.

Overvoltage Protection

The IC limits the output voltage of the buck converters by turning off the high-side gate driver at approximately 109% of the regulated output voltage. The output voltage needs to come back in regulation before the high-side gate driver starts switching again.

Design Procedure

Buck Converter Design Procedure

Effective Input Voltage Range in Buck Converters

Although the MAX20034 can operate from input supplies up to 36V (42V transients) and regulate down to 1V, the minimum voltage conversion ratio (V_{OUT}/V_{IN}) might be limited by the minimum controllable on-time. For proper fixed-frequency PWM operation and optimal efficiency, Buck 1 and Buck 2 should operate in continuous conduction during normal operating conditions. For continuous conduction, set the voltage-conversion ratio as follows:

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(MIN)} \times f_{SW}$$

where $t_{ON(MIN)}$ is 50ns (typ) and f_{SW} is the switching frequency in Hz. If the desired voltage conversion does not meet the above condition, pulse skipping occurs to decrease the effective duty cycle. Decrease the switching frequency if constant switching frequency is required. The same is true for the maximum voltage conversion ratio.

The maximum voltage conversion ratio is limited by the maximum duty cycle (97%).

$$\frac{V_{OUT}}{V_{IN} - V_{DROP}} < 0.97$$

where $V_{DROP} = I_{OUT} (R_{ON,HS} + R_{DCR})$ is the sum of the parasitic voltage drops in the high-side path, and f_{SW} is the programmed switching frequency. During low-drop operation, the device reduces f_{SW} to 80kHz. In practice, the above condition should be met with adequate margin for good load-transient response.

Setting the Output Voltage in Buck Converters

Connect FB1 and FB2 to BIAS to enable the fixed buck controller output voltages (5V and 3.3V) set by a preset internal resistive voltage-divider connected between the output (OUT_) and AGND. To externally adjust the output voltage between 1V and 10V, connect a resistive divider from the output (OUT_) to FB_ to AGND (see the *Typical Operating Circuit*). Calculate R_{FB_1} and R_{FB_2} with the following equation:

$$R_{FB\_1} = R_{FB\_2}\left[\left(\frac{V_{OUT\_}}{V_{FB\_}}\right) - 1\right]$$

where $V_{FB\_}$ = 1V (typ) (see the *Electrical Characteristics* table).

DC output accuracy specifications in the *Electrical Characteristics* table refer to the error comparator's threshold, $V_{FB\_}$ = 1V (typ). When the inductor conducts continuously, the device regulates the peak of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output ripple voltage.

In discontinuous-conduction mode (skip or STDBY active and I_{OUT} < $I_{LOAD(SKIP)}$), the device regulates the valley of the output ripple, so the output voltage has a DC regulation level higher than the error-comparator threshold.

Inductor Selection in Buck Converters

Three key inductor parameters must be specified for operation with the MAX20034: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To determine the optimum inductance, knowing the typical duty cycle (D) is important.

$$D = \frac{V_{OUT}}{V_{IN}} \text{ or } D = \frac{V_{OUT}}{V_{IN} - I_{OUT}(R_{DS(ON)} + R_{DCR})}$$

if the R_{DCR} of the inductor and $R_{DS(ON)}$ of the MOSFET are available with V_{IN} = (V_{BAT} - V_{DIODE}). All values should be typical to optimize the design for normal operation.

Inductance

The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, efficiency, and transient-response requirements.

- Lower inductor values increase LIR, which minimizes size and cost, and improves transient response at the cost of reduced efficiency due to higher peak currents.

- Higher inductance values decrease LIR, which increases efficiency by reducing the RMS current at the cost of requiring larger output capacitors to meet load-transient specifications.

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L_{MIN1} = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times I_{OUT} \times LIR}$$

where V_{IN}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions).

The next equation ensures that the inductor current downslope is less than the internal slope compensation:

$$m \geq \frac{m2}{2}$$

$$m2 = \frac{V_{OUT}}{L} \times A_{VCS} \times R_{CS}$$

where m is the internal slope compensation, m2 is the inductor current downslope, A_{VCS} is current-sense gain (11V/V), and R_{CS} is current-sense resistor.

Solving for L and adding 1.5 multiplier to account for tolerances in the system:

$$L_{MIN2} = \frac{(V_{OUT} \times A_{VCS} \times R_{CS} \times 1.5)}{2m}$$

Select the larger of L_{MIN1} and L_{MIN2} as L_{MIN}.

The maximum inductor value is recommended to:

$$L_{MAX} = 1.6 \times L_{MIN}$$

For example, in a typical-use case, 5V output voltage and 5A output current, R_{CS} is 15mΩ, m is 0.4V/µs for 2.2MHz and 0.08V/µs for 400kHz. For 2.2MHz:

$$L_{MIN} = \frac{(5 \times 11 \times 0.015 \times 1.5)}{(2 \times 0.4)} = 1.5\,\mu H$$

$$L_{MAX} = 1.6 \times 1.5 = 2.4\,\mu H$$

Therefore, a 2.2µH inductor is chosen for 2.2MHz.

For 400kHz, L_{MIN} is calculated as 7.7µH and L_{MAX} is 12.3µH; therefore, a 10µH inductor is chosen.

Peak Inductor Current

Inductors are rated for maximum saturation current. The maximum inductor current equals the maximum load current, in addition to half the peak-to-peak ripple current:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is calculated as:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where $\Delta I_{INDUCTOR}$ is in mA, L is in µH, and f_{SW} is in kHz.

Once the peak current and inductance are known, the inductor can be selected. The saturation current should be larger than I_{PEAK}, or at least in a range where the inductance does not degrade significantly. The MOSFETs are required to handle the same range of current without dissipating too much power.

MOSFET Selection in Buck Converters

Each step-down controller drives two external logic-level n-channel MOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs include the items in the following sections.

Threshold Voltage

All four n-channel MOSFETs must be a logic-level type, with guaranteed on-resistance specifications at $V_{GS} = 4.5V$. If the internal regulator is bypassed (for example: $V_{EXTVCC} = 3.3V$), the n-channel MOSFETs should be chosen to have guaranteed on-resistance at that gate-to-source voltage.

Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)

All MOSFETs must be chosen with an appropriate V_{DS} rating to handle all V_{IN} voltage conditions.

Current Capability

The n-channel MOSFETs must deliver the average current to the load and the peak current during switching. Choose MOSFETs with the appropriate average current at $V_{GS} = 4.5V$, or $V_{GS} = V_{EXTVCC}$ when the internal linear regulator is bypassed. For load currents below approximately 3A, dual MOSFETs in a single package can be an economical solution. To reduce switching noise for smaller MOSFETs, use a series resistor in the BST_ path and additional gate capacitance. Contact the factory for guidance using gate resistors.

Current-Sense Measurement

For the best current-sense accuracy and overcurrent protection, use a ±1% tolerance current-sense resistor between the inductor and output, as shown in Figure 1A. This configuration constantly monitors the inductor current, allowing accurate current-limit protection. Use low-inductance current-sense resistors for accurate measurement.

Alternatively, high-power applications that do not require highly accurate current-limit protection can reduce the overall power dissipation by connecting a series RC circuit across the inductor (see Figure 1B) with an equivalent time constant:

$$R_{CSHL} = \left(\frac{R2}{R1+R2}\right)R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}}\left(\frac{1}{R1} + \frac{1}{R2}\right)$$

where R_{CSHL} is the required current-sense resistor and R_{DCR} is the inductor's series DC resistor. Use the inductance and R_{DCR} values provided by the inductor manufacturer. If DCR sense is the preferred current-sense method, the recommended resistor value for R1 (Figure 1B) should be less than 1kΩ.

Carefully observe the PCB layout guidelines to ensure the noise and DC errors do no corrupt the differential current-sense signals seen by CS_ and OUT_. Place the sense resistor close to the device with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

Input Capacitor in Buck Converters

The discontinuous input current of the buck converters cause large input ripple currents and therefore the input capacitor must be carefully chosen to withstand the input ripple current and keep the input-voltage ripple within design requirements. The 180° ripple phase operation increases the frequency of the input-capacitor ripple current to twice the individual converter switching frequency. When using ripple phasing, the worst-case input-capacitor ripple current is when the converter with the highest output current is on.

The input-voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR} that peaks at the end of an on-cycle.
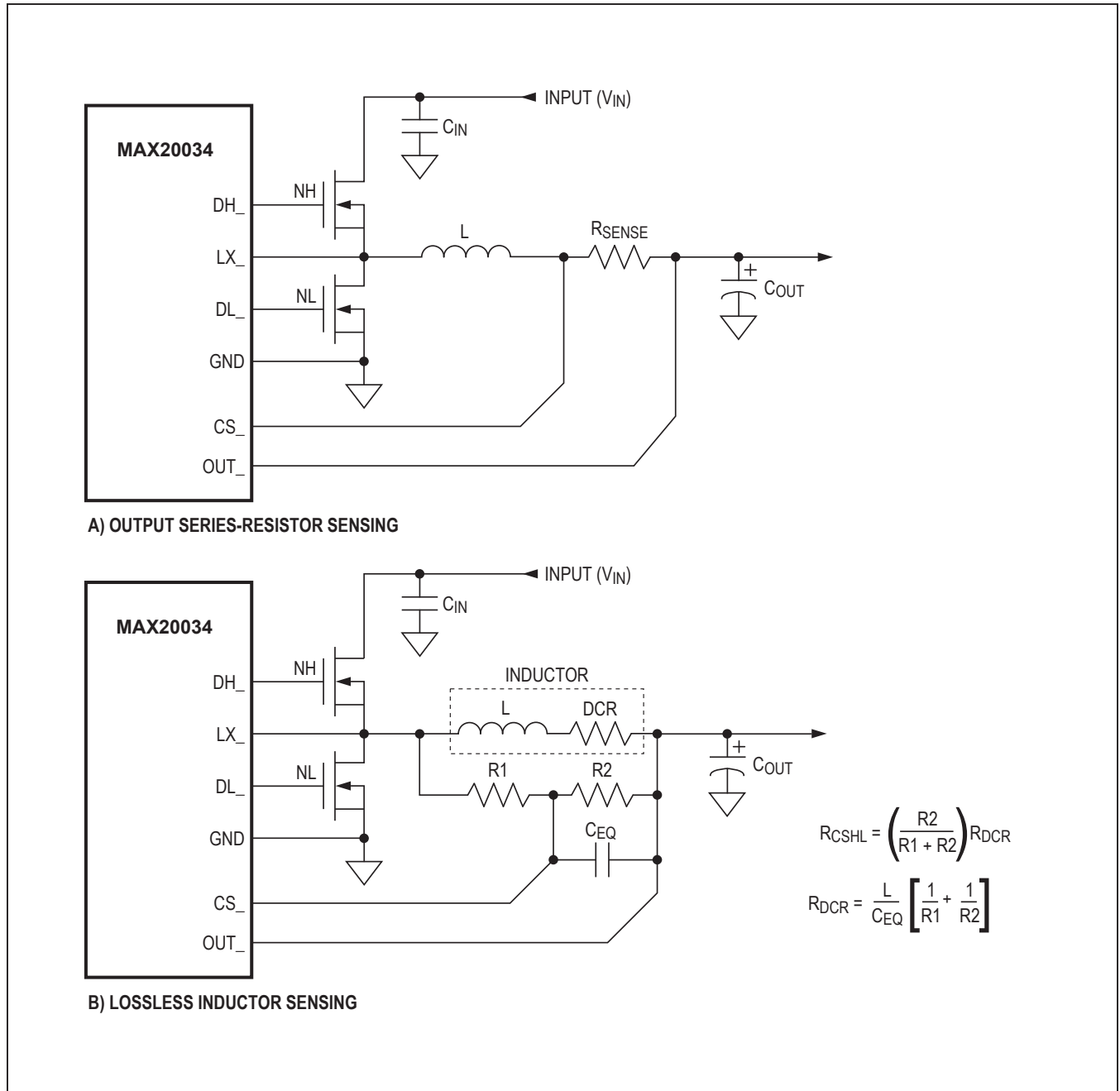
Figure 1. Current-Sense Configurations

The formulas shown in the figure:

$$R_{CSHL} = \left(\frac{R2}{R1 + R2}\right) R_{DCR}$$

$$R_{DCR} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

Calculate the input capacitance and ESR required for a specific ripple using the following equation:

$$ESR[\Omega] = \frac{\Delta V_{ESR}}{\left(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN}[\mu F] = \frac{I_{LOAD(MAX)} \times \left(\frac{V_{OUT}}{V_{IN}}\right)}{(\Delta V_Q \times f_{SW})}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$I_{LOAD(MAX)}$ is the maximum output current in A, ΔI_{P-P} is the peak-to-peak inductor current in A, f_{SW} is the switching frequency in MHz, and L is the inductor value in µH.

The internal 5V linear regulator (BIAS) includes an output UVLO with hysteresis to avoid unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. At lower input voltage, additional input capacitance helps avoid possible undershoot below the undervoltage-lockout threshold during transient loading.

Output Capacitor in Buck Converters

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. The capacitor is usually selected by ESR and the voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the *Transient Considerations* section). However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability.

The total voltage sag (V_{SAG}) can be calculated as follows:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2}{2C_{OUT}((V_{IN} \times D_{MAX}) - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)}(t - \Delta t)}{C_{OUT}}$$

The amount of overshoot (V_{SOAR}) during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT}V_{OUT}}$$

ESR Considerations

The output-filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple, so the output capacitor's size depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

In standby mode, the inductor current becomes discontinuous, with peak currents set by the idle-mode current-sense threshold ($V_{CS,SKIP}$ = 26mV (typ)).

Transient Considerations

The output capacitor must be large enough to absorb the inductor energy while transitioning from no-load to full-load condition without tripping the overvoltage fault protection. The total output voltage sag is the sum of the voltage sag while the inductor is ramping up, and the voltage sag before the next pulse can occur. Therefore:

$$C_{OUT} = \frac{L(\Delta I_{LOAD(MAX)})^2}{2V_{SAG}(V_{IN} \times D_{MAX} - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)}(t - \Delta t)}{V_{SAG}}$$

where D_{MAX} is the maximum duty factor (approximately 95%), L is the inductor value in µH, C_{OUT} is the output capacitor value in µF, t is the switching period (1/f_{SW}) in µs, and Δt equals (V_{OUT}/V_{IN}) x t.

The IC uses a peak current-mode-control scheme that regulates the output voltage by forcing the required current through the external inductor, so the controller uses the voltage drop across the DC resistance of the inductor or the alternate series current-sense resistor to measure the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier

compensation than voltage-mode control. A single series resistor (R_C) and capacitor (C_C) is all that is required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (see Figure 2). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor (C_F) from COMP to AGND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback-divider, and an error amplifier, as shown in Figure 2. The power modulator has a DC gain set by g_{mc} x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The loop response is set by the following equations:

$$GAIN_{MOD(dc)} = g_{mc} \times R_{LOAD}$$

where R_{LOAD} = $V_{OUT}/I_{LOUT(MAX)}$ in Ω and g_{mc} =1/(A_{V_CS} x R_{DC}) in S. A_{V_CS} is the voltage gain of the current-sense amplifier and is typically 11V/V. R_{DC} is the DC resistance of the inductor or the current-sense resistor in Ω.

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

The unity-gain frequency of the power stage is set by C_{OUT} and g_{mc}:

$$f_{UGAINpMOD} = \frac{g_{mc}}{2\pi \times C_{OUT}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting C_{OUT} = n x $C_{OUT(EACH)}$, and ESR = $ESR_{(EACH)}$/n. Note that the capacitor zero for a parallel combination of alike capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB}$ = V_{FB}/V_{OUT}, where V_{FB} is 1V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)}$ = $g_{m,EA}$ x $R_{OUT,EA}$, where $g_{m,EA}$ is the error-amplifier transconductance, which is 470µS

(typ), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 2.2MΩ (typ) (see the *Electrical Characteristics* table.)

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{PEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C, where the loop gain equals 1 (0dB)). Thus:

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/15th the switching frequency and much higher than the power-modulator pole (f_{pMOD}). Select a value for f_C in the range:

$$f_{pMOD} \ll f_C \le \frac{f_{SW}}{15}$$

At the crossover frequency, the total loop gain must be equal to 1. Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(f_C)} = 1$$

$$GAIN_{EA(f_C)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(f_C)} = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(f_C)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP to AGND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

The following is a numerical example to calculate the compensation network component values of Figure 2:

- A_{V_CS} = 11V/V
- R_{DCR} = 15mΩ
- g_{mc} = 1/(A_{V_CS} x R_{DC}) = 1/(11 x 0.015) = 6.06
- V_{OUT} = 5V
- $I_{OUT(MAX)}$ = 5.33A
- R_{LOAD} = V_{OUT}/$I_{OUT(MAX)}$ = 5V/5.33A = 0.9375Ω
- C_{OUT} = 2x47µF = 94µF
- ESR = 9mΩ/2 = 4.5mΩ
- f_{SW} = 0.403MHz

$$GAIN_{MOD(dc)} = 6.06 \times 0.9375 = 5.68$$

$$f_{pMOD} = \frac{1}{2\pi \times 94µF \times 0.9375} \approx 1.8kHz$$

$$f_{pMOD} << f_C \leq \frac{f_{SW}}{15}$$

$$1.8kHz << f_C \leq 80.6kHz$$

select f_C = 25kHz:

$$f_{zMOD} = \frac{1}{2\pi \times 4.5mΩ \times 94µF} \approx 376kHz$$

since f_{zMOD} > f_C:
- $R_C \approx 25kΩ$
- $C_C \approx 3.3nF$
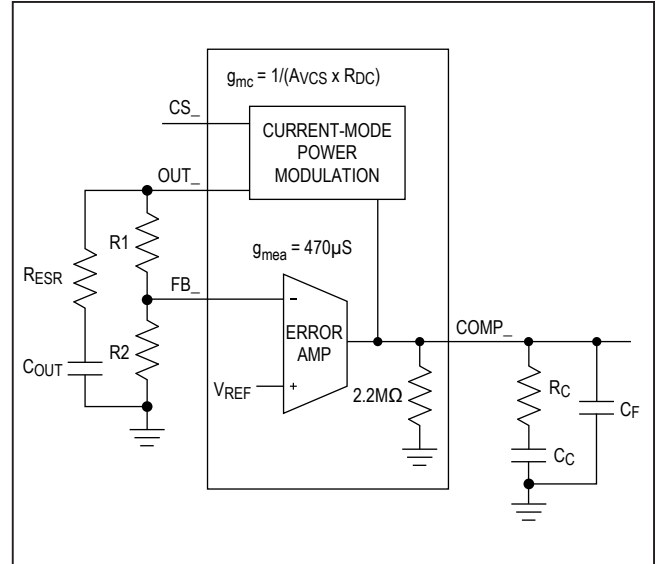- $C_F \approx 18pF$

Figure 2. Compensation Network

Applications Information

Layout Recommendations

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (see Figure 3). If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.

- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full load efficiency by 1% or more.

- Minimize current-sensing errors by connecting CS_ and OUT_. Use kelvin sensing directly across the current-sense resistor ($R_{SENSE\_}$). A high-frequency filter is required if operating above 1.8MHz. The recommended RC filter values are 20Ω/100pF. Refer to the MAX20034 EV kit data sheet schematic for details.

- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (FB_, CS_, and OUT_).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side FET, C_{IN}, $C_{OUT\_}$, and Schottky). If possible, make all these connections on the top layer with wide, copper-filled areas.

2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite DL_ and DH_ to keep LX_, PGND, DH_, and the DL_ gate drive lines short and wide. The DL_ and DH_ gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.

3) Group the gate-drive components (BST_ diode and capacitor and LDO bypass capacitor BIAS) together near the controller IC. Be aware that gate currents of up to 1A flow from the bootstrap capacitor to BST_,

from DH_ to the gate of the external HS switch and from the LX_ pin to the inductor. Up to 100mA of current flow from the BIAS capacitor through the bootstrap diode to the bootstrap capacitor. Dimension those traces accordingly.

4) Make the DC-DC controller ground connections as shown in Figure 3. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go; and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly under the IC.

5) Connect the output-power planes directly to the output-filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close as possible to the load.
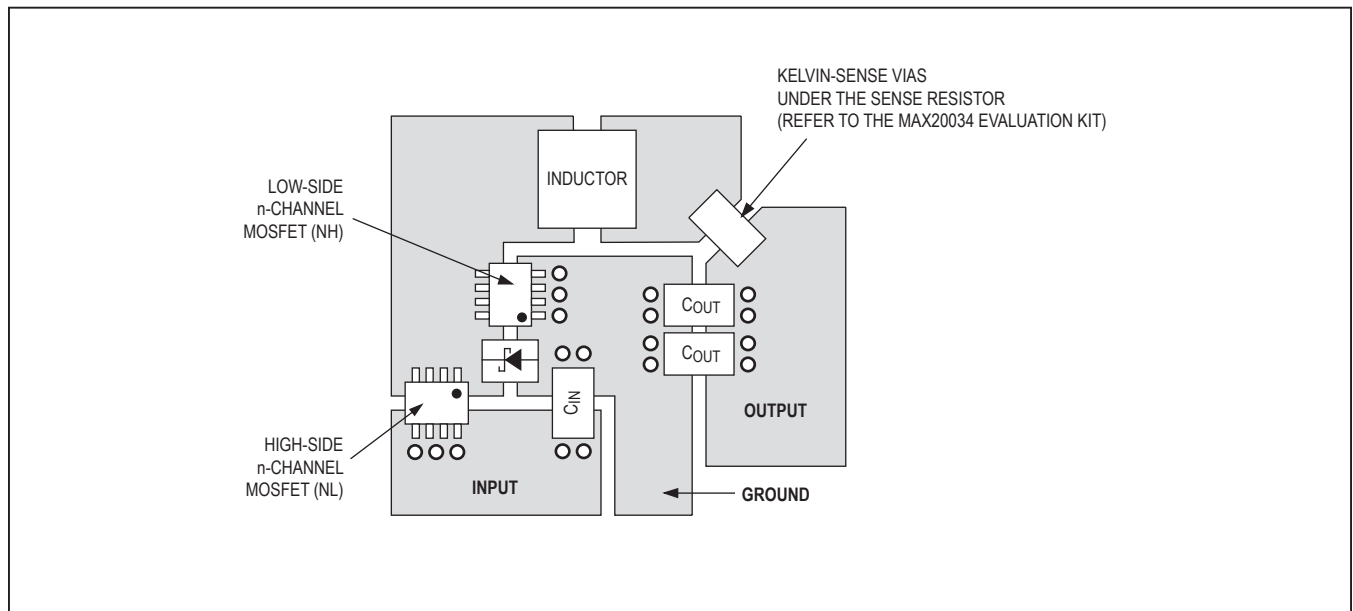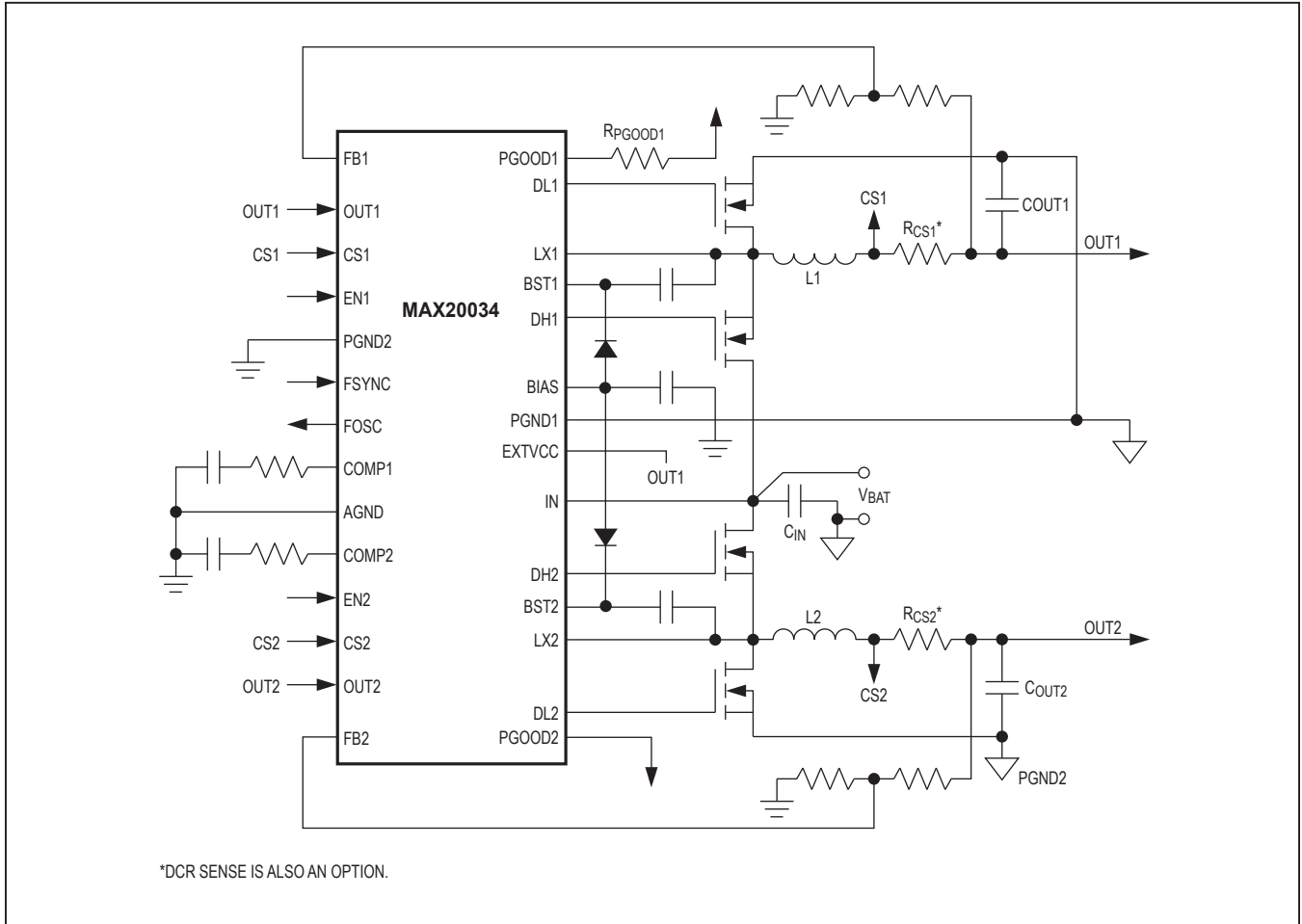

Figure 3. Layout Example

Typical Operating Circuit

*DCR SENSE IS ALSO AN OPTION.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	V_{OUT}		SPREAD SPECTRUM
			ADJUSTABLE	FIXED	
MAX20034ATIR/VY+	-40°C to +125°C	28 TQFN-EP**	1V to 10V	5V/3.3V	Off
MAX20034ATIS/VY+	-40°C to +125°C	28 TQFN-EP**	1V to 10V	5V/3.3V	On

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial release	—
1	2/18	Removed future product status from MAX20034ATIR/VY+ in *Ordering Information*	23
2	4/18	Updated the *Simplified Block Diagram*, TOC01–TOC02, TOC08, TOC11–TOC12, TOC23, *Pin Description* table, and the *Inductance* and *Transient Considerations* section.	2, 6–7, 9, 11, 15, 19–20