

# Datasheet – MPEG Video/Audio Codec Modules – Standard Version

System-On-Chip (SOC) Technologies

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## 1. Overview of SOC SoM Modules

### 1.1 Overview of SOC SoMs

The SOC SoMs (System-On-Module) are small circuit boards with FPGA, DDRs, Flash memory, and clocks in one module to support FPGA-based systems. Table-1 lists the current SOC SoMs, with product code and the FPGA chip on each of the modules. A module can be configured into an application SoM by using the applicable firmware. The module is connected to a user PCB through a standard DDR3 SODIMM connector. Customers can order the blank SoMs from SOC and use their own firmware to make SoM products. Datasheet, application notes, and reference designs are provided in separated documents. This datasheet, however, details the SOC MPEG codec modules based on the SOC codec IP cores and the SoMs.

Table-1 SOC SoMs – Product Code and the FPGA chip on the module

Item #	SOM Product Code	FPGA Chip on the Module	FPGA Part Number
1	SoM-X-SLX150	Spartan-6 XC6SLX150	
2	SoM-X-A200T	Artix-7 XC7A200T	
3	SoM-X-Z7035	Zynq-7 XC7Z7035	
4	SoM-X-Z7045	Zynq-7 XC7Z7045	
5	SoM-I-SX660	Arria-10 SX066	

Fig. 1 shows a photo of the modules. Figs. 2-5 show the dimensions of SoM-X-SLX150, SoM-X-A200T, SoM-X-Z7035, and SoM-I-SX660 respectively. The SoM-X-Z7045 is identical to the SoM-X-Z7035, except the FPGA chip.



Fig. 1 SOC SoM modules

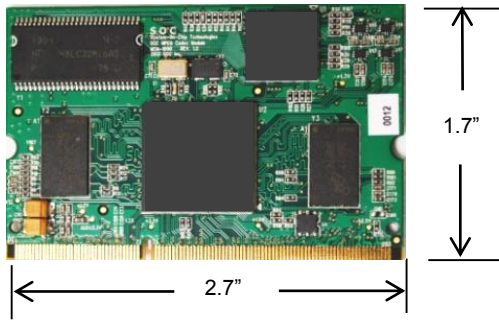


Fig. 2. Dimension of SoM-X-SLX150

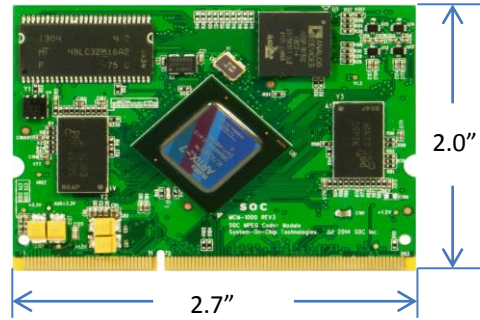


Fig. 3. Dimension of SoM-X-A200T

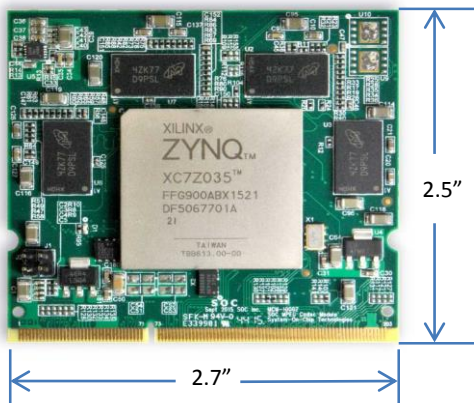


Fig. 4. Dimension of SoM-X-Z7035

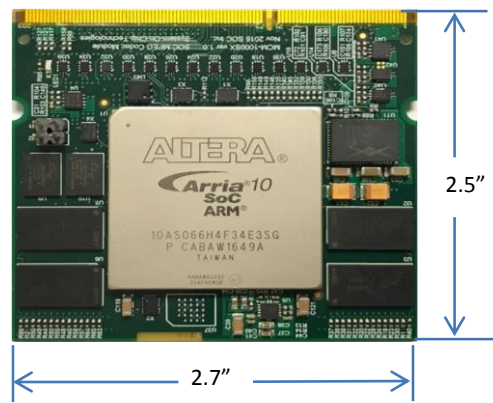


Fig. 5. Dimension of SoM-I-SX660

## 1.2 Product Code for the SOC SoMs

The SOC SoM product code provides the information of the FPGA chip on the module and the temperature ranges. Fig. 6 shows the product code convention for the SOC SoMs.

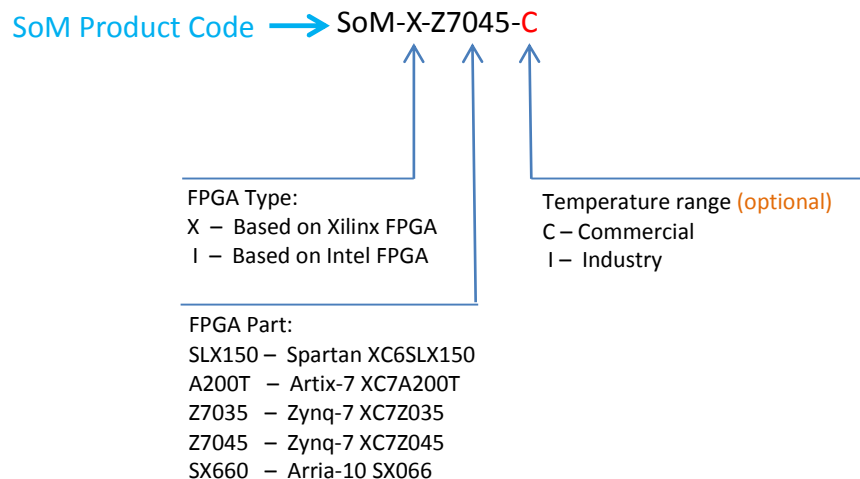


Fig. 6. The SOC SoM product code format

### 1.3 Overview of SOC Codec Modules

SOC configures the SoMs into MPEG codec modules using the SOC codec IP cores, for video/audio compression, decompression, and transcoding functions. Table-2 lists the SoMs and the resolution capacities when they are configured into codec modules. The product code for the SOC codec modules are discussed in following Section 1.4.

Table-2 SOC Codec modules – SoM Product Code, the FPGA chip on the module, and resolution capabilities

	SoM Product Code	FPGA Chip on the Module	Codec module Resolution Capacity
1	SoM-X-SLX150	Spartan-6 XC6SLX150	H.264 or MPEG-2 HD up to 1080@30 <i>(MOQ of 100pcs required)</i>
2	SoM-X-A200T	Artix-7 XC7A200T	H.264 or MPEG-2 HD, 1080@30 and 1080@60
3	SoM-X-Z7035 (or SoM-X-Z7045)	Zynq-7 XC7Z035 (or XC7Z045)	H.264 4k@30
4	SoM-X-Z7045	Zynq-7 XC7Z045	H.265 1080@60 and 4k@30
5	SoM-I-SX660	Arria-10 SX066	H.264 4k@60 and 8k@30 H.265 4k@60

### 1.4 Product Code for SOC Codec Modules

The SOC codec modules are pre-configured SoMs using the SOC codec IP cores (encoder, decoders, and transcoders, etc). Once a SoM is configured, it becomes a functional module according to the IP core used to configure it. SOC offers a series of MPEG codec modules as standard products. Fig. 7 shows the product code format for the SOC MPEG codec modules.

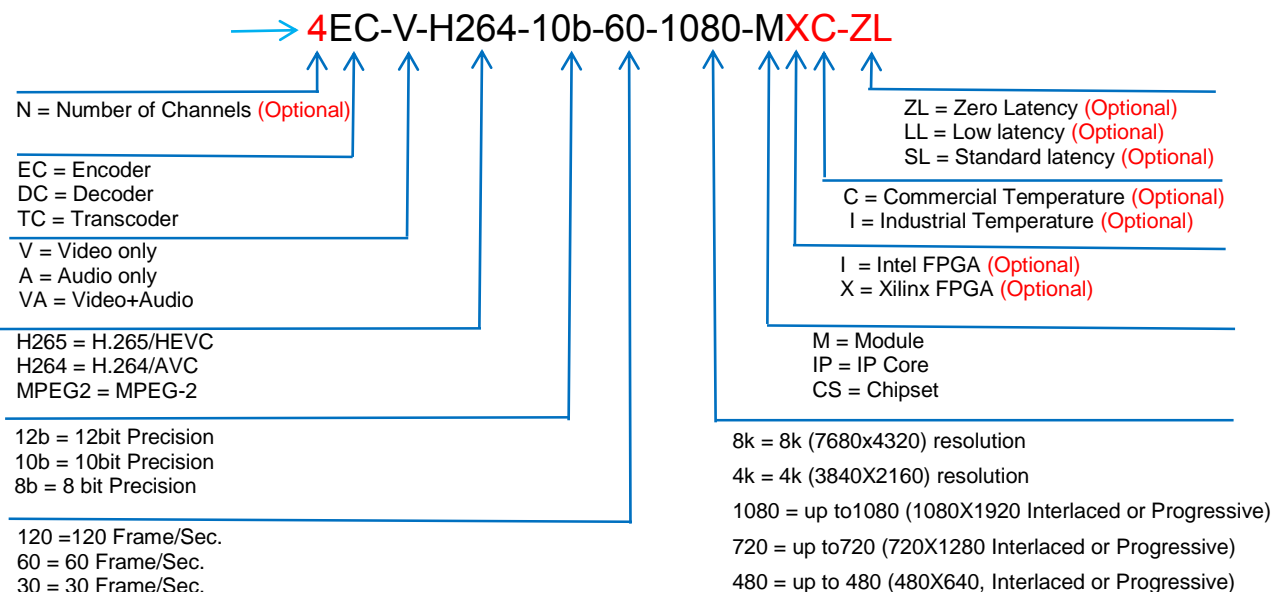


Fig. 7. The SOC Codec Module product code format



As shown in Fig. 7, the product code of the SOC codec module reflects the functionality (Encoder, Decode, or Transcoder, etc.) and the technical specification of the module (MPEG standard, resolution, frame rate, and precision). It has the same format for the SOC MPEG codec IP cores and chipsets, as SOC offers IP core licensing and chipsets as separated product lines. There are optional fields in the product code, which can be included or ignored. These optional fields include:

1. The number of channels
2. FPGA type, Intel or Xilinx
3. Temperature, commercial or industrial
4. Latency, Zero, Standard, or lower latency.

It is noted that the information of the SoM used for the codec module is not reflected in the Codec Module product code. This is intended to reduce the length of the product code. However, the product code of the SoM that is used for a specific Codec Module can be added together with the Codec Module product code to identify the SoM on which a given Codec Module is based. For example:

SoM-X-Z7045-C

EC-V-H264-10b-60-1080-M-ZL

Would mean a Codec Module made from the SoM that has a Zynq-7045 FPGA of commercial temperature, and configured into a Video Encoder module with the specifications of H.264, 10bit, 1080@60 resolution, and zero latency.

## 2. Connecting the Module to a User PCB

The SoM modules have identical edge pins that are compatible with standard DDR3 SODIMM 204 pin connector. The following off-the-shelf DDR3 SODIMM connectors can be used to connect the SOC SoMs or the codec modules onto a user PCB:

1. MM80-204B1-1
2. MM80-204B1-1E
3. AS0A621-U2SN-7F
4. AS0A621-H2S6-7H

Fig. 8 shows a photo of a standard 204 pin DDR3 SODIMM PCB connector. Refer to the datasheet of the connector used for the physical dimension and PCB design requirements.



Fig. 8 A photo of the standard 204 pin DDR3 SODIMM connector

### 3. Overview SOC Standard Codec Modules

The above described SoMs: the **SoM-X-SLX150** (based on Spatran-6 FPGA), **SoM-X-A200T** (based on Artix-7 FPGA), **SoM-X-Z7035/SoM-X-Z7045**(based on Zynq-7 FPGAs), and **SoM-I-SX660** (based on Intel Arria-10 FPGAs) can be configured into different products by downloading the desired firmware. At SOC, we produce encoder, decoder, transcoder, and multi-channel encoder or decoder SoMs for video compression functions, by configuring the SoMs using the **SOC MPEG Codec IP** cores.

The standard encoder modules: H.265, H.264, and MPEG-2, take raw video and audio as input and output TS streams, via the edge pins of the modules, as shown in Fig. 9. The standard decoder modules: H.265, H.264, and MPEG-2, take TS stream as inputs and output decoded video and audio, via the edge pins of the modules, as shown in Fig. 10. There are also control signal pins, to allow the user control of the encoder or decoder.

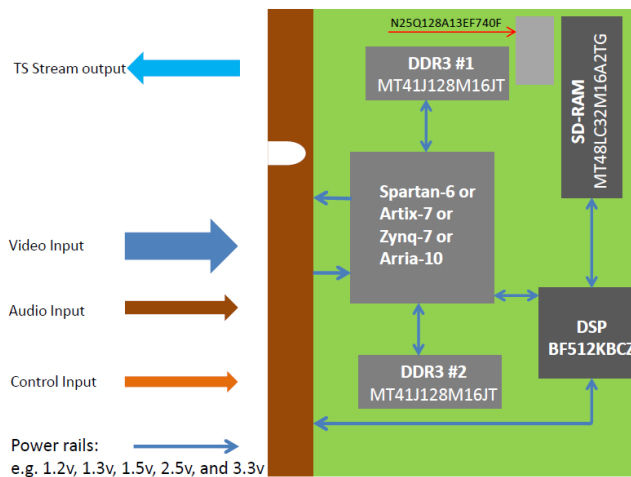


Fig. 9 SOC Standard encoder modules (H.265, H.264, or MPEG-2)

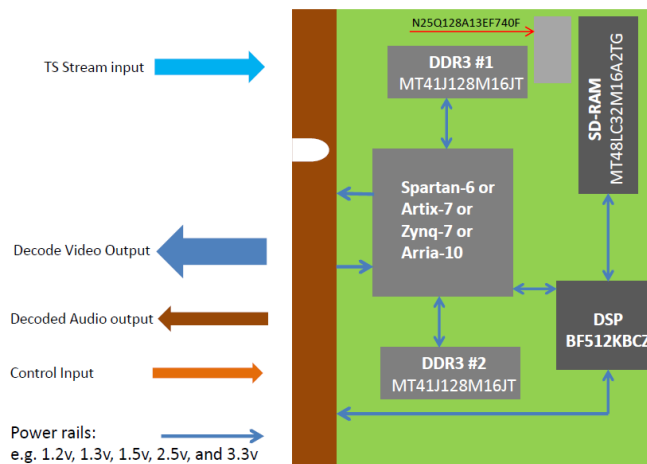


Fig. 10 SOC Standard decoder modules (H.265, H.264, or MPEG-2)

**Appendix-A** provides the details of the Standard Codec Modules, including the product tables which list the product codes along with the specifications. Customers can order the modules according the specifications required by using the corresponding product code.

The pin assignments, pin voltages, and signal formats for standard encoder modules, decoder modules, and transcoder modules are detailed in this Datasheet respectively.

*It should be noted that not all of the modules listed in Appendix-A are discussed in this Datasheet. Pin assignments and electrical properties for the modules that are not provided in this document will be provided on demand basis.*

SOC also offers customized modules according to customer requirements, such as Transcoder modules, Multi-channel encoder or decoder modules, and modules with non-standard I/Os. For details, contact SOC sales at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com)

One of the popular extended versions of the standard codec modules is the –NET version which integrates the SOC low latency network stack (UDP/IP over Ethernet) into the encoder or decoder module. The pin assignments, pin voltages, and signal formats for the –NET version encoder and decoder modules are detailed in the document:

**[Datasheet – MPEG Video/Audio Codec Modules –NET Version](#)**

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## 4. The H.264 (and MPEG-2) HD Encoder Modules

### 4.1 Pin Assignments and Pin Voltages

The HD (1080@30 and 1080@60) encoder modules for H.264 or MPEG-2 have the same pin assignments and electrical properties. The SoM (module hardware) for H.264 or MPEG-2 HD resolution encoder uses the SoM-X-A200T (the Artix-7 A200T FPGA).

*Note: The H.264 (or MPEG-2) HD 1080@30 Encoder can use the SoM-X-SLX150 module. But, it is a legacy product which is offered only for special orders (with volume). The Datasheet for the H.264 HD 1080@30 Encoder on the SoM-X-SLX150 module is available on request.*

This Section provides the pin assignments and electrical properties for H.264 or MPEG-2 HD encoder module which is based on the SoM-X-A200T. Table-3 lists the pin assignments and the pin voltages.

The schematics of SoM-X-A200T edge connector are attached in Appendix-B of this document, which shows the pin numbers for data, clock, control, and power. It should be noted that the encoder module uses only some of the edge pins, and not all of the edge pins are used.

Table-3 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Artix-7 datasheet provides further information regarding the properties of these pins, and can be used as a reference for use PCB design when the SoM-X-A200T is used.

**Table 3: HD Encoder Module (based on SoM-X-A200T) Pin Assignment and Pin Voltages**

Description	SoM-X-A200T Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
Video Clock	105	Input	AB15	3.3V	LVC MOS33
Video Horizontal Sync	133	Input	M18	1.5V	LVC MOS15
Video Vertical Sync	113	Input	AB17	3.3V	LVC MOS33
Video Display Enable	67	Input	J15	1.5V	LVC MOS15
Video Data Luma[0]	135	Input	N20	1.5V	LVC MOS15
Video Data Luma[1]	137	Input	N19	1.5V	LVC MOS15
Video Data Luma[2]	116	Input	G15	1.5V	LVC MOS15
Video Data Luma[3]	118	Input	H15	1.5V	LVC MOS15
Video Data Luma[4]	124	Input	G16	1.5V	LVC MOS15
Video Data Luma[5]	126	Input	J16	1.5V	LVC MOS15
Video Data Luma[6]	128	Input	J17	1.5V	LVC MOS15
Video Data Luma[7]	130	Input	H17	1.5V	LVC MOS15
Video Data Luma[8]	132	Input	G18	1.5V	LVC MOS15
Video Data Luma[9]	134	Input	N18	1.5V	LVC MOS15
Video Data Chroma[0]	143	Input	L18	1.5V	LVC MOS15
Video Data Chroma[1]	145	Input	M20	1.5V	LVC MOS15
Video Data Chroma[2]	147	Input	L19	1.5V	LVC MOS15
Video Data Chroma[3]	149	Input	L20	1.5V	LVC MOS15
Video Data Chroma[4]	151	Input	K18	1.5V	LVC MOS15

Video Data Chroma[5]	153	Input	K19	1.5V	LVC MOS15
Video Data Chroma[6]	155	Input	J20	1.5V	LVC MOS15
Video Data Chroma[7]	157	Input	J21	1.5V	LVC MOS15
Video Data Chroma[8]	159	Input	J19	1.5V	LVC MOS15
Video Data Chroma[9]	161	Input	H19	1.5V	LVC MOS15
SPDIF Audio	27	Input	G13	1.5V	LVC MOS15
Transport Stream Buffer Ready	29	Input	H13	1.5V	LVC MOS15
Transport Stream Clock	31	Output	H14	1.5V	LVC MOS15
Transport Stream Data Valid	33	Output	J14	1.5V	LVC MOS15
Transport Stream Data[0]	152	Output	B20	3.3V	LVC MOS33
Transport Stream Data[1]	154	Output	C19	3.3V	LVC MOS33
Transport Stream Data[2]	158	Output	A19	3.3V	LVC MOS33
Transport Stream Data[3]	160	Output	A18	3.3V	LVC MOS33
Transport Stream Data[4]	162	Output	T18	3.3V	LVC MOS33
Transport Stream Data[5]	164	Output	T20	3.3V	LVC MOS33
Transport Stream Data[6]	166	Output	T19	3.3V	LVC MOS33
Transport Stream Data[7]	156	Output	A20	3.3V	LVC MOS33
Uart_tx	90	Output	U18	3.3V	LVC MOS33
Uart_rx	88	Input	Y12	3.3V	LVC MOS33

## 4.2 Signal Formats

### 4.2.1 Video Clock Signal (Input)

The **Video Clock** signal has two functions: (1) It is the clock for the input video data, and (2) it is the clock that drives the encoder engine.

The **Video Clock** signal usually comes from the video input interface chip, such as HDMI or SDI. It is the clock for the input video data. It is also used for driving the encoder engine. A local clock source (e.g. oscillator) is required to drive the video input interface chip. The frequency varies according to the resolution of the video input. The following are the clock frequencies for standard video resolutions.

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

### 4.2.2 Video Data Signals (Input)

The input to the encoder module (H.264 or MPEG-2) is raw video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma; and 10 input lines: **Video Data Chroma[0]** to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]**, **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros. All of the Video Data signals are single-ended.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization. A **Video Clock** coming from the video interface chip (refer to Section 4.2.1 for the clock frequencies) is required to provide the timing for the parallel input of luma, chroma, as well as for

the **Video Horizontal Sync** and **Video Vertical Sync** signals. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Display Enable signal** at high, when active pixels are being sent out. The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section 4.2.1.

#### 4.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

#### 4.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**; along with the Transport Stream output data clock **Transport Stream Clock**. The frequency of the Transport Stream Data clock is 27MHz.

**Transport Stream Buffer Ready** and **Transport Stream Data Valid** are the signals to inform the user side to take over the signals.

#### 4.2.5 Encoder Control Signals (Input and Output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the encoder. **Uart\_rx** receives the command from an external control device. **Uart\_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Encoder API User Manual](#) for more details.

### 4.3 Power Rails of SoM-X-A200T

Table-4 lists the power and ground pins. Refer to Appendix-B for the pins of power and ground on the edge connector of the SoM-X-A200T module.

**Table-4: SoM-X-A200T Power and Ground Pins**

SoM-X-A200T Connector Pin	Voltage
1,3,5,7,9,11,13,15	3.3V
10,12,14,16	1.2V
22,24,26,28,30,32	1.5V
189,191,193,195,197,199	2.5V
188,190,192,194	1.3V
43,45,47,49,51,53,55,57	1.0V
2,4,6,8,18,20,34,36,42,44,62,72	Ground
17,35,37,39,41,71	Ground
73,75,129	Ground
74	Ground
175,177,185,187,203	Ground
184,186,200,202,204	Ground

#### 4.4 Power Requirement and Supply Current

The total power, at operation, required by a given encoder module ranges from 2 to 5 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-5 provides a power estimation for each rail for the carrier board PCB design purpose.

**Table-5: Power supply estimation for the carrier board PCB design**

Power Rail	Current (A)	Power (W)
3.3V	0.23	0.76
2.5V	0.62	1.55
1.5V	0.78	1.16
1.3V	0.23	0.30
1.2V	0.47	0.57
1.0V	2.12	2.12

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 19 of this document. The reference designs provide not only the power system design and clock distributions, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for design licensing details.

#### 4.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once all of the power rails are ready, the module will start to boot. The booting time is less than 2 seconds.

(Left Empty here intentionally)

## 5. The H.264 (and MPEG-2) HD Decoder Modules

### 5.1 Pin Assignments and Pin Voltages

The modules of H.264 HD (1080@30 and 1080@60) decoders and the MPEG-2 HD decoder have the same pin assignment. The module for HD resolution decoding uses the SoM-X-A200T (with the Artix-7 A200T FPGA which is the same as the one used for the HD Encoder).

*Note: The H.264 HD 1080@30 Decoder can use the SoM-X-SLX150 module. But, it is a legacy product which is offered only for special orders (with volume). The Datasheet for the H.264 HD 1080@30 Decoder on the SoM-X-SLX150 module is available on request.*

This section details the pin assignments and pin voltages for the HD decoder (H.264 and MPEG-2) modules. Table-6 shows the pin assignments and the pin voltages.

The schematics of SoM-X-A200T edge connector are attached in Appendix-B of this document. Appendix-B shows the pin numbers for data, clock, control, and power, which are connected to the FPGA (Artix-7 XC7A200T). It should be noted that the decoder module uses only some of the available edge pins that are connected to the FPGA (some of the pins are not used).

It should also be noted that the HD encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

**Table-6: HD Decoder Module (based on SoM-X-A200T) Pin Assignment**

Description	SoM-X-A200T Edge Connector Pin	Direction	FPGA Pin #	Voltage	IO Standard
Decoder Clock	80	Input	R17	3.3V	LVCN0533
Use Decoder Clock	63	Input	L14	1.5V	LVCN0515
Video Clock	105	Output	AB15	3.3V	LVCN0533
Video Horizontal Sync	133	Output	M18	1.5V	LVCN0515
Video Vertical Sync	113	Output	AB17	3.3V	LVCN0533
Video Display Enable	67	Output	J15	1.5V	LVCN0515
Video Data Luma[0]	135	Output	N20	1.5V	LVCN0515
Video Data Luma[1]	137	Output	N19	1.5V	LVCN0515
Video Data Luma[2]	116	Output	G15	1.5V	LVCN0515
Video Data Luma[3]	118	Output	H15	1.5V	LVCN0515
Video Data Luma[4]	124	Output	G16	1.5V	LVCN0515
Video Data Luma[5]	126	Output	J16	1.5V	LVCN0515
Video Data Luma[6]	128	Output	J17	1.5V	LVCN0515
Video Data Luma[7]	130	Output	H17	1.5V	LVCN0515
Video Data Luma[8]	132	Output	G18	1.5V	LVCN0515
Video Data Luma[9]	134	Output	N18	1.5V	LVCN0515
Video Data Chroma[0]	143	Output	L18	1.5V	LVCN0515
Video Data Chroma[1]	145	Output	M20	1.5V	LVCN0515
Video Data Chroma[2]	147	Output	L19	1.5V	LVCN0515
Video Data Chroma[3]	149	Output	L20	1.5V	LVCN0515
Video Data Chroma[4]	151	Output	K18	1.5V	LVCN0515



Video Data Chroma[5]	153	Output	K19	1.5V	LVC MOS15
Video Data Chroma[6]	155	Output	J20	1.5V	LVC MOS15
Video Data Chroma[7]	157	Output	J21	1.5V	LVC MOS15
Video Data Chroma[8]	159	Output	J19	1.5V	LVC MOS15
Video Data Chroma[9]	161	Output	H19	1.5V	LVC MOS15
SPDIF Audio	27	Output	G13	1.5V	LVC MOS15
Transport Stream Clock ( <b>27MHz</b> )	31	Input	H14	1.5V	LVC MOS33
Transport Stream Data Valid	33	Input	J14	1.5V	LVC MOS33
Transport Stream Data[0]	152	Input	B20	3.3V	LVC MOS33
Transport Stream Data[1]	154	Input	C19	3.3V	LVC MOS33
Transport Stream Data[2]	158	Input	A19	3.3V	LVC MOS33
Transport Stream Data[3]	160	Input	A18	3.3V	LVC MOS33
Transport Stream Data[4]	162	Input	T18	3.3V	LVC MOS33
Transport Stream Data[5]	164	Input	T20	3.3V	LVC MOS33
Transport Stream Data[6]	166	Input	T19	3.3V	LVC MOS33
Transport Stream Data[7]	<b>156</b>	Input	A20	3.3V	LVC MOS33
Uart_tx	90	Output	U18	3.3V	LVC MOS33
Uart_rx	88	Input	Y12	3.3V	LVC MOS33

## 5.2 Signal Formats

### 5.2.1 Clock Signals

When an SDI port on the carrier board is used to send out the decoded video data, the SDI clock should be connected to the **Decoder Clock** and **Use Decoder Clock** should be tied high. This will automatically synchronize the decoder outputs with the SDI interface. Internally generated clock is used if **Use Decoder Clock** is tied low.

The SDI clock frequencies are:

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

The **Video Clock** signal is the clock for the video data output by the decoder. The frequency of the **Video clock** is determined by the video resolution, which are:

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60.

### 5.2.2 Video Data Signals (Output)

The output of the HD decoder module (H.264 or MPEG-2) is the decoded video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma and 10 lines, and, **Video Data Chroma[0]**

to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]**, **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. A **Video Clock** (refer to Section 5.2.1 for the clock frequencies) is sent out, which provides the timing for the parallel inputs of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync** signals. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

Output data are sampled at the rising edge of the clock. (The clock rates will correspond to the resolution and frame rate, as discussed in Section 5.2.1.)

### 5.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

### 5.2.4 TS Stream Signals (Input)

The input of the decoder module is an MPEG transport stream, which is sent into the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**. **Transport Stream Clock** (27MHz) is the clock for the **Transport Stream Data** lines. The **Transport Stream Data Valid** signal informs the decoder that the input is valid.

### 5.2.5 Decoder Control Signals (Input and Output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the decoder. **Uart\_rx** receives the command from an external control device. **Uart\_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Decoder API User Manual](#) for details.

## 5.3 Power Rails of SoM-X-A200T

The power rails for the HD (H.264 or MPEG-2) decoder module is the same as the ones for the HD encoder module. Refer to Table-2 for the power and ground pins. Also, refer to Appendix-B for the power and ground pins on the edge connector of the SoM-X-A200T module.

## 5.4 Power Requirement and Supply Current

The total power at operation required by a given decoder ranges from 2 to 4 Watts, depending on the resolution and frame rate. Since the decoder requires less power than the encoder, the power supply for the encoder can be used as a reference for the carrier board PCB designs. It is listed here again for convenience, as Table-7.

**Table-7: Power supply estimation for the carrier board PCB design**

Power Rail	Current (A)	Power (W)
3.3V	0.23	0.76
2.5V	0.62	1.55
1.5V	0.78	1.16
1.3V	0.23	0.30
1.2V	0.47	0.57
1.0V	2.12	2.12

## 5.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once all of the power rails are supplied, the module will start to boot. The booting time is less than 2 seconds.

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## 6. The H.264 4k@30 Encoder Modules

### 6.1 Pin Assignments and Pin Voltages

The SoM-X-Z7035 or SoM-X-Z7045 module is used for H.264 4K@30 resolution. The pin assignment and electrical properties are the same for SoM-X-Z7035 and SoM-X-Z7045.

Table-8 lists the pin assignments and the pin voltages for the 4K@30 encoder modules based on the SoM-X-Z7045 (SoM-X-Z7035 and SoM-X-Z7045 are the same).

The schematics of SoM-X-Z7045 edge connector are attached in Appendix-C of this document, which shows the pin numbers for data, clock, control, and power.

Table-8 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Zynq-7000 datasheet provides further information regarding the properties of these pins, and can be used as a reference for user PCB designs that use the SoM-X-Z7045 module.

**Table-8: 4K@30 Encoder Module (based on SoM-X-Z7045) Pin Assignment and Pin Voltages**

Description	SoM-X-Z7045 Edge Connector	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset B	156	Input	B19	3.3V	LVC MOS33
Video Clock 0	63	Input	AC18	1.5V	LVC MOS15
Video Clock 1	80	Input	AF15	3.3V	LVC MOS33
Video Clock 2	144	Input	AE28	3.3V	LVC MOS33
Video Clock 3	105	Input	AG21	3.3V	LVC MOS33
Video Horizontal Sync	133	Input	W24	1.5V	LVC MOS15
Video Vertical Sync	113	Input	AF22	3.3V	LVC MOS33
Video Display Enable	67	Input	AD18	1.5V	LVC MOS15
Video Data 0 Luma[0]	135	Input	W25	1.5V	LVC MOS15
Video Data 0 Luma[1]	137	Input	W26	1.5V	LVC MOS15
Video Data 0 Luma[2]	116	Input	V27	1.5V	LVC MOS15
Video Data 0 Luma[3]	118	Input	W28	1.5V	LVC MOS15
Video Data 0 Luma[4]	124	Input	W29	1.5V	LVC MOS15
Video Data 0 Luma[5]	126	Input	W30	1.5V	LVC MOS15
Video Data 0 Luma[6]	128	Input	V28	1.5V	LVC MOS15
Video Data 0 Luma[7]	130	Input	V29	1.5V	LVC MOS15
Video Data 0 Luma[8]	132	Input	T30	1.5V	LVC MOS15
Video Data 0 Luma[9]	134	Input	U30	1.5V	LVC MOS15
Video Data 1 Luma[0]	117	Input	AG22	3.3V	LVC MOS33
Video Data 1 Luma[1]	119	Input	AH22	3.3V	LVC MOS33
Video Data 1 Luma[2]	121	Input	AJ21	3.3V	LVC MOS33
Video Data 1 Luma[3]	123	Input	AK21	3.3V	LVC MOS33
Video Data 1 Luma[4]	125	Input	AF23	3.3V	LVC MOS33

Video Data 1 Luma[5]	127	Input	AF24	3.3V	LVC MOS33
Video Data 1 Luma[6]	92	Input	AJ23	3.3V	LVC MOS33
Video Data 1 Luma[7]	94	Input	AJ24	3.3V	LVC MOS33
Video Data 1 Luma[8]	96	Input	AG24	3.3V	LVC MOS33
Video Data 1 Luma[9]	98	Input	AG25	3.3V	LVC MOS33
Video Data 2 Luma[0]	77	Input	AJ16	3.3V	LVC MOS33
Video Data 2 Luma[1]	79	Input	AK16	3.3V	LVC MOS33
Video Data 2 Luma[2]	81	Input	AH17	3.3V	LVC MOS33
Video Data 2 Luma[3]	83	Input	AH16	3.3V	LVC MOS33
Video Data 2 Luma[4]	85	Input	AH18	3.3V	LVC MOS33
Video Data 2 Luma[5]	87	Input	AJ18	3.3V	LVC MOS33
Video Data 2 Luma[6]	78	Input	AF13	3.3V	LVC MOS33
Video Data 2 Luma[7]	82	Input	AG15	3.3V	LVC MOS33
Video Data 2 Luma[8]	84	Input	AG17	3.3V	LVC MOS33
Video Data 2 Luma[9]	86	Input	AG16	3.3V	LVC MOS33
Video Data 3 Luma[0]	107	Input	AH21	3.3V	LVC MOS33
Video Data 3 Luma[1]	122	Input	AH29	3.3V	LVC MOS33
Video Data 3 Luma[2]	115	Input	AE22	3.3V	LVC MOS33
Video Data 3 Luma[3]	146	Input	AF28	3.3V	LVC MOS33
Video Data 3 Luma[4]	148	Input	AF29	3.3V	LVC MOS33
Video Data 3 Luma[5]	150	Input	AG29	3.3V	LVC MOS33
Video Data 3 Luma[6]	100	Input	AH23	3.3V	LVC MOS33
Video Data 3 Luma[7]	102	Input	AH24	3.3V	LVC MOS33
Video Data 3 Luma[8]	104	Input	AJ25	3.3V	LVC MOS33
Video Data 3 Luma[9]	106	Input	AK25	3.3V	LVC MOS33
Video Data 0 Chroma[0]	143	Input	T29	1.5V	LVC MOS15
Video Data 0 Chroma[1]	145	Input	U29	1.5V	LVC MOS15
Video Data 0 Chroma[2]	147	Input	R28	1.5V	LVC MOS15
Video Data 0 Chroma[3]	149	Input	T28	1.5V	LVC MOS15
Video Data 0 Chroma[4]	151	Input	P30	1.5V	LVC MOS15
Video Data 0 Chroma[5]	153	Input	R30	1.5V	LVC MOS15
Video Data 0 Chroma[6]	155	Input	N29	1.5V	LVC MOS15
Video Data 0 Chroma[7]	157	Input	P29	1.5V	LVC MOS15
Video Data 0 Chroma[8]	159	Input	N28	1.5V	LVC MOS15
Video Data 0 Chroma[9]	161	Input	P28	1.5V	LVC MOS15
Video Data 1 Chroma[0]	89	Input	AK17	3.3V	LVC MOS33
Video Data 1 Chroma[1]	91	Input	AK18	3.3V	LVC MOS33
Video Data 1 Chroma[2]	93	Input	AF19	3.3V	LVC MOS33
Video Data 1 Chroma[3]	95	Input	AG19	3.3V	LVC MOS33
Video Data 1 Chroma[4]	97	Input	AH19	3.3V	LVC MOS33
Video Data 1 Chroma[5]	99	Input	AJ19	3.3V	LVC MOS33
Video Data 1 Chroma[6]	101	Input	AF20	3.3V	LVC MOS33
Video Data 1 Chroma[7]	103	Input	AG20	3.3V	LVC MOS33
Video Data 1 Chroma[8]	109	Input	AJ20	3.3V	LVC MOS33
Video Data 1 Chroma[9]	111	Input	AK20	3.3V	LVC MOS33
Video Data 2 Chroma[0]	38	Input	AE12	3.3V	LVC MOS33
Video Data 2 Chroma[1]	40	Input	AF12	3.3V	LVC MOS33
Video Data 2 Chroma[2]	50	Input	AG12	3.3V	LVC MOS33

Video Data 2 Chroma[3]	52	Input	AH12	3.3V	LVC MOS33
Video Data 2 Chroma[4]	54	Input	AH14	3.3V	LVC MOS33
Video Data 2 Chroma[5]	56	Input	AH13	3.3V	LVC MOS33
Video Data 2 Chroma[6]	58	Input	AJ14	3.3V	LVC MOS33
Video Data 2 Chroma[7]	60	Input	AJ13	3.3V	LVC MOS33
Video Data 2 Chroma[8]	59	Input	AK13	3.3V	LVC MOS33
Video Data 2 Chroma[9]	61	Input	AK12	3.3V	LVC MOS33
Video Data 3 Chroma[0]	108	Input	AJ26	3.3V	LVC MOS33
Video Data 3 Chroma[1]	110	Input	AK26	3.3V	LVC MOS33
Video Data 3 Chroma[2]	112	Input	AH26	3.3V	LVC MOS33
Video Data 3 Chroma[3]	114	Input	AH27	3.3V	LVC MOS33
Video Data 3 Chroma[4]	136	Input	AK27	3.3V	LVC MOS33
Video Data 3 Chroma[5]	138	Input	AK28	3.3V	LVC MOS33
Video Data 3 Chroma[6]	139	Input	AJ28	3.3V	LVC MOS33
Video Data 3 Chroma[7]	141	Input	AJ29	3.3V	LVC MOS33
Video Data 3 Chroma[8]	140	Input	AJ30	3.3V	LVC MOS33
Video Data 3 Chroma[9]	142	Input	AK30	3.3V	LVC MOS33
SPDIF Audio	27	Input	Y20	1.5V	LVC MOS15
Transport Stream Buffer	29	Input	AA20	1.5V	LVC MOS15
Transport Stream Clock	31	Output	AA18	1.5V	LVC MOS15
Transport Stream Data	33	Output	AA19	1.5V	LVC MOS15
Transport Stream Data	152	Output	AF30	3.3V	LVC MOS33
Transport Stream Data	154	Output	AG30	3.3V	LVC MOS33
Transport Stream Data	158	Output	AE30	3.3V	LVC MOS33
Transport Stream Data	160	Output	AB29	3.3V	LVC MOS33
Transport Stream Data	162	Output	AB30	3.3V	LVC MOS33
Transport Stream Data	164	Output	AA27	3.3V	LVC MOS33
Transport Stream Data	166	Output	AA28	3.3V	LVC MOS33
Transport Stream Data	120	Output	AH28	3.3V	LVC MOS33
Uart_tx	90	Output	AK15	3.3V	LVC MOS33
Uart_rx	88	Input	AJ15	3.3V	LVC MOS33

## 6.2 Signal Formats

### 6.2.1 Clock Signals (Input)

The 4k@30 encoder has 4 input clocks, **Video Clock 0** (pin #63), **Video Clock 1** (pin #80), **Video Clock 2** (pin #144), and **Video Clock 3** (pin #105). These clocks match the four of 3G SDI inputs for one 4k@30 video. The clock rate is 74.25 MHz, and the video data are sampled at dual data rate, at both the rising and falling edges of the clock. However, if one 4k input is used on the carrier board, such as HDMI 1.4/2.0 or 6/12G SDI, only **Video Clock 0** is needed which is also 74.25 MHz, with dual data rate as well.

### 6.2.2 Video Data Signals (Input)

The input to the encoder module is raw video data in YUV format (4:2:2 or 4:2:0), with 40 input lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma, and, 40 input lines: **Video Data 0 Chroma[0]** to **Video Data 3**

**Chroma[9]**, for the Chroma. The precision is either 8 bits or 10 bits. For 8-bit precision, the Most Significant Luma and Chroma pins (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization if embedded SAV/EAV are not used. The video clocks (refer to Section 6.2.1) provide the timing for the parallel input of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync** signals. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Video Display Enable** signal at high, when active pixels are being sent out.

The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section 6.2.1.

### 6.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

### 6.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**, along with the Transport Stream output data clock **Transport Stream Clock** (pin # 31). The frequency of the Transport Stream Data clock is 27MHz.

**Transport Stream Buffer Ready** (pin # 29) and **Transport Stream Data Valid** (pin # 33) are the signals to inform the user side to take over the signals.

### 6.2.5 Encoder Control Signals (Input and Output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the encoder. **Uart\_rx** receives the command from an external control device. **Uart\_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Encoder API User Manual](#) for more details.

An external reset **PS Soft Reset\_B** (pin # 156) is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

## 6.3 Power Rails of SoM-X-Z7045

Refer to Appendix-B for the pins of power and ground on the edge connector of the SoM-X-Z7045 module. The power rails are: 1.0V, 1.2V, 1.3V, 1.5V, 2.5V, and 3.3V.

## 6.4 Power Requirement and Supply Current

The total power, at operation, required by a given encoder module ranges from 3 to 6 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-9 lists the power estimations for PCB designs. It should be noted that the estimated total power showing in Table-9 is higher than the real power consumption of the module. It should also be noted that the power rails 1.8v and 2.0v are generated on the module, by using some of the input power rails. Carrier board PCB designers need not to consider these two rails.

**Table-9: Power estimation for the H.264 4k@30 encoder module**

Power Rail	Current (A)	Power (W)
3.3V	0.31	1.02
2.5V	0.84	2.09
1.5V	0.60	0.90
1.3V	0.19	0.24
1.2V	0.15	0.18
1.0V	3.60	3.60

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both the module and the carrier board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 19 of this document is for 4k resolution. The reference design provides not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: [sales@soctechologies.com](mailto:sales@soctechologies.com) for design licensing information.

## 6.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once all of the power rails are supplied, the module will start to boot. The booting time is less than 2 seconds.

(Left Empty here intentionally)



## 7. The H.264 4K@30 Decoder Modules

### 7.1 Pin Assignments and Pin Voltages

The modules for H.264 4K@30 resolution decoder use the SoM-X-Z7035 or Zynq-7045. This section details the pin assignment and pin voltages for H.264 4K@30 decoder modules based on the SoM-X-Z7045 hardware (the SoM-X-Z7035 is the same).

Table-10 shows the pin assignments and the pin voltages for H.264 4k decoder modules based on the SoM-X-Z7045.

The schematics of SoM-X-Z7045 edge connector are attached in Appendix-C of this document. Appendix-C shows the pin numbers for data, clock, control, and power, which are connected to the FPGA (Zynq-7035 or 7045, which are pin-compatible).

It should be noted that the 4K@30 encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

**Table-10: H.264 4K@30 Decoder Module (based on SoM-X-Z7045) Pin Assignment**

Description	SoM-X-Z7045 Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset_B	156	Input	B19	3.3V	LVC MOS33
Decoder Clock	76	Input	AE13	3.3V	LVC MOS33
Video Clock	105	Output	AG21	3.3V	LVC MOS33
Video Horizontal Sync	133	Output	W24	1.5V	LVC MOS15
Video Vertical Sync	113	Output	AF22	1.5V	LVC MOS33
Video Display Enable	67	Output	AD18	1.5V	LVC MOS15
Video Data 0 Luma[0]	135	Output	W25	1.5V	LVC MOS15
Video Data 0 Luma[1]	137	Output	W26	1.5V	LVC MOS15
Video Data 0 Luma[2]	116	Output	V27	1.5V	LVC MOS15
Video Data 0 Luma[3]	118	Output	W28	1.5V	LVC MOS15
Video Data 0 Luma[4]	124	Output	W29	1.5V	LVC MOS15
Video Data 0 Luma[5]	126	Output	W30	1.5V	LVC MOS15
Video Data 0 Luma[6]	128	Output	V28	1.5V	LVC MOS15
Video Data 0 Luma[7]	130	Output	V29	1.5V	LVC MOS15
Video Data 0 Luma[8]	132	Output	T30	1.5V	LVC MOS15
Video Data 0 Luma[9]	134	Output	U30	1.5V	LVC MOS15
Video Data 1 Luma[0]	117	Output	AG22	3.3v	LVC MOS33
Video Data 1 Luma[1]	119	Output	AH22	3.3v	LVC MOS33
Video Data 1 Luma[2]	121	Output	AJ21	3.3V	LVC MOS33
Video Data 1 Luma[3]	123	Output	AK21	3.3V	LVC MOS33
Video Data 1 Luma[4]	125	Output	AF23	3.3V	LVC MOS33
Video Data 1 Luma[5]	127	Output	AF24	3.3V	LVC MOS33

Video Data 1 Luma[6]	92	Output	AJ23	3.3V	LVC MOS33
Video Data 1 Luma[7]	94	Output	AJ24	3.3V	LVC MOS33
Video Data 1 Luma[8]	96	Output	AG24	3.3V	LVC MOS33
Video Data 1 Luma[9]	98	Output	AG25	3.3V	LVC MOS33
Video Data 2 Luma[0]	77	Output	AJ16	3.3V	LVC MOS33
Video Data 2 Luma[1]	79	Output	AK16	3.3V	LVC MOS33
Video Data 2 Luma[2]	81	Output	AH17	3.3V	LVC MOS33
Video Data 2 Luma[3]	83	Output	AH16	3.3V	LVC MOS33
Video Data 2 Luma[4]	85	Output	AH18	3.3V	LVC MOS33
Video Data 2 Luma[5]	87	Output	AJ18	3.3V	LVC MOS33
Video Data 2 Luma[6]	78	Output	AF13	3.3V	LVC MOS33
Video Data 2 Luma[7]	82	Output	AG15	3.3V	LVC MOS33
Video Data 2 Luma[8]	84	Output	AG17	3.3V	LVC MOS33
Video Data 2 Luma[9]	86	Output	AG16	3.3V	LVC MOS33
Video Data 3 Luma[0]	107	Output	AH21	3.3V	LVC MOS33
Video Data 3 Luma[1]	122	Output	AH29	3.3V	LVC MOS33
Video Data 3 Luma[2]	115	Output	AE22	3.3V	LVC MOS33
Video Data 3 Luma[3]	146	Output	AF28	3.3V	LVC MOS33
Video Data 3 Luma[4]	148	Output	AF29	3.3V	LVC MOS33
Video Data 3 Luma[5]	150	Output	AG29	3.3V	LVC MOS33
Video Data 3 Luma[6]	100	Output	AH23	3.3V	LVC MOS33
Video Data 3 Luma[7]	102	Output	AH24	3.3V	LVC MOS33
Video Data 3 Luma[8]	104	Output	AJ25	3.3V	LVC MOS33
Video Data 3 Luma[9]	106	Output	AK25	3.3V	LVC MOS33
Video Data 0 Chroma[0]	143	Output	T29	1.5V	LVC MOS15
Video Data 0 Chroma[1]	145	Output	U29	1.5V	LVC MOS15
Video Data 0 Chroma[2]	147	Output	R28	1.5V	LVC MOS15
Video Data 0 Chroma[3]	149	Output	T28	1.5V	LVC MOS15
Video Data 0 Chroma[4]	151	Output	P30	1.5V	LVC MOS15
Video Data 0 Chroma[5]	153	Output	R30	1.5V	LVC MOS15
Video Data 0 Chroma[6]	155	Output	N29	1.5V	LVC MOS15
Video Data 0 Chroma[7]	157	Output	P29	1.5V	LVC MOS15
Video Data 0 Chroma[8]	159	Output	N28	1.5V	LVC MOS15
Video Data 0 Chroma[9]	161	Output	P28	1.5v	LVC MOS15
Video Data 1 Chroma[0]	89	Output	AK17	3.3V	LVC MOS33
Video Data 1 Chroma[1]	91	Output	AK18	3.3V	LVC MOS33
Video Data 1 Chroma[2]	93	Output	AF19	3.3V	LVC MOS33
Video Data 1 Chroma[3]	95	Output	AG19	3.3V	LVC MOS33
Video Data 1 Chroma[4]	97	Output	AH19	3.3V	LVC MOS33
Video Data 1 Chroma[5]	99	Output	AJ19	3.3V	LVC MOS33
Video Data 1 Chroma[6]	101	Output	AF20	3.3V	LVC MOS33
Video Data 1 Chroma[7]	103	Output	AG20	3.3V	LVC MOS33
Video Data 1 Chroma[8]	109	Output	AJ20	3.3V	LVC MOS33

Video Data 1 Chroma[9]	111	Output	AK20	3.3V	LVC MOS33
Video Data 2 Chroma[0]	38	Output	AE12	3.3V	LVC MOS33
Video Data 2 Chroma[1]	40	Output	AF12	3.3V	LVC MOS33
Video Data 2 Chroma[2]	50	Output	AG12	3.3V	LVC MOS33
Video Data 2 Chroma[3]	52	Output	AH12	3.3V	LVC MOS33
Video Data 2 Chroma[4]	54	Output	AH14	3.3V	LVC MOS33
Video Data 2 Chroma[5]	56	Output	AH13	3.3V	LVC MOS33
Video Data 2 Chroma[6]	58	Output	AJ14	3.3V	LVC MOS33
Video Data 2 Chroma[7]	60	Output	AJ13	3.3V	LVC MOS33
Video Data 2 Chroma[8]	59	Output	AK13	3.3V	LVC MOS33
Video Data 2 Chroma[9]	61	Output	AK12	3.3V	LVC MOS33
Video Data 3 Chroma[0]	108	Output	AJ26	3.3V	LVC MOS33
Video Data 3 Chroma[1]	110	Output	AK26	3.3V	LVC MOS33
Video Data 3 Chroma[2]	112	Output	AH26	3.3V	LVC MOS33
Video Data 3 Chroma[3]	114	Output	AH27	3.3V	LVC MOS33
Video Data 3 Chroma[4]	136	Output	AK27	3.3V	LVC MOS33
Video Data 3 Chroma[5]	138	Output	AK28	3.3V	LVC MOS33
Video Data 3 Chroma[6]	139	Output	AJ28	3.3V	LVC MOS33
Video Data 3 Chroma[7]	141	Output	AJ29	3.3V	LVC MOS33
Video Data 3 Chroma[8]	140	Output	AJ30	3.3V	LVC MOS33
Video Data 3 Chroma[9]	142	Output	AK30	3.3V	LVC MOS33
SPDIF Audio	27	Output	Y20	1.5V	LVC MOS15
Transport Stream Clock	31	Input	AA18	1.5V	LVC MOS15
Transport Stream Data Valid	33	input	AA19	1.5V	LVC MOS15
Transport Stream Data [0]	152	input	AF30	3.3V	LVC MOS33
Transport Stream Data [1]	154	input	AG30	3.3V	LVC MOS33
Transport Stream Data [2]	158	input	AE30	3.3V	LVC MOS33
Transport Stream Data [3]	160	input	AB29	3.3V	LVC MOS33
Transport Stream Data [4]	162	input	AB30	3.3V	LVC MOS33
Transport Stream Data [5]	164	input	AA27	3.3V	LVC MOS33
Transport Stream Data [6]	166	input	AA28	3.3V	LVC MOS33
Transport Stream Data [7]	120	input	AH28	3.3V	LVC MOS33
Uart_tx	90	Output	AK15	3.3V	LVC MOS33
Uart_rx	88	Input	AJ15	3.3V	LVC MOS33

## 7.2 Signal Formats

### 7.2.1 Video Clock Signal (Output)

The Decoder Clock signal is an input clock for driving the decoder engine. When an SDI port on the carrier board is used to send out the decoded video data, the SDI clock can be connected to the Decoder Clock. This will automatically synchronize the decoder outputs with the SDI interface. The SDI clock frequency is 74.25MHz, for 4K@30.

The **Video Clock** signal (pin # 105) is the clock signal that provides the timing for the parallel luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync** signals. The default is 74.25 MHz for 4K@30.

### 7.2.2 Video Data Signals (Output)

The output of the H.264 4k@30 decoder module is the decoded video data in YUV format (4:2:2 or 4:2:0), with 40 output lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma, and, 40 lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision can be either 8-bit precision or 10-bit precision. For 8-bit precision, the Most Significant Bits of luma and chroma output lines (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

### 7.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

### 7.2.4 Decoder Control Signals (Input and output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the decoder. **Uart\_rx** receives the command from an external control device. **Uart\_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Decoder API User Manual](#) for details.

## 7.3 Power Rails of SoM-X-Z7045

The power rails for H.264 4K@30 decoder are the same as the H.264 4k@30 encoder. Refer to Appendix-C for the pins of power and ground on the edge connector of the SoM-X-Z7045 module.

## 7.4 Power Requirement and Supply Current

The total power, at operation, required by a given encoder module ranges from 3 to 5 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-11 lists the power estimations for PCB designs. It should be noted that the power rails 1.8v and 2.0v are generated on the module using the input power rails. PCB designers for the carrier boards do not need to consider these two rails.

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards. The VTR-4000C, discussed in Section 19 of this document, is for 4k resolution. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for further details.

**Table-11: Power estimation for the H.264 4k@30 decoder module**

Power Rail	Current (A)	Power (W)
3.3V	0.31	1.02
2.5V	0.84	2.09
1.5V	0.60	0.90
1.3V	0.19	0.24
1.2V	0.15	0.18
1.0V	3.60	3.60

## 7.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once all of the power rails are supplied, the module will start to boot. The booting time is less than 2 seconds.

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## 8. The H.264 4k@60 Encoder Modules

### 8.1 Pin Assignments and Pin Voltages

The SoM-I-SX660 is used for the 4K@60 resolution encoder module. Table-10 lists the pin assignments and the pin voltages for the 4K@60 encoder modules based on the SoM-I-SX660.

The schematics of SoM-I-SX660 edge connector are attached in Appendix-D of this document, which shows the pin numbers for data, clock, control, and power.

Table-12 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Arria-10 datasheet provides further information regarding the properties of these pins, and can be used as a reference.

**Table-12: 4K@60 Encoder Module (based on SoM-I-SX660) Pin Assignment and Pin Voltages**

Description	Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
Reset In	19	Input	G18	3.3v	LVC MOS33
Video Clock 0	105	Input	AM15	3.3v	LVC MOS33
Video Clock 1	107	Input	AL15	3.3v	LVC MOS33
Video Clock 2	113	Input	E18	3.3v	LVC MOS33
Video Clock 3	115	Input	E17	3.3v	LVC MOS33
Video Data 0 Luma[0]	54	Input	AF19	3.3v	LVC MOS33
Video Data 0 Luma[1]	56	Input	AE19	3.3v	LVC MOS33
Video Data 0 Luma[2]	59	Input	AD19	3.3v	LVC MOS33
Video Data 0 Luma[3]	61	Input	AE18	3.3v	LVC MOS33
Video Data 0 Luma[4]	77	Input	AF18	3.3v	LVC MOS33
Video Data 0 Luma[5]	79	Input	AG18	3.3v	LVC MOS33
Video Data 0 Luma[6]	85	Input	AC17	3.3v	LVC MOS33
Video Data 0 Luma[7]	87	Input	AD17	3.3v	LVC MOS33
Video Data 0 Luma[8]	88	Input	AE16	3.3v	LVC MOS33
Video Data 0 Luma[9]	90	Input	AE17	3.3v	LVC MOS33
Video Data 1 Luma[0]	80	Input	AP16	3.3v	LVC MOS33
Video Data 1 Luma[1]	82	Input	AP17	3.3v	LVC MOS33
Video Data 1 Luma[2]	104	Input	AL13	3.3v	LVC MOS33
Video Data 1 Luma[3]	106	Input	AK13	3.3v	LVC MOS33
Video Data 1 Luma[4]	109	Input	AN15	3.3v	LVC MOS33
Video Data 1 Luma[5]	111	Input	AP15	3.3v	LVC MOS33
Video Data 1 Luma[6]	117	Input	AN13	3.3v	LVC MOS33
Video Data 1 Luma[7]	119	Input	AM13	3.3v	LVC MOS33
Video Data 1 Luma[8]	121	Input	AN14	3.3v	LVC MOS33
Video Data 1 Luma[9]	123	Input	AP14	3.3v	LVC MOS33
Video Data 2 Luma[0]	139	Input	F19	3.3v	LVC MOS33
Video Data 2 Luma[1]	140	Input	G20	3.3v	LVC MOS33
Video Data 2 Luma[2]	141	Input	E19	3.3v	LVC MOS33
Video Data 2 Luma[3]	142	Input	F20	3.3v	LVC MOS33

Video Data 2 Luma[4]	144	Input	K21	3.3v	LVC MOS33
Video Data 2 Luma[5]	146	Input	J21	3.3v	LVC MOS33
Video Data 2 Luma[6]	148	Input	K19	3.3v	LVC MOS33
Video Data 2 Luma[7]	150	Input	L19	3.3v	LVC MOS33
Video Data 2 Luma[8]	169	Input	F18	3.3v	LVC MOS33
Video Data 2 Luma[9]	170	Input	G21	3.3v	LVC MOS33
Video Data 3 Luma[0]	69	Input	N3	1.5v	LVC MOS15
Video Data 3 Luma[1]	131	Input	M6	1.5v	LVC MOS15
Video Data 3 Luma[2]	133	Input	M7	1.5v	LVC MOS15
Video Data 3 Luma[3]	143	Input	J4	1.5v	LVC MOS15
Video Data 3 Luma[4]	145	Input	J5	1.5v	LVC MOS15
Video Data 3 Luma[5]	147	Input	N4	1.5v	LVC MOS15
Video Data 3 Luma[6]	149	Input	N5	1.5v	LVC MOS15
Video Data 3 Luma[7]	153	Input	L5	1.5v	LVC MOS15
Video Data 3 Luma[8]	155	Input	L4	1.5v	LVC MOS15
Video Data 3 Luma[9]	157	Input	K4	1.5v	LVC MOS15
Video Data 0 Chroma[0]	50	Input	AM18	3.3v	LVC MOS33
Video Data 0 Chroma[1]	52	Input	AN18	3.3v	LVC MOS33
Video Data 0 Chroma[2]	58	Input	AK18	3.3v	LVC MOS33
Video Data 0 Chroma[3]	60	Input	AL18	3.3v	LVC MOS33
Video Data 0 Chroma[4]	76	Input	AM17	3.3v	LVC MOS33
Video Data 0 Chroma[5]	78	Input	AN17	3.3v	LVC MOS33
Video Data 0 Chroma[6]	96	Input	AL16	3.3v	LVC MOS33
Video Data 0 Chroma[7]	98	Input	AM16	3.3v	LVC MOS33
Video Data 0 Chroma[8]	101	Input	AL14	3.3v	LVC MOS33
Video Data 0 Chroma[9]	103	Input	AK14	3.3v	LVC MOS33
Video Data 1 Chroma[0]	86	Input	AH17	3.3v	LVC MOS33
Video Data 1 Chroma[1]	92	Input	AG16	3.3v	LVC MOS33
Video Data 1 Chroma[2]	81	Input	AJ17	3.3v	LVC MOS33
Video Data 1 Chroma[3]	83	Input	AK17	3.3v	LVC MOS33
Video Data 1 Chroma[4]	84	Input	AG17	3.3v	LVC MOS33
Video Data 1 Chroma[5]	89	Input	AJ16	3.3v	LVC MOS33
Video Data 1 Chroma[6]	91	Input	AK16	3.3v	LVC MOS33
Video Data 1 Chroma[7]	97	Input	AJ15	3.3v	LVC MOS33
Video Data 1 Chroma[8]	99	Input	AH15	3.3v	LVC MOS33
Video Data 1 Chroma[9]	100	Input	AJ14	3.3v	LVC MOS33
Video Data 2 Chroma[0]	93	Input	B22	3.3v	LVC MOS33
Video Data 2 Chroma[1]	95	Input	A21	3.3v	LVC MOS33
Video Data 2 Chroma[2]	108	Input	B21	3.3v	LVC MOS33
Video Data 2 Chroma[3]	110	Input	B20	3.3v	LVC MOS33
Video Data 2 Chroma[4]	112	Input	C20	3.3v	LVC MOS33
Video Data 2 Chroma[5]	114	Input	D20	3.3v	LVC MOS33
Video Data 2 Chroma[6]	120	Input	E21	3.3v	LVC MOS33
Video Data 2 Chroma[7]	122	Input	D21	3.3v	LVC MOS33
Video Data 2 Chroma[8]	136	Input	D22	3.3v	LVC MOS33
Video Data 2 Chroma[9]	138	Input	C22	3.3v	LVC MOS33
Video Data 3 Chroma[0]	116	Input	N9	1.5v	LVC MOS15
Video Data 3 Chroma[1]	118	Input	P9	1.5v	LVC MOS15

Video Data 3 Chroma[2]	124	Input	R8	1.5v	LVC MOS15
Video Data 3 Chroma[3]	126	Input	R7	1.5v	LVC MOS15
Video Data 3 Chroma[4]	128	Input	N8	1.5v	LVC MOS15
Video Data 3 Chroma[5]	130	Input	M8	1.5v	LVC MOS15
Video Data 3 Chroma[6]	132	Input	K7	1.5v	LVC MOS15
Video Data 3 Chroma[7]	134	Input	L8	1.5v	LVC MOS15
Video Data 3 Chroma[8]	135	Input	N7	1.5v	LVC MOS15
Video Data 3 Chroma[9]	137	Input	P7	1.5v	LVC MOS15
SPDIF Audio	174	Input	H20	3.3v	LVC MOS33
Transport Stream Buffer	29	Input	L1	1.5v	LVC MOS15
Transport Stream Clock	31	Output	K1	1.5v	LVC MOS15
Transport Stream Data	33	Output	K2	1.5v	LVC MOS15
Transport Stream Data [0]	46	Output	J1	1.5v	LVC MOS15
Transport Stream Data [1]	48	Output	J2	1.5v	LVC MOS15
Transport Stream Data [2]	63	Output	L3	1.5v	LVC MOS15
Transport Stream Data [3]	65	Output	K3	1.5v	LVC MOS15
Uart_tx	163	Output	H17	3.3v	LVC MOS33
Uart_rx	164	Input	J17	3.3v	LVC MOS33

## 8.2 Signal Formats

### 8.2.1 Clock Signals (Input)

The 4k@60 encoder has 4 input clocks, **Video Clock 0** (pin # 105), **Video Clock 1** (pin # 107), **Video Clock 2** (pin # 113), and **Video Clock 3** (pin # 115). These clocks match the four of 3G SDI inputs for one 4k@60 video. The clock rate is 148.5MHz, and the video data are sampled at dual data rate, at both the rising and falling edges of the clock. However, if one 4k input is used on the carrier board, such as HDMI 2.0 or 12G SDI, only **Video Clock 0** is needed which takes the input video clock is 148.5 MHz for 4k@60.

### 8.2.2 Video Data Signals (Input)

The input to the encoder module is raw video data in YUV format (4:2:2 or 4:2:0), with 40 input lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma, and, 40 input lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision is either 8 bits or 10 bits. For 8-bit precision, the Most Significant Luma and Chroma pins (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

The video data are sampled at both the rising and falling edges of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **8.2.1**.

### 8.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.



### 8.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 4 Dual data rate parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[4]**, along with the Transport Stream output data clock **Transport Stream Clock** (pin # 31). The frequency of the Transport Stream Data clock is 27MHz.

**Transport Stream Buffer Ready** (pin # 28) and **Transport Stream Data Valid** (pin # 33) are the signals to inform the user side to take over the signals.

### 8.2.5 Encoder Control Signals (Input and Output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the encoder. **Uart\_rx** receives the command from an external control device. **Uart\_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Encoder API User Manual](#) for more details.

An external reset **PS Soft Reset\_B** (pin # 156) is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

## 8.3 Power Rails of SoM-I-SX660

Refer to Appendix-D for the pins of power and ground on the edge connector of the SoM-I-SX660 module. The power rails are: 1.0V, 1.2V, 1.3V, 1.5V, 2.5V, and 3.3V. However, only the 3.3V and 2.5V power supplies are required. The rest of the power rails are not used, which should be ignored.

## 8.4 Power Requirement and Supply Current

The SoM-I-SX660 requires only two power rails to be supplied to the module from the carrier board, which are 3.3V and 2.5V. All the rest of the voltages are created on the module. Table-13 provide the currents required for the two power rails, which can be used for all 4K@60 encoders and decoders.

**Table-13: Power estimation for the H.264 4k@60 encoder module**

Power Rail	Current (A)	Power (W)
3.3V	3.2	10.5
2.5V	1.7	4.2

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both the module and the carrier board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 19 of this document is for 4k resolution. The reference design provides not

only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for design licensing information.

## 8.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once all of the power rails are supplied, the module will start to boot. The booting time is less than 2 seconds.

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## 9. The H.264 4K@60 Decoder Modules

### 9.1 Pin Assignments and Pin Voltages

The modules for H.264 4K@60 resolution decoder use the SoM-I-SX660 as well. This section details the pin assignment and pin voltages for H.264 4K@60 decoder modules based on the SoM-I-SX660 hardware.

Table-14 shows the pin assignments and the pin voltages for H.264 4k@60 decoder modules based on the SoM-I-SX660.

The schematics of SoM-I-SX660 edge connector are attached in Appendix-D of this document. Appendix-D shows the pin numbers for data, clock, control, and power, which are connected to the FPGA.

It should be noted that the 4K@60 encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

**Table-14: H.264 4K@60 Decoder Module (based on SoM-I-SX660) Pin Assignment**

Description	Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
Reset In	19	Input	G18	3.3v	LVC MOS33
Video Clock 0	100	Output	AJ14	3.3v	LVC MOS33
Video Clock 1	89	Output	AJ16	3.3v	LVC MOS33
Video Clock 2	93	Output	B22	3.3v	LVC MOS33
Video Clock 3	135	Output	N7	1.5v	LVC MOS15
Video Data 0 Luma[0]	54	Output	AF19	3.3v	LVC MOS33
Video Data 0 Luma[1]	56	Output	AE19	3.3v	LVC MOS33
Video Data 0 Luma[2]	59	Output	AD19	3.3v	LVC MOS33
Video Data 0 Luma[3]	61	Output	AE18	3.3v	LVC MOS33
Video Data 0 Luma[4]	77	Output	AF18	3.3v	LVC MOS33
Video Data 0 Luma[5]	79	Output	AG18	3.3v	LVC MOS33
Video Data 0 Luma[6]	85	Output	AC17	3.3v	LVC MOS33
Video Data 0 Luma[7]	87	Output	AD17	3.3v	LVC MOS33
Video Data 0 Luma[8]	88	Output	AE16	3.3v	LVC MOS33
Video Data 0 Luma[9]	90	Output	AE17	3.3v	LVC MOS33
Video Data 1 Luma[0]	56	Output	AP16	3.3v	LVC MOS33
Video Data 1 Luma[1]	80	Output	AP17	3.3v	LVC MOS33
Video Data 1 Luma[2]	82	Output	AL13	3.3v	LVC MOS33
Video Data 1 Luma[3]	104	Output	AK13	3.3v	LVC MOS33
Video Data 1 Luma[4]	106	Output	AN15	3.3v	LVC MOS33
Video Data 1 Luma[5]	109	Output	AP15	3.3v	LVC MOS33
Video Data 1 Luma[6]	111	Output	AN13	3.3v	LVC MOS33
Video Data 1 Luma[7]	117	Output	AM13	3.3v	LVC MOS33
Video Data 1 Luma[8]	119	Output	AN14	3.3v	LVC MOS33
Video Data 1 Luma[9]	121	Output	AP14	3.3v	LVC MOS33

Video Data 2 Luma[0]	139	Output	F19	3.3v	LVC MOS33
Video Data 2 Luma[1]	140	Output	G20	3.3v	LVC MOS33
Video Data 2 Luma[2]	141	Output	E19	3.3v	LVC MOS33
Video Data 2 Luma[3]	142	Output	F20	3.3v	LVC MOS33
Video Data 2 Luma[4]	144	Output	K21	3.3v	LVC MOS33
Video Data 2 Luma[5]	146	Output	J21	3.3v	LVC MOS33
Video Data 2 Luma[6]	148	Output	K19	3.3v	LVC MOS33
Video Data 2 Luma[7]	150	Output	L19	3.3v	LVC MOS33
Video Data 2 Luma[8]	115	Output	E17	3.3v	LVC MOS33
Video Data 2 Luma[9]	167	Output	G21	3.3v	LVC MOS33
Video Data 3 Luma[0]	69	Output	N3	1.5v	LVC MOS15
Video Data 3 Luma[1]	153	Output	L5	1.5v	LVC MOS15
Video Data 3 Luma[2]	133	Output	L6	1.5v	LVC MOS15
Video Data 3 Luma[3]	143	Output	J4	1.5v	LVC MOS15
Video Data 3 Luma[4]	145	Output	J5	1.5v	LVC MOS15
Video Data 3 Luma[5]	147	Output	N4	1.5v	LVC MOS15
Video Data 3 Luma[6]	149	Output	N5	1.5v	LVC MOS15
Video Data 3 Luma[7]	159	Output	M2	1.5v	LVC MOS15
Video Data 3 Luma[8]	155	Output	L4	1.5v	LVC MOS15
Video Data 3 Luma[9]	157	Output	K4	1.5v	LVC MOS15
Video Data 0 Chroma[0]	50	Output	AM18	3.3v	LVC MOS33
Video Data 0 Chroma[1]	52	Output	AN18	3.3v	LVC MOS33
Video Data 0 Chroma[2]	58	Output	AK18	3.3v	LVC MOS33
Video Data 0 Chroma[3]	60	Output	AL18	3.3v	LVC MOS33
Video Data 0 Chroma[4]	76	Output	AM17	3.3v	LVC MOS33
Video Data 0 Chroma[5]	78	Output	AN17	3.3v	LVC MOS33
Video Data 0 Chroma[6]	96	Output	AL16	3.3v	LVC MOS33
Video Data 0 Chroma[7]	98	Output	AM16	3.3v	LVC MOS33
Video Data 0 Chroma[8]	101	Output	AL14	3.3v	LVC MOS33
Video Data 0 Chroma[9]	103	Output	AK14	3.3v	LVC MOS33
Video Data 1 Chroma[0]	38	Output	AH18	3.3v	LVC MOS33
Video Data 1 Chroma[1]	40	Output	AH19	3.3v	LVC MOS33
Video Data 1 Chroma[2]	81	Output	AJ17	3.3v	LVC MOS33
Video Data 1 Chroma[3]	83	Output	AK17	3.3v	LVC MOS33
Video Data 1 Chroma[4]	84	Output	AG17	3.3v	LVC MOS33
Video Data 1 Chroma[5]	86	Output	AH17	3.3v	LVC MOS33
Video Data 1 Chroma[6]	91	Output	AK16	3.3v	LVC MOS33
Video Data 1 Chroma[7]	97	Output	AJ15	3.3v	LVC MOS33
Video Data 1 Chroma[8]	99	Output	AH15	3.3v	LVC MOS33
Video Data 1 Chroma[9]	105	Output	AM15	3.3v	LVC MOS33
Video Data 2 Chroma[0]	113	Output	E18	3.3v	LVC MOS33
Video Data 2 Chroma[1]	95	Output	A21	3.3v	LVC MOS33
Video Data 2 Chroma[2]	108	Output	B21	3.3v	LVC MOS33
Video Data 2 Chroma[3]	110	Output	B20	3.3v	LVC MOS33
Video Data 2 Chroma[4]	112	Output	C20	3.3v	LVC MOS33
Video Data 2 Chroma[5]	114	Output	D20	3.3v	LVC MOS33
Video Data 2 Chroma[6]	120	Output	E21	3.3v	LVC MOS33
Video Data 2 Chroma[7]	122	Output	D21	3.3v	LVC MOS33

Video Data 2 Chroma[8]	136	Output	D22	3.3v	LVC MOS33
Video Data 2 Chroma[9]	138	Output	C22	3.3v	LVC MOS33
Video Data 3 Chroma[0]	116	Output	N9	1.5v	LVC MOS15
Video Data 3 Chroma[1]	118	Output	P9	1.5v	LVC MOS15
Video Data 3 Chroma[2]	124	Output	R8	1.5v	LVC MOS15
Video Data 3 Chroma[3]	126	Output	R7	1.5v	LVC MOS15
Video Data 3 Chroma[4]	67	Output	N2	1.5v	LVC MOS15
Video Data 3 Chroma[5]	130	Output	M8	1.5v	LVC MOS15
Video Data 3 Chroma[6]	132	Output	K7	1.5v	LVC MOS15
Video Data 3 Chroma[7]	134	Output	L8	1.5v	LVC MOS15
Video Data 3 Chroma[8]	128	Output	N8	1.5v	LVC MOS15
Video Data 3 Chroma[9]	137	Output	P7	1.5v	LVC MOS15
Video Out Mode	161	Output	M3	1.5v	LVC MOS15
Video Clock in	107	Input	AL15	1.5v	LVC MOS15
SPDIF Audio	174	Output	H20	3.3v	LVC MOS33
Transport Stream Ready	29	Output	L1	1.5v	LVC MOS15
Transport Stream Data	33	Input	K2	1.5v	LVC MOS15
Transport Stream Clock in	131	Input	K6	1.5v	LVC MOS15
Transport Stream Data [0]	46	Input	J1	1.5v	LVC MOS15
Transport Stream Data [1]	48	Input	J2	1.5v	LVC MOS15
Transport Stream Data [2]	63	Input	L3	1.5v	LVC MOS15
Transport Stream Data [3]	65	Input	K3	1.5v	LVC MOS15
Uart_tx	163	Output	H17	3.3v	LVC MOS33
Uart_rx	164	Input	J17	3.3v	LVC MOS33

## 9.2 Signal Formats

### 9.2.1 Video Clock Signal (Output)

The **Video Clock** signal (pin # 105) is the clock signal that provides the timing for the parallel luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync** signals. The default is 148.5MHz for 4K@60.

### 9.2.2 Video Data Signals (Output)

The output of the H.264 4k@30 decoder module is the decoded video data in YUV format (4:2:2 or 4:2:0), with 40 output lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma, and, 40 lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision can be either 8-bit precision or 10-bit precision. For 8-bit precision, the Most Significant Bits of luma and chroma output lines (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

### 9.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

#### 9.2.4 Decoder Control Signals (Input and output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the decoder. **Uart\_rx** receives the command from an external control device. **Uart\_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Decoder API User Manual](#) for details.

### 9.3 Power Rails of SoM-I-SX660

The power rails for H.264 4k@60 decoder module are the same as the H.264 4k@60 encoder. Refer to Appendix-C for the pins of power and ground on the edge connector of the SoM-I-SX660 module.

### 9.4 Power Requirement and Supply Current

The SoM-I-SX660 requires only two power rails to be supplied to the module from the carrier board, which are 3.3V and 2.5V. All the rest of the voltages are created on the module. Table-15 provides the currents required for the two power rails, which can be used for all 4K@60 encoders and decoders. Please note that Table-13 and Table-15 are identical, since the power supplies for the encoder and decoder models are the same.

**Table-15: Power estimation for the H.264 4k@60 decoder module**

Power Rail	Current (A)	Power (W)
3.3V	3.2	10.5
2.5V	1.7	4.2

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both the module and the carrier board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 19 of this document is for 4k resolution. The reference design provides not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for design licensing information.

### 9.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once the all of the power rails are supplied, the module will start to boot. The booting time is less than 2 seconds.

(Left Empty here intentionally)

## 10. The H.265 HD Encoder Modules

### 10.1 Pin Assignments and Pin Voltages

The SoM-X-Z7045 is used for H.265 HD (1080@30 or 1080@60) resolution encoder modules. It is noted that the H.265 HD encoder can use either the SoM-X-Z7045 or SoM-I-SX660. This Section provides the pin assignments and electrical properties for H.265 HD encoder module based on the SoM-X-Z7045. Table-16 lists the pin assignments and the pin voltages. Pin assignments for the H.265 HD encoder based on the SoM-I-SX660 are provided separately when needed.

The schematics of SoM-X-Z7045 edge connector are attached in Appendix-C of this document, which shows the pin numbers for data, clock, control, and power. It should be noted that the encoder module uses only some of the edge pins, and not all of the edge pins are used.

Table-16 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Zynq-7000 datasheet provides further information regarding the properties of these pins, and can be used as a reference for user PCB designs that uses the SoM-X-Z7045.

**Table 16: HD Encoder Module (based on SoM-X-Z7045) Pin Assignment and Pin Voltages**

Description	SoM-X-Z7045 Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset_B	156	Input	B19	3.3V	LVC MOS33
Video Clock	105	Input	AG21	3.3V	LVC MOS33
Video Horizontal Sync	133	Input	W24	1.5V	LVC MOS15
Video Vertical Sync	113	Input	AF22	3.3V	LVC MOS33
Video Display Enable	67	Input	AD18	1.5V	LVC MOS15
Video Data Luma[0]	107	Input	AH21	3.3V	LVC MOS33
Video Data Luma[1]	122	Input	AH29	3.3V	LVC MOS33
Video Data Luma[2]	115	Input	AE22	3.3V	LVC MOS33
Video Data Luma[3]	146	Input	AF28	3.3V	LVC MOS33
Video Data Luma[4]	148	Input	AF29	3.3V	LVC MOS33
Video Data Luma[5]	150	Input	AG29	3.3V	LVC MOS33
Video Data Luma[6]	100	Input	AH23	3.3V	LVC MOS33
Video Data Luma[7]	102	Input	AH24	3.3V	LVC MOS33
Video Data Luma[8]	104	Input	AJ25	3.3V	LVC MOS33
Video Data Luma[9]	106	Input	AK25	3.3V	LVC MOS33
Video Data Chroma[0]	108	Input	AJ26	3.3V	LVC MOS33
Video Data Chroma[1]	110	Input	AK26	3.3V	LVC MOS33
Video Data Chroma[2]	112	Input	AH26	3.3V	LVC MOS33
Video Data Chroma[3]	114	Input	AH27	3.3V	LVC MOS33
Video Data Chroma[4]	136	Input	AK27	3.3V	LVC MOS33
Video Data Chroma[5]	138	Input	AK28	3.3V	LVC MOS33
Video Data Chroma[6]	139	Input	AJ28	3.3V	LVC MOS33
Video Data Chroma[7]	141	Input	AJ29	3.3V	LVC MOS33
Video Data Chroma[8]	140	Input	AJ30	3.3V	LVC MOS33
Video Data Chroma[9]	142	Input	AK30	3.3V	LVC MOS33
SPDIF Audio	27	Input	Y20	1.5V	LVC MOS15
Transport Stream Buffer Ready	29	Input	AA20	1.5V	LVC MOS15

Transport Stream Clock	31	Output	AA18	1.5V	LVCMS15
Transport Stream Data Valid	33	Output	AA19	1.5V	LVCMS15
Transport Stream Data[0]	152	Output	AF30	3.3V	LVCMS33
Transport Stream Data[1]	154	Output	AG30	3.3V	LVCMS33
Transport Stream Data[2]	158	Output	AE30	3.3V	LVCMS33
Transport Stream Data[3]	160	Output	AB29	3.3V	LVCMS33
Transport Stream Data[4]	162	Output	AB30	3.3V	LVCMS33
Transport Stream Data[5]	164	Output	AA27	3.3V	LVCMS33
Transport Stream Data[6]	166	Output	AA28	3.3V	LVCMS33
Transport Stream Data[7]	120	Output	AH28	3.3V	LVCMS33
Uart_tx	90	Output	AK15	3.3V	LVCMS33
Uart_rx	88	Input	AJ15	3.3V	LVCMS33

## 10.2 Signal Formats

### 10.2.1 Video Clock Signal (Input)

The **Video Clock** signal (pin # 105) has two functions: (1) It is the clock for the input video data, and (2) it is the clock that drives the encoder engine.

The **Video Clock** signal usually comes from the video input interface chip, such as HDMI or SDI. It is the clock for the input video data. It is also used for driving the encoder engine. The frequency varies according to the resolution of the video input. The following are the clock frequencies for standard video resolutions.

4. 27MHz, for SD resolution
5. 74.25MHz, for 720@60 and 1080@30
6. 148.5MHz, for 1080@60

### 10.2.2 Video Data Signals (Input)

The input to the encoder module (H.264 or MPEG-2) is raw video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma; and, 10 input lines: **Video Data Chroma[0]** to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]**, **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization. A **Video Clock** (refer to Section 10.2.1 for the clock frequencies) is required, which provides the timing for the parallel input of luma, chroma, as well as for the **Video Horizontal Sync** and **Video Vertical Sync** signals. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Display Enable signal** at high, when active pixels are being sent out. The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section 10.2.1.



### 10.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

### 10.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**; along with the Transport Stream output data clock **Transport Stream Clock**. The frequency of the Transport Stream Data clock is 27MHz.

**Transport Stream Buffer Ready** and **Transport Stream Data Valid** are the signals to inform the user side to take over the signals.

### 10.2.5 Encoder Control Signals (Input and Output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the encoder. **Uart\_rx** receives the command from external control device. **Uart\_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Encoder API User Manual](#) for more details.

An external reset PS Soft Reset\_B (pin # 156) is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

## 10.3 Power Rails of SoM-X-Z45

Refer to Appendix-C for the pins of power and ground on the edge connector of the SoM-X-Z7045 module.

## 10.4 Power Requirement and Supply Current

The total power, at operation, required by a given encoder module ranges from 2 to 10 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-17 lists the power estimation, at 1080p@60 resolution, for PCB design purpose. It should be noted that the measured real power consumption is lower than the estimated power consumption, as the power estimation is for PCB design uses.

It should be noted that the power rails of 1.8v is generated on the module, using the 2.5v power input from the edge pin. PCB designers need only to design the 6 power rails listed in Table-17, as the 1.8v is generated on the module.

**Table-17: Power estimation for the encoder module (1080p@60 resolution)**

Power Rail	Current (A)	Power (W)
3.3V	0.37	1.22
2.5V	0.99	2.48
1.5V	1.25	1.87
1.3V	0.37	0.58
1.2V	0.75	0.90
1.0V	3.39	3.39

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 19 of this document. The reference designs provide not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for design licensing details.

## 10.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once all of the power rails are supplied, the module will start to boot. The booting time is less than 2 seconds.

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## 11. The H.265 HD Decoder Modules

### 11.1 Pin Assignments and Pin Voltages

The H.265 HD 1080@30 and 1080@60 decoders have the same pin assignment. The module for HD resolution decoding uses the SoM-X-Z7045. Also, pin assignments for the H.265 HD decoder based on the SoM-I-SX660 are provided separately when needed.

This section details the pin assignments and pin voltages for the H.265 HD decoder modules. Table-18 shows the pin assignments and the pin voltages.

The schematics of SoM-X-Z7045 edge connector are attached in Appendix-C of this document. Appendix-C shows the pin numbers for data, clock, control, and power, which are connected to the FPGA. It should be noted that the decoder module uses only some of the available edge pins that are connected to the FPGA (some of the pins are not used).

It should also be noted that the HD encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

**Table-18: HD Decoder Module (based on SoM-X-Z7045) Pin Assignment**

Description	SoM-X-Z7045 Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset_B	156	Input	B19	3.3V	LVCNOS33
Decoder Clock	80	Input	AB13	3.3V	LVCNOS33
Video Clock	105	Output	AG21	3.3V	LVCNOS33
Video Horizontal Sync	133	Output	W24	1.5V	LVCNOS15
Video Vertical Sync	113	Output	AF22	3.3V	LVCNOS33
Video Display Enable	67	Output	AD18	1.5V	LVCNOS15
Video Data Luma[0]	107	Output	AH21	3.3V	LVCNOS33
Video Data Luma[1]	122	Output	AH29	3.3V	LVCNOS33
Video Data Luma[2]	115	Output	AE22	3.3V	LVCNOS33
Video Data Luma[3]	146	Output	AF28	3.3V	LVCNOS33
Video Data Luma[4]	148	Output	AF29	3.3V	LVCNOS33
Video Data Luma[5]	150	Output	AG29	3.3V	LVCNOS33
Video Data Luma[6]	100	Output	AH23	3.3V	LVCNOS33
Video Data Luma[7]	102	Output	AH24	3.3V	LVCNOS33
Video Data Luma[8]	104	Output	AJ25	3.3V	LVCNOS33
Video Data Luma[9]	106	Output	AK25	3.3V	LVCNOS33
Video Data Chroma[0]	108	Output	AJ26	3.3V	LVCNOS33
Video Data Chroma[1]	110	Output	AK26	3.3V	LVCNOS33
Video Data Chroma[2]	112	Output	AH26	3.3V	LVCNOS33
Video Data Chroma[3]	114	Output	AH27	3.3V	LVCNOS33
Video Data Chroma[4]	136	Output	AK27	3.3V	LVCNOS33
Video Data Chroma[5]	138	Output	AK28	3.3V	LVCNOS33
Video Data Chroma[6]	139	Output	AJ28	3.3V	LVCNOS33
Video Data Chroma[7]	141	Output	AJ29	3.3V	LVCNOS33
Video Data Chroma[8]	140	Output	AJ30	3.3V	LVCNOS33
Video Data Chroma[9]	142	Output	AK30	3.3V	LVCNOS33

SPDIF Audio	27	Output	Y20	1.5V	LVC MOS15
Transport Stream Clock ( <b>27MHz</b> )	93	Input	AA18	1.5V	LVC MOS15
Transport Stream Data Valid	106	Input	AA19	1.5V	LVC MOS15
Transport Stream Data[0]	77	Input	AF30	3.3V	LVC MOS33
Transport Stream Data[1]	79	Input	AG30	3.3V	LVC MOS33
Transport Stream Data[2]	81	Input	AE30	3.3V	LVC MOS33
Transport Stream Data[3]	83	Input	AB29	3.3V	LVC MOS33
Transport Stream Data[4]	85	Input	AB30	3.3V	LVC MOS33
Transport Stream Data[5]	87	Input	AA27	3.3V	LVC MOS33
Transport Stream Data[6]	89	Input	AA28	3.3V	LVC MOS33
Transport Stream Data[7]	91	Input	AH28	3.3V	LVC MOS33
Uart_tx	90	Output	AK15	3.3V	LVC MOS33
Uart_rx	88	Input	AJ15	3.3V	LVC MOS33

## 11.2 Signal Formats

### 11.2.1 Clock Signals

When an SDI port on the carrier board is used to send out the decoded video data, the SDI clock should be connected to the Decoder Clock and Use Decoder Clock should be tied high. This will automatically synchronize the decoder outputs with the SDI interface. Internally generated clock is used if Use Decoder Clock is tied low.

The SDI clock frequencies are:

8. 27MHz, for SD resolution
9. 74.25MHz, for 720@60 and 1080@30
10. 148.5MHz, for 1080@60

The **Video Clock** signal (pin # 105) is the clock for the video data output by the decoder. The frequency of the **Video clock** is determined by the video resolution, which are:

11. 27MHz, for SD resolution
12. 74.25MHz, for 720@60 and 1080@30
13. 148.5MHz, for 1080@60.

### 11.2.2 Video Data Signals (Output)

The output of the HD decoder module (H.264 or MPEG-2) is the decoded video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma; and 10 lines, **Video Data Chroma[0]** to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]**, **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. A **Video Clock** (refer to Section 11.2.1 for the clock frequencies) is sent out, which provides the timing for the parallel inputs of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync** signals. The **Video Display Enable** signal (pin #150) is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

Output data are sampled at the rising edge of the clock. (The clock rates will correspond to the resolution and frame rate, as discussed in Section 11.2.1.)

### 11.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

### 11.2.4 TS Stream Signals (Input)

The input of the decoder module is an MPEG transport stream, which is sent into the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**. **Transport Stream Clock** (27MHz) is the clock for the **Transport Stream Data** lines. The **Transport Stream Data Valid** signal informs the decoder that the input is valid.

### 11.2.5 Decoder Control Signals (Input and Output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the decoder. **Uart\_rx** receives the command from an external control device. **Uart\_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Decoder API User Manual](#) for details.

## 11.3 Power Rails of SoM-X-Z7045

The power rails for the H.265 HD decoder module is the same as the ones for the H.265 HD encoder module. Refer to Appendix-C for the power and ground pins on the edge connector of the SoM-X-Z7045 module.

## 11.4 Power Requirement and Supply Current

The total power at operation required by a given decoder ranges from 3 to 8 Watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-19 lists the power estimation for each rail, for PCB design purpose. It should be noted that the estimated total power showing in Table-19 is higher than the real power consumption of the module, the power estimation in Table-19 is for PCB design purpose.

Again, the power rails of 1.8v are generated on the module, using the 2.5v power input from the edge pin. PCB designers need only to design the 6 power rails listed in Table-19.

**Table-19: Power estimation for the decoder module (1080p@60 resolution)**

Power Rail	Current (A)	Power (W)
3.3V	0.37	1.22
2.5V	0.99	2.48
1.5V	1.25	1.87
1.3V	0.37	0.58
1.2V	0.75	0.90
1.0V	3.39	3.39

Since the decoder module normally shares the power supplies with the carrier board (user PCB), the power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 19 of this document. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: [sales@soctechologies.com](mailto:sales@soctechologies.com) for further details.

## 11.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once all of the power rails are supplied, the module will start to boot. The booting time is less than 2 seconds.

(Left Empty here intentionally)

## 12. The H.265 4k@30 Encoder Modules

### Note:

**The “Pin Assignments and Pin Voltages” of H.265 4k@30 Encoder Module is identical to the “Pin Assignments and Pin Voltages” of H.264 4k@30 Encoder Module detailed in Section 6. However, Pin Assignments and Pin Voltages of H.265 4k@30 Encoder Module is provided here in this Section for completion.**

### 12.1 Pin Assignments and Pin Voltages

The H.265 4k@30 encoder uses the SoM-X-Z7045 module. The pin assignments are the same as the H.264 4k@30 encoder module.

Table-20 lists the pin assignments and the pin voltages for the H.265 4K@30 encoder modules based on the SoM-X-Z7045.

The schematics of SoM-X-Z7045 edge connector are attached in Appendix-C of this document, which shows the pin numbers for data, clock, control, and power.

Table-20 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Zynq-7000 datasheet provides further information regarding the properties of these pins, and can be used as a reference.

**Table-20: 4K@30 Encoder Module (based on SoM-X-Z7045) Pin Assignment and Pin Voltages**

Description	SoM-X-Z7045	Edge	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset B	156		Input	B19	3.3V	LVC MOS33
Video Clock 0	63		Input	AC18	1.5v	LVC MOS15
Video Clock 1	80		Input	AF15	3.3v	LVC MOS33
Video Clock 2	144		Input	AE28	3.3v	LVC MOS33
Video Clock 3	105		Input	AG21	3.3v	LVC MOS33
Video Horizontal Sync	133		Input	W24	1.5v	LVC MOS15
Video Vertical Sync	113		Input	AF22	3.3v	LVC MOS33
Video Display Enable	67		Input	AD18	1.5v	LVC MOS15
Video Data 0 Luma[0]	135		Input	W25	1.5v	LVC MOS15
Video Data 0 Luma[1]	137		Input	W26	1.5v	LVC MOS15
Video Data 0 Luma[2]	116		Input	V27	1.5v	LVC MOS15
Video Data 0 Luma[3]	118		Input	W28	1.5v	LVC MOS15
Video Data 0 Luma[4]	124		Input	W29	1.5v	LVC MOS15
Video Data 0 Luma[5]	126		Input	W30	1.5v	LVC MOS15
Video Data 0 Luma[6]	128		Input	V28	1.5v	LVC MOS15
Video Data 0 Luma[7]	130		Input	V29	1.5v	LVC MOS15
Video Data 0 Luma[8]	132		Input	T30	1.5v	LVC MOS15

Video Data 0 Luma[9]	134	Input	U30	1.5v	LVC MOS15
Video Data 1 Luma[0]	117	Input	AG22	3.3v	LVC MOS33
Video Data 1 Luma[1]	119	Input	AH22	3.3v	LVC MOS33
Video Data 1 Luma[2]	121	Input	AJ21	3.3v	LVC MOS33
Video Data 1 Luma[3]	123	Input	AK21	3.3v	LVC MOS33
Video Data 1 Luma[4]	125	Input	AF23	3.3v	LVC MOS33
Video Data 1 Luma[5]	127	Input	AF24	3.3v	LVC MOS33
Video Data 1 Luma[6]	92	Input	AJ23	3.3v	LVC MOS33
Video Data 1 Luma[7]	94	Input	AJ24	3.3v	LVC MOS33
Video Data 1 Luma[8]	96	Input	AG24	3.3v	LVC MOS33
Video Data 1 Luma[9]	98	Input	AG25	3.3v	LVC MOS33
Video Data 2 Luma[0]	77	Input	AJ16	3.3v	LVC MOS33
Video Data 2 Luma[1]	79	Input	AK16	3.3v	LVC MOS33
Video Data 2 Luma[2]	81	Input	AH17	3.3v	LVC MOS33
Video Data 2 Luma[3]	83	Input	AH16	3.3v	LVC MOS33
Video Data 2 Luma[4]	85	Input	AH18	3.3v	LVC MOS33
Video Data 2 Luma[5]	87	Input	AJ18	3.3v	LVC MOS33
Video Data 2 Luma[6]	78	Input	AF13	3.3v	LVC MOS33
Video Data 2 Luma[7]	82	Input	AG15	3.3v	LVC MOS33
Video Data 2 Luma[8]	84	Input	AG17	3.3v	LVC MOS33
Video Data 2 Luma[9]	86	Input	AG16	3.3v	LVC MOS33
Video Data 3 Luma[0]	107	Input	AH21	3.3v	LVC MOS33
Video Data 3 Luma[1]	122	Input	AH29	3.3v	LVC MOS33
Video Data 3 Luma[2]	115	Input	AE22	3.3v	LVC MOS33
Video Data 3 Luma[3]	146	Input	AF28	3.3v	LVC MOS33
Video Data 3 Luma[4]	148	Input	AF29	3.3v	LVC MOS33
Video Data 3 Luma[5]	150	Input	AG29	3.3v	LVC MOS33
Video Data 3 Luma[6]	100	Input	AH23	3.3v	LVC MOS33
Video Data 3 Luma[7]	102	Input	AH24	3.3v	LVC MOS33
Video Data 3 Luma[8]	104	Input	AJ25	3.3v	LVC MOS33
Video Data 3 Luma[9]	106	Input	AK25	3.3v	LVC MOS33
Video Data 0 Chroma[0]	143	Input	T29	1.5v	LVC MOS15
Video Data 0 Chroma[1]	145	Input	U29	1.5v	LVC MOS15
Video Data 0 Chroma[2]	147	Input	R28	1.5v	LVC MOS15
Video Data 0 Chroma[3]	149	Input	T28	1.5v	LVC MOS15
Video Data 0 Chroma[4]	151	Input	P30	1.5v	LVC MOS15
Video Data 0 Chroma[5]	153	Input	R30	1.5v	LVC MOS15
Video Data 0 Chroma[6]	155	Input	N29	1.5v	LVC MOS15
Video Data 0 Chroma[7]	157	Input	P29	1.5v	LVC MOS15
Video Data 0 Chroma[8]	159	Input	N28	1.5v	LVC MOS15
Video Data 0 Chroma[9]	161	Input	P28	1.5v	LVC MOS15
Video Data 1 Chroma[0]	89	Input	AK17	3.3v	LVC MOS33
Video Data 1 Chroma[1]	91	Input	AK18	3.3v	LVC MOS33
Video Data 1 Chroma[2]	93	Input	AF19	3.3v	LVC MOS33
Video Data 1 Chroma[3]	95	Input	AG19	3.3v	LVC MOS33
Video Data 1 Chroma[4]	97	Input	AH19	3.3v	LVC MOS33
Video Data 1 Chroma[5]	99	Input	AJ19	3.3v	LVC MOS33
Video Data 1 Chroma[6]	101	Input	AF20	3.3v	LVC MOS33



Video Data 1 Chroma[7]	103	Input	AG20	3.3v	LVC MOS33
Video Data 1 Chroma[8]	109	Input	AJ20	3.3v	LVC MOS33
Video Data 1 Chroma[9]	111	Input	AK20	3.3v	LVC MOS33
Video Data 2 Chroma[0]	38	Input	AE12	3.3v	LVC MOS33
Video Data 2 Chroma[1]	40	Input	AF12	3.3v	LVC MOS33
Video Data 2 Chroma[2]	50	Input	AG12	3.3v	LVC MOS33
Video Data 2 Chroma[3]	52	Input	AH12	3.3v	LVC MOS33
Video Data 2 Chroma[4]	54	Input	AH14	3.3v	LVC MOS33
Video Data 2 Chroma[5]	56	Input	AH13	3.3v	LVC MOS33
Video Data 2 Chroma[6]	58	Input	AJ14	3.3v	LVC MOS33
Video Data 2 Chroma[7]	60	Input	AJ13	3.3v	LVC MOS33
Video Data 2 Chroma[8]	59	Input	AK13	3.3v	LVC MOS33
Video Data 2 Chroma[9]	61	Input	AK12	3.3v	LVC MOS33
Video Data 3 Chroma[0]	108	Input	AJ26	3.3v	LVC MOS33
Video Data 3 Chroma[1]	110	Input	AK26	3.3v	LVC MOS33
Video Data 3 Chroma[2]	112	Input	AH26	3.3v	LVC MOS33
Video Data 3 Chroma[3]	114	Input	AH27	3.3v	LVC MOS33
Video Data 3 Chroma[4]	136	Input	AK27	3.3v	LVC MOS33
Video Data 3 Chroma[5]	138	Input	AK28	3.3v	LVC MOS33
Video Data 3 Chroma[6]	139	Input	AJ28	3.3v	LVC MOS33
Video Data 3 Chroma[7]	141	Input	AJ29	3.3v	LVC MOS33
Video Data 3 Chroma[8]	140	Input	AJ30	3.3v	LVC MOS33
Video Data 3 Chroma[9]	142	Input	AK30	3.3v	LVC MOS33
SPDIF Audio	27	Input	Y20	1.5v	LVC MOS15
Transport Stream Buffer Ready	29	Input	AA20	1.5v	LVC MOS15
Transport Stream Clock	31	Output	AA18	1.5v	LVC MOS15
Transport Stream Data Valid	33	Output	AA19	1.5v	LVC MOS15
Transport Stream Data [0]	152	Output	AF30	3.3v	LVC MOS33
Transport Stream Data [1]	154	Output	AG30	3.3v	LVC MOS33
Transport Stream Data [2]	158	Output	AE30	3.3v	LVC MOS33
Transport Stream Data [3]	160	Output	AB29	3.3v	LVC MOS33
Transport Stream Data [4]	162	Output	AB30	3.3v	LVC MOS33
Transport Stream Data [5]	164	Output	AA27	3.3v	LVC MOS33
Transport Stream Data [6]	166	Output	AA28	3.3v	LVC MOS33
Transport Stream Data [7]	120	Output	AH28	3.3v	LVC MOS33
Uart_tx	90	Output	AK15	3.3v	LVC MOS33
Uart_rx	88	Input	AJ15	3.3v	LVC MOS33

## 12.2 Signal Formats

### 12.2.1 Clock Signals (Input)

The 4k@30 encoder has 4 input clocks, **Video Clock 0** (pin #63), **Video Clock 1** (pin #80), **Video Clock 2** (pin #144), and **Video Clock 3** (pin #105). These clocks match the four of 3G SDI inputs for one 4k@30 video. The clock rate is 74.25 MHz, and the video data are sampled at dual data rate, at both the rising and falling edges of the clock.

However, if one 4k input is used on the carrier board, such as HDMI 1.4/2.0 or 6/12G SDI, only **Video Clock 0** is needed which is also 74.25 MHz, with dual data rate as well.

### 12.2.2 Video Data Signals (Input)

The input to the encoder module is raw video data in YUV format (4:2:2 or 4:2:0), with 40 input lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma; and, 40 input lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision is either 8 bits or 10 bits. For 8-bit precision, the Most Significant Luma and Chroma pins (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization if embedded SAV/EAV are not used. The video clocks (refer to Section 12.2.1) provide the timing for the parallel input of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync** signals. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Video Display Enable** signal at high, when active pixels are being sent out.

The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section 12.2.1.

### 12.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

### 12.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**, along with the Transport Stream output data clock **Transport Stream Clock** (pin # 31). The frequency of the Transport Stream Data clock is 27MHz.

**Transport Stream Buffer Ready** (pin # 29) and **Transport Stream Data Valid** (pin # 33) are the signals to inform the user side to take over the signals.

### 12.2.5 Encoder Control Signals (Input and Output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the encoder. **Uart\_rx** receives the command from external control device. **Uart\_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Encoder API User Manual](#) for more details.

An external reset **PS Soft Reset\_B** (pin # 156) is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

### 12.3 Power Rails of SoM-X-Z7045

Refer to Appendix-B for the pins of power and ground on the edge connector of the SoM-X-Z7045 module. The power rails are: 1.0V, 1.2V, 1.3V, 1.5V, 2.5V, and 3.3V.

### 12.4 Power Requirement and Supply Current

The total power, at operation, required by a given encoder module ranges from 3 to 6 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-21 lists the power estimations for each rail, at 4k@30 resolution, which can be for PCB design purpose. It should be noted that the estimated total power showing in Table-21 is higher than the real power consumption of the module, as it is for PCB design purposes. It should also be noted that the power rails 1.8v and 2.0v are generated on the module, by using some of the input power rails. Carrier board PCB designers need not to consider these two rails.

**Table-21: Power estimation for the H.265 4k@30 encoder module**

Power Rail	Current (A)	Power (W)
3.3V	0.50	1.63
2.5V	1.34	3.34
1.5V	0.96	1.44
1.3V	0.03	0.38
1.2V	0.24	0.29
1.0V	5.76	5.76

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both the module and the carrier board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 19 of this document is for 4k resolution. The reference design provides not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for design licensing information.

### 12.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once all of the power rails are supplied, the module will start to boot. The booting time is less than 2 seconds.

## 13. The H.265 4K@30 Decoder Modules

### Note:

The “Pin Assignments and Pin Voltages” of H.265 4k@30 Decoder Module is identical to the “Pin Assignments and Pin Voltages” of H.264 4k@30 Decoder Module detailed in Section 7. However, Pin Assignments and Pin Voltages of H.265 4k@30 Decoder Module it is provided here in this Section for completion.

### 13.1 Pin Assignments and Pin Voltages

The H.265 4K@30 decoder uses the SoM-X-Z45. The pin assignment is the same as the H.264 4K@30 decoder. This section provides again the pin assignment and pin voltages for H.265 4K@30 decoder modules based on the SoM-X-Z7045.

Table-22 shows the pin assignments and the pin voltages for H.265 4k@30 decoder modules based on the SoM-X-Z45.

The schematics of SoM-X-Z7045 edge connector are attached in Appendix-C of this document. Appendix-C shows the pin numbers for data, clock, control, and power, which are connected to the FPGA.

It should be noted that the H.265 4K@30 encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

**Table-22: 4K@30 Decoder Module (based on SoM-X-Z7045) Pin Assignment**

Description	SoM-X-Z7045 Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset_B	156	Input	B19	3.3V	LVC MOS33
Video Clock	105	Output	AG21	3.3v	LVC MOS33
Video Horizontal Sync	133	Output	W24	1.5v	LVC MOS15
Video Vertical Sync	113	Output	AF22	3.3v	LVC MOS33
Video Display Enable	67	Output	AD18	1.5v	LVC MOS15
Video Data 0 Luma[0]	135	Output	W25	1.5v	LVC MOS15
Video Data 0 Luma[1]	137	Output	W26	1.5v	LVC MOS15
Video Data 0 Luma[2]	116	Output	V27	1.5v	LVC MOS15
Video Data 0 Luma[3]	118	Output	W28	1.5v	LVC MOS15
Video Data 0 Luma[4]	124	Output	W29	1.5v	LVC MOS15
Video Data 0 Luma[5]	126	Output	W30	1.5v	LVC MOS15
Video Data 0 Luma[6]	128	Output	V28	1.5v	LVC MOS15
Video Data 0 Luma[7]	130	Output	V29	1.5v	LVC MOS15
Video Data 0 Luma[8]	132	Output	T30	1.5v	LVC MOS15
Video Data 0 Luma[9]	134	Output	U30	1.5v	LVC MOS15
Video Data 1 Luma[0]	117	Output	AG22	3.3v	LVC MOS33

Video Data 1 Luma[1]	119	Output	AH22	3.3v	LVC MOS33
Video Data 1 Luma[2]	121	Output	AJ21	3.3v	LVC MOS33
Video Data 1 Luma[3]	123	Output	AK21	3.3v	LVC MOS33
Video Data 1 Luma[4]	125	Output	AF23	3.3v	LVC MOS33
Video Data 1 Luma[5]	127	Output	AF24	3.3v	LVC MOS33
Video Data 1 Luma[6]	92	Output	AJ23	3.3v	LVC MOS33
Video Data 1 Luma[7]	94	Output	AJ24	3.3v	LVC MOS33
Video Data 1 Luma[8]	96	Output	AG24	3.3v	LVC MOS33
Video Data 1 Luma[9]	98	Output	AG25	3.3v	LVC MOS33
Video Data 2 Luma[0]	77	Output	AJ16	3.3v	LVC MOS33
Video Data 2 Luma[1]	79	Output	AK16	3.3v	LVC MOS33
Video Data 2 Luma[2]	81	Output	AH17	3.3v	LVC MOS33
Video Data 2 Luma[3]	83	Output	AH16	3.3v	LVC MOS33
Video Data 2 Luma[4]	85	Output	AH18	3.3v	LVC MOS33
Video Data 2 Luma[5]	87	Output	AJ18	3.3v	LVC MOS33
Video Data 2 Luma[6]	78	Output	AF13	3.3v	LVC MOS33
Video Data 2 Luma[7]	82	Output	AG15	3.3v	LVC MOS33
Video Data 2 Luma[8]	84	Output	AG17	3.3v	LVC MOS33
Video Data 2 Luma[9]	86	Output	AG16	3.3v	LVC MOS33
Video Data 3 Luma[0]	107	Output	AH21	3.3v	LVC MOS33
Video Data 3 Luma[1]	122	Output	AH29	3.3v	LVC MOS33
Video Data 3 Luma[2]	115	Output	AE22	3.3v	LVC MOS33
Video Data 3 Luma[3]	146	Output	AF28	3.3v	LVC MOS33
Video Data 3 Luma[4]	148	Output	AF29	3.3v	LVC MOS33
Video Data 3 Luma[5]	150	Output	AG29	3.3v	LVC MOS33
Video Data 3 Luma[6]	100	Output	AH23	3.3v	LVC MOS33
Video Data 3 Luma[7]	102	Output	AH24	3.3v	LVC MOS33
Video Data 3 Luma[8]	104	Output	AJ25	3.3v	LVC MOS33
Video Data 3 Luma[9]	106	Output	AK25	3.3v	LVC MOS33
Video Data 0 Chroma[0]	143	Output	T29	1.5v	LVC MOS15
Video Data 0 Chroma[1]	145	Output	U29	1.5v	LVC MOS15
Video Data 0 Chroma[2]	147	Output	R28	1.5v	LVC MOS15
Video Data 0 Chroma[3]	149	Output	T28	1.5v	LVC MOS15
Video Data 0 Chroma[4]	151	Output	P30	1.5v	LVC MOS15
Video Data 0 Chroma[5]	153	Output	R30	1.5v	LVC MOS15
Video Data 0 Chroma[6]	155	Output	N29	1.5v	LVC MOS15
Video Data 0 Chroma[7]	157	Output	P29	1.5v	LVC MOS15
Video Data 0 Chroma[8]	159	Output	N28	1.5v	LVC MOS15
Video Data 0 Chroma[9]	161	Output	P28	1.5v	LVC MOS15
Video Data 1 Chroma[0]	89	Output	AK17	3.3v	LVC MOS33
Video Data 1 Chroma[1]	91	Output	AK18	3.3v	LVC MOS33
Video Data 1 Chroma[2]	93	Output	AF19	3.3v	LVC MOS33
Video Data 1 Chroma[3]	95	Output	AG19	3.3v	LVC MOS33

Video Data 1 Chroma[4]	97	Output	AH19	3.3v	LVC MOS33
Video Data 1 Chroma[5]	99	Output	AJ19	3.3v	LVC MOS33
Video Data 1 Chroma[6]	101	Output	AF20	3.3v	LVC MOS33
Video Data 1 Chroma[7]	103	Output	AG20	3.3v	LVC MOS33
Video Data 1 Chroma[8]	109	Output	AJ20	3.3v	LVC MOS33
Video Data 1 Chroma[9]	111	Output	AK20	3.3v	LVC MOS33
Video Data 2 Chroma[0]	38	Output	AE12	3.3v	LVC MOS33
Video Data 2 Chroma[1]	40	Output	AF12	3.3v	LVC MOS33
Video Data 2 Chroma[2]	50	Output	AG12	3.3v	LVC MOS33
Video Data 2 Chroma[3]	52	Output	AH12	3.3v	LVC MOS33
Video Data 2 Chroma[4]	54	Output	AH14	3.3v	LVC MOS33
Video Data 2 Chroma[5]	56	Output	AH13	3.3v	LVC MOS33
Video Data 2 Chroma[6]	58	Output	AJ14	3.3v	LVC MOS33
Video Data 2 Chroma[7]	60	Output	AJ13	3.3v	LVC MOS33
Video Data 2 Chroma[8]	59	Output	AK13	3.3v	LVC MOS33
Video Data 2 Chroma[9]	61	Output	AK12	3.3v	LVC MOS33
Video Data 3 Chroma[0]	108	Output	AJ26	3.3v	LVC MOS33
Video Data 3 Chroma[1]	110	Output	AK26	3.3v	LVC MOS33
Video Data 3 Chroma[2]	112	Output	AH26	3.3v	LVC MOS33
Video Data 3 Chroma[3]	114	Output	AH27	3.3v	LVC MOS33
Video Data 3 Chroma[4]	136	Output	AK27	3.3v	LVC MOS33
Video Data 3 Chroma[5]	138	Output	AK28	3.3v	LVC MOS33
Video Data 3 Chroma[6]	139	Output	AJ28	3.3v	LVC MOS33
Video Data 3 Chroma[7]	141	Output	AJ29	3.3v	LVC MOS33
Video Data 3 Chroma[8]	140	Output	AJ30	3.3v	LVC MOS33
Video Data 3 Chroma[9]	142	Output	AK30	3.3v	LVC MOS33
SPDIF Audio	27	Output	Y20	1.5v	LVC MOS15
Transport Stream Clock	31	Input	AA18	1.5v	LVC MOS15
Transport Stream Data Valid	33	input	AA19	1.5v	LVC MOS15
Transport Stream Data [0]	152	input	AF30	3.3v	LVC MOS33
Transport Stream Data [1]	154	input	AG30	3.3v	LVC MOS33
Transport Stream Data [2]	158	input	AE30	3.3v	LVC MOS33
Transport Stream Data [3]	160	input	AB29	3.3v	LVC MOS33
Transport Stream Data [4]	162	input	AB30	3.3v	LVC MOS33
Transport Stream Data [5]	164	input	AA27	3.3v	LVC MOS33
Transport Stream Data [6]	166	input	AA28	3.3v	LVC MOS33
Transport Stream Data [7]	120	input	AH28	3.3v	LVC MOS33
Uart_tx	90	Output	AK15	3.3v	LVC MOS33
Uart_rx	88	Input	AJ15	3.3v	LVC MOS33

## 13.2 Signal Formats

### 13.2.1 Video Clock Signal (Output)

The Decoder Clock signal is an input clock for driving the decoder engine. When an SDI port on the carrier board is used to send out the decoded video data, the SDI clock can be connected to the Decoder Clock. This will automatically synchronize the decoder outputs with the SDI interface. The SDI clock frequency is 74.25MHz, for 4K@30.

### 13.2.2 Video Data Signals (Output)

The output of the H.264 4k@30 decoder module is the decoded video data in YUV format (4:2:2 or 4:2:0), with 40 output lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma, and, 40 lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision can be either 8-bit precision or 10-bit precision. For 8-bit precision, the Most Significant Bits of luma and chroma output lines (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. The **Video Display Enable signal** is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

### 13.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

### 13.2.4 Decoder Control Signals (Input and output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the decoder. **Uart\_rx** receives the command from an external control device. **Uart\_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Decoder API User Manual](#) for details.

## 13.3 Power Rails of SoM-X-Z7045

The power rails for H.265 4k@30 decoder are the same as the H.264 4k@30 encoder. Refer to Appendix-C for the pins of power and ground on the edge connector of the SoM-X-Z7045 module.

## 13.4 Power Requirement and Supply Current

Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-23 lists the power estimations for each rail, at 4k@30 resolution, which can be used for PCB designs for the

4k@30 module. It should be noted that the power rails 1.8v and 2.0v are generated on the module using the input power rails. PCB designers for the carrier boards need not to consider these two rails.

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards. The VTR-4000C, discussed in Section 19 of this document, is for 4k resolution. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for further details.

**Table-23: Power estimation for the H.265 4K@30 decoder module**

Power Rail	Current (A)	Power (W)
3.3V	0.50	1.64
2.5V	1.34	3.36
1.5V	0.96	1.44
1.3V	0.30	0.40
1.2V	0.24	0.29
1.0V	5.76	5.76

### 13.5 Booting Sequence and Booting Time

The module design has considered the booting sequence of the FPGA on the module. Therefore, there is no booting sequence requirement by the module for carrier board designs, i.e. the power rails can be supplied to the module at the same time or at any sequence. Once all of the power rails are supplied, the module will start to boot. The booting time is less than 2 seconds.

(Left Empty here intentionally)



## **14. The H.265 4k@60 Encoder Modules**

To be added

## **15. The H.265 4K@60 Decoder Modules**

To be added

(Left Empty here intentionally)

## 16. The H.264-to-MPEG2 HD Transcoder Module

### 16.1 Pin Assignments and Pin Voltages

The SOC Transcoder IP cores are “full decoding plus re-encoding”, based on the SOC decoder and encoder IP cores. The H.264-to-MPEG2 Transcoder is a core combining the SOC H.264 decoder and the SOC MPEG-2 encoder, which achieves the best transcoding quality.

The HD (1080@30 and 1080@60) transcoder module from H.264 to MPEG-2 uses the SoM-X-A200T (the Artix-7 A200T FPGA), and the SOC H.264-to-MPEG2 Transcoder IP core.

This Section provides the pin assignments and pin voltages for the H.264-to-MPEG2 transcoder module based on the SoM-X-A200T are provided in Table-24.

The schematics of SoM-X-A200T edge connector are attached in Appendix-B of this document, which shows the pin numbers for data, clock, control, and power. It should be noted that the encoder module uses only some of the edge pins, and not all of the edge pins are used.

**Table 24: HD Encoder Module (based on SoM-X-A200T) Pin Assignment and Pin Voltages**

Description	SoM-X-A200T Edge Connector Pin #	Direction	Voltage
TS_CLK	105	input	3v3
TS_DATA7	157	input	3v3
TS_DATA6	155	input	3v3
TS_DATA5	153	input	3v3
TS_DATA4	151	input	3v3
TS_DATA3	149	input	3v3
TS_DATA2	147	input	3v3
TS_DATA1	145	input	3v3
TS_DATA0	143	input	3v3
TS_DV	159	input	3v3
TS_CLK	146	Output	3v3
TS_DATA7	156	Output	3v3
TS_DATA6	166	Output	3v3
TS_DATA5	164	Output	3v3
TS_DATA4	162	Output	3v3
TS_DATA3	160	Output	3v3
TS_DATA2	158	Output	3v3
TS_DATA1	154	Output	3v3
TS_DATA0	152	Output	3v3
TS_DV	148	Output	3v3
TS_RDY	150	Output	3v3

## 16.2 Signal Formats

### 16.2.1 Clock Signal (Input)

The TS\_CLK signal (pin # 105) has two functions: (1) It is the clock for the input video data, and (2) it is the clock that drives the transcoder engine.

### 16.2.2 Input TS stream Signals

The input of the transcoder module is MPEG Transport Stream (TS), which is sent into the module by 8 parallel lines: TS\_DATA0 to TS\_DATA7, along with the data valid signal TS\_DV.

### 16.2.3 Output TS stream Signals

The output of the transcoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: TS\_DATA0 to TS\_DATA7, along with the data valid signal TS\_DV and the data ready signal TS\_RDY.

## 16.3 Power Rails of SoM-X-A200T

The power rails for the HD (H.264 or MPEG-2) H.264-to-MPEG2 transcoder module is the same as the ones for the HD encoder module. Refer to Table-2 for the power and ground pins. Also, refer to Appendix-B for the power and ground pins on the edge connector of the SoM-X-A200T module.

## 16.4 Power Requirement and Supply Current

In the transcoder case, the power consumption is the total power of the decoder and the encoder. Refer to **Section 5** for the H.264 HD decoder power and **Section 4** for the MPEG-2 encoder power.

Since the transcoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 19 of this document. The reference designs provide not only the power system design and clock distributions, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for design licensing details.

(Left Empty here intentionally)

## **17. The MPEG2-to-H.264 HD Transcoder Module**

The Pin assignment, pin voltages, and the power of the MPEG2-to-H.264 Transcoder are identical to those of the H.264-to-MPEG2 Transcoder.

(Left Empty here intentionally)

## **18. The H.264-to-H.265 HD and 4k@30 Transcoder Module**

**On request**

## 19. Carrier Boards and Evaluation Kits

### 19.1 Overview of SOC Carrier Boards and Evaluation Kits

SOC has several boards that have the connector for the SOC SoMs and Codec Modules. A carrier board combined with a generic SoM can be used for product development of user SoMs, in which case the users develop their own firmware to make the generic SOMs into their own products.

The carrier boards combined with the SOC codec SOMs become evaluation kits for the SOC Codec Modules. Since the SOC Codec Modules are based on the SOC codec IP cores, the evaluation kits are also used for evaluation of both the SOC codec modules and IP cores. The eval kits can also be used as product development platforms.

### 19.2 VTR-S1000 Carrier Board

Fig. 11 shows a photo of the VTR-S1000 board. Major components and I/O ports are marked in the figure. Refer to the [User Guide of VTR -S1000](#) for further details.

SOC licenses the Schematics of VTR-S1000 to the customers that have purchased the eval kit VTR-S1000 and encoder (or decoder) Modules. Firmware of the VTR-S1000, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, [sales@soctechnologies.com](mailto:sales@soctechnologies.com), for details.

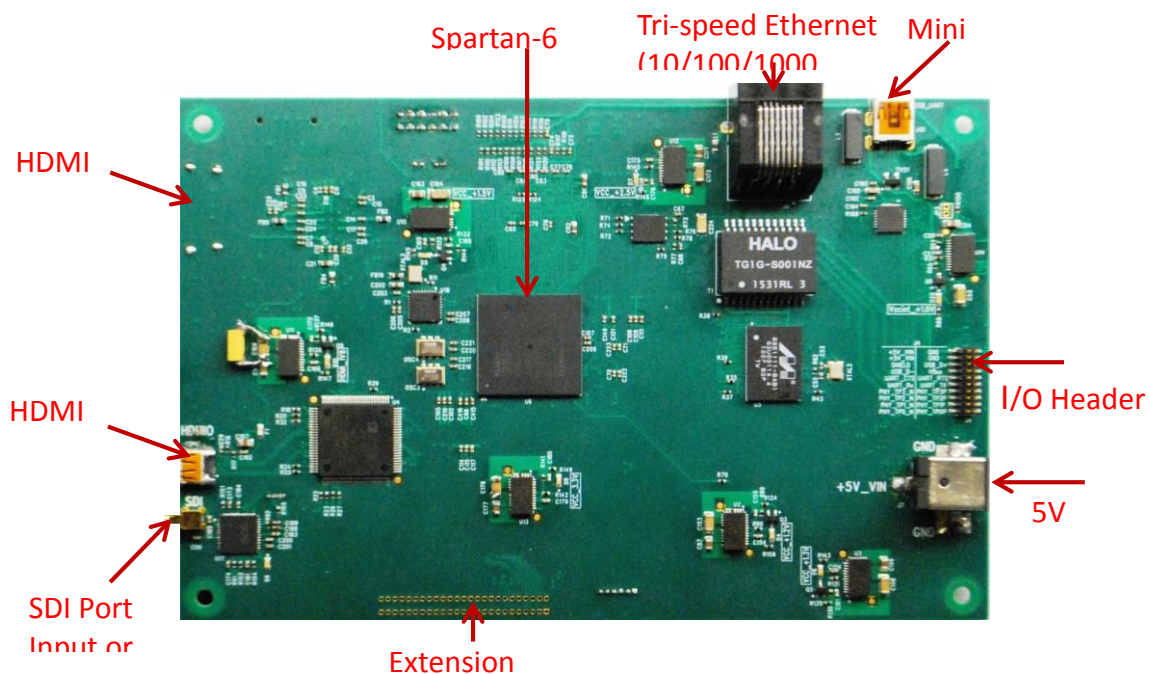


Fig. 11. VTR-S1000 carrier board

### 19.3 VTR-4000C Carrier Board

Fig. 12 shows the top view of the VTR-4000C board. Major components and I/O ports are marked in the figure. Refer to the [User Guide of VTR-4000C](#) for further details.

SOC licenses the Schematics of VTR-4000C to the customers that have purchased encoder (or decoder) Modules. Firmware of the VTR-4000C, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, [sales@soctechnologies.com](mailto:sales@soctechnologies.com), for details.

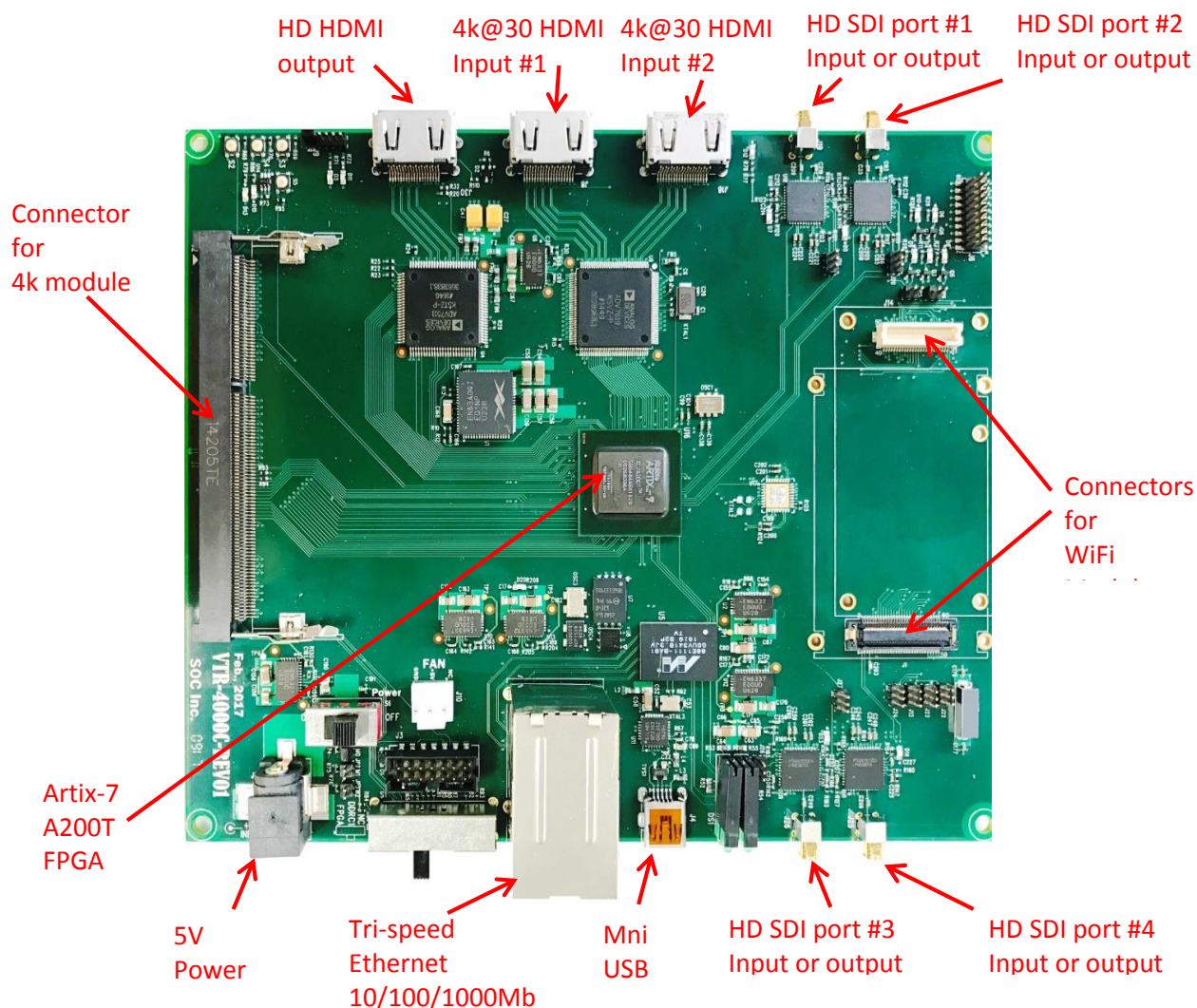


Fig. 12. VTR-4000C carrier board top view

## 19.4 VoIP-X-4K Carrier Board

Fig. 13 shows the top view of the VoIP-X-4K board. Major components and I/O ports are marked in the figure. Refer to the [User Guide of VoIP-X-4K](#) for further details.

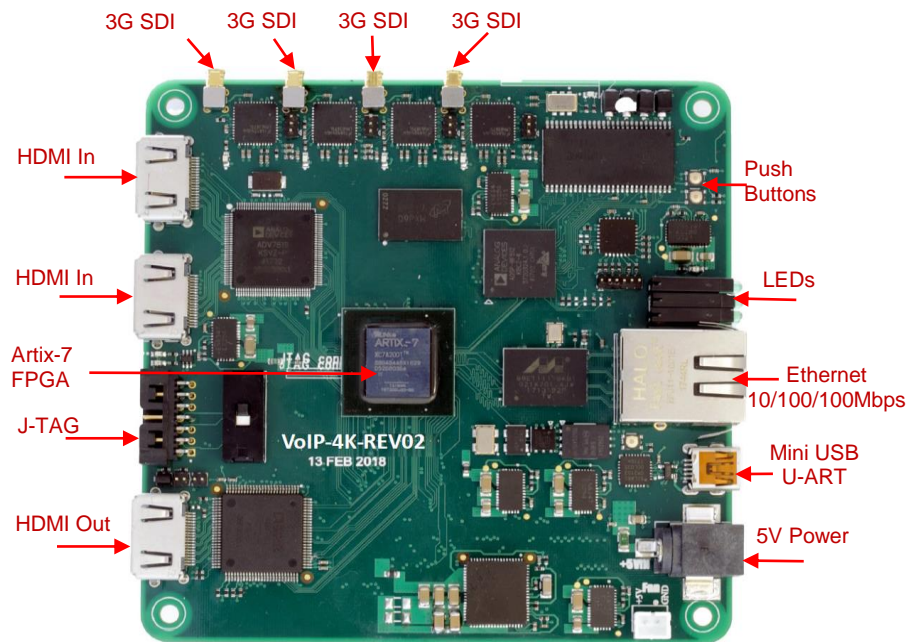


Fig. 13. VoIP-X-4K Carrier board top view

SOC licenses the Schematics of VoIP-X-4K to the customers that have purchased encoder (or decoder) Modules. Firmware of the VoIP-X-4K, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, [sales@soctechnologies.com](mailto:sales@soctechnologies.com), for details.

## 19.5 The Codec Module Evaluation Kits

The Carrier boards described in the above Sections 19.2, 19.3, and 19.4 are used to evaluate the SOC codec modules, codec IP cores, or chipsets. For each codec module listed in Appendix-A, an evaluation kit is available, which consists the codec module and a carrier board. The product code of the Evaluation Kit is the same as the codec module, except the letter “M” is replaced by “EV” which means Evaluation kit. It is note that the SOC codec modules chipset are based on the same IP cores of SOC.



## 20. Ordering Information

### 20.1 Ordering of SOC Generic SoMs

Fig. 6 shows the product code system for the SOC SoM modules. Customer can order SoMs using the Product Code listed in Table-2.

### 20.2 Ordering of SOC Codec Modules

Fig. 7 shows the product code naming convention for the SOC MPEG codec modules, IP cores, and chipsets. Customers can order the SOC codec modules listed in Appendix-A. Non-standard codec modules can be ordered following the same naming format (minimum order quantity is required for non-standard modules).

## 20. Contact Information

Please contact SOC head office or distributor for product details and to place an order.

Head Office

System-On-Chip (SOC) Technologies Inc.

86 Rankin Street

Waterloo, ON, Canada N2V 1V9

Telephone: 1-519-880-8609

E-mail: [sales@soctechnologies.com](mailto:sales@soctechnologies.com)

## 21. Document Revisions

Version #	Revision Date	Notes
V.1.0	10/05/2017	First release
V.1.1	19/05/2017	Minor revision
V.2.0	20/05/2017	Major revision (adding 4k)
V.2.1	05/06/2017	Minor revision
V.2.2	10/10/2017	Minor revision
V.3.0	01/06/2018	Major revision
V.4.0	15/05/2019	Major revision

## Appendix-A Factory Standard Codec Modules

### Note:

It is noted that the Temperature and Latency Grade identifiers are not included in the Codec Module product code in the tables. These identifiers are optional, which can be added in the customer orders. The temperature identifier can be either “C” for Commercial Temperature or “I” for Industrial Temperature. The Latency Identifier can be “ZL” for Zero Latency, “LL” for Low Latency, or “SL” for Standard Latency. These latencies are: “ZL” = 0.25ms, “LL” = 1 Frame latency, and “SL” = 2 Frame latency.

### A.1 H.264 HD (720@30, 720@60,1080@30, and 1080@60) Encoder Modules

Table-A.1-1 provides a list of standard H.264 HD video (without audio) Encoder Modules. Table-A.1-2 provides a list of standard H.264 HD video&audio Encoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.1-1: H.264 HD Video Encoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-H264-8b-30-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
EC-V-H264-8b-60-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-A200T
EC-V-H264-8b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
EC-V-H264-10b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no	SoM-X-A200T
EC-V-H264-8b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-A200T
EC-V-H264-10b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no	SoM-X-A200T

**Table-A.1-2: H.264 HD Video/Audio Encoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-VA-H264-8b-30-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC	SoM-X-A200T
EC-VA-H264-8b-60-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC	SoM-X-A200T
EC-VA-H264-8b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC	SoM-X-A200T
EC-VA-H264-10b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC	SoM-X-A200T
EC-VA-H264-8b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC	SoM-X-A200T
EC-VA-H264-10b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC	SoM-X-A200T

## A.2 MPEG-2 HD (720@30, 720@60, 1080@30, and 1080@60) Encoder Modules

Table-A.2-1 provides a list of standard MPEG-2 HD video (without audio) Encoder Modules. Table-A.2-2 provides a list of standard MPEG-2 HD video&audio Encoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.2-1: MPEG-2 HD Video Encoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-MPEG2-8b-30-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
EC-V- MPEG2-8b-60-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-A200T
EC-V- MPEG2-8b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
EC-V- MPEG2-8b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-A200T

**Table-A.2-2: MPEG-2 HD Video/Audio Encoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-VA- MPEG2-8b-30-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	MPEG2-L2?	SoM-X-A200T
EC-VA- MPEG2-8b-60-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	MPEG2-L2?	SoM-X-A200T
EC-VA- MPEG2-8b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	MPEG2-L2?	SoM-X-A200T
EC-VA- MPEG2-8b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	MPEG2-L2?	SoM-X-A200T

### A.3 H.264 HD (720@30, 720@60, 1080@30, and 1080@60) Decoder Modules

Table-A.3-1 provides a list of standard H.264 HD video (without audio) Decoder Modules. Table-A.3-2 provides a list of standard H.264 HD video&audio Decoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.3-1: H.264 HD Video Decoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-H264-8b-30-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
DC-V-H264-8b-60-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-A200T
DC-V-H264-8b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
DC-V-H264-10b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no	SoM-X-A200T
DC-V-H264-8b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-A200T
DC-V-H264-10b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no	SoM-X-A200T

**Table-A.3-2: H.264 HD Video/Audio Decoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-VA-H264-8b-30-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC	SoM-X-A200T
DC-VA-H264-8b-60-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC	SoM-X-A200T
DC-VA-H264-8b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC	SoM-X-A200T
DC-VA-H264-10b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC	SoM-X-A200T
DC-VA-H264-8b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC	SoM-X-A200T
DC-VA-H264-10b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC	SoM-X-A200T

#### A.4 MPEG-2 HD (720@30, 720@60,1080@30, and 1080@60) Decoder Modules

Table-A.4-1 provides a list of standard MPEG-2 HD video (without audio) Decoder Modules. Table-A.4-2 provides a list of standard MPEG-2 HD video&audio Decoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.4-1: MPEG-2 HD Video Decoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-MPEG2-8b-30-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
DC-V- MPEG2-8b-60-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-A200T
DC-V- MPEG2-8b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
DC-V- MPEG2-8b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-A200T

**Table-A.4-2: MPEG-2 HD Video/Audio Decoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-VA- MPEG2-8b-30-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	MPEG2-L2AAC?	SoM-X-A200T
DC-VA- MPEG2-8b-60-720-M	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	MPEG2-L2AAC?	SoM-X-A200T
DC-VA- MPEG2-8b-30-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	MPEG2-L2AAC?	SoM-X-A200T
DC-VA- MPEG2-8b-60-1080-M	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	MPEG2-L2AAC?	SoM-X-A200T

## A.5 H.264 4k@30 Encoder Modules

Table-A.5-1 provides a list of standard H.264 4k@30 video (without audio) Encoder Modules. Table-A.5-2 provides a list of standard H.264 4k@30 video&audio Encoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.5-1: H.264 4k@30 Video Encoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-H264-8b-30-4k-M	H.264	up to High	4k	4:2:0/4:2:2	8 bits	30fps	no	SoM-X-Z7035/7045
EC-V-H264-10b-30-4k-M	H.264	up to High	4k	4:2:0/4:2:2	up to 10 bits	30fps	no	SoM-X-Z7035/7045

**Table-A.5-2: H.264 4k@30 Video/Audio Encoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-VA-H264-8b-30-4k-M	H.264	up to High	4k	4:2:0/4:2:2	8 bits	30fps	AAC	SoM-X-Z7035/7045
EC-VA-H264-10b-30-4k-M	H.264	up to High	4k	4:2:0/4:2:2	up to 10 bits	30fps	AAC	SoM-X-Z7035/7045

## A.6 H.264 4k@30 Decoder Modules

Table-A.6-1 provides a list of standard H.264 4k@30 video (without audio) Decoder Modules. Table-A.6-2 provides a list of standard H.264 4k@30 video&audio Decoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.6-1: H.264 4k@30 Video Decoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-H264-8b-30-4k-M	H.264	up to High	4k	4:2:0/4:2:2	8 bits	30fps	no	SoM-X-Z7035/7045
DC-V-H264-10b-30-4k-M	H.264	up to High	4k	4:2:0/4:2:2	up to 10bits	30fps	no	SoM-X-Z7035/7045

**Table-A.6-2: H.264 4k@30 Video/Audio Decoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-VA-H264-8b-30-4k-M	H.264	up to High	4k	4:2:0/4:2:2	8 bits	30fps	AAC	SoM-X-Z7035/7045
DC-VA-H264-10b-30-4k-M	H.264	up to High	4k	4:2:0/4:2:2	up to 10 bits	30fps	AAC	SoM-X-Z7035/7045

## A.7 H.264 4k@60 Encoder Modules

Table-A.7-1 provides a list of standard H.264 4k@60 video (without audio) Encoder Modules. Table-A.7-2 provides a list of standard H.264 4k@60 video&audio Encoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.7-1: H.264 4k@60 Video Encoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-H264-8b-60-4k-M	H.264	up to High	4k	4:2:0/4:2:2	8 bits	60fps	no	SoM-I-SX660
EC-V-H264-10b-60-4k-M	H.264	up to High	4k	4:2:0/4:2:2	up to 10 bits	60fps	no	SoM-I-SX660

**Table-A.7-2: H.264 4k@60 Video/Audio Encoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-VA-H264-8b-60-4k-M	H.264	up to High	4k	4:2:0/4:2:2	8 bits	60fps	AAC	SoM-I-SX660
EC-VA-H264-10b-60-4k-M	H.264	up to High	4k	4:2:0/4:2:2	up to 10 bits	60fps	AAC	SoM-I-SX660

## A.8 H.264 4k@60 Decoder Modules

Table-A.8-1 provides a list of standard H.264 4k@60 video (without audio) Decoder Modules. Table-A.8-2 provides a list of standard H.264 4k@60 video&audio Decoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.8-1: H.264 4k@60 Video Decoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-H264-8b-60-4k-M	H.264	up to High	4k	4:2:0/4:2:2	8 bits	60fps	no	SoM-I-SX660
DC-V-H264-10b-60-4k-M	H.264	up to High	4k	4:2:0/4:2:2	up to 10 bits	60fps	no	SoM-I-SX660

**Table-A.8-2: H.264 4k@60 Video/Audio Decoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-VA-H264-8b-60-4k-M	H.264	up to High	4k	4:2:0/4:2:2	8 bits	60fps	AAC	SoM-I-SX660
DC-VA-H264-10b-60-4k-M	H.264	up to High	4k	4:2:0/4:2:2	up to 10 bits	60fps	AAC	SoM-I-SX660

## A.9 H.265 HD (720@30, 720@60, 1080@30, and 1080@60) Encoder Modules

Table-A.9-1 provides a list of standard H.265 HD video (without audio) Encoder Modules. Table-A.9-2 provides a list of standard H.265 HD video&audio Encoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.9-1: H.265 HD Video Encoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-H265-8b-30-720-M	H.265/HEVC	Main 8	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-Z7045
EC-V-H265-8b-60-720-M	H.265/HEVC	Main 8	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-Z7045
EC-V-H265-8b-30-1080-M	H.265/HEVC	Main 8	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-Z7045
EC-V-H265-10b-30-1080-M	H.265/HEVC	Main 10	up to 1080i/p	4:2:0/4:2:2	10 bits	up to 30fps	no	SoM-X-Z7045
EC-V-H265-8b-60-1080-M	H.265/HEVC	Main 8	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-Z7045
EC-V-H265-10b-60-1080-M	H.265/HEVC	Main 10	up to 1080i/p	4:2:0/4:2:2	10 bits	up to 60fps	no	SoM-X-Z7045

**Table-A.9-2: H.265 HD Video/Audio Encoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-VA-H265-8b-30-720-M	H.265/HEVC	Main 8	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC	SoM-X-Z7045
EC-VA-H265-8b-60-720-M	H.265/HEVC	Main 8	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC	SoM-X-Z7045
EC-VA-H265-8b-30-1080-M	H.265/HEVC	Main 8	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC	SoM-X-Z7045
EC-VA-H265-10b-30-1080-M	H.265/HEVC	Main 10	up to 1080i/p	4:2:0/4:2:2	10 bits	up to 30fps	AAC	SoM-X-Z7045
EC-VA-H265-8b-60-1080-M	H.265/HEVC	Main 8	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC	SoM-X-Z7045
EC-VA-H265-10b-60-1080-M	H.265/HEVC	Main 10	up to 1080i/p	4:2:0/4:2:2	10 bits	up to 60fps	AAC	SoM-X-Z7045



## A.10 H.265 HD (720@30, 720@60,1080@30, and 1080@60) Decoder Modules

Table-A.10-1 provides a list of standard H.265 HD video (without audio) Decoder Modules. Table-A.10-2 provides a list of standard H.265 HD video&audio Decoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.10-1: H.265 HD Video Decoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-H265-8b-30-720-M	H.265/HEVC	Main 8	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-Z7045
DC-V-H265-8b-60-720-M	H.265/HEVC	Main 8	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-Z7045
DC-V-H265-8b-30-1080-M	H.265/HEVC	Main 8	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	SoM-X-Z7045
DC-V-H265-10b-30-1080-M	H.265/HEVC	Main 10	up to 1080i/p	4:2:0/4:2:2	10 bits	up to 30fps	no	SoM-X-Z7045
DC-V-H265-8b-60-1080-M	H.265/HEVC	Main 8	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	SoM-X-Z7045
DC-V-H265-10b-60-1080-M	H.265/HEVC	Main 10	up to 1080i/p	4:2:0/4:2:2	10 bits	up to 60fps	no	SoM-X-Z7045

**Table-A.10-2: H.265 HD Video/Audio Decoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-VA-H265-8b-30-720-M	H.265/HEVC	Main 8	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC	SoM-X-Z7045
DC-VA-H265-8b-60-720-M	H.265/HEVC	Main 8	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC	SoM-X-Z7045
DC-VA-H265-8b-30-1080-M	H.265/HEVC	Main 8	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC	SoM-X-Z7045
DC-VA-H265-10b-30-1080-M	H.265/HEVC	Main 10	up to 1080i/p	4:2:0/4:2:2	10 bits	up to 30fps	AAC	SoM-X-Z7045
DC-VA-H265-8b-60-1080-M	H.265/HEVC	Main 8	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC	SoM-X-Z7045
DC-VA-H265-10b-60-1080-M	H.265/HEVC	Main 10	up to 1080i/p	4:2:0/4:2:2	10 bits	up to 60fps	AAC	SoM-X-Z7045

## A.11 H.265 4k@30 Encoder Modules

Table-A.11-1 provides a list of standard H.265 4k@30 video (without audio) Encoder Modules. Table-A.11-2 provides a list of standard H.265 4k@30 video&audio Encoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.11-1: H.265 4k@30 Video Encoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-H265-8b-30-4k-M	H.265	Main 8	4k	4:2:0/4:2:2	8 bits	30fps	no	SoM-X-Z7045
EC-V-H265-10b-30-4k-M	H.265	Main 10	4k	4:2:0/4:2:2	up to 10 bits	30fps	no	SoM-X-Z7045

**Table-A.11-2: H.265 4k@30 Video/Audio Encoder Modules (both video and audio):**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-VA-H265-8b-30-4k-M	H.265	Main 8	4k	4:2:0/4:2:2	8 bits	30fps	AAC	SoM-X-Z7045
EC-VA-H265-10b-30-4k-M	H.265	Main 10	4k	4:2:0/4:2:2	up to 10 bits	30fps	AAC	SoM-X-Z7045

## A.12 H.265 4k@30 Decoder Modules

Table-A.12-1 provides a list of standard H.265 4k@30 video (without audio) Decoder Modules. Table-A.12-2 provides a list of standard H.265 4k@30 video&audio Decoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.12-1: H.265 4k@30 Video Decoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-H265-8b-30-4k-M	H.265	Main 8	4k	4:2:0/4:2:2	8 bits	30fps	no	SoM-X-Z7045
DC-V-H265-10b-30-4k-M	H.265	Main 10	4k	4:2:0/4:2:2	up to 10 bits	30fps	no	SoM-X-Z7045

**Table-A.12-2: H.265 4k@30 Video/Audio Decoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-VA-H265-8b-30-4k-M	H.265	Main 8	4k	4:2:0/4:2:2	8 bits	30fps	AAC	SoM-X-Z7045
DC-VA-H265-10b-30-4k-M	H.265	Main 10	4k	4:2:0/4:2:2	up to 10 bits	30fps	AAC	SoM-X-Z7045

A.13 H.265 4k@60 Encoder Modules

To be added

A.14 H.265 4k@60 Decoder Modules

To be added

## A.17 H.264-to-MPEG2 Transcoder Modules

Table-A.17-1 provides a list of standard H.264-to-MPEG2 Video Transcoder Modules. Table-A.17-2 provides a list of standard H.264-to-MPEG2 Video and Audio Transcoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.17-1: H.264-to-MPEG2 Video Transcoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-H.264-to-MPEG2-8b-30-720-M	H.264 to MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
TC-V- H.264-to-MPEG2-8b-60-720-M	H.264 to MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no	SoM-X-A200T
TC-V- H.264-to-MPEG2-8b-30-1080-M	H.264 to MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
TC-V- H.264-to-MPEG2-8b-60-1080-M	H.264 to MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no	SoM-X-A200T

**Table-A.17-2: H.264-to-MPEG2 Video&Audio Transcoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-VA- H.264-to -MPEG2-8b-30-720-M	H.264 to MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	AAC to MPEG2-L2?	SoM-X-A200T
TC-VA- H.264-to -MPEG2-8b-60-720-M	H.264 to MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	AAC to MPEG2-L2?	SoM-X-A200T
TC-VA- H.264-to -MPEG2-8b-30-1080-M	H.264 to MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	AAC to MPEG2-L2?	SoM-X-A200T
TC-VA- H.264-to -MPEG2-8b-60-1080-M	H.264 to MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	AAC to MPEG2-L2?	SoM-X-A200T

## A.18 MPEG2-to-H.264 Transcoder Modules

Table-A.18-1 provides a list of standard MPEG2-to-H.264 Video Transcoder Modules. Table-A.18-2 provides a list of standard MPEG-2-to-H.264 Video and Audio Transcoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.18-1: MPEG2-to-H264 Video Transcoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-MPEG2-to-H264-8b-30-720-M	MPEG2 to H.264	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
TC-V- MPEG2-to-H264-8b-60-720-M	MPEG2 to H.264	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no	SoM-X-A200T
TC-V- MPEG2-to-H264-8b-30-1080-M	MPEG2 to H.264	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no	SoM-X-A200T
TC-V- MPEG2-to-H264-8b-60-1080-M	MPEG2 to H.264	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no	SoM-X-A200T

**Table-A.20-2: MPEG2-to-H264 Video&Audio Transcoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-MPEG2-to-H264-8b-30-720-M	MPEG2 to H.264	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2 to AAC	SoM-X-A200T
TC-V- MPEG2-to-H264-8b-60-720-M	MPEG2 to H.264	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2 to AAC	SoM-X-A200T
TC-V- MPEG2-to-H264-8b-30-1080-M	MPEG2 to H.264	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2 to AAC	SoM-X-A200T
TC-V- MPEG2-to-H264-8b-60-1080-M	MPEG2 to H.264	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2 to AAC	SoM-X-A200T

## A.21 H.264-to-H.265 Transcoder Modules

Table-A.21-1 provides a list of standard H.264-to-H.265 Video Transcoder Modules. Table-A.21-2 provides a list of standard H.264-to-H.265 Video and Audio Transcoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A21-1: H.264-to-H.265 Video Transcoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-H.264-to-H.265-8b-30-720-M	H.264 to H.265	High to Main 8	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no	SoM-I-SX660
TC-V-H.264-to-H.265-10b-30-720-M	H.264 to H.265	High to Main 10	up to 720i/p	up to 4:2:2	10 bits	up to 30fps	no	SoM-I-SX660
TC-V- H.264-to-H.265-8b-60-720-M	H.264 to H.265	High to Main 8	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no	SoM-I-SX660
TC-V- H.264-to-H.265-10b-60-720-M	H.264 to H.265	High to Main 10	up to 720i/p	up to 4:2:2	10 bits	up to 60fps	no	SoM-I-SX660
TC-V- H.264-to-H.265-8b-30-1080-M	H.264 to H.265	High to Main 8	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no	SoM-I-SX660
TC-V- H.264-to-H.265-10b-30-1080-M	H.264 to H.265	High to Main 10	up to 1080i/p	up to 4:2:2	10 bits	up to 30fps	no	SoM-I-SX660
TC-V- H.264-to-H.265-8b-60-1080-M	H.264 to H.265	High to Main 8	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no	SoM-I-SX660
TC-V- H.264-to-H.265-10b-60-1080-M	H.264 to H.265	High to Main 10	up to 1080i/p	up to 4:2:2	10 bits	up to 60fps	no	SoM-I-SX660

**Table-A21-2: H.264-to-H.265 Video & Audio Transcoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-H.264-to-H.265-8b-30-720-M	H.264 to H.265	High to Main 8	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	AAC	SoM-I-SX660
TC-V-H.264-to-H.265-10b-30-720-M	H.264 to H.265	High to Main 10	up to 720i/p	up to 4:2:2	10 bits	up to 30fps	AAC	SoM-I-SX660
TC-V- H.264-to-H.265-8b-60-720-M	H.264 to H.265	High to Main 8	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	AAC	SoM-I-SX660
TC-V- H.264-to-H.265-10b-60-720-M	H.264 to H.265	High to Main 10	up to 720i/p	up to 4:2:2	10 bits	up to 60fps	AAC	SoM-I-SX660
TC-V- H.264-to-H.265-8b-30-1080-M	H.264 to H.265	High to Main 8	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	AAC	SoM-I-SX660
TC-V- H.264-to-H.265-10b-30-1080-M	H.264 to H.265	High to Main 10	up to 1080i/p	up to 4:2:2	10 bits	up to 30fps	ACC	SoM-I-SX660
TC-V- H.264-to-H.265-8b-60-1080-M	H.264 to H.265	High to Main 8	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	AAC	SoM-I-SX660
TC-V- H.264-to-H.265-10b-60-1080-M	H.264 to H.265	High to Main 10	up to 1080i/p	up to 4:2:2	10 bits	up to 60fps	AAC	SoM-I-SX660

## A.22 H.265-to-H.264 Transcoder Modules

Table-A.22-1 provides a list of standard H.265-to-H.264 Video Transcoder Modules. Table-A.22-2 provides a list of standard H.265-to-H.264 Video and Audio Transcoder Modules. The product code, specifications, and the SoM hardware are detailed in the table.

**Table-A.22-1: H.265-to-H.264 Video Transcoder Modules (video only without audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-H.265-to-H.264-8b-30-720-M	H.265 to H.264	Main 8 to High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no	SoM-I-SX660
TC-V-H.265-to-H.264-10b-30-720-M	H.265 to H.264	Main 10 to High	up to 720i/p	up to 4:2:2	10 bits	up to 30fps	no	SoM-I-SX660
TC-V- H.265-to-H.264-8b-60-720-M	H.265 to H.264	Main 8 to High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no	SoM-I-A660SX
TC-V- H.265-to-H.264-10b-60-720-M	H.265 to H.264	Main 10 to High	up to 720i/p	up to 4:2:2	10 bits	up to 60fps	no	SoM-I-SX660
TC-V- H.265-to-H.264-8b-30-1080-M	H.265 to H.264	Main 8 to High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no	SoM-I-SX660
TC-V- H.265-to-H.264-10b-30-1080-M	H.265 to H.264	Main 10 to High	up to 1080i/p	up to 4:2:2	10 bits	up to 30fps	no	SoM-I-SX660
TC-V- H.265-to-H.264-8b-60-1080-M	H.265 to H.264	Main 8 to High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no	SoM-I-SX660
TC-V- H.265-to-H.264-10b-60-1080-M	H.265 to H.264	Main 10 to High	up to 1080i/p	up to 4:2:2	10 bits	up to 60fps	no	SoM-I-SX660

**Table-A.22-2: H.265-to-H.264 Video & Audio Transcoder Modules (both video and audio):**

Product #	Specifications							SoM
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-H.265-to-H.264-8b-30-720-M	H.265 to H.264	Main 8 to High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	AAC	SoM-I-SX660
TC-V-H.265-to-H.264-10b-30-720-M	H.265 to H.264	Main 10 to High	up to 720i/p	up to 4:2:2	10 bits	up to 30fps	AAC	SoM-I-SX660
TC-V- H.265-to-H.264-8b-60-720-M	H.265 to H.264	Main 8 to High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	AAC	SoM-I-SX660
TC-V- H.265-to-H.264-10b-60-720-M	H.265 to H.264	Main 10 to High	up to 720i/p	up to 4:2:2	10 bits	up to 60fps	AAC	SoM-I-SX660
TC-V- H.265-to-H.264-8b-30-1080-M	H.265 to H.264	Main 8 to High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	AAC	SoM-I-SX660
TC-V- H.265-to-H.264-10b-30-1080-M	H.265 to H.264	Main 10 to High	up to 1080i/p	up to 4:2:2	10 bits	up to 30fps	AAC	SoM-I-SX660
TC-V- H.265-to-H.264-8b-60-1080-M	H.265 to H.264	Main 8 to High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	AAC	SoM-I-SX660
TC-V- H.265-to-H.264-10b-60-1080-M	H.265 to H.264	Main 10 to High	up to 1080i/p	up to 4:2:2	10 bits	up to 60fps	AAC	SoM-I-SX660

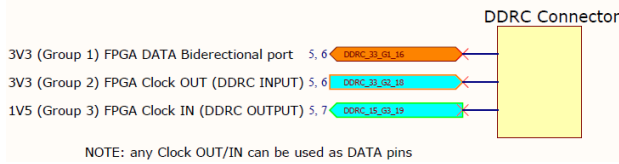
### A.23 Non-Standard Codec Modules

The previous section provides the information on SOC's factory standard MPEG codec modules. Customers can order modules based on customer specific requirements (non-standard modules). There is a Minimum Order Quantity (MOQ) required for customized configurations. Contact SOC sales [sale@soctechnologies.com](mailto:sale@soctechnologies.com) for information.



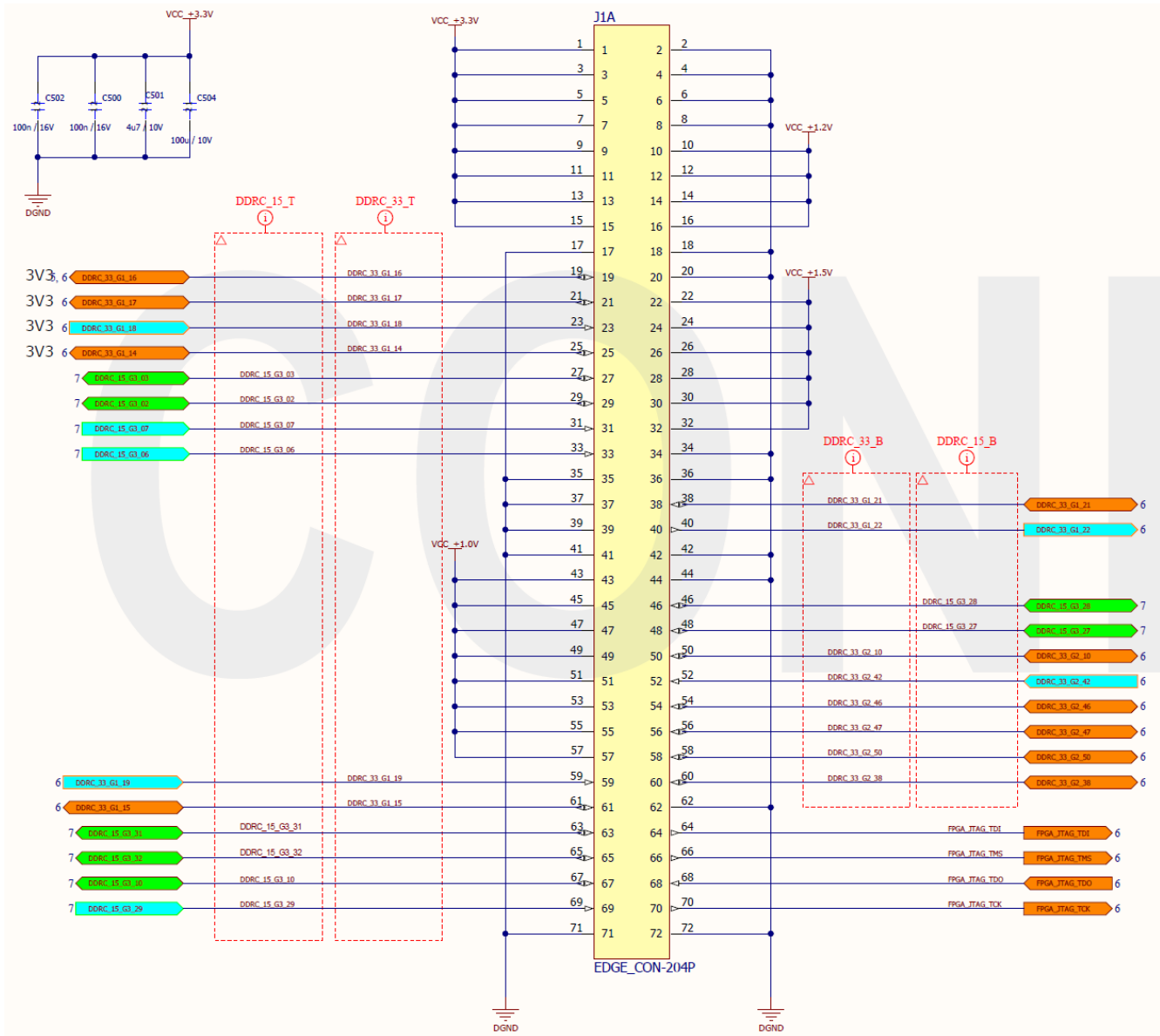
## Appendix - B SoM-X-A200T Edge Connector Schematics

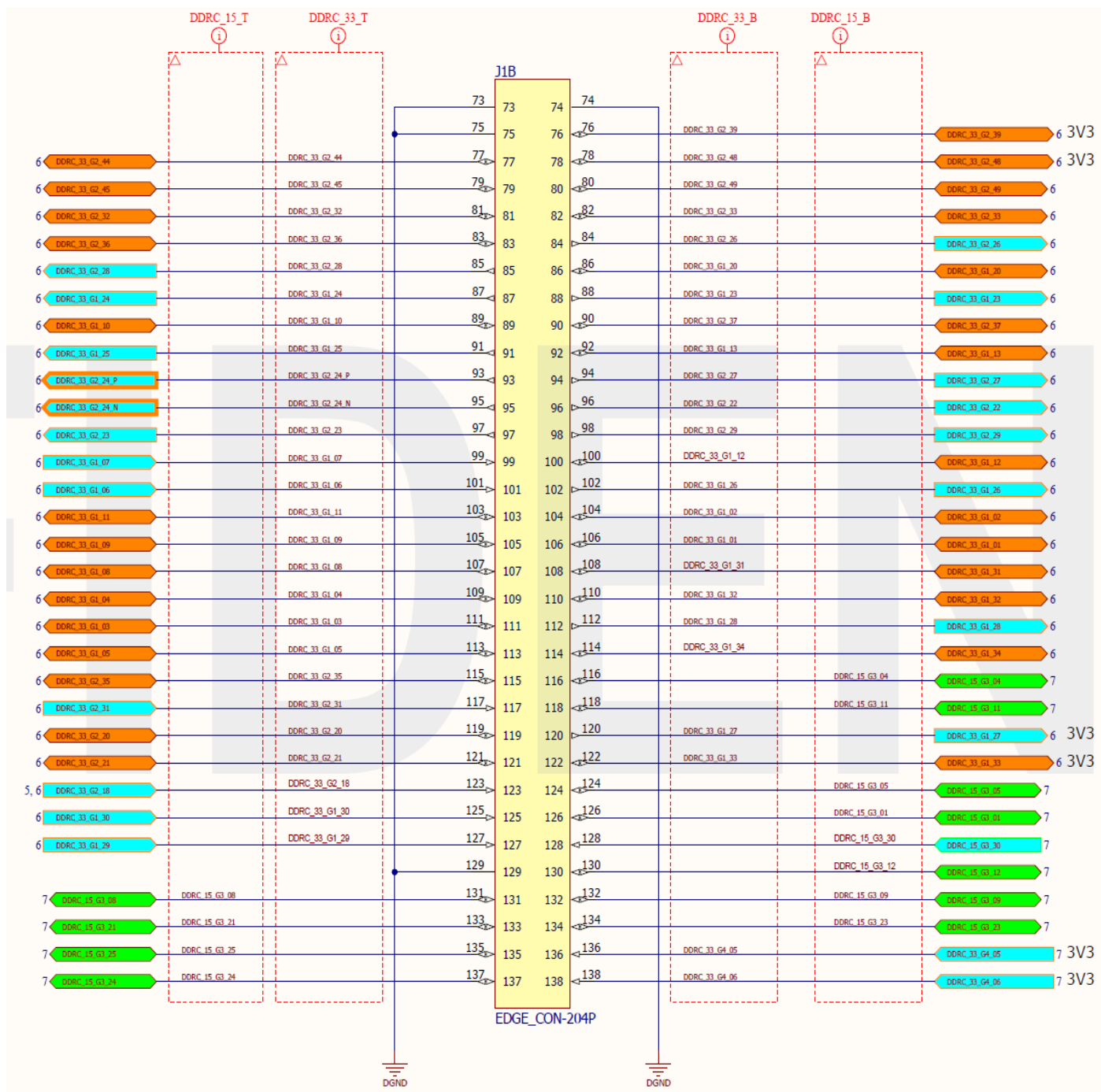
### Legend

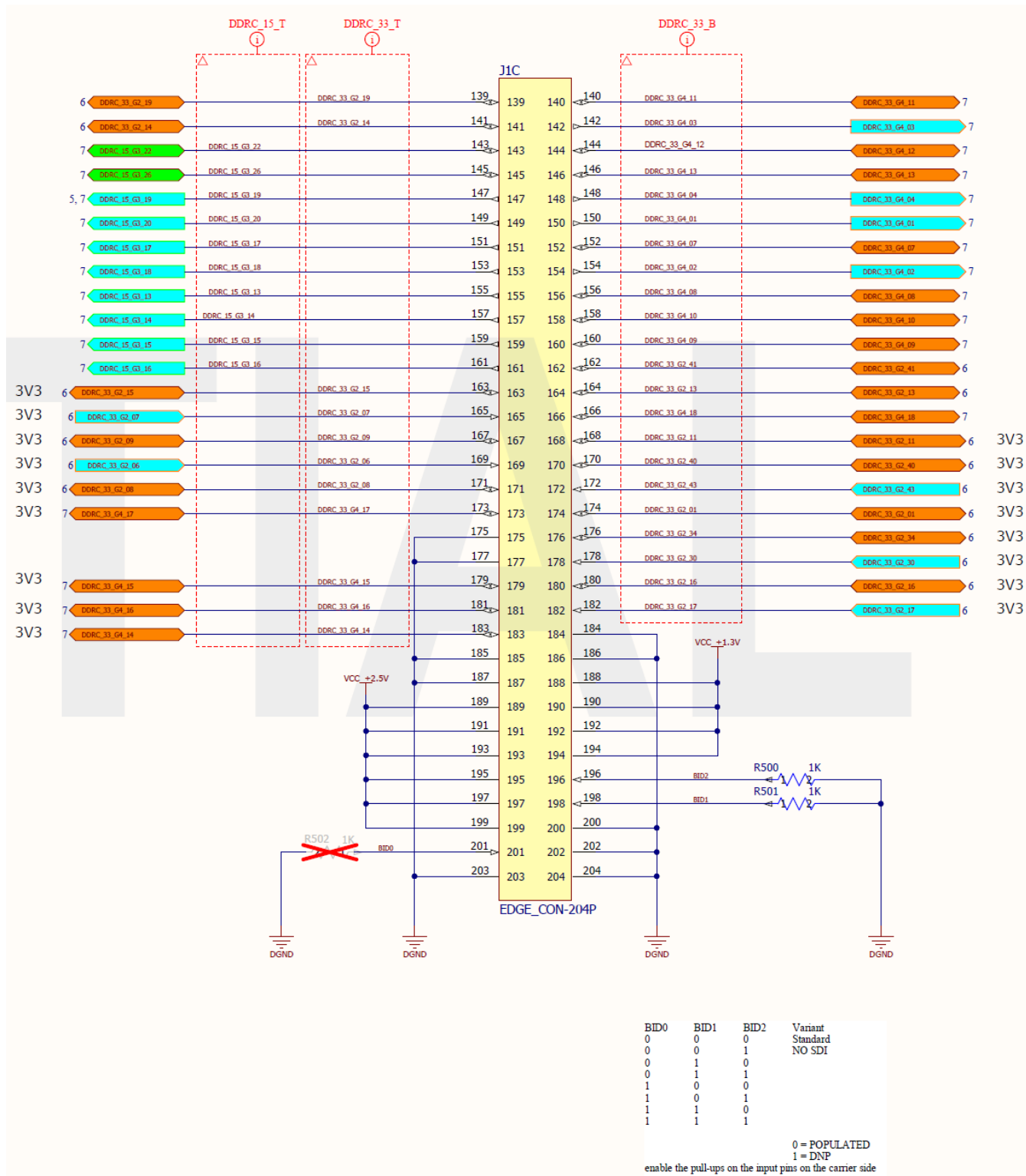


FPGA - DDRC signals (97 @ 3V3, 32 @ 1V5)

- 34 x DDRC Signals Group 1 @ 3V3
- 45 x DDRC Signals Group 2 @ 3V3
- 32 x DDRC Signals Group 3 @ 1V5
- 18 x DDRC Signals Group 4 @ 3V3

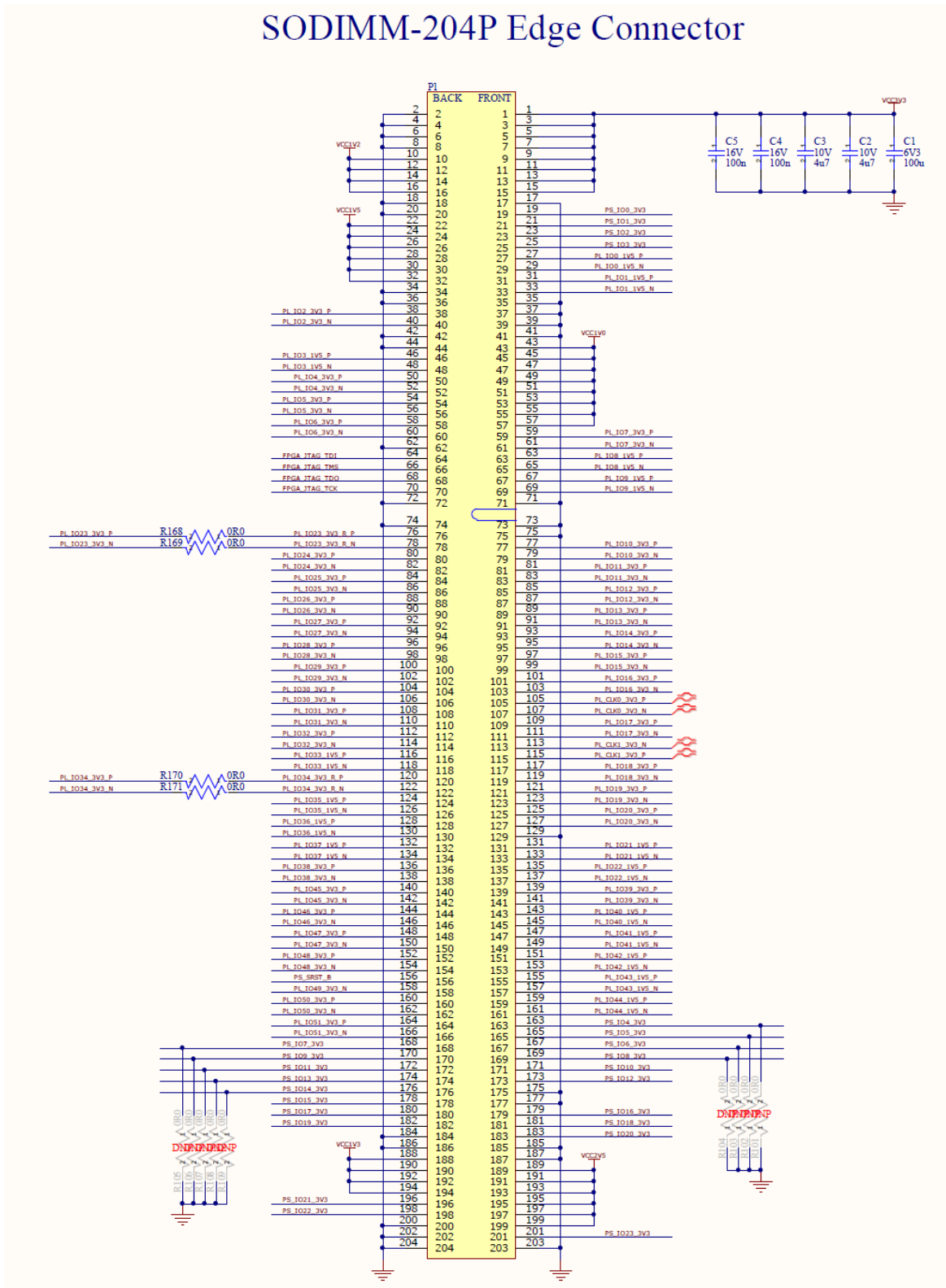






### Appendix - C SoM-X-Z7045 Edge Connector Schematics

#### SODIMM-204P Edge Connector



FPGA_JTAG_TDI	FPGA_JTAG_TDI
FPGA_JTAG_TMS	FPGA_JTAG_TMS
FPGA_JTAG_TDO	FPGA_JTAG_TDO
FPGA_JTAG_TCK	FPGA_JTAG_TCK

JTAG

To FPGA Bank 0  
3V3 Signals

PS_I00_3V3	PS_I00_3V3
PS_I01_3V3	PS_I01_3V3
PS_I02_3V3	PS_I02_3V3
PS_I03_3V3	PS_I03_3V3
PS_I04_3V3	PS_I04_3V3
PS_I05_3V3	PS_I05_3V3
PS_I06_3V3	PS_I06_3V3
PS_I07_3V3	PS_I07_3V3
PS_I08_3V3	PS_I08_3V3
PS_I09_3V3	PS_I09_3V3
PS_I010_3V3	PS_I010_3V3
PS_I011_3V3	PS_I011_3V3
PS_I012_3V3	PS_I012_3V3
PS_I013_3V3	PS_I013_3V3
PS_I014_3V3	PS_I014_3V3
PS_I015_3V3	PS_I015_3V3
PS_I016_3V3	PS_I016_3V3
PS_I017_3V3	PS_I017_3V3
PS_I018_3V3	PS_I018_3V3
PS_I019_3V3	PS_I019_3V3
PS_I020_3V3	PS_I020_3V3
PS_I021_3V3	PS_I021_3V3
PS_I022_3V3	PS_I022_3V3
PS_I023_3V3	PS_I023_3V3

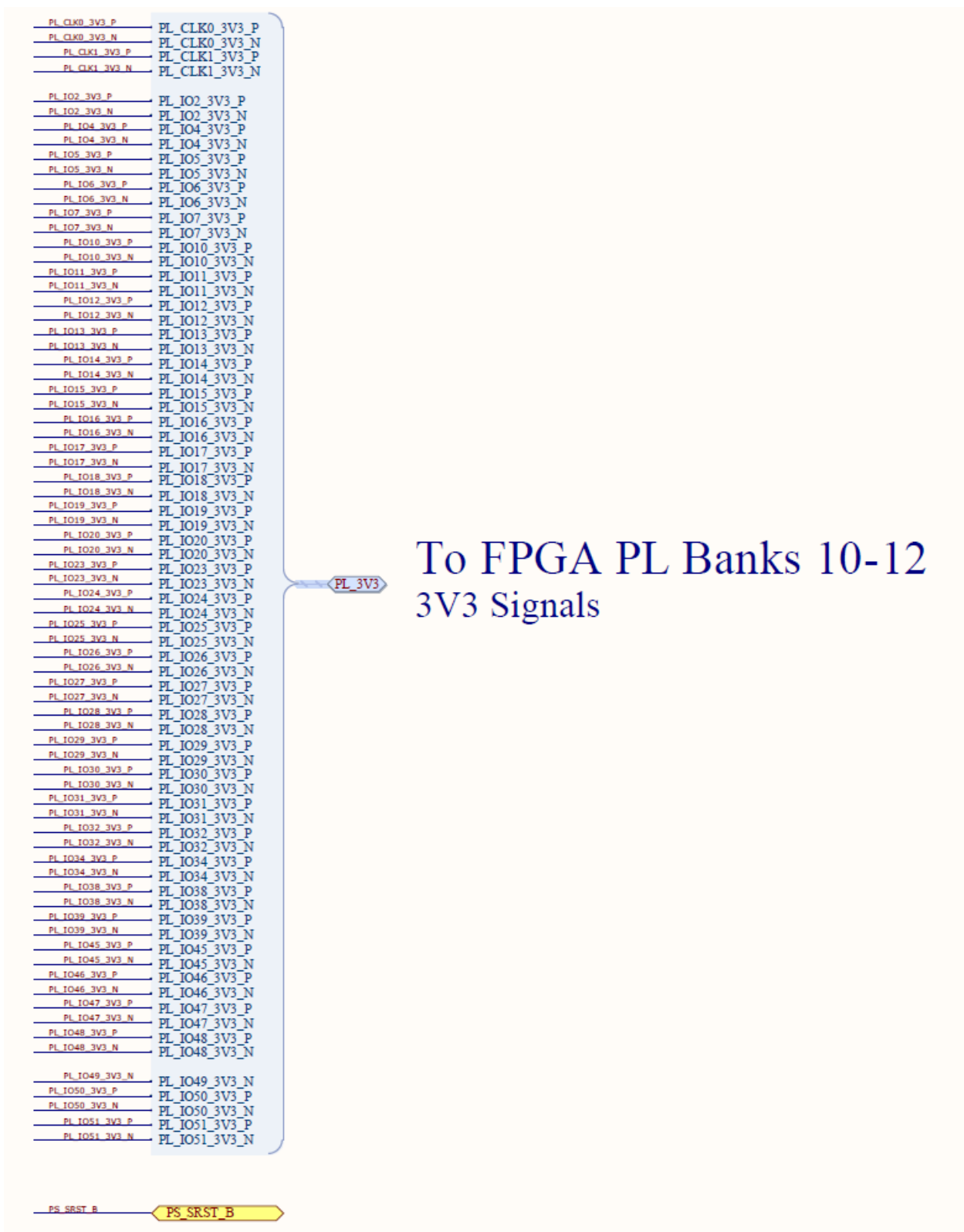
PS\_3V3

To FPGA PS Banks 500, 501  
3V3 Signals

PL_I00_1V5_P	PL_I00_1V5_P
PL_I00_1V5_N	PL_I00_1V5_N
PL_I01_1V5_P	PL_I01_1V5_P
PL_I01_1V5_N	PL_I01_1V5_N
PL_I03_1V5_P	PL_I03_1V5_P
PL_I03_1V5_N	PL_I03_1V5_N
PL_I08_1V5_P	PL_I08_1V5_P
PL_I08_1V5_N	PL_I08_1V5_N
PL_I09_1V5_P	PL_I09_1V5_P
PL_I09_1V5_N	PL_I09_1V5_N
PL_I021_1V5_P	PL_I021_1V5_P
PL_I021_1V5_N	PL_I021_1V5_N
PL_I022_1V5_P	PL_I022_1V5_P
PL_I022_1V5_N	PL_I022_1V5_N
PL_I033_1V5_P	PL_I033_1V5_P
PL_I033_1V5_N	PL_I033_1V5_N
PL_I035_1V5_P	PL_I035_1V5_P
PL_I035_1V5_N	PL_I035_1V5_N
PL_I036_1V5_P	PL_I036_1V5_P
PL_I036_1V5_N	PL_I036_1V5_N
PL_I037_1V5_P	PL_I037_1V5_P
PL_I037_1V5_N	PL_I037_1V5_N
PL_I040_1V5_P	PL_I040_1V5_P
PL_I040_1V5_N	PL_I040_1V5_N
PL_I041_1V5_P	PL_I041_1V5_P
PL_I041_1V5_N	PL_I041_1V5_N
PL_I042_1V5_P	PL_I042_1V5_P
PL_I042_1V5_N	PL_I042_1V5_N
PL_I043_1V5_P	PL_I043_1V5_P
PL_I043_1V5_N	PL_I043_1V5_N
PL_I044_1V5_P	PL_I044_1V5_P
PL_I044_1V5_N	PL_I044_1V5_N

PL\_1V5

To FPGA PL Banks 9, 13  
1V5 Signals



## To FPGA PL Banks 10-12 3V3 Signals

## Appendix - D SoM-I-SX660 Edge Connector Schematics

### SODIMM-204P Edge Connector

