

SN54ABT2952A, SN74ABT2952A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS203D – AUGUST 1992 – REVISED JANUARY 1998

- State-of-the-Art *EPIC-II^B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions
- Noninverting Outputs
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

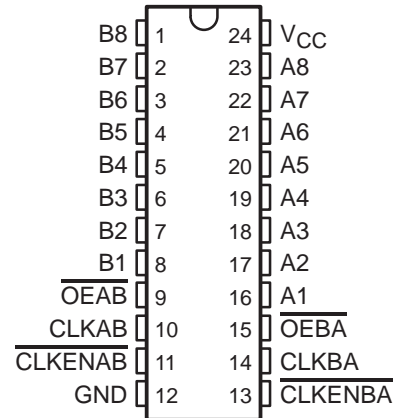
description

The 'ABT2952A transceivers consist of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

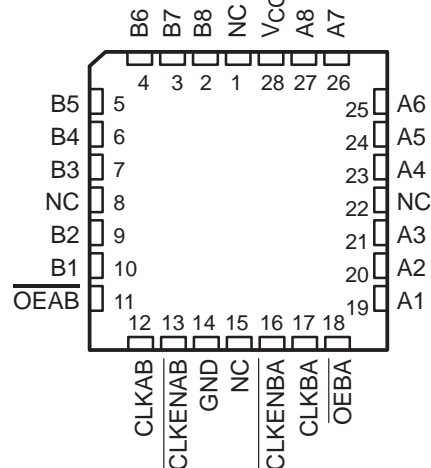
To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT2952A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT2952A is characterized for operation from -40°C to 85°C .

SN54ABT2952A . . . JT OR W PACKAGE
SN74ABT2952A . . . DB, DW, PW, OR NT PACKAGE
(TOP VIEW)



SN54ABT2952A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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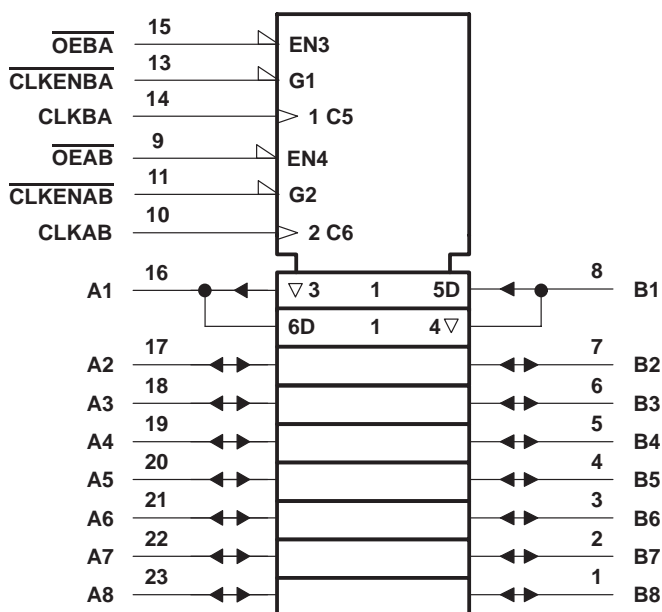
FUNCTION TABLE†

INPUTS				OUTPUT
CLKENAB	CLKAB	OEAB	A	B
H	X	L	X	B ₀ ‡
X	H or L	L	X	B ₀ ‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar, but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.

‡ Level of B before the indicated steady-state input conditions were established

logic symbols§

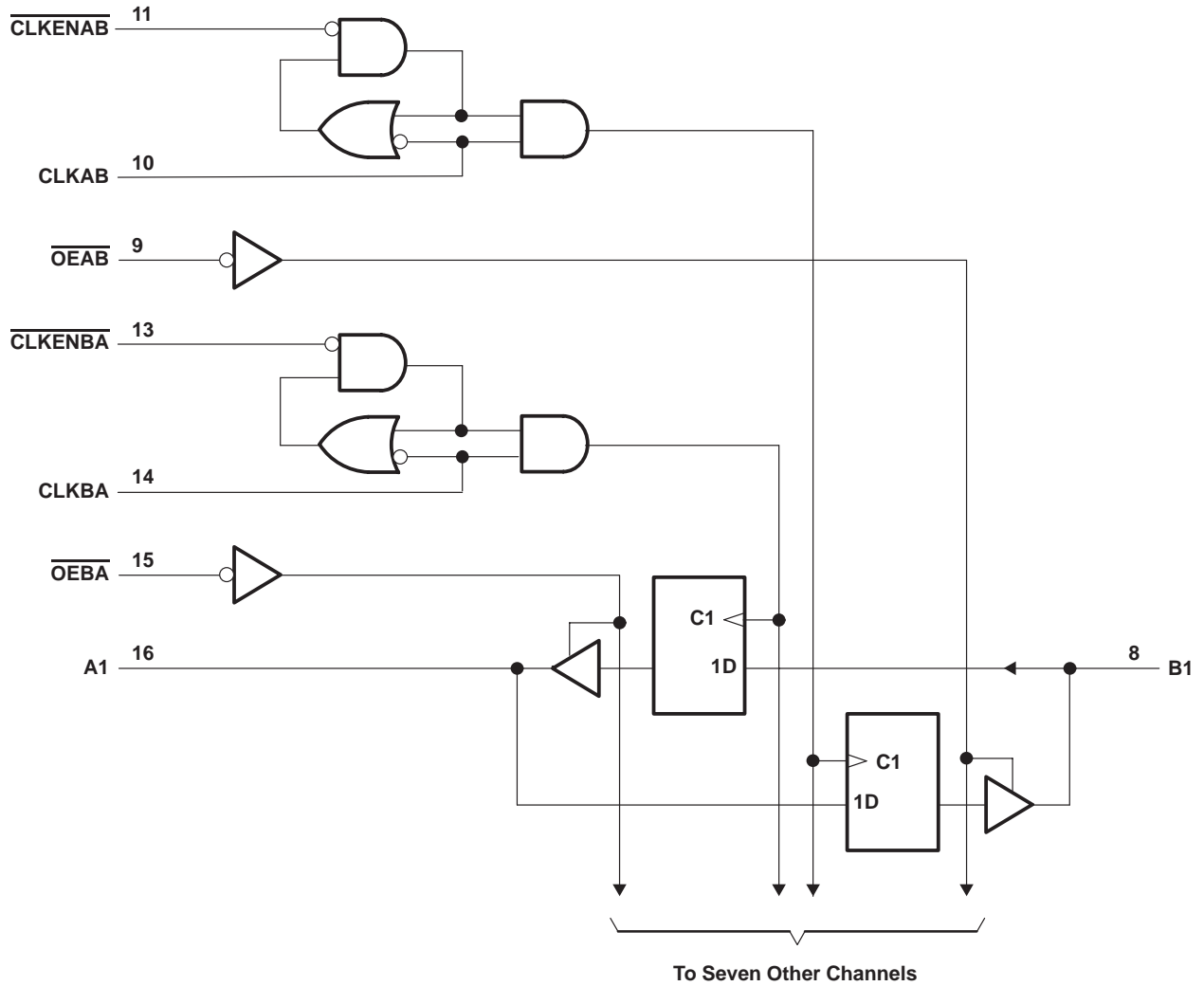


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT2952A	96 mA
SN74ABT2952A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	104°C/W
DW package	81°C/W
NT package	67°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT2952A		SN74ABT2952A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT2952A		SN74ABT2952A		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5			2.5	V
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3			3	
	V _{CC} = 4.5 V, I _{OH} = -24 mA	2			2				
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA			0.55		0.55			V
				0.55*				0.55	
V _{hys}			100						mV
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1		±1		±1	μA
	A or B ports			±100		±100		±100	
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V			50*		10		50	μA
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V			-50*		-10		-50	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100*				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high			50		50		50	μA
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I _{CC}	A or B ports, V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		1	250	250	250	250	μA
		Outputs low		24	35	35	35	35	mA
		Outputs disabled		0.5	250	250	250	250	μA
ΔI _{CC} ¶	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	Control inputs, V _I = 2.5 V or 0.5 V			3.5					pF
C _{io}	A or B ports, V _O = 2.5 V or 0.5 V			7.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 5 V, T _A = 25°C		SN54ABT2952A		SN74ABT2952A		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency	0	150	0	150	0	150	MHz	
t _w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns	
t _{su}	Setup time before CLK↑	A or B	High or low	2.5		3		2.5	ns
		CLKEN		3		3			
t _h	Hold time after CLK↑	A or B		1.5		1.5		1.5	ns
		CLKEN		2		2		2	



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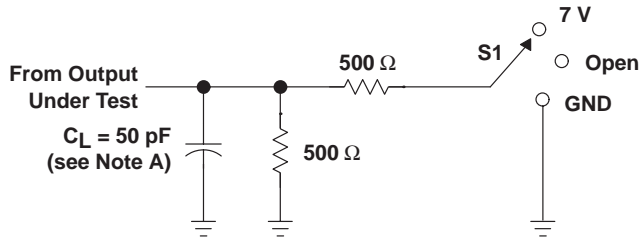
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT2952A		SN74ABT2952A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLKAB or CLKBA	B or A	2	3.3	5.2	2	6.3	2	5.9	ns
t_{PHL}			2.5	4	6.1	2.5	6.8	2.5	6.3	
t_{PZH}	\overline{OEBA} or \overline{OEAB}	A or B	1.5	3.2	4.7	1.5	5.7	1.5	5.6	ns
t_{PZL}			2	3.7	5.7	2	6.7	2	6.6	
t_{PHZ}	\overline{OEBA} or \overline{OEAB}	A or B	1.5	3.5	5.1	1.5	6.5	1.5	6.4	ns
t_{PLZ}			1.5	3.4	5.9	1.5	6.7	1.5	6.2	

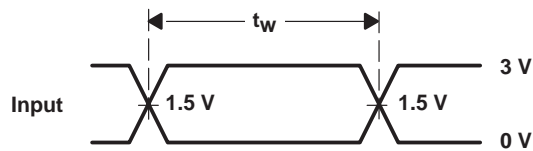


PARAMETER MEASUREMENT INFORMATION

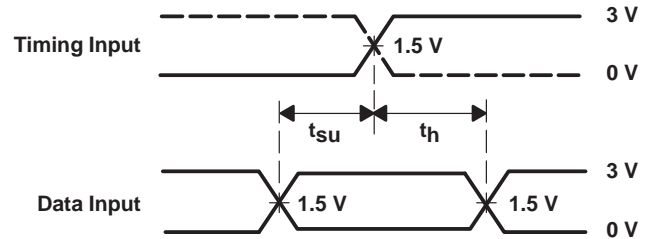


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

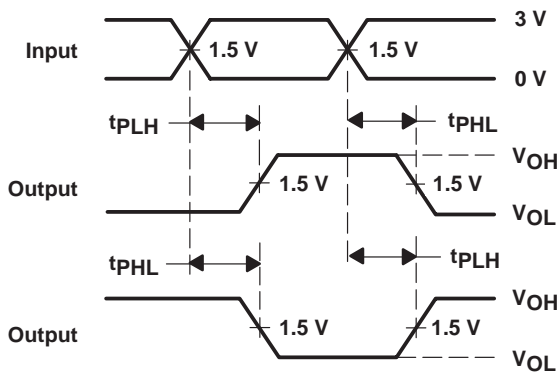
LOAD CIRCUIT



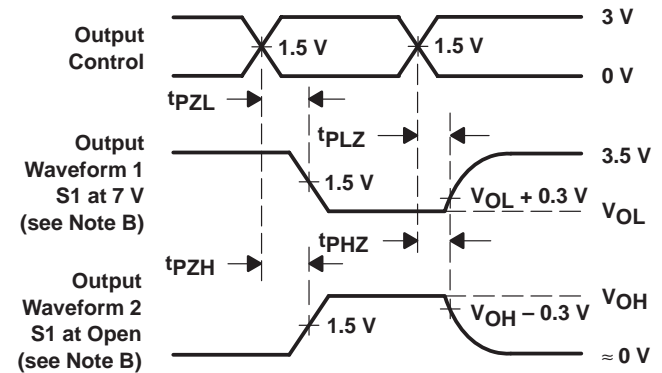
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9308602QLA	ACTIVE	CDIP	JT	24	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9308602QL A SNJ54ABT2952AJ T	Samples
SN74ABT2952ADWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2952A	Samples
SNJ54ABT2952AJT	ACTIVE	CDIP	JT	24	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9308602QL A SNJ54ABT2952AJ T	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ABT2952A, SN74ABT2952A :

- Catalog: [SN74ABT2952A](#)
- Military: [SN54ABT2952A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT2952ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT2952ADWR	SOIC	DW	24	2000	350.0	350.0	43.0

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



4040110/C 08/96

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

DW (R-PDSO-G24)

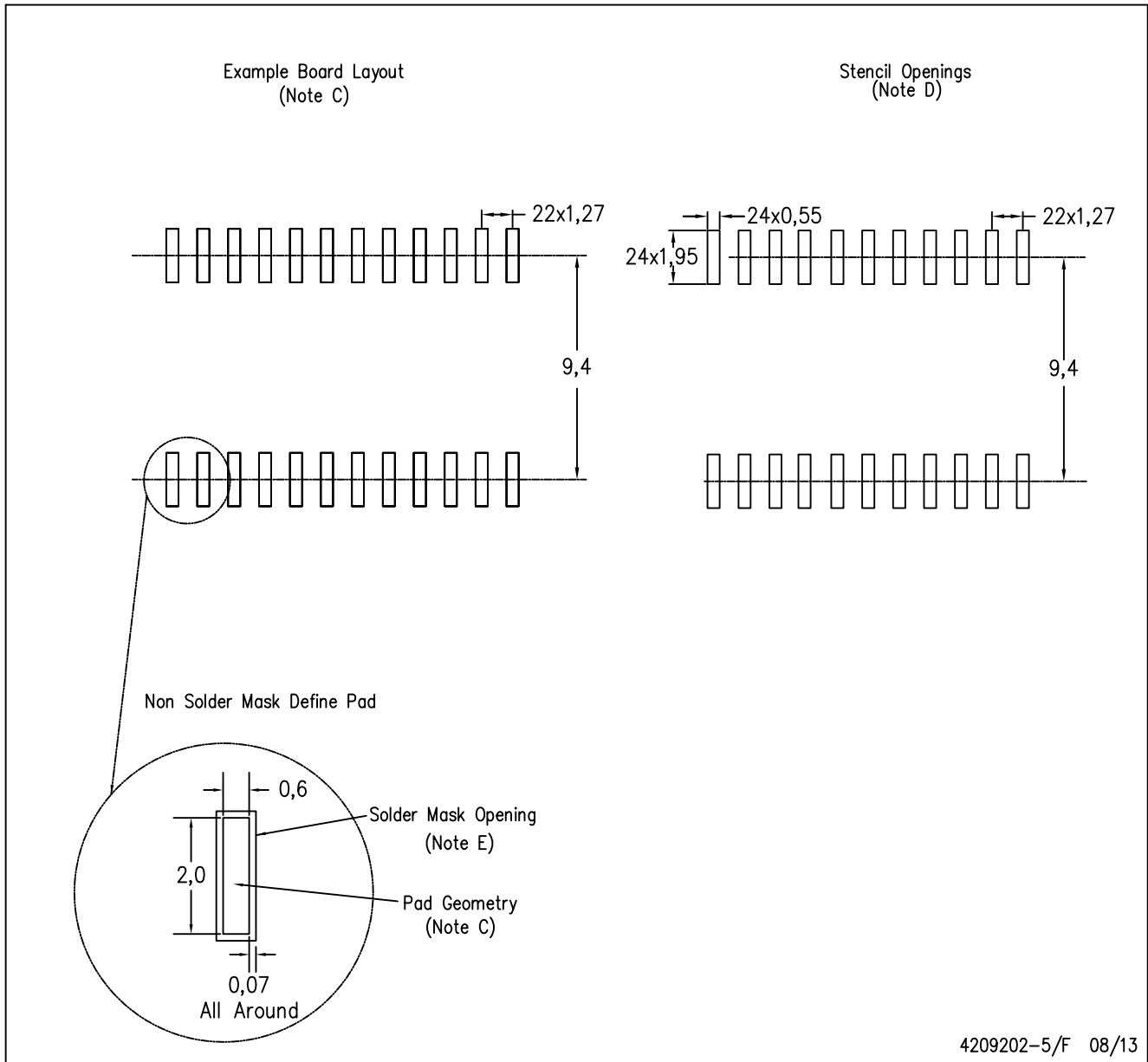
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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