

# EiceDRIVER™ gate driver 1EDI3023AS

## Single channel isolated IGBT driver



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Technical documents



Simulation



Family overview



Support



RoHS



ISO 26262 compliant

## Features

- Single channel isolated IGBT driver using coreless transformer technology
- For IGBTs up to 1200 V
- CMTI up to 150 V/ns at 1000 V
- 8 kV basic insulation according to VDE V 0884-11:2017-01
- Basic insulation recognized according to UL 1577
- Min. 12 A peak current rail-to-rail output
- Propagation delay 60 ns typical
- Typ. 10 A integrated Active Miller Clamp supports unipolar switching
- Integrated ADC for DC-link measurements
- Integrated safety features to support ASIL B(D):
  - Redundant DESAT and OCP protection
  - Gate and output stage monitoring
  - Shoot-through protection
  - Primary/secondary supply monitoring
  - Internal supervision
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL B
- Green Product (RoHS compliant)



## Potential applications

- Traction inverters for HEV and EV
- Auxiliary inverters for HEV and EV
- High power DC/DC converters

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

## Description

The EiceDRIVER™ gate driver 1EDI3023AS is a high-voltage IGBT driver designed for automotive motor drives above 5 kW. The device is based on Infineon's coreless transformer (CT) technology, providing galvanic insulation between low voltage and high voltage domains. The device has been designed to support 400 V, 600 V and 1200 V IGBT technologies.

# EiceDRIVER™ gate driver 1EDI3023AS

## Single channel isolated IGBT driver



### Description

The device features a high output stage of minimum 12 A peak current. A comprehensive feature set allows advanced protection of the device and the power switch, as well as optimized driver performance and robustness.

The device can be connected on the low voltage side (“primary” side) to 5 V and 3.3 V logic.

On the high voltage side (secondary side), the device is dimensioned to drive the gate of IGBTs directly. Short propagation delays and controlled internal tolerances lead to a minimal distortion of the PWM signal. In addition, there is a Miller clamping stage with minimum 12 A integrated, which allows unipolar supply of the IGBT.

The device features an integrated ADC for DC link measurement and a detailed error diagnosis via a PWM signal.

A large panel of safety related functions supports functional safety requirements at system level as per ISO 26262. Besides, these integrated features ease the implementation of a transition to safe-state.

Type	Package	Marking
1EDI3023AS	PG-DSO-20	1EDI3023AS

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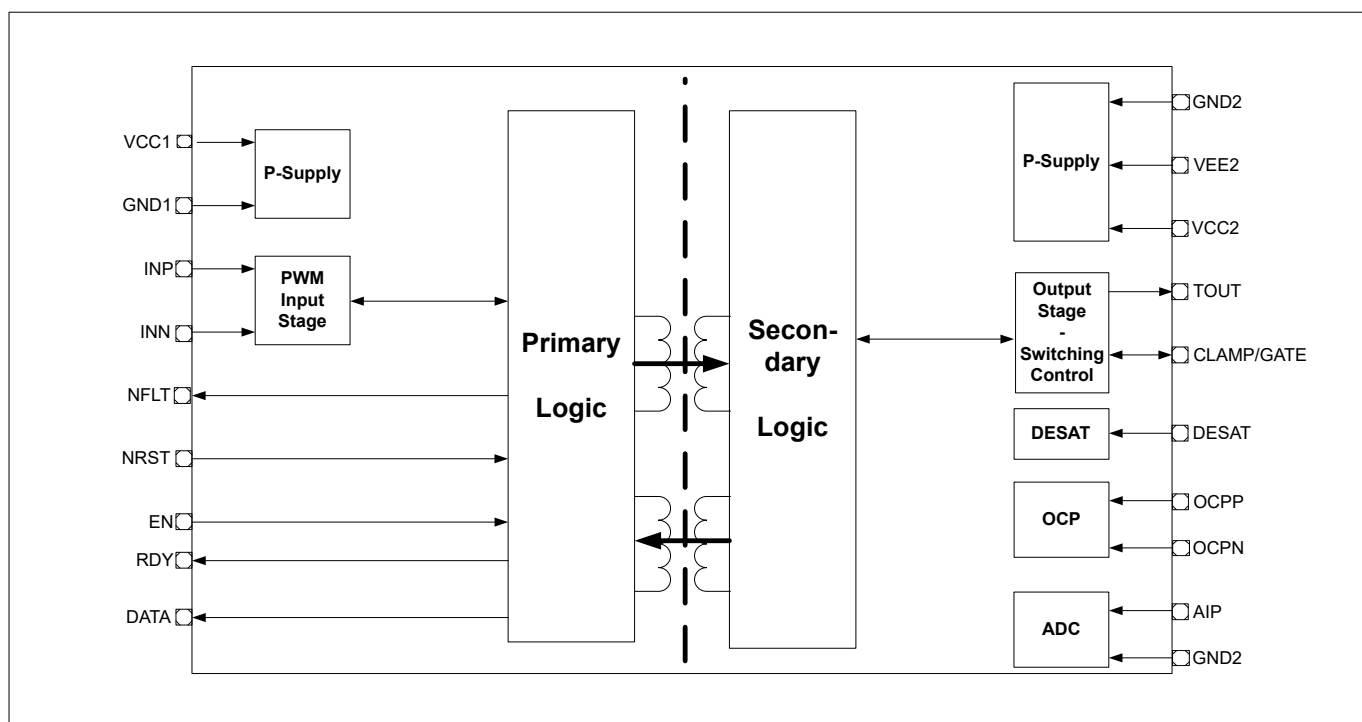
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**1 Block diagram**

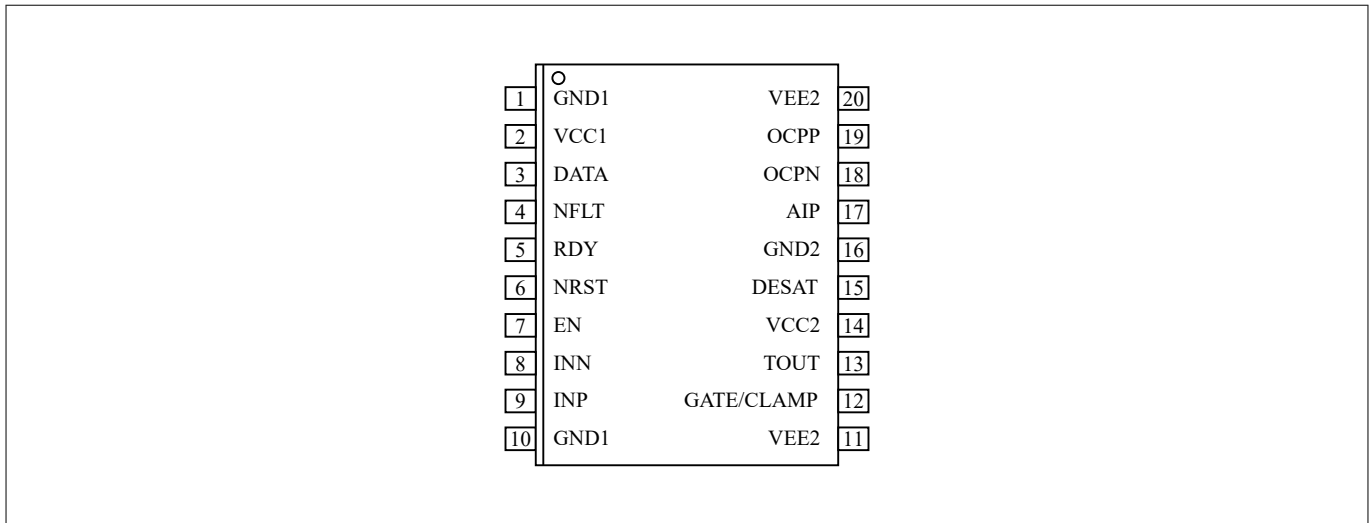
**1 Block diagram**



**Figure 1 Block diagram**

**2 Pin configuration**

**2 Pin configuration**



**Figure 2 Pin assignment**

**2.1 Pin definitions and functions**

**Table 1 Pin definition and functions**

Pin #	Pin name	I/O	Voltage class	Function
1	GND1	Ground	Primary ground	Ground connection for the primary side.
2	VCC1	Supply	Primary supply	5 V/3.3 V power supply for the primary side (referring to GND1).
3	DATA	Output	5 V primary	The data pin is used for ADC or diagnosis data. This pin is a push-pull output which is driving a PWM signal according to the data.
4	NFLT	Output	5 V primary	The fault open-drain signal is used to report failure events triggered by DESAT or OCP protection. As a result the pin is driven to low. This pin has to be connected externally to VCC1 with a pull-up resistance.
5	RDY	Output	5 V primary	The ready open-drain signal is used to report failure events like UVLO1, UVLO2, OVLO2, Life Sign Lost, Output Stage Error, Gate Monitoring Error, etc. As a result this pin is driven to low. This pin has to be connected externally to VCC1 with a pull-up resistance.
6	NRST	Input	5 V primary	The reset signal is used to clear the failure/fault events which triggered RDY or NFLT active low. The signal is clearing an error on rising edge. An internal pull-down resistance is driving this pin to low state in case the pin is floating.
7	EN	Input	5 V primary	The enable signal allows the logic on the primary side to enable or disable the device. The logic levels are according

**(table continues...)**

**2 Pin configuration**

**Table 1 (continued) Pin definition and functions**

Pin #	Pin name	I/O	Voltage class	Function
				to the used power supply. An internal weak pull-down resistance is disabling the device in case the pin is floating.
8	INN	Input	5 V primary	The inverting PWM signal is used for monitoring for shoot through protection. An internal weak pull-up resistor to VCC1 drives this input to high state in case the pin is floating.
9	INP	Input	5 V primary	The non-inverting PWM signal of the driver. An internal weak pull-down resistor to GND1 drives this input to low state in case the pin is floating.
10	GND1	Ground	Primary ground	Ground connection for the primary side.
11	VEE2	Supply	Secondary supply	Negative power supply for the secondary side (referring to GND2).
12	GATE/ CLAMP	Input/ Output	15 V secondary	The gate monitoring and clamp signal is monitoring the gate of the power switch and clamping the gate to VEE2 if the threshold VCLAMP is reached.
13	TOUT	Output	15 V secondary	The transistor drive voltage signal switches the power switch gate to VCC2 or VEE2, according to the PWM input.
14	VCC2	Supply	Secondary supply	Positive power supply for the secondary side (referring to GND2).
15	DESAT	Input	15 V secondary	The desaturation protection signal monitors the voltage across the power switch. An internal current source to VCC2 drives this signal to high level in case it is floating.
16	GND2	Ground	Secondary ground	Reference ground for the secondary side.
17	AIP	Input	5 V secondary	The ADC function can be used to monitor the DC-link voltage. The internal current source is disabled.
18	OCPN	Input	5 V secondary	The negative over current protection signal is differential therefore it should be always close to OCPP signal. A common-mode filter should be applied to the OCPP signal.
19	OCPP	Input	5 V secondary	The positive over current protection signal is differential therefore it should be always close to OCPN signal. A common-mode filter should be applied to the OCPN signal. An internal weak pull-up resistor drives this input to high state in case the pin is floating.
20	VEE2	Supply	Secondary supply	Negative power supply for the secondary side (referring to GND2).

**3 General product characteristics**

**3 General product characteristics**

**3.1 Absolute maximum ratings**

**Table 2 Absolute maximum ratings**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified). Absolute maximum ratings are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Absolute maximum ratings are not subject to production test, specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Positive power supply (primary)	$V_{VCC1\_MAX}$	-0.3	-	7	V	Referenced to GND1	PRQ-560
Positive power supply (secondary)	$V_{VCC2\_MAX}$	-0.3	-	30	V	Referenced to GND2	PRQ-561
Negative power supply (secondary)	$V_{VEE2\_MAX}$	-13	-	0.3	V	Referenced to GND2	PRQ-562
Power supply voltage difference (secondary) VCC2-VEE2	$V_{VCC2-VEE2\_MAX}$	-	-	40	V		PRQ-563
Voltages on any I/O pin on primary side (INP, INN, NRST, DATA, RDY, NFLT, EN)	$V_{INX\_MAX}$	-0.3	-	$V_{VCC1} + 0.3$	V	Referenced to GND1	PRQ-564
AIP voltage	$V_{AIP\_MAX}$	-0.3	-	$V_{VCC2} + 0.3$	V		PRQ-789
DESAT voltage	$V_{DESAT\_MAX}$	-0.3	-	$V_{VCC2} + 0.3$	V	Referenced to GND2	PRQ-566
OCP	$V_{OCP\_MAX}$	-2.8	-	2.8	V	Referenced to GND2	PRQ-788
OCPN	$V_{OCPN\_MAX}$	-2.8	-	2.8	V	Referenced to GND2	PRQ-831
Maximum Clamp/gate voltage	$V_{Clamp/Gate\_MAX}$	$V_{VEE2} - 0.3$	-	$V_{VCC2} + 0.3$	V	Referenced to GND2	PRQ-567
TOUT voltage	$V_{OUT\_MAX}$	$V_{VEE2} - 0.3$	-	$V_{VCC2} + 0.3$	V	Referenced to GND2	PRQ-568

**(table continues...)**



**3 General product characteristics**

**Table 2 (continued) Absolute maximum ratings**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified). Absolute maximum ratings are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Absolute maximum ratings are not subject to production test, specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
TOUT high output maximum current	$I_{\text{OUTH\_MAX}}$	-15	-	-	A	$t_{\text{MAX}} = 1.5 \mu\text{s}$ , non-repetitive	PRQ-569
TOUT low output maximum current	$I_{\text{OUTL\_MAX}}$	-	-	15	A	$t_{\text{MAX}} = 1.5 \mu\text{s}$ , non-repetitive	PRQ-570
Gate/Clamp low maximum output current	$I_{\text{Gate/Clamp\_Max}}$	-	-	15	A	$t_{\text{MAX}} = 1.5 \mu\text{s}$ , non-repetitive	PRQ-848
Current on output logic pins (DATA, RDY, NFLT)	$ I_{\text{OUTx\_MAX}} $	-	-	10	mA		PRQ-572
ESD immunity	$V_{\text{ESD\_HBM}}$	-2	-	2	kV	HBM according to AEC Q100-002, CDM according to AEC Q100-011	PRQ-573
Storage temperature	$T_{\text{s\_MAX}}$	-55	-	150	$^{\circ}\text{C}$		PRQ-575
Junction temperature	$T_{\text{J\_MAX}}$	-40	-	150	$^{\circ}\text{C}$		PRQ-790

**3.2 Functional range**

**Table 3 Functional range**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Positive power supply (primary)	$V_{\text{VCC1}}$	3	-	5.5	V	Referenced to GND1	PRQ-579
VCC1 ramp-up slew-rate	$t_{\text{RP1}}$	-	-	2000	V/ms		PRQ-797

**(table continues...)**

**3 General product characteristics**

**Table 3 (continued) Functional range**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VCC2 ramp-up slew-rate	$t_{RP2}$	0.65 0	–	1000	V/ms		PRQ-798
Negative power supply (secondary)	$V_{VEE2}$	-11.5	-5	0	V	Referenced to GND2	PRQ-581
VEE2 ramp-up slew-rate	$t_{RP3}$	-0.10 0	–	-100 0	V/ms		PRQ-799
Power supply voltage difference (secondary) VCC2-VEE2	$V_{VCC2-VEE2}$	–	–	25	V		PRQ-582
Junction temperature	$T_J$	-40	–	150	$^{\circ}\text{C}$		PRQ-588
Common mode transient immunity	$dV_{ISO}/dt$	-150	–	150	kV/ $\mu\text{s}$	For voltages up to 1000 V	PRQ-589
Voltages on any I/O pin on primary side (INP, INN, NRST, DATA, RDY, NFLT)	$V_{INx}$	0	–	$V_{VCC1}$	V	Referenced to GND1	PRQ-583

**3.3 Thermal characteristics**

The thermal capability of the device is depending on the used power module. The following formula and parameters can be used to calculate the maximum switching frequency for a dedicated power module:

$$f_{SW} = \frac{P_{SW} \cdot (R_{DSON-OSLN} + R_g)}{(V_{VCC2} - V_{VEE2})^2 \cdot C_{Gate} \cdot R_{DSON-OSLN}}$$

**Figure 3 Formula to calculate the maximum switching frequency in application**

Where the maximum switching losses are  $P_{SW} = P_{DIS2} - P_{IDLE\_sec}$ ,  $R_g$  is the external gate resistor,  $C_{Gate}$  is the maximum gate charge of the power switch, and  $R_{DSON-OSLN}$  is the internal gate resistor.

*Note:* This formula is only valid if ON/OFF resistors have the same value.

**3 General product characteristics**

**3.3.1 Thermal characteristics parameters**

**Table 4 Thermal characteristics parameters**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power Dissipation - Primary Chip	$P_{DIS1}$	–	40	–	mW	$T_{AMB} = 25^\circ\text{C}$ , $V_{VCC1} = 5\text{ V}$ , PWM duty cycle = 50%, Normal_Mode, no $C_{LOAD}$ , no $R_{LOAD}$ on TOUT, average value (peak current neglected)	PRQ-946
Power Dissipation - Secondary Chip	$P_{DIS2}$	–	300	–	mW	$T_{AMB} = 25^\circ\text{C}$ , $V_{VCC2} = \text{typ.}$ , $V_{VEE2} = \text{typ.}$ , PWM duty cycle = 50%, Normal_Mode, no $C_{LOAD}$ , no $R_{LOAD}$ on TOUT, average value (peak current neglected)	PRQ-947
Switching frequency	$f_{SW}$	–	25	430	kHz	$V_{VCC2} = 18\text{ V}$ , $V_{VEE2} = -5\text{ V}$ , $C_{Gate} = 9\text{ nF}$ , $R_g = 6\ \Omega$ , $T_{AMB} = 25^\circ\text{C}$	PRQ-839
Thermal Resistance Junction to Ambient (25°C)	$R_{THJA}$	–	85	–	K/W	$T_{amb} = 25^\circ\text{C}$	PRQ-932
Thermal Resistance Junction to Ambient (125°C)	$R_{THJA,125}$	–	71	–	K/W	$T_{AMB} = 125^\circ\text{C}$	PRQ-975
Thermal Resistance Junction to Case (bottom)	$R_{THJCBOT}$	–	60	–	K/W	$T_{amb} = 25^\circ\text{C}$	PRQ-933
Thermal Resistance Junction to Case (top)	$R_{THJCTOP}$	–	52	–	K/W	$T_{amb} = 25^\circ\text{C}$	PRQ-934
Thermal Resistance Junction to Board (25°C)	$R_{THJBOARD}$	–	45.4	–	K/W	$T_{amb} = 25^\circ\text{C}$ , power losses on secondary side $\leq 500\text{ mW}$ , power losses on primary side $\leq 50\text{ mW}$	PRQ-1031
$\Psi$ - Pseudo Thermal Resistance Junction to Case (top)	$R_{PSIJT}$	–	21	–	K/W	$T_{amb} = 25^\circ\text{C}$	PRQ-935

**3 General product characteristics**

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**3.4 Insulation characteristics**

**Table 5 Insulation characteristics for reinforced and basic insulation in compliance with DIN VDE V 0884-11:2017-01. Input to output test conditions according to method a) and b) follow the more stringent requirements as of reinforced insulation.**

Description	Symbol	Value	Unit
Installation classification per IEC 60664-1, Table F.1 for rated mains voltage $\leq 150 V_{RMS}$ for rated mains voltage $\leq 300 V_{RMS}$ for rated mains voltage $\leq 600 V_{RMS}$ for rated mains voltage $\leq 1000 V_{RMS}$		– I-IV I-IV I-III (IV for basic) I-II (III for basic)	–
Climatic classification		40/125/21	–
Pollution degree (IEC 60664-1)		2	–
Minimum external creepage	CPG	8	mm
Minimum external clearance	CLR	8	mm
Minimum comparative tracking index	CTI	400	–
Maximum repetitive insulation voltage	$V_{IORM, reinforced}$ $V_{IORM, basic}$	1767 1420	$V_{PEAK}$
Maximum rated transient insulation voltage	$V_{IOTM}$	8000	$V_{PEAK}$
Maximum surge insulation voltage for reinforced insulation Test voltage in subgroup #1 = $1.6 * V_{IOSM, reinforced} = 11kV$	$V_{IOSM, reinforced}$	6875	$V_{PEAK}$
Maximum surge insulation voltage for basic insulation Test voltage in subgroup #1 = $1.3 * V_{IOSM, basic} = 10.4kV$	$V_{IOSM, basic}$	8000	$V_{PEAK}$
Input to output test voltage, method b) $V_{ini, b} = 1.2 * V_{iotm}, V_{pd(m)} = V_{iorm, reinforced} * 1.875$ , 100% production test with $t_{ini, b} = 1 s$	$q_{pd}$	< 5	pC
Input to output test voltage, method a) $V_{ini, a} = V_{iotm}, V_{pd(m)} = V_{iorm, reinforced} * 1.6$ , sample test with $t_{ini, a} = 60 s$	$q_{pd}$	< 5	pC
Insulation resistance at $100\text{ °C} \leq T_{amb} \leq 125\text{ °C}$ , $V_{io} = 500 V$	$R_{IO}$	$>10^{12}$	$\Omega$
Insulation resistance at $T_S = 150\text{ °C}$ , $V_{io} = 500 V$	$R_{IO\_S}$	$>10^9$	$\Omega$

**Table 6 Insulation characteristics recognized according to UL 1577**

Parameter	Symbol	Characteristic	Unit
Insulation withstand voltage / 1 min	$V_{ISO}$	5700	V(rms)
Insulation test voltage / 1 s	$V_{ISO}$	6000	V(rms)

(table continues...)  
 Datasheet

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**3 General product characteristics**

**Table 6** (continued) **Insulation characteristics recognized according to UL 1577**

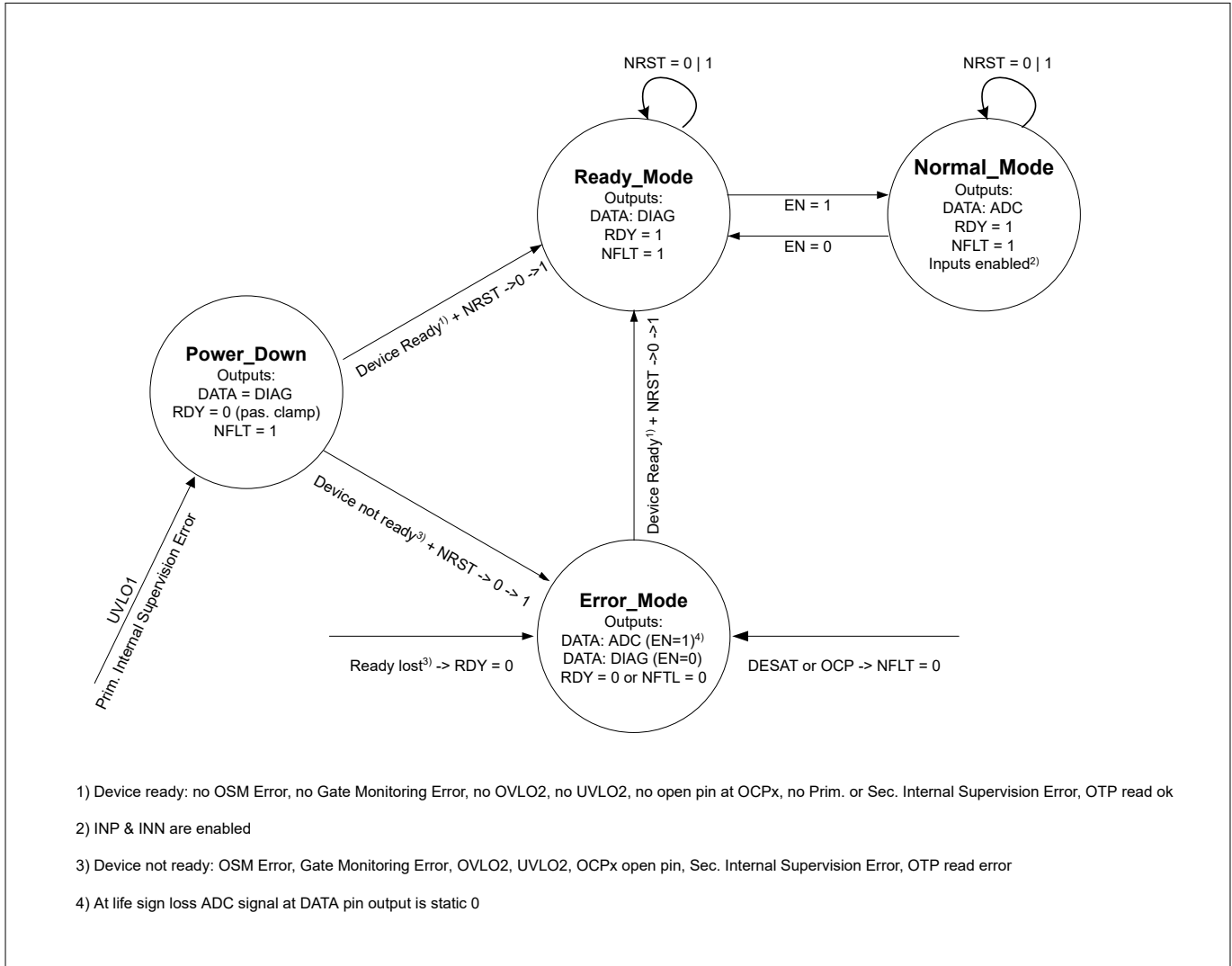
<b>Parameter</b>	<b>Symbol</b>	<b>Characteristic</b>	<b>Unit</b>
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*Note:* The insulation characteristics only apply when the device is operated within the safety limits given by the absolute maximum ratings.

**4 Operating modes**

**4 Operating modes**

**4.1 Operating modes diagram**



**Figure 4 Operating modes state diagram**

*Note:*

- Life sign lost will be detected only if communication has been established once.
- External pull-up required on RDY and NFLT (open drain output)

**4.2 Operating modes description**

The device has the following modes which it can operate in:

- Ready\_Mode (not enabled)
- Error\_Mode (Failure/Fault event occurred)
- Normal\_Mode (Device enabled)

**Reset**

If the NRST signal is low the device keeps its operating mode (no influence on PWM). Further the rising edge on NRST signal will reset the failure/fault event memory.

## 4 Operating modes

### Power Down and Start up

The device is in Power\_Down\_Mode at start-up or if an UVLO1 error occurs. In both cases it will not operate. If the device is partly supplied (e.g. VCC1 only) the device will enter Error\_Mode. Therefore supplies should rise within the specified slew rates to a valid voltage level according to given operating conditions. Afterwards a rising edge on NRST will bring the device into Ready\_Mode (no Failure or Fault Event occurred).

### Mode Transitions

Once in Ready\_Mode the change to Normal\_Mode can be done with setting EN signal to "high level" (voltage level differs with VCC1 level), changing it to "low level" is also the returning into Ready\_Mode. The transition into Error\_Mode can only be done with the according events which are:

- OCP event
- DESAT event
- UVLO2 event
- OVLO2 event
- Sec. Internal Supervision Error
- Output Stage Monitor Error
- Gate Monitoring Error
- OCPx pin open
- OTP read error

### Error\_Mode

In Error\_Mode a "low level" on signal EN will issue diagnosis information on the DATA pin. This diagnosis information states details about the failure root cause. A "high level" on signal EN issues the ADC information, identical to Normal\_Mode.

A rising edge on NRST and no failure or fault active will transition the device back to Ready\_Mode (or to Normal\_Mode if signal EN is set). In Ready\_Mode diagnosis information is available on the DATA pin. See also the operating modes diagram for further information.

## 4.3 Single failure events in Normal\_Mode

**Table 7 Single failure events in Normal\_Mode**

Failure Event	Output stage reaction	Resulting pin status changes
DESAT when TOUT = high (VCC2)	Safe turn-off	NFLT = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
OCP when TOUT = high (VCC2)	Safe turn-off	NFLT = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
Gate monitoring error	Safe turn-off when TOUT = high (VCC2)	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
OSM error	Tri-state	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
UVLO2	Normal switch-off	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
OVLO2	Normal switch-off	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
UVLO1	Normal switch-off	RDY = 0; DATA = 0
Prim. internal supervision error	Normal switch-off	RDY = 0; DATA = 0
Sec. internal supervision error	Normal switch-off	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
OCPx pin open	Normal switch-off	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)

**5 Power supply**

**5 Power supply**

**5.1 Bipolar and unipolar supplies**

The device is designed to support two different supply configurations, bipolar supply and unipolar supply.

*Note: In bipolar supply the driver is typically supplied with a positive voltage of 15 V at VCC2 and a negative voltage of -5 V at VEE2 (referenced to GND2). The negative supply prevents a dynamic turn on due to the additional charge which is generated from the input capacitance current of the power switch times the negative supply voltage. GATE/CLAMP has to be connected to the gate of the power switch in all power supply configurations.*

**5.2 Electrical characteristics power supply**

**Table 8 Electrical characteristics power supply**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Quiescent Current Input Chip (VCC1)	$I_{QVCC1}$	3	5	-	mA	Ready_Mode, all primary I/Os without impact on Ready_Mode open, $V_{VCC1} = 5\text{ V}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$	PRQ-937
Operating Current VCC1 (TOUT = high (VCC2))	$I_{OPVCC1\_ON}$	-	10	12	mA	Normal_Mode, INN = 0, INP = 1, EN = 1, NRST = 1, outputs open, $V_{VCC1} = 5\text{ V}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$	PRQ-938
Operating Current VCC1 (TOUT = low (VEE2))	$I_{OPVCC1\_OFF}$	-	5.5	7	mA	Normal_Mode, INN = 0, INP = 0, EN = 1, NRST = 1, outputs open, $V_{VCC1} = 5\text{ V}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$	PRQ-939
Operating Current VCC2 (TOUT = high (VCC2))	$I_{OPVCC2\_ON}$	-	11	13	mA	Normal_Mode, INN = 0, INP = 1, EN = 1, NRST = 1, primary outputs open, OCPx = 0, DESAT = 0, Gate shorted to TOUT, $V_{VCC1} = 5\text{ V}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$ , other pins open	PRQ-1036
Operating Current VCC2 (TOUT = low (VEE2))	$I_{OPVCC2\_OFF}$	6	11	13	mA	Normal_Mode, INN = 0, INP = 0, EN = 1, NRST = 1, primary outputs open, OCPx = 0, DESAT = 0, Gate shorted to TOUT, $V_{VCC1} = 5\text{ V}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$ , other pins open	PRQ-1037
Operating Current VEE2 (TOUT = high (VCC2))	$I_{OPVEE2\_ON}$	-	1.5	2	mA	Normal_Mode, INN = 0, INP = 1, EN = 1, NRST = 1, primary outputs open, OCPx = 0, DESAT = 0, Gate shorted to TOUT, $V_{VCC1} = 5\text{ V}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$ , other pins open	PRQ-944
Operating Current VEE2	$I_{OPVEE2\_OFF}$	0.5	1.5	2	mA	Normal_Mode, INN = 0, INP = 0, EN = 1, NRST = 1, primary outputs open, OCPx = 0,	PRQ-945

**(table continues...)**



**5 Power supply**

**Table 8 (continued) Electrical characteristics power supply**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
(TOUT = low (VEE2))						DESAT = 0, Gate shorted to TOUT, $V_{VCC1} = 5\text{ V}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$ , other pins open	

**6 Switching characteristics**

**6 Switching characteristics**

**6.1 Functional description switching**

The voltage on pin TOUT ranges from  $V_{VEE2}$  to  $V_{VCC2}$  (referenced to GND2).

The device supports short propagation delay for On and Off switching of  $t_{PDON}$  and  $t_{PDOFF}$ .

**6.2 Electrical characteristics switching**

**Table 9 Electrical characteristics switching**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High level output peak current	$I_{OUTH}$			- 12	A	INP = $V_{VCC1}$ , INN = $V_{GND1}$ , EN = $V_{VCC1}$ , TOUT = $V_{VCC2}$ , CLAMP/GATE = $V_{VEE2}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$ , $C_{LOAD} = 200\text{ nF}$	PRQ-662
Low level output peak current	$I_{OUTL}$	12			A	INP = $V_{GND1}$ , INN = $V_{GND1}$ , EN = $V_{VCC1}$ , TOUT = $V_{VEE2}$ , CLAMP/GATE = $V_{VCC2}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$ , $C_{LOAD} = 200\text{ nF}$	PRQ-663
Propagation delay - On	$t_{PDON}$	40	60	120	ns	$V_{CC1} = \text{typ.}$ , $V_{CC2} = \text{typ.}$ , $V_{EE2} = \text{typ.}$ , Start: INP rising edge at $V_{\text{digital,input(high)}}$ , Stop: TOUT rising edge at $V_{VEE2} + 1.5\text{ V}$ , no load, no gate resistance	PRQ-770
Propagation delay - Off	$t_{PDOFF}$	40	60	120	ns	$V_{CC1} = \text{typ.}$ , $V_{CC2} = \text{typ.}$ , $V_{EE2} = \text{typ.}$ , Start: INP falling edge at $V_{\text{digital,input(low)}}$ , Stop: TOUT falling edge at $V_{VCC2} - 1.5\text{ V}$ , no load, no gate resistance	PRQ-851
Propagation delay distortion	$t_{\text{Prop,dis}}$	-20	-	20	ns	$t_{PDON} - t_{PDOFF}$ , $t_{PDON}$ & $t_{PDOFF}$ measured @ same $T_{JUNC}$	PRQ-803
Propagation delay EN to turn-on (INP = high)	$t_{PDENON}$	10	60	120	ns	$V_{VCC1} = \text{typ.}$ ; $V_{VCC2} = \text{typ.}$ , $V_{VEE2} = \text{typ.}$ , INP = high, INN = GND1, TOUT = $V_{VEE2} + 1.5\text{ V}$ , referring to VEE2 (rising edge)	PRQ-968
Propagation delay EN to turn-off (INP = high)	$t_{PDENOFF}$	10	60	120	ns	$V_{VCC1} = \text{typ.}$ , $V_{VCC2} = \text{typ.}$ , $V_{VEE2} = \text{typ.}$ , INP = high, INN = GND1, TOUT = $V_{VCC2} - 1.5\text{ V}$ referring to VEE2 (falling edge)	PRQ-967
TOUT rise time 90 %	$t_{\text{Rise1}}$	-	-	55	ns	no $C_{LOAD}$ , no $R_{LOAD}$ , $V_{VCC2} = \text{typ.}$ , $V_{VEE2} = \text{typ.}$ , $V_{TOUT} = V_{VEE2} + 1.5\text{ V}$ to $V_{TOUT} = V_{VCC2} - 1.5\text{ V}$	PRQ-801
TOUT rise time 70 %	$t_{\text{Rise2}}$	-	-	35	ns	no $C_{LOAD}$ , no $R_{LOAD}$ , $V_{VCC2} = \text{typ.}$ , $V_{VEE2} = \text{typ.}$ , $V_{TOUT} = V_{VEE2} + 1.5\text{ V}$ to $V_{TOUT} = V_{VCC2} - 6\text{ V}$	PRQ-958

**(table continues...)**

**6 Switching characteristics**

**Table 9 (continued) Electrical characteristics switching**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Fall time	$t_{\text{Fall}}$	–	–	45	ns	No $C_{\text{LOAD}}$ , no $R_{\text{LOAD}}$ , $V_{\text{VCC2}} = \text{typ.}$ , $V_{\text{VEE2}} = \text{typ.}$ , $V_{\text{TOUT}} = V_{\text{VCC2}} - 1.5 \text{ V}$ to $V_{\text{TOUT}} = V_{\text{VEE2}} + 1.5 \text{ V}$	PRQ-802
TOUT RDSON High-side	$R_{\text{DS(on)-OSHN}}$		0.30		$\Omega$	N-MOS, tolerances according to $R_{\text{DS(on)-OSLN}}$	PRQ-1032
TOUT RDSON High-side P&N	$R_{\text{DS(on)-OSHtot}}$	0.3	–	1	$\Omega$	N-MOS and P-MOS, voltage drop $V_{\text{VCC2}} - V_{\text{TOUT}} < 1 \text{ V}$	PRQ-849
TOUT RDSON Low-side	$R_{\text{DS(on)-OSLN}}$	0.07	–	0.35	$\Omega$	N-MOS, voltage drop $V_{\text{TOUT}} - V_{\text{VEE2}} < 1 \text{ V}$	PRQ-850

*Note: The defined minimum/maximum value of  $I_{\text{OUTx}}$  is the minimum current which the device delivers under the given conditions. In general the device is capable to deliver higher output currents than the defined minimum/maximum. The maximum output current needs to be limited by an external gate resistor to stay inside the defined absolute maximum rating parameters regarding maximum peak current (equivalent energy needs to be considered) and maximum junction temperature.*

7 Protection and monitoring functions

7 Protection and monitoring functions

7.1 DESAT protection

7.1.1 Functional description DESAT protection

The device monitors the voltage across the power switch when TOUT = high(VCC2), after the DESAT blanking time is elapsed. If the corresponding reference level ( $V_{DESATX}$ ) is reached, it issues a safe turn-off within  $t_{DESAT2OFF}$ , then changes into Error\_Mode and signals a NFLT low in  $t_{NFLT\_DESAT}$ .

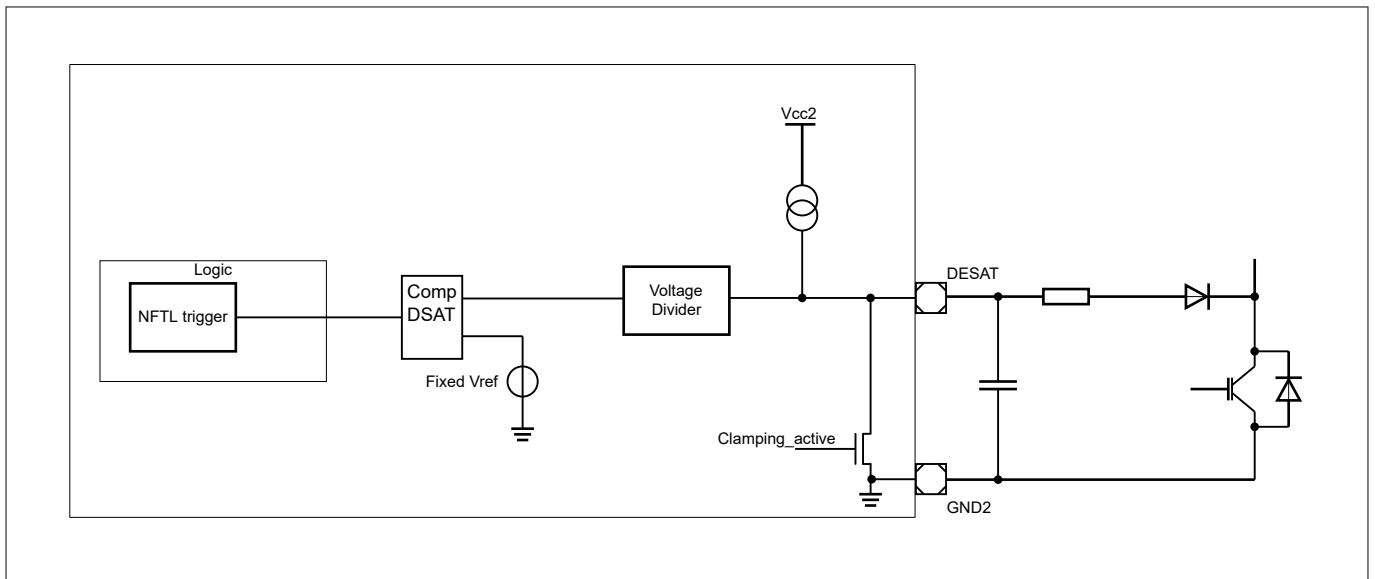
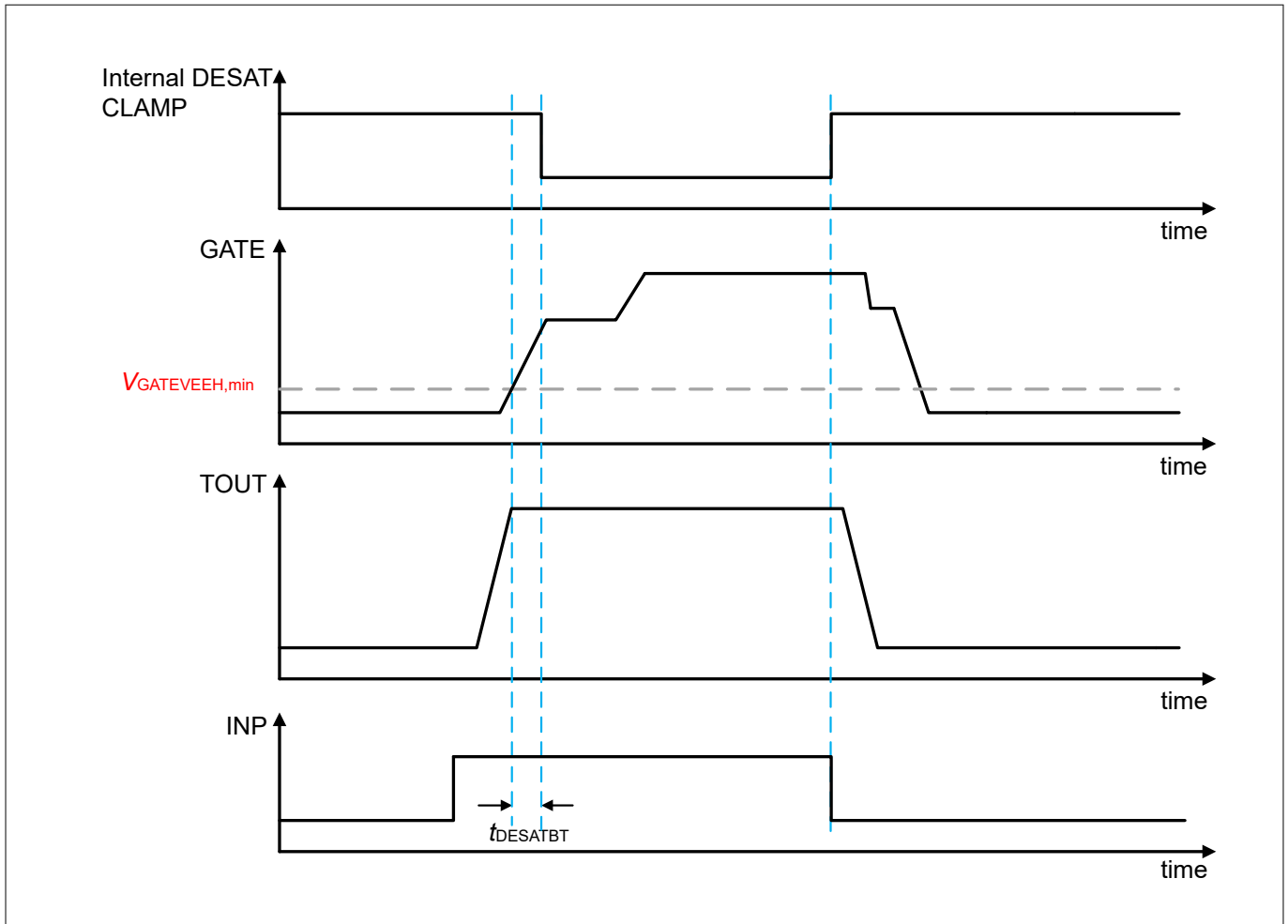


Figure 5 DESAT diagram of principal functionality

The DESAT pin has an internal clamping which clamps DESAT to  $V_{DESATL}$  in case TOUT = low (VEE2), TOUT =  $V_{SOFFPLT}$  or in case of OSM (tristate).

**7 Protection and monitoring functions**



**Figure 6** DESAT clamping and blanking timing diagram

**7.1.2 Electrical characteristics DESAT protection**

**Table 10** Electrical characteristics DESAT protection

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DESAT reference level	$V_{DESAT0}$	8.6	9	9.3	V	$V_{CC2} = \text{typ.}, V_{EE2} = \text{typ.}$	PRQ-734
DESAT current source	$I_{DESATCS}$	-550	-500	-450	$\mu\text{A}$	$V_{CC2} = \text{typ.}, V_{EE2} = \text{typ.}, V_{DESAT} \leq 10\text{ V}$	PRQ-800
DESAT low voltage	$V_{DESATL}$	0	200	300	mV	Referenced to GND2, DESAT clamping enabled, $I_{\text{sink}} = 5\text{ mA}$	PRQ-693

**(table continues...)**

**7 Protection and monitoring functions**

**Table 10 (continued) Electrical characteristics DESAT protection**

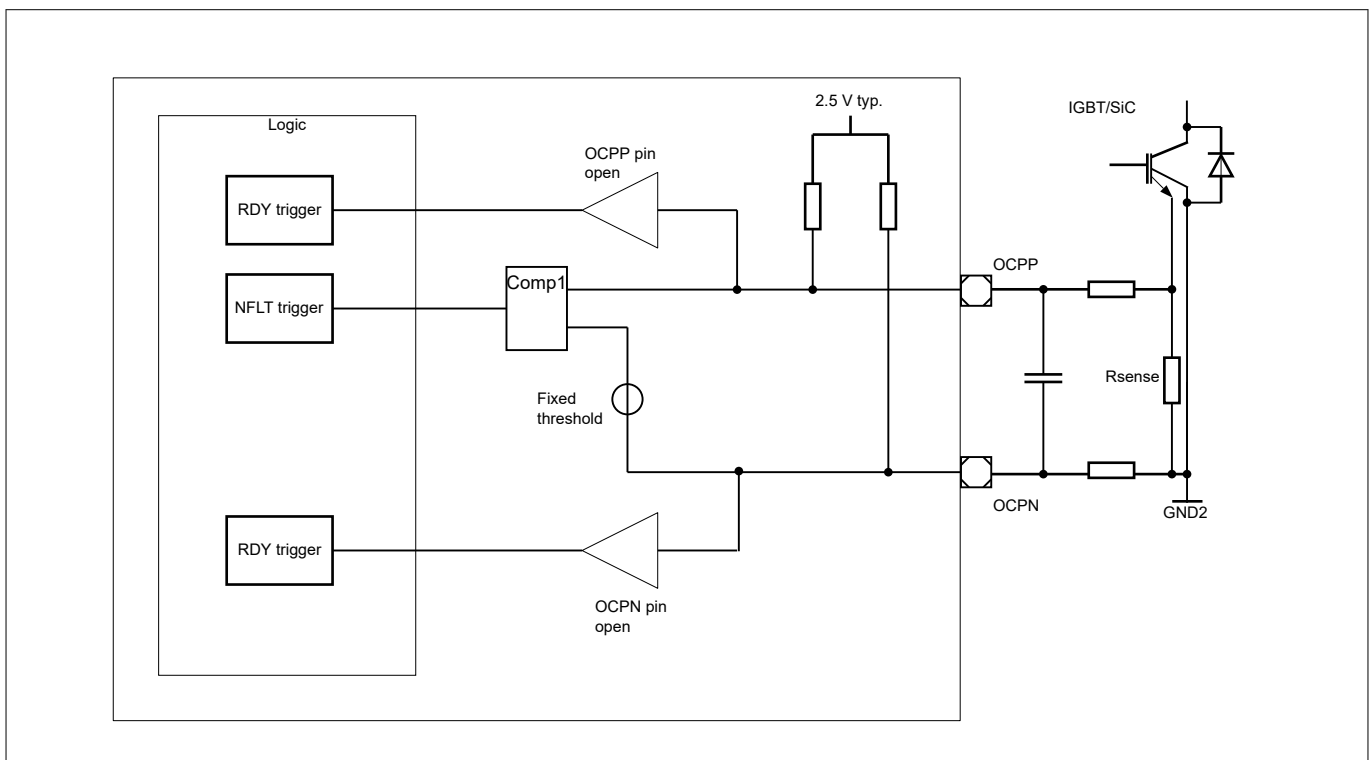
$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DESAT detection & reaction time	$t_{\text{DESAT2OFF}}$	100	300	400	ns	$V_{\text{DESAT\_Overdrive}} = 2\text{ V}$ , Slew rate @ DESAT = $10\text{ V}/\mu\text{s}$ ; $\text{TOUT} = V_{\text{VCC2}} - 1.5\text{ V}$ , after DESAT blanking time elapsed, $C_{\text{LOAD\_TOUT}} = \text{no load}$ , no resistive load	PRQ-841
DESAT blanking time	$t_{\text{DESATBT}}$	120	320	400	ns	From $V_{\text{GATEVEEH}}$ to release of clamping (Desat pin voltage rising above $0.5\text{ V}$ , with internal current source, no external $C_{\text{DESAT}}$ ), no $C_{\text{Load}}/R_{\text{Load}}$ on TOUT	PRQ-969
DESAT input voltage range	$V_{\text{DESAT}}$	0	–	$V_{\text{VCC2}}$	V	Referenced to GND2	PRQ-690

**7.2 Over Current Protection (OCP)**

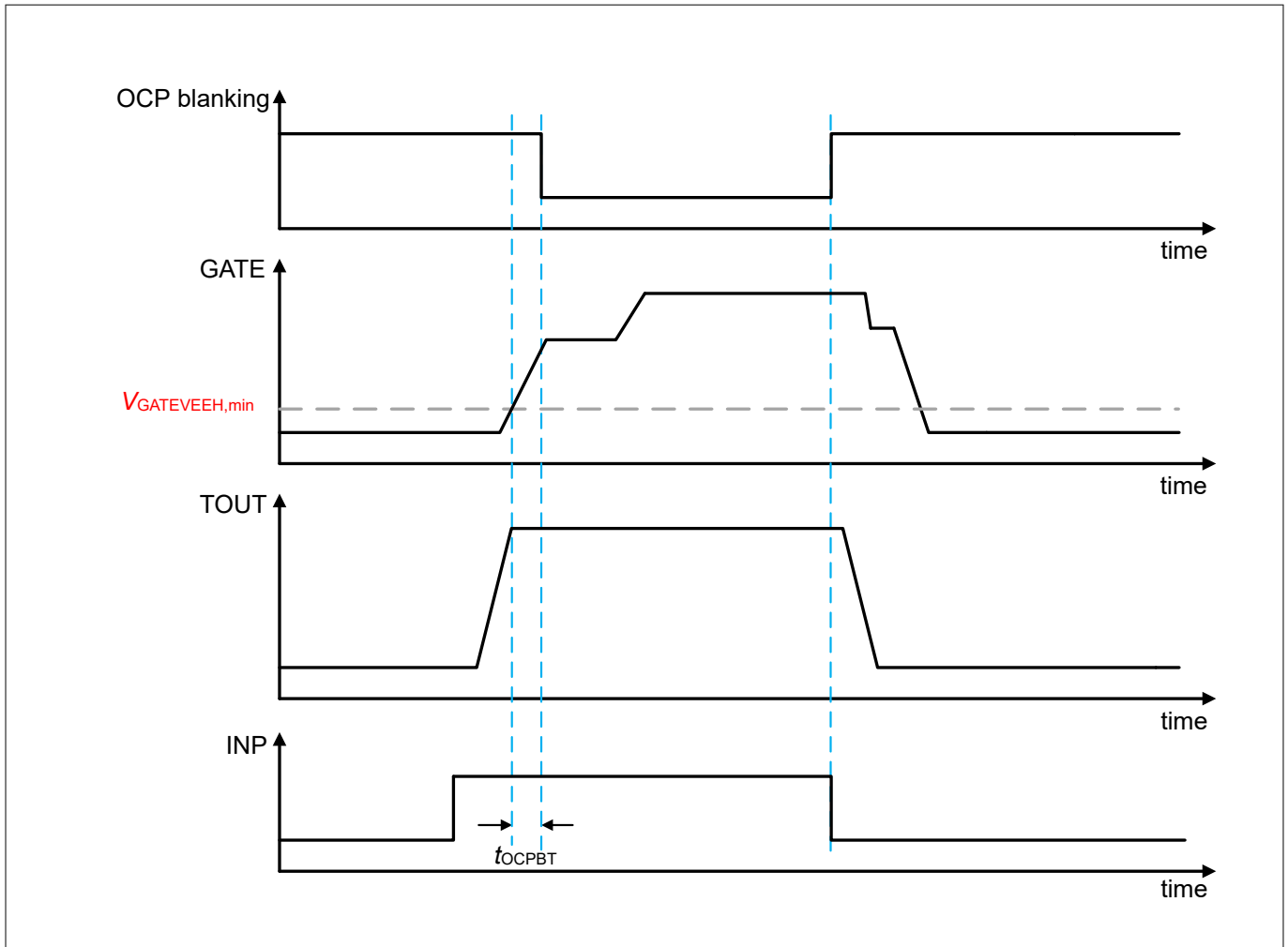
**7.2.1 Functional description OCP protection**

The device monitors the voltage difference between OCPP and OCPN when TOUT = high (VCC2) after the OCP blanking time is elapsed. If the corresponding reference level ( $V_{\text{OCPDx}}$ ) is reached, it issues a safe turn-off within  $t_{\text{OCP2OFF}}$ , then changes into Error\_Mode and signals a NFLT low in  $t_{\text{NFLT\_OCP}}$ .



**Figure 7 OCP diagram of principal functionality**

**7 Protection and monitoring functions**



**Figure 8** OCP blanking time

**7.2.2 Electrical characteristics OCP protection**

**Table 11** Electrical characteristics OCP

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overcurrent error detection threshold	$V_{\text{OCPD1}}$	270	300	330	mV	$V_{\text{OCPP}} - V_{\text{OCPN}}$	PRQ-695
OCP & OCPN pull-up resistance	$R_{\text{PUOCP2}}$	26	38	50	k $\Omega$		PRQ-697
OCP & OCPN voltage	$V_{\text{OCP}}$	-1	-	1	V	referring to GND2	PRQ-793

**(table continues...)**

**7 Protection and monitoring functions**

**Table 11 (continued) Electrical characteristics OCP**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCP detection & reaction time	$t_{\text{OCP2OFF}}$	100	300	400	ns	$V_{\text{OCP\_Overdrive}} = 200 \text{ mV}$ , slew rate = 100 mV/ns, TOUT = $V_{\text{VCC2}} - 1.5 \text{ V}$ , after OCP blanking time elapsed, $C_{\text{LOAD\_TOUT}} = \text{no load}$ , no resistive load	PRQ-842
OCP blanking time	$t_{\text{OCPBT}}$	120	320	400	ns	From $V_{\text{GATEVEEH}}$ to release of blanking. $V_{\text{OCP\_Overdrive}} = 200 \text{ mV}$ , slew rate = 100 mV/ns, no $C_{\text{Load}}/R_{\text{Load}}$ on TOUT	PRQ-1014
OCP pin open detection voltage	$V_{\text{OCPOPEN}}$	2.2	2.45	2.6	V		PRQ-1030

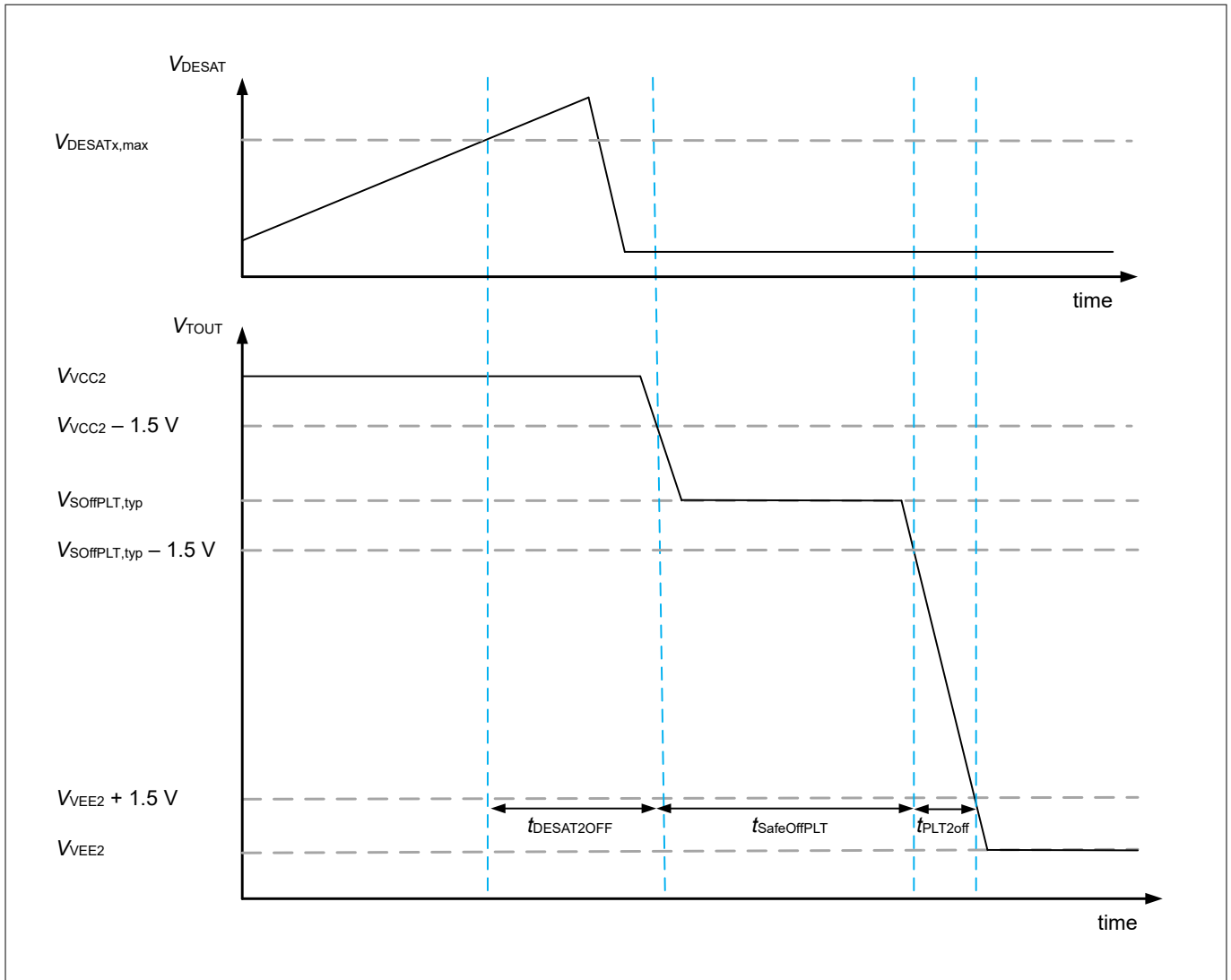
**7.3 Safe turn-off**

**7.3.1 Functional description safe turn-off**

The device enables a two-level turn-off in case of a fault.



**7 Protection and monitoring functions**



**Figure 9 Two level turn-off principle for safe turn-off**

- Note:
- Safe turn-off is only enabled at DESAT, OCP and gate monitoring error (if TOUT = high (VCC2) events).
  - DESAT is only used as an example, can be replaced by OCP and gate monitoring.

**7.3.2 Electrical characteristics safe turn-off**

**Table 12 Electrical characteristics safe turn-off**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Safe turn-off plateau time	$t_{SafeOffPLT}$	1	–	1.5	$\mu s$		PRQ-918
Plateau to turn-off time	$t_{PLT2off}$	10	–	50	ns	No $R_{Load}$ , no $C_{Load}$	PRQ-973

**(table continues...)**

**7 Protection and monitoring functions**

**Table 12 (continued) Electrical characteristics safe turn-off**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Safe turn-off plateau voltage level	$V_{SOFFPLT}$	8.46	9	9.54	V	$V_{VCC2} \geq V_{SOFFPLT,max} + 2\text{ V}$ , $C_{LOAD\_TOUT} = 68\text{ nF}$ , $R_{LOAD\_TOUT} = 1.7\ \Omega$	PRQ-919

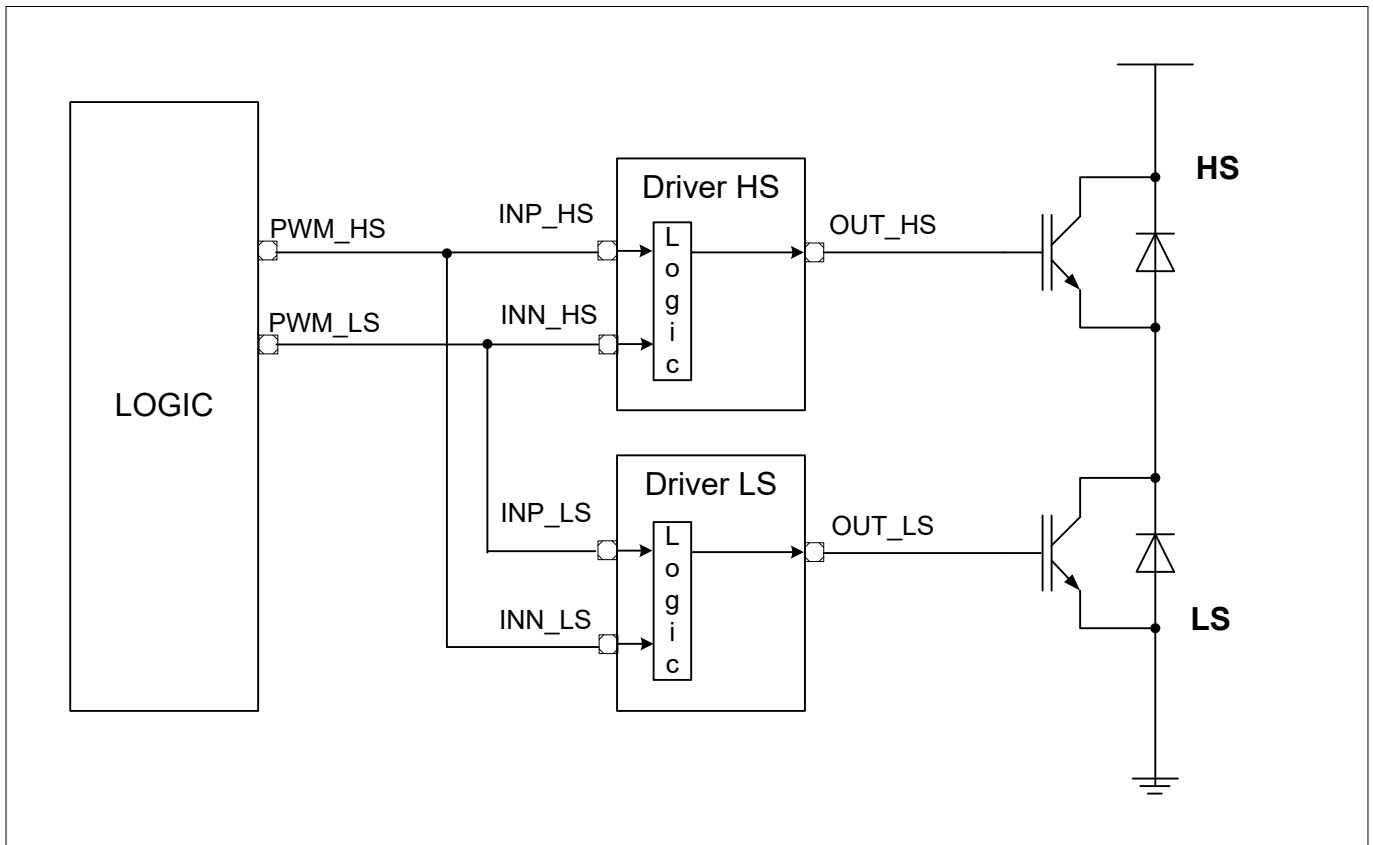
**7.4 Shoot Through Protection (STP)**

**7.4.1 Functional description STP**

The device has a Shoot Through Protection (STP) function to prevent both high-side and low-side switches to be activated simultaneously.

*Note:* STP is always active. However, setting the INN pin to GND1 deactivates the function.

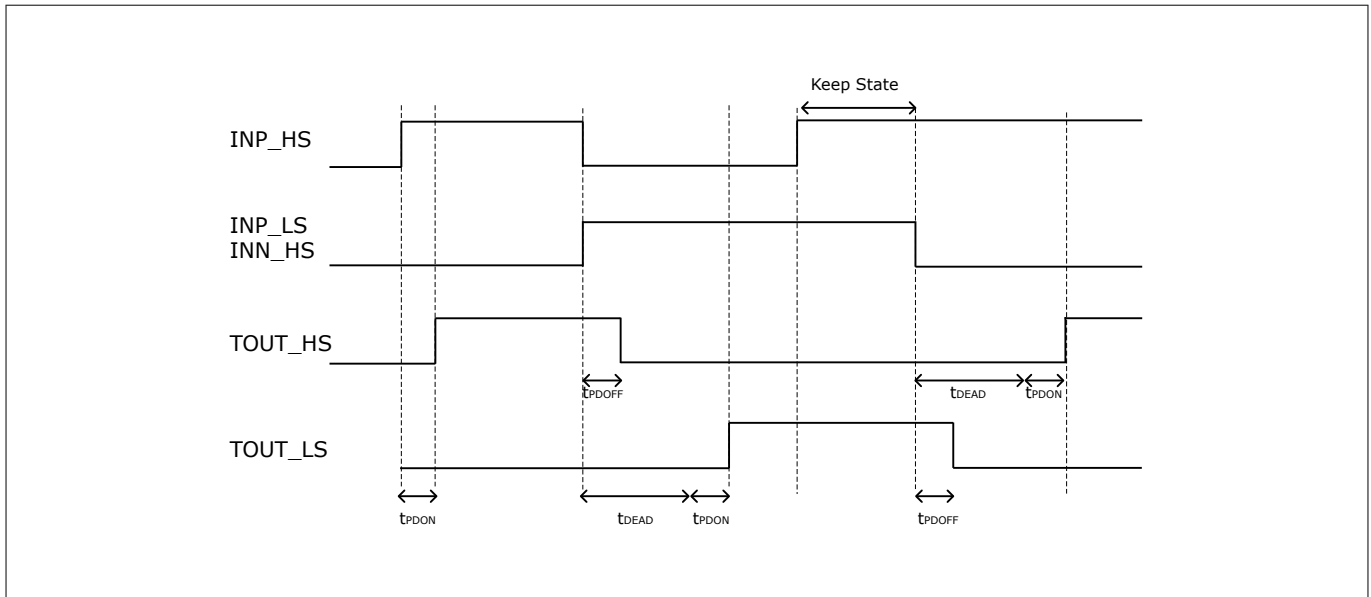
If one of the drivers is in ON state, the driver’s counterpart PWM input is inhibited, preventing it to turn on.



**Figure 10 Shoot through protection application diagram**

The device follows the shoot through protection timing diagram shown below:

**7 Protection and monitoring functions**



**Figure 11** Shoot through protection timing diagram

**7.4.2 Electrical characteristics STP**

**Table 13** Electrical characteristics STP

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Dead time for shoot through protection	$t_{DEAD3}$	650	800	950	ns		PRQ-729

**7.5 Power supply monitoring**

**7.5.1 Functional description power supply monitoring**

The device is equipped with an undervoltage lockout for the primary supply (VCC1) and secondary supply (VCC2) in order to ensure correct switching of the power switch.

*Note:* In all under voltage conditions the ASC signal still works until the voltage drops below VASCOFF at VCC2.

The device turns off the power switch and ignores signals at INP and INN (goes into Power\_Down Mode) if the power supply VCC1 drops below  $V_{UVLO1L}$ . It returns to Ready\_Mode if the voltage at VCC1 is above  $V_{UVLO1H}$  and the device received a rising edge at NRST.

The device turns off the power switch within  $t_{UVLO22OFF}$  and ignores signals at INP and INN (go into Error\_Mode) within  $t_{PS2RDY}$  if the power supply VCC2 drops below  $V_{UVLO2L\_X}$ . It returns to Ready\_Mode if the voltage at VCC2 is above  $V_{UVLO2H\_X}$  and the device received a rising edge at NRST.

The device is equipped with an overvoltage lockout for the secondary supply VCC2 in order to prevent damage of the power switch.

## 7 Protection and monitoring functions

*Note:* The ASC signal will overwrite the turn-off command, which may lead to damage of the power switch (power switch).

The device turns off the power switch within  $t_{OVLO22OFF}$  and ignores signals at INP and INN (go into Error\_Mode) within  $t_{PS2RDY}$  if the power supply  $V_{VCC2}$  rises above  $V_{OVLO2H\_x}$ . It returns to Ready\_Mode if the voltage  $V_{VCC2}$  is below  $V_{OVLO2L\_x}$  and the device received a rising edge at NRST.

- Note:*
- In Error\_Mode, RDY changes to 0.
  - Turn-off means normal switch-off and not a safe turn-off.
  - Exception: ASC function  $\rightarrow$  TOUT = high (VCC2).

### 7.5.2 Electrical characteristics power supply monitoring

**Table 14** Electrical characteristics power supply monitoring

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UVLO1 threshold low	$V_{UVLO1L}$	2.6	2.75	–	V	@ VCC1, referenced to GND1	PRQ-741
UVLO1 threshold high	$V_{UVLO1H}$	–	2.85	2.95	V	@ VCC1, referenced to GND1	PRQ-740
UVLO1 hysteresis	$V_{UVLO1HYS}$	–	80	100	mV		PRQ-742
OVLO2 threshold high	$V_{OVLO2H\_3}$	17.8	18.5	19.0	V	@ VCC2, referenced to GND2	PRQ-889
OVLO2 threshold low	$V_{OVLO2L\_3}$	17.1	17.7	18.2	V	@ VCC2, referenced to GND2	PRQ-890
OVLO2 hysteresis	$V_{OVLO2HYS}$	400	800	–	mV	$V_{OVLO2H\_x} - V_{OVLO2L\_x}$	PRQ-896
UVLO2 threshold high	$V_{UVLO2H\_1}$	12.2	12.6	13	V	@ VCC2, referenced to GND2	PRQ-750
UVLO2 threshold low	$V_{UVLO2L\_1}$	11.4	11.8	12.2	V	@ VCC2, referenced to GND2	PRQ-752
UVLO2 hysteresis	$V_{UVLO2HYS}$	720	800	880	mV		PRQ-755
UVLO1 detection & reaction time	$t_{UVLO12OFF}$	–	500	800	ns	Slewrate = 2 V/ $\mu$ s, Overdrive = +/- 300 mV	PRQ-914

(table continues...)

**7 Protection and monitoring functions**

**Table 14 (continued) Electrical characteristics power supply monitoring**

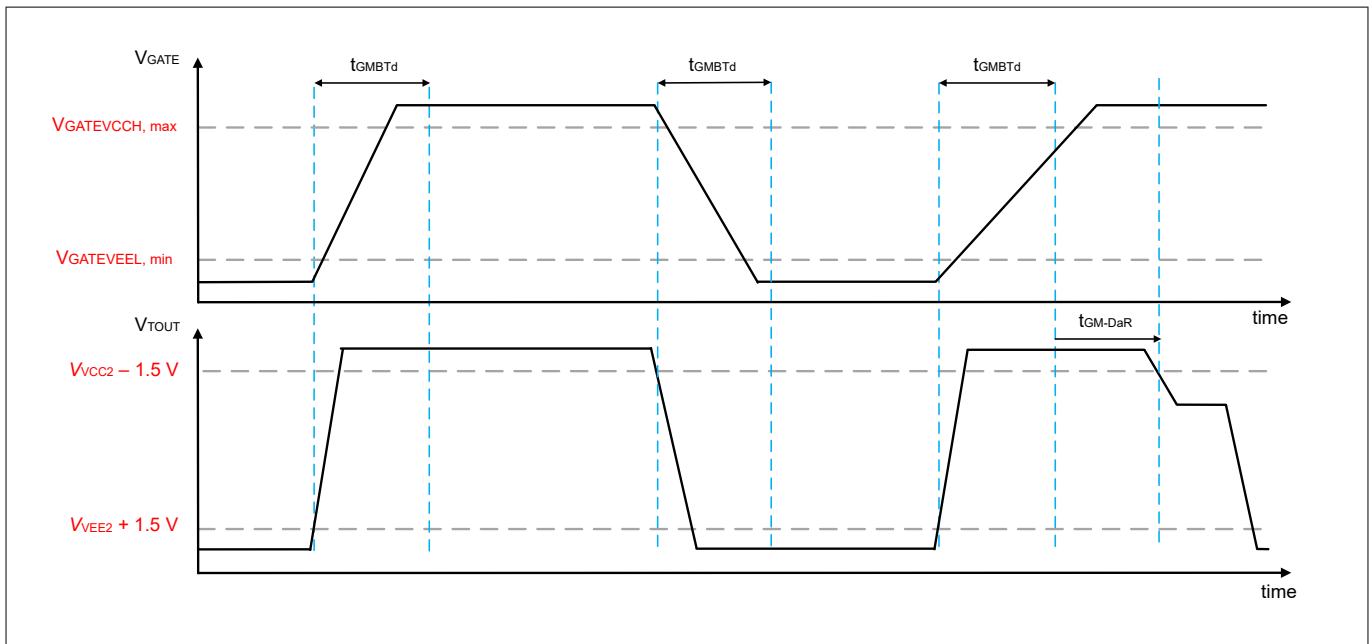
$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UVLO2 detection & reaction time	$t_{UVLO22OFF}$	-	500	800	ns	Slewwrate=10 V/ $\mu$ s; Overdrive=+/-200 mV	PRQ-915
OVLO2 detection & reaction time	$t_{OVLO22OFF}$	-	500	800	ns	Slewwrate=10 V/ $\mu$ s; Overdrive=+/-200 mV	PRQ-916
Power supply monitoring detection and notification time	$t_{PS2RDY}$	-	-	2.5	$\mu$ s	VCC2 = typ., VEE2 = typ.	PRQ-976

**7.6 Gate monitoring**

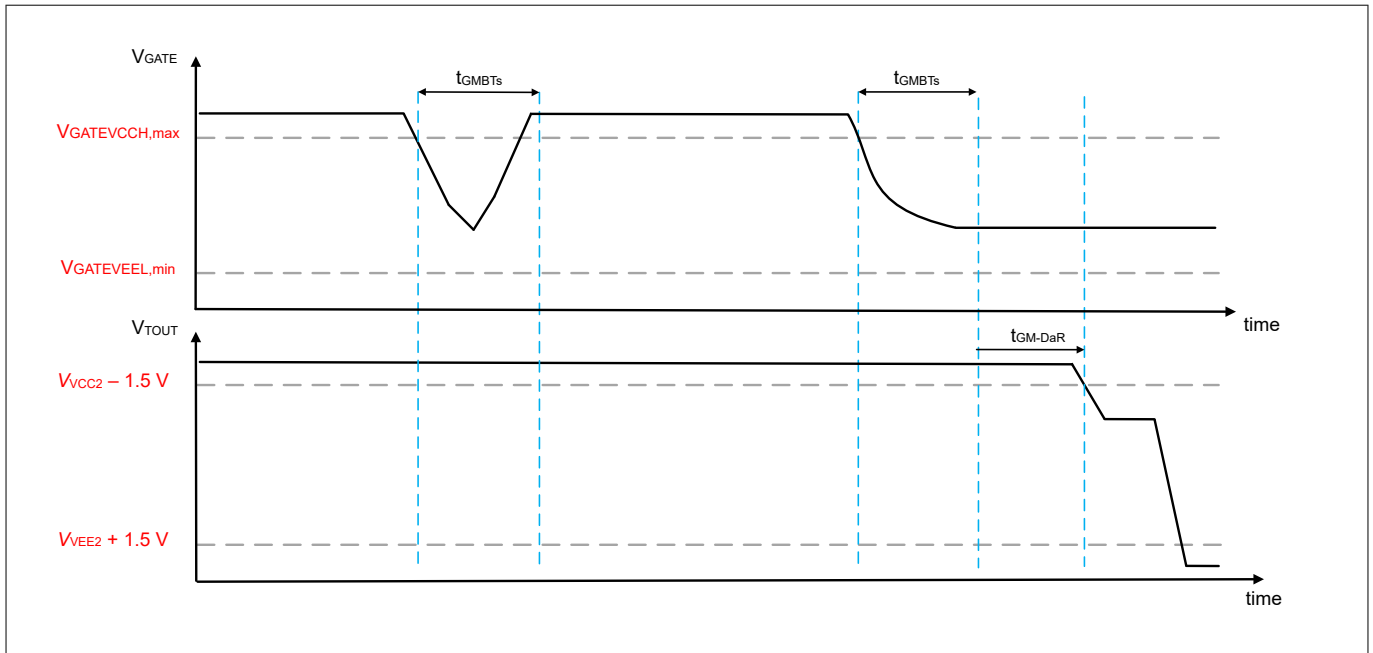
**7.6.1 Functional description gate monitoring**

The device monitors in the time frame of  $t_{GMBT}$  (dynamic or static) the gate signal  $V_{GATE}$  at pin CLAMP/GATE to ensure the signal  $V_{TOUT}$  reaches the threshold value of  $V_{GATE}$  properly. If monitoring conditions are violated, the device issues a safe turn-off (if TOUT = high (VCC2) in less than  $t_{GM-DaR}$  and changes to Error\_Mode in less than  $t_{RDY\_GM}$ .



**Figure 12 Dynamic gate monitoring timing diagram**

**7 Protection and monitoring functions**



**Figure 13** Static gate monitoring timing diagram

**7.6.2 Electrical characteristics gate monitoring**

**Table 15** Electrical characteristics gate monitoring

$T_J = -40^{\circ}C$  to  $150^{\circ}C$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate monitoring detection and reaction time	$t_{GM-DaR}$	450	650	900	ns	$V_{CC2} = \text{typ.}, V_{EE2} = \text{typ.}$	PRQ-853
Gate monitoring detection and notification time	$t_{RDY\_GM}$	-	1.5	2.5	$\mu s$	$V_{CC2} = \text{typ.}, V_{EE2} = \text{typ.}$	PRQ-910
Dynamic gate monitoring blanking time	$t_{GMBTd3}$	6.99	7.6	8.21	$\mu s$	$V_{EE2} = \text{typ.}, V_{CC2} = \text{typ.}$	PRQ-979
Static gate monitoring blanking time	$t_{GMBTs3}$	7.40	7.9	8.40	$\mu s$	$V_{EE2} = \text{typ.}, V_{CC2} = \text{typ.}$	PRQ-983

(table continues...)

**7 Protection and monitoring functions**

**Table 15 (continued) Electrical characteristics gate monitoring**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

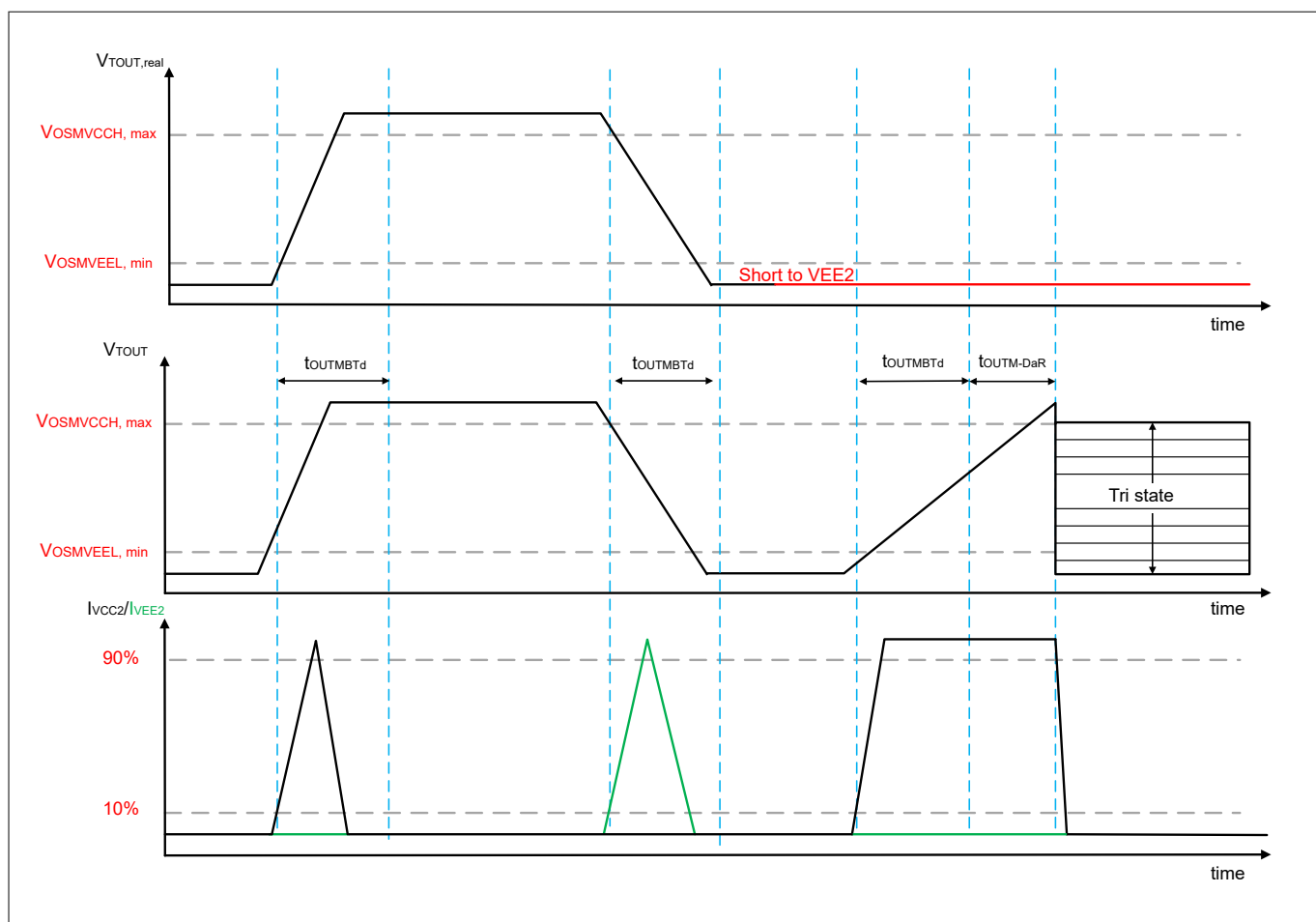
Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate monitoring VCC2 voltage threshold high level	$V_{\text{GATEVCCH}}$	$V_{\text{VCC2}} - 2.3$	$V_{\text{VCC2}} - 2.1$	$V_{\text{VCC2}} - 1.9$	V	$t_{\text{GMBT}}$ is active	PRQ-855
Gate monitoring VCC2 voltage threshold low level	$V_{\text{GATEVCCL}}$	$V_{\text{VCC2}} - 3.2$	$V_{\text{VCC2}} - 3$	$V_{\text{VCC2}} - 2.8$	V	$t_{\text{GMBT}}$ is active	PRQ-962
Gate monitoring VEE2 voltage threshold high level	$V_{\text{GATEVEEH}}$	$V_{\text{VEE2}} + 2.8$	$V_{\text{VEE2}} + 3$	$V_{\text{VEE2}} + 3.2$	V	$t_{\text{GMBT}}$ is active	PRQ-963
Gate monitoring VEE2 voltage threshold low level	$V_{\text{GATEVEEL}}$	$V_{\text{VEE2}} + 1.9$	$V_{\text{VEE2}} + 2.1$	$V_{\text{VEE2}} + 2.3$	V	$t_{\text{GMBT}}$ is active	PRQ-856

**7.7 Output stage monitoring**

**7.7.1 Functional description output stage monitoring**

The output stage monitoring checks whether the internal output signal is according to the given PWM or ASC input signal in the time frame of  $t_{\text{OUTMBTX}}$ , otherwise the device issues a tri-state for the output stage in less than  $t_{\text{OUTM-DaR}}$  and changes to Error\_Mode in less than  $t_{\text{RDY-OSM}}$ .

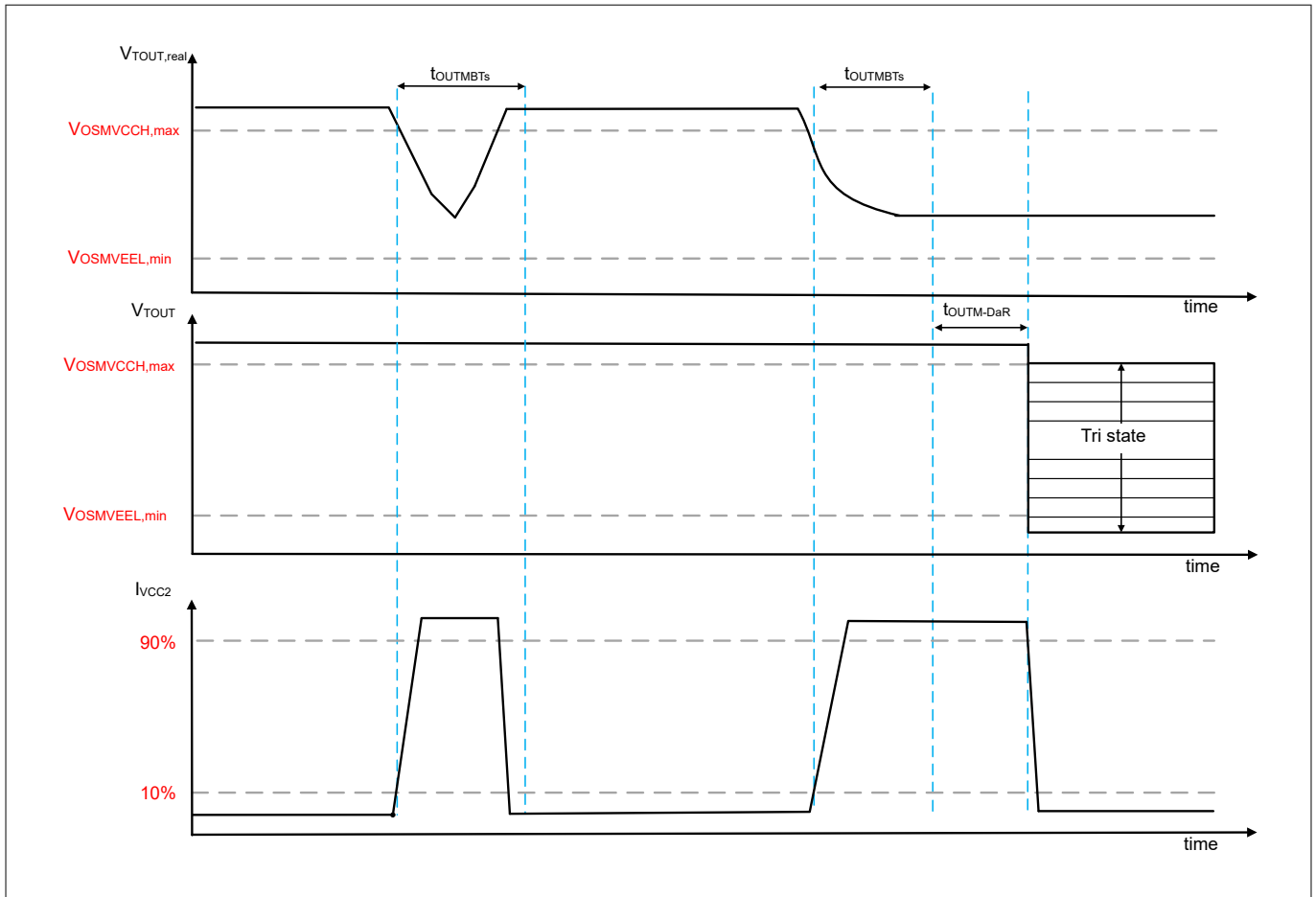
**7 Protection and monitoring functions**



**Figure 14**      **Dynamic output stage monitoring working principle**



**7 Protection and monitoring functions**



**Figure 15** Static output stage monitoring working principle

Note: The passive clamping at TOUT is working.

**7.7.2 Electrical characteristics output stage monitoring**

**Table 16** Electrical characteristics output stage monitoring

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output stage monitoring detection and reaction time	$t_{\text{OUTM-DaR}}$	200	350	500	ns	VCC2 = typ., VEE2 = typ.	PRQ-859
Output stage monitoring detection and	$t_{\text{RDY\_OSM}}$	-	1.5	2.5	$\mu\text{s}$	VCC2 = typ., VEE2 = typ.	PRQ-964

(table continues...)

**7 Protection and monitoring functions**

**Table 16 (continued) Electrical characteristics output stage monitoring**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
notification time							
Dynamic output stage monitoring blanking time	$t_{\text{OUTMBTd3}}$	600	800	1000	ns	VEE2 = typ., VCC2 = typ.	PRQ-922
Static output stage monitoring blanking time	$t_{\text{OUTMBTs3}}$	1000	–	1200	ns	VEE2 = typ., VCC2 = typ.	PRQ-925
Output stage monitoring VCC2 voltage threshold high level	$V_{\text{OSMVCCH}}$	$V_{\text{VCC2}} - 2.3$	$V_{\text{VCC2}} - 2.1$	$V_{\text{VCC2}} - 1.9$	V	$t_{\text{OUTBT}}$ is active	PRQ-863
Output stage monitoring VCC2 voltage threshold low level	$V_{\text{OSMVCCL}}$	$V_{\text{VCC2}} - 3.2$	$V_{\text{VCC2}} - 3$	$V_{\text{VCC2}} - 2.8$	V	$t_{\text{OUTBT}}$ is active	PRQ-965
Output stage monitoring VEE2 voltage threshold high level	$V_{\text{OSMVEEH}}$	$V_{\text{VEE2}} + 2.8$	$V_{\text{VEE2}} + 3$	$V_{\text{VEE2}} + 3.2$	V	$t_{\text{OUTBT}}$ is active	PRQ-966
Output stage monitoring VEE2 voltage threshold low level	$V_{\text{OSMVEEL}}$	$V_{\text{VEE2}} + 1.9$	$V_{\text{VEE2}} + 2.1$	$V_{\text{VEE2}} + 2.3$	V	$t_{\text{OUTBT}}$ is active	PRQ-864

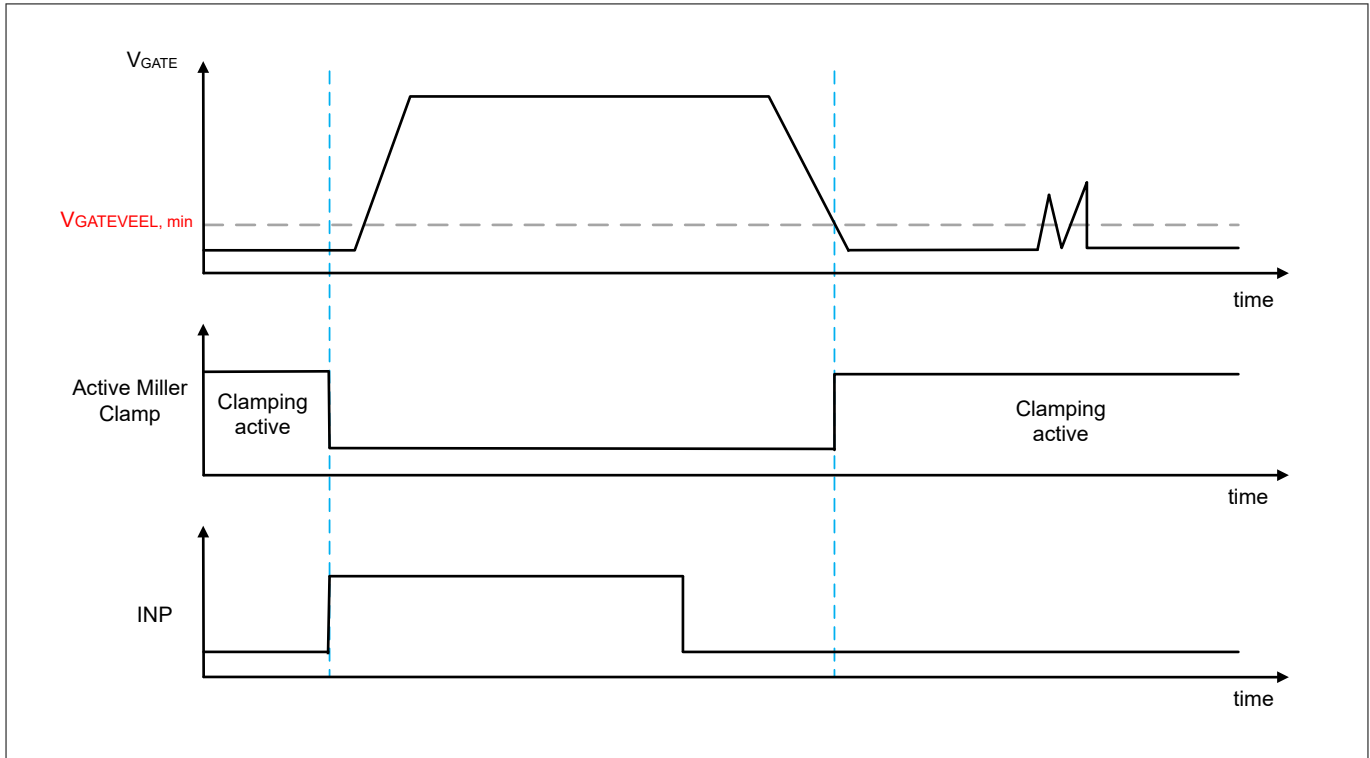
**8 Clamping functions**

**8 Clamping functions**

**8.1 Active Miller clamp**

**8.1.1 Functional description Active Miller clamp**

The clamp output is activated if the gate voltage  $V_{GATE}$  goes below  $V_{GATEVEEL}$  during turn-off.



**Figure 16 Active Miller clamp timing diagram**

*Note:* In a half bridge configuration the switched off power switch tends to dynamically turn on during the turn on phase of the opposite power switch. A Miller clamp allows sinking the Miller current across a low impedance path in this high  $dV/dt$  situation. Therefore, in many applications the use of a negative supply voltage can be avoided.

**8.1.2 Electrical characteristics Active Miller clamp**

**Table 17 Electrical characteristics Active Miller clamp**

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low level clamp peak current	$I_{CLAMPL}$	9.5	10		A	TOUT = low ( $V_{VEE2}$ ), CLAMP/GATE = $V_{CLAMP}$ , $V_{VCC2} = 15\text{ V}$ , $V_{VEE2} = -5\text{ V}$	PRQ-667
CLAMP/GATE voltage	$V_{CLAMP/GATE}$	$V_{VEE2}$	-	$V_{VCC2}$	V	Referenced to GND2, no load	PRQ-586

**(table continues...)**

**8 Clamping functions**

**Table 17 (continued) Electrical characteristics Active Miller clamp**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CLAMP R <sub>DS(on)</sub>	R <sub>DS(on)-CLAMP</sub>	0.08	–	0.35	Ω	Voltage drop $V_{VCC2} - V_{TOUT} < 1\text{ V}$	PRQ-852

**8.2 Passive clamping**

**8.2.1 Functional description passive clamping**

If the secondary chip is not supplied, the pin GATE/CLAMP is passively clamped to VEE2.

**8.2.2 Electrical characteristics passive clamping**

**Table 18 Electrical characteristics passive clamping**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

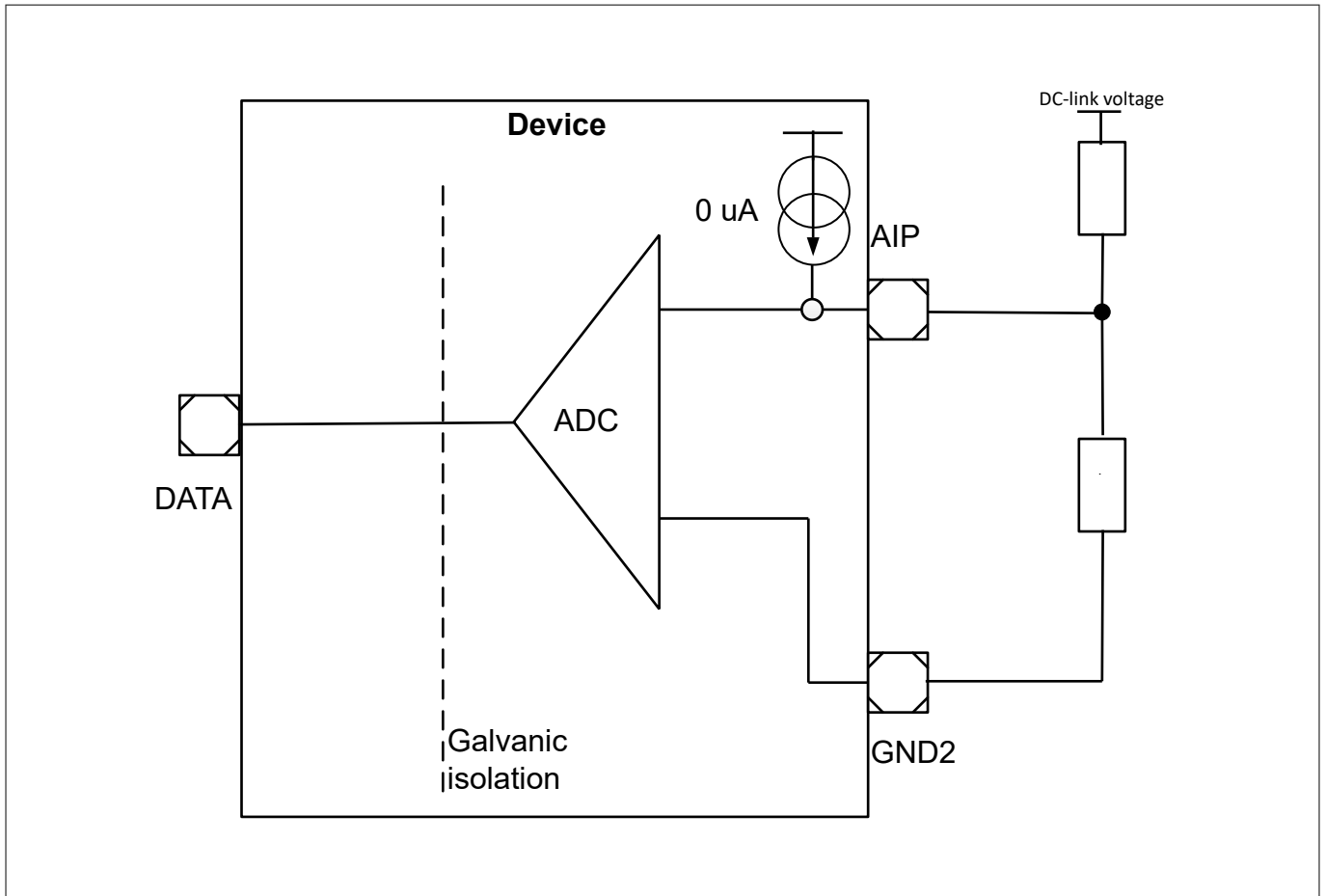
Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GATE passive clamping voltage (I <sub>CLAMP</sub> = 10 mA)	V <sub>PCLPG1</sub>	–	–	V <sub>VEE2</sub> + 2 V	V	Secondary chip not supplied (VCC2 floating, VEE2 = 0 V), I <sub>Clamp</sub> = 10 mA	PRQ-738
GATE passive clamping voltage (I <sub>CLAMP</sub> = 100 mA)	V <sub>PCLPG2</sub>	–	–	V <sub>VEE2</sub> + 2.2 V	V	Secondary chip not supplied (VCC2 floating, VEE2 = 0 V), I <sub>Clamp</sub> = 100 mA	PRQ-882

## 9 Analog-to-Digital Converter (ADC)

### 9.1 Functional description ADC

The device has an ADC to measure the DC-link voltage.

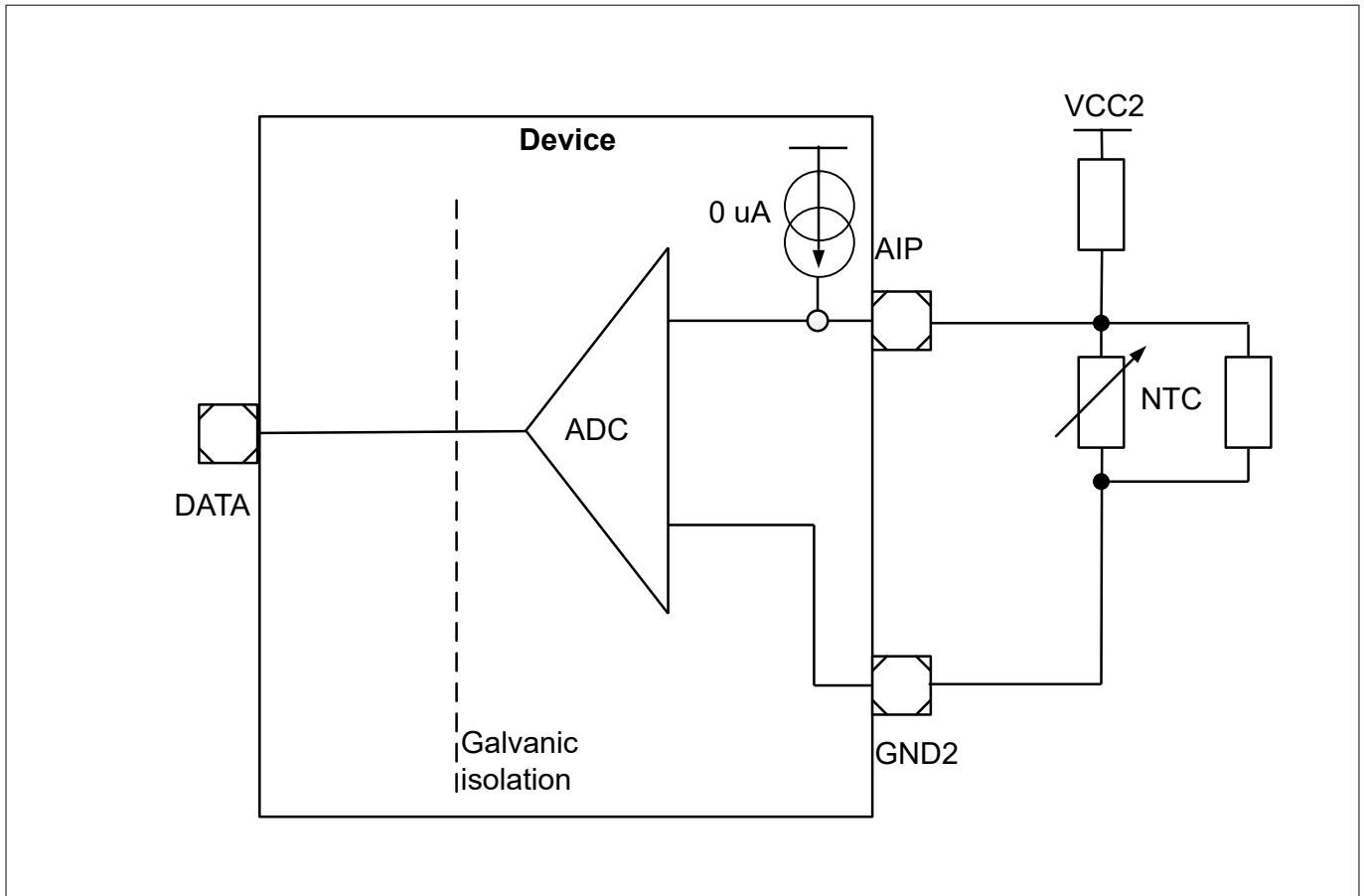
The integrated ADC allows the measurement of the DC-link voltage. The internal current source  $I_{ADC,ref}$  is deactivated. The voltage signal  $V_{AIP}$  is encoded to a PWM signal that is passed through the isolation to DATA pin on the primary side. The Total Unadjusted Error is the square sum of errors ( $INL$ ,  $ER_{OFF}$  and  $ER_{GAIN}$ ).



**Figure 17 DC-link measurement diagram**

The integrated ADC allows isolated temperature sensing. The internal current source  $I_{ADC,ref}$  is disabled. The voltage signal  $V_{AIP}$  is encoded to a PWM signal that is passed through the isolation to DATA pin on the primary side. The Total Unadjusted Error is the square sum of errors ( $INL$ ,  $ER_{OFF}$  and  $ER_{GAIN}$ ).

**9 Analog-to-Digital Converter (ADC)**



**Figure 18 ADC application diagram with NTC.**

Note:  $V_{IADC, effective} = (V_{IADC} * ER_{GAIN} / 100)$

**9.2 Electrical characteristics ADC**

**Table 19 Electrical characteristics ADC**

$T_J = -40^{\circ}C$  to  $150^{\circ}C$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC resolution		-	-	12	bit		PRQ-609
Ideal ADC input voltage full scale	$V_{IADC}$	-	4.82	-			PRQ-794
ADC Gain Error	$ER_{GAIN}$	-1.5	-	+1.5	%FS	Refers to $V_{IADC}$ , valid for Input range $V_{AIP} - V_{GND2} = 0.4 V \dots 4.4 V$	PRQ-897
ADC Offset Error	$ER_{OFF}$	-0.25	-	+0.25	%FS	Refers to $V_{IADC}$ , valid for Input range $V_{AIP} - V_{GND2} = 0.4 V \dots 4.4 V$	PRQ-898

**(table continues...)**

**9 Analog-to-Digital Converter (ADC)**

**Table 19 (continued) Electrical characteristics ADC**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC INL	INL	–	0.02 4	0.07 3	%FS	Refers to $V_{IADC}$ , valid for Input range $V_{AIP} - V_{GND2} = 0.4\text{ V} \dots 4.4\text{ V}$	PRQ-899
ADC DNL	DNL	–	0.00 7	0.02 5	%FS	Refers to $V_{IADC}$ , valid for Input range $V_{AIP} - V_{GND2} = 0.4\text{ V} \dots 4.4\text{ V}$	PRQ-900
ADC sample rate	$f_{SAMPLE}$	2.28	2.4	2.52	kHz	12 bit	PRQ-903
ADC leakage current	$I_{leakADC}$	-3		3	$\mu\text{A}$	$V_{AIP} = 4\text{ V}$	PRQ-1034

**10 Interface**

**10 Interface**

**10.1 Reset (NRST)**

**10.1.1 Functional description NRST**

The NRST pin is the reset input of the device.  
 All errors cleared with a rising edge on NRST.

**10.1.2 Electrical characteristics NRST**

**Table 20 Electrical characteristics NRST**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Minimum reset duration time	$t_{NRST}$	10	–	–	$\mu\text{s}$		PRQ-764

**10.2 Ready (RDY)**

**10.2.1 Functional description RDY**

The RDY pin reports whether the device is ready.

*Note: Ready means: no OSM error, no gate monitoring error, no OVLO2, no UVLO2, no open pin at OCPx, no prim. or sec. internal supervision error, OTP read ok.*

The RDY pin has a passive clamping.

*Note: Passive clamping keeps RDY = 0 in case of no supply.*

**10.2.2 Electrical characteristics RDY**

**Table 21 Electrical characteristics RDY**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RDY open drain output low level	$V_{RDY(low)}$	–	–	0.5	V	$V_{VCC1} \geq 3.0\text{ V}, I_{load} = 5\text{ mA}$	PRQ-840

**(table continues...)**



## 10 Interface

**Table 21 (continued) Electrical characteristics RDY**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RDY output low passive clamping	$V_{RDYCLAMP}$	–	0.5	1	V	$I_{RDYCLAMP} = 500 \mu\text{A}$ , $V_{CC1} = \text{floating}$ , all I/O = floating	PRQ-834
Power up timing prim.	$t_{PUprim}$	–	100	1500	$\mu\text{s}$	Time from UVLO1 release to device operable, secondary chip running	PRQ-959
Power up timing sec.	$t_{PUsec}$	–	100	1500	$\mu\text{s}$	Time from UVLO2 release to device operable, primary chip running	PRQ-960
Time from rising Edge NRST to RDY = high	$t_{NRST2RDY}$	50	–	200	ns	No error detected	PRQ-961

## 10.3 Fault (NFLT)

### 10.3.1 Functional description NFLT

The device has an active low fault pin (NFLT) to report DESAT and OCP short circuit events.

If the device switches off the output stage due to a DESAT or OCP event, it goes to Error\_Mode and signals the event on pin NFLT with  $\text{NFLT} = 0$  within  $t_{NFLT\_DESAT}$  or  $t_{NFLT\_OCP}$ .

*Note:* Switch off means safe turn-off.

The device keeps the fault signal available unless a reset event takes place.

### 10.3.2 Electrical characteristics NFLT

**Table 22 Electrical characteristics NFLT**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCP event detection to NFLT activation	$t_{NFLT\_OCP}$	–	1.2	2.3	$\mu\text{s}$	$V_{OCP\_Overdrive} = \pm 200 \text{ mV}$ , slew rate = 100 mV/ns, $\text{NFLT} = 90 \%$ , $R_{PU\_NFLT} = 1 \text{ k}\Omega$	PRQ-614
DESAT event detection to NFLT activation	$t_{NFLT\_DESAT}$	–	1.5	2.5	$\mu\text{s}$	$V_{DESAT\_Overdrive} = \pm 200 \text{ mV}$ , slew rate = 10 V/ $\mu\text{s}$ , $\text{NFLT} = 90 \%$ , $R_{PU\_NFLT} = 1 \text{ k}\Omega$	PRQ-844

(table continues...)

## 10 Interface

**Table 22 (continued) Electrical characteristics NFLT**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
NFLT open drain output low level	$V_{\text{NFLT}}$	–	–	0.5	V	$V_{\text{VCC1}} \geq 3.0 \text{ V};  I_{\text{NFLT}}  = 5 \text{ mA}$	PRQ-791

## 10.4 I/O levels

**Table 23 I/O levels**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

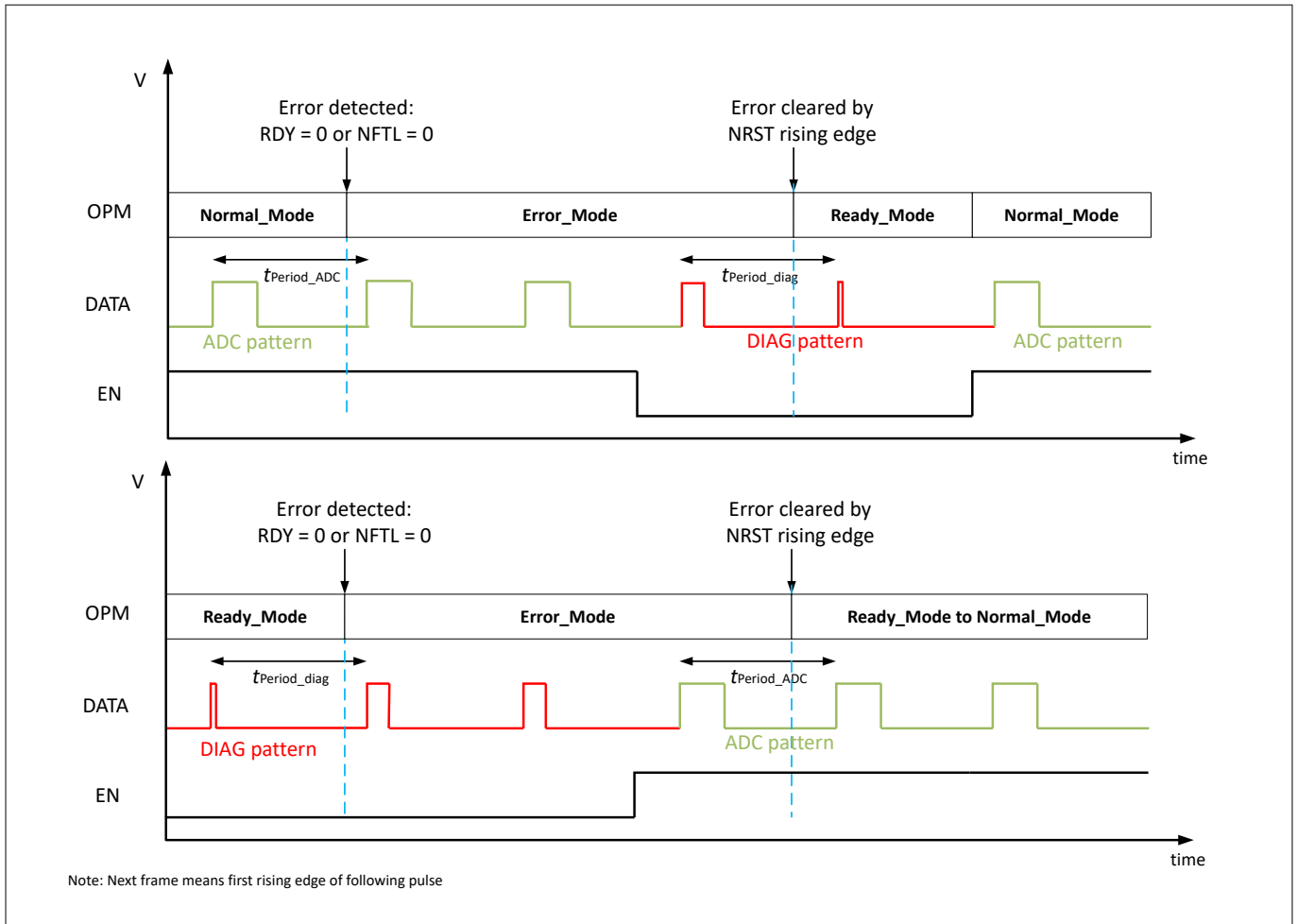
Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Primary digital input low level	$V_{\text{digital, input (low)}}$	0	–	0.8	V		PRQ-704
Primary digital input high level	$V_{\text{digital, input (high)}}$	2	–	$V_{\text{VCC1}}$	V		PRQ-705
INP high/low duration	$t_{\text{INPPD}}$	750	–	–	ns	$V_{\text{VCC1}}=\text{typ.}, V_{\text{VCC2}}=\text{typ.}, V_{\text{VEE2}}=\text{typ.}, 50\%$ to 50%	PRQ-970
INN high/low duration	$t_{\text{INNPD}}$	750	–	–	ns	$V_{\text{VCC1}}=\text{typ.}, V_{\text{VCC2}}=\text{typ.}, V_{\text{VEE2}}=\text{typ.}, 50\%$ to 50%	PRQ-971
Weak pull down resistance NRST, EN, INP	$R_{\text{PDIN1}}$	40	48	60.5	$\text{k}\Omega$		PRQ-929
Weak pull up resistance INN	$R_{\text{PDINN}}$	40	52	60.5	$\text{k}\Omega$		PRQ-930

## 10.5 DATA read-out

### 10.5.1 Functional description DATA

In case the device switches to Error\_Mode and EN pin is low, diagnostic data are available, starting with the next frame. In Ready\_Mode diagnostic data are available. In Normal\_Mode and in Error\_Mode, when EN pin is high, ADC result data are available.

**10 Interface**



**Figure 19 DATA pin ADC and diagnostic transition timing diagram**

The 12 bit ADC data is pulse width modulated to a signal with a period of  $t_{Period\_ADC}$ .  
 The duty cycle for 12 bit ADC data always remains in the range of  $D_{ADC}$  regardless of the ADC input.  
 The following diagnostic functions are reported in Ready\_Mode and in Error\_Mode, if EN = 0:

- UVLO2
- OVLO2
- Gate monitoring
- Output stage monitoring
- OCP
- DESAT
- Sec. internal supervision error (Parity, OTP, PMU\_Supervision error)

The 8 bit diagnostic functions is pulse width modulated to a signal with a period of  $t_{Period\_Diag}$ .  
 The duty cycle of the DATA pin always remains in the range of  $D_{Diag}$  regardless of the diagnostic status.

Note: 0% and 100% duties are not allowed at DATA pin.

**Table 24 Diagnostic read-out at DATA pin**

BIT <sub>x</sub>	Value	Description	Value	Description	Example: Single failure DESAT
BIT 0	0	PRIM NOT READY	1	PRIM READY	1

(table continues...)

**10 Interface**

**Table 24 (continued) Diagnostic read-out at DATA pin**

BIT <sub>x</sub>	Value	Description	Value	Description	Example: Single failure DESAT
BIT 1	0		1		1
BIT 2	0		1		1
BIT 3	0		1		1
BIT 4	Reserved (always 0)				
BIT 5	0	No OSM Error	1	OSM Error	0
BIT 6	0	No GATEMON Error	1	GATEMON Error	0
BIT 7	0	No DESAT Error	1	DESAT Error	1
BIT 8	0	No OCP Error	1	OCP Error	0
BIT 9	0	No UVLO2 Error	1	UVLO2 Error	0
BIT 10	0	No OVLO2 Error	1	OVLO2 Error	0
BIT 11	0	SEC READY	1	SEC NOT READY	0
<b>Result from example diagnostic read-out:</b>					Duty cycle = 3.49 %

The duty cycle for diagnostic read-out can be calculated using the following formula:

$$DC = \frac{\sum(BIT_x \cdot 2^x)}{4096}$$

**Figure 20 Formula to calculate the duty cycle for diagnostic read-out**

**10.5.2 Electrical characteristics DATA**

**Table 25 Electrical characteristics DATA**

T<sub>J</sub> = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC DATA duty cycle range	D <sub>ADC</sub>	0.36	–	99.6	%	No life sign lost, no primary reset	PRQ-782
Diagnostic duty cycle range	D <sub>Diag</sub>	0.36	–	99.6	%		PRQ-783

**(table continues...)**

**10 Interface**

**Table 25 (continued) Electrical characteristics DATA**

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC DATA period	$t_{\text{Period\_ADC}}$	95	100	105	$\mu\text{s}$		PRQ-784
Diagnostic period	$t_{\text{Period\_Diag}}$	95	100	105	$\mu\text{s}$		PRQ-785
DATA output low level	$V_{\text{DATA,output}} t(\text{low})$	-	0	0.5	V	$V_{\text{VCC1}} \geq 3.0 \text{ V},  I_{\text{load}}  = 5 \text{ mA}$	PRQ-706
DATA output high level	$V_{\text{DATA,output}} t(\text{high})$	$V_{\text{VCC1}} - 0.5$	$V_{\text{VCC1}}$	-	V	$V_{\text{VCC1}} \geq 3.0 \text{ V},  I_{\text{load}}  = 5 \text{ mA}$	PRQ-707

**11 Application information**

**11 Application information**

The external component values are specified as typical values in a typical application. Deviation of the nominal values are specified as min or max values, if applicable. Unless otherwise specified the deviation for external components are:

- Resistor:  $\pm 10\%$
- Capacitor:  $-50\% \dots +30\%$

*Note:* The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

**11.1 Electrical characteristics external components**

**Table 26 Electrical characteristics external components**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Decoupling capacitance (between VCC1 and GND1)	$C_{dVCC1}$	0.55	1.1	–	$\mu\text{F}$	Total capacitance refers to $1 \mu\text{F}$ capacitance + $0.1 \mu\text{F}$ close to the device. Max value depends on $t_{RP1}$ .	PRQ-1002
Decoupling capacitance (between VCC2 and GND2)	$C_{dVCC2}$	–	11	–	$\mu\text{F}$	Total capacitance refers to $10 \mu\text{F}$ capacitance + $1 \mu\text{F}$ close to the device. Values depend on external $C_{LOAD}$ . Max value depends on $t_{RP2}$ .	PRQ-1001
Decoupling capacitance (between VEE2 and GND2)	$C_{dVEE2}$	–	11	–	$\mu\text{F}$	Total capacitance refers to $10 \mu\text{F}$ capacitance + $1 \mu\text{F}$ close to the device. Max value depends on $t_{RP3}$ .	PRQ-1000
Pull-up resistance	$R_{pu}$	–	10	–	$\text{k}\Omega$	Min value depends on $I_{OUTx\_MAX}$ .	PRQ-1015
Filter resistance	$R_{Filter}$	–	1	–	$\text{k}\Omega$	Value must fit to application	PRQ-1016
Filter capacitance	$C_{Filter}$	–	47	–	$\text{pF}$	Value must fit to application	PRQ-1017
DESAT resistance	$R_{Desat}$	1	2.2	–	$\text{k}\Omega$	Depends on maximum current and on $V_{DESATx}$ deviation.	PRQ-1018
DESAT filter capacitance	$C_{Desat}$	50	100	–	$\text{pF}$	Depends on required response time.	PRQ-1019
OCP sense resistor	$R_{OCPSense}$	–	0.47	–	$\Omega$	Value depends on power switch specification, voltage rating of OCP pin has to be considered.	PRQ-1021
OCPP filter resistance	$R_{OCPP}$	–	10	–	$\Omega$	Depends on required response time. Consider internal pull-up.	PRQ-1022

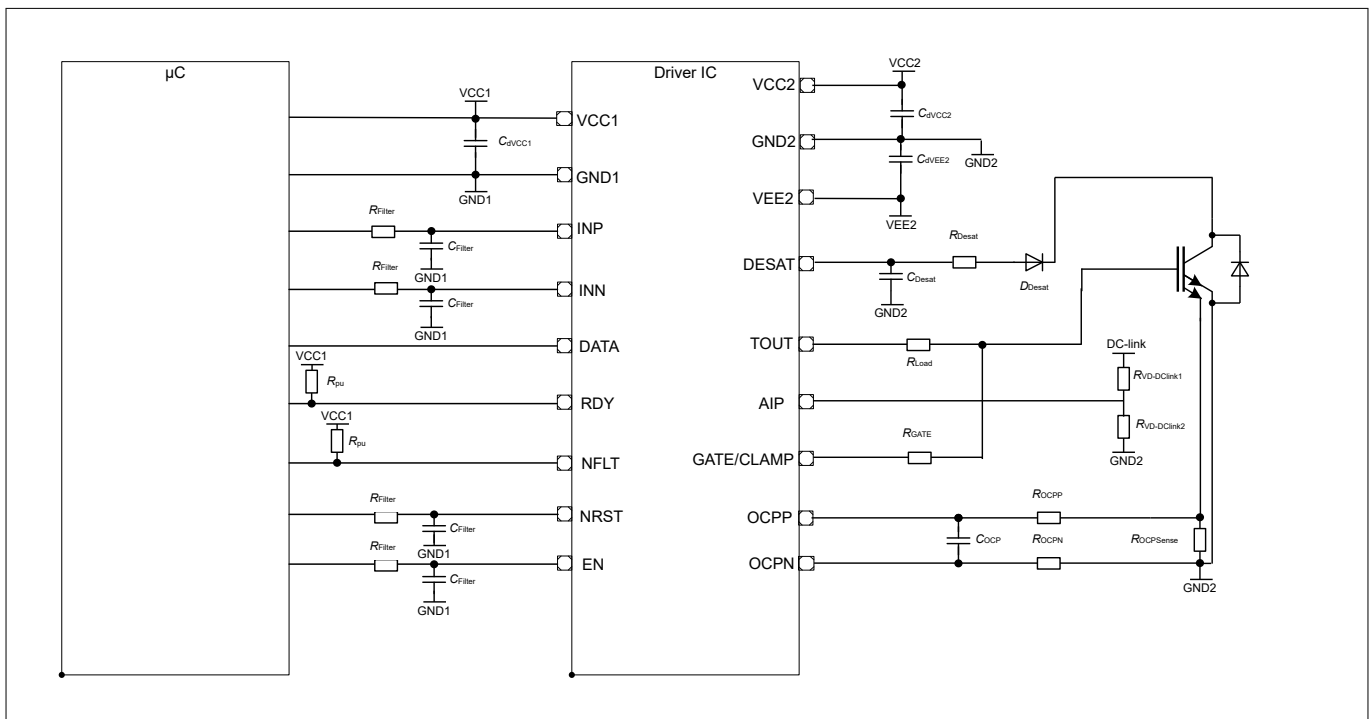
**(table continues...)**

**11 Application information**

**Table 26 (continued) Electrical characteristics external components**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCPP filter capacitance	$C_{OCP}$	-	10	-	pF	Depends on required response time	PRQ-1023
OCPN resistance	$R_{OCPN}$	-	10	-	$\Omega$	Should match to OCPP filter resistor. Consider internal pull-up.	PRQ-1024
TOUT resistance	$R_{Load}$	1.7	-	-	$\Omega$	Min resistor value required according to max output current in functional range. Max value limited by gate monitoring feature.	PRQ-1025
GATE/CLAMP series resistance	$R_{GATE}$	-	0	-	$\Omega$	Optional component. Voltage across resistor impacts Active Miller clamping feature.	PRQ-1028

**11.2 Typical application example**

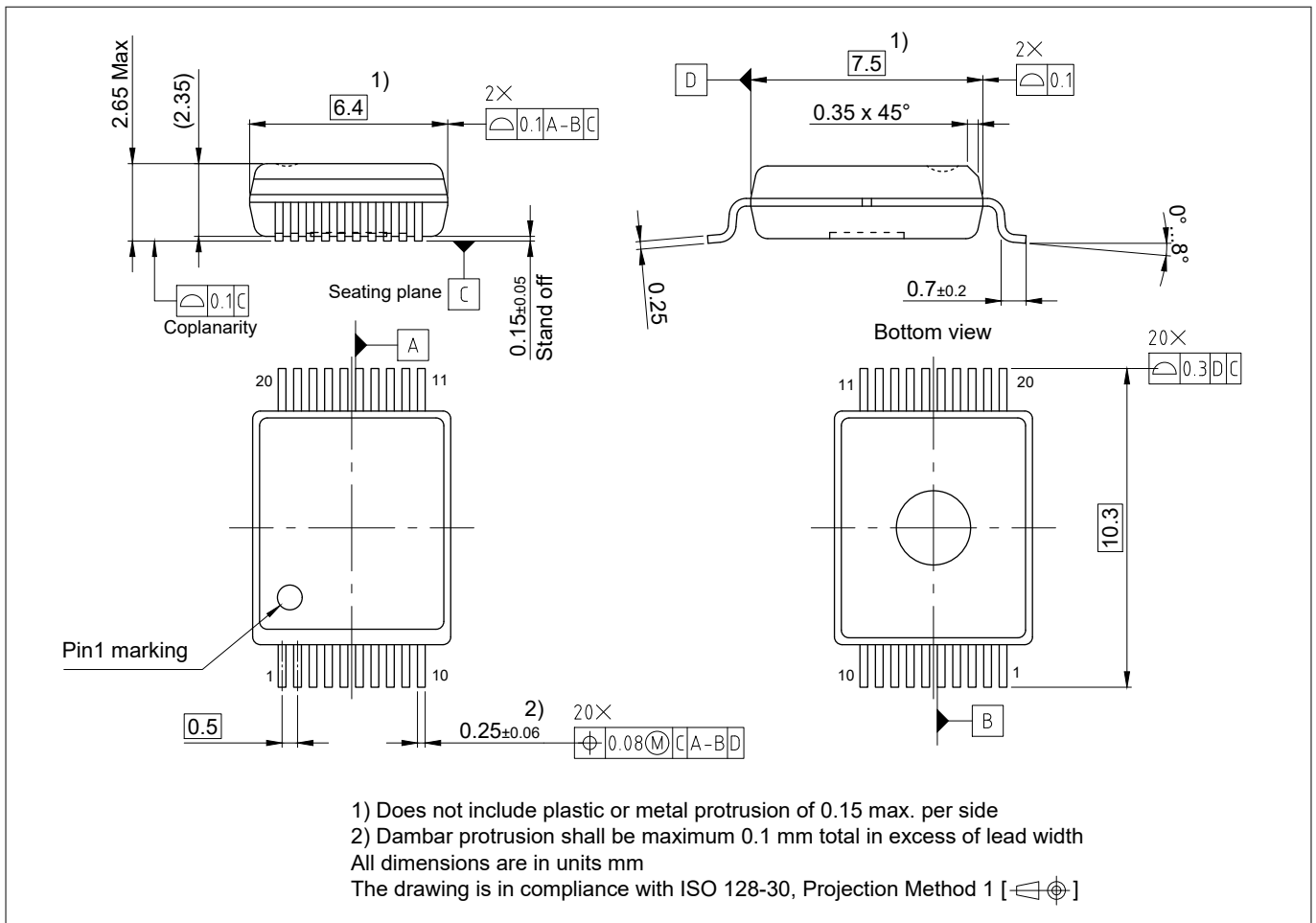


**Figure 21 Typical application example with ADC**

*Note: This is a very simplified example. The function must be verified in the real application.*

**12 Package information**

**12 Package information**



**Figure 22 PG-DSO-20**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Information on alternative packages**

Please visit [www.infineon.com/packages](http://www.infineon.com/packages).



**Revision history**

## Revision history

Revision	Date	Changes
1.1	2022-02-17	<a href="#">Chapter 3.2</a> updated <ul style="list-style-type: none"><li>• Table 3 updated<ul style="list-style-type: none"><li>- VCC1, VEE2, VCC2 ramp-up slew-rates reduced</li><li>- ramp-down condition removed</li></ul></li></ul> <a href="#">Chapter 3.4</a> updated <ul style="list-style-type: none"><li>• Table 5 updated<ul style="list-style-type: none"><li>- extended by further electrical information</li><li>- additional reinforced insulation options</li></ul></li></ul>
1.01	2021-06-25	Typo in insulation certification standard corrected
1.0	2021-03-18	Initial datasheet created

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