

## Evaluating the **AD9671** JESD204B for Octal Ultrasound AFE with Digital Demodulator

### FEATURES

Full featured evaluation board for testing the **AD9671**  
PC software for control of the **AD9671** using a USB interface

### EQUIPMENT NEEDED

**AD9671** evaluation board (AD9671EBZ)  
Analog signal source and antialiasing filter  
6 V switching power supply, 2.5 A  
**HSC-ADC-EVALEZ** board  
12 V switching power supply, 2.5 A, provided with the **HSC-ADC-EVALEZ** board  
CUI EPS060250UH-PHP-SZ, provided  
PC running Windows® operating system  
PC with USB 2.0 port, recommended (USB 1.1 compatible)  
Spectrum analyzer for CW Doppler mode  
USB cable, provided with the **HSC-ADC-EVALEZ** board

### DOCUMENTS NEEDED

**AD9671** data sheet

### SOFTWARE NEEDED

**VisualAnalog**  
**SPIController**

### GENERAL DESCRIPTION

The AD9671EBZ evaluation board enables testing and evaluation of the **AD9671** octal ultrasound analog front end (AFE) device. The AD9671EBZ evaluation board offers eight Subminiature Version A (SMA) connector inputs for all eight channels. The AD9671EBZ evaluation board connects to the **HSC-ADC-EVALEZ** field programmable gate array (FPGA) data capture board, and enables data capture via a USB connection to a PC. **SPIController** software enables flexible configuration of the **AD9671**, and **VisualAnalog**® software offers a powerful data capture as well as signal analysis tools.

### EVALUATION BOARD CONNECTION DIAGRAM

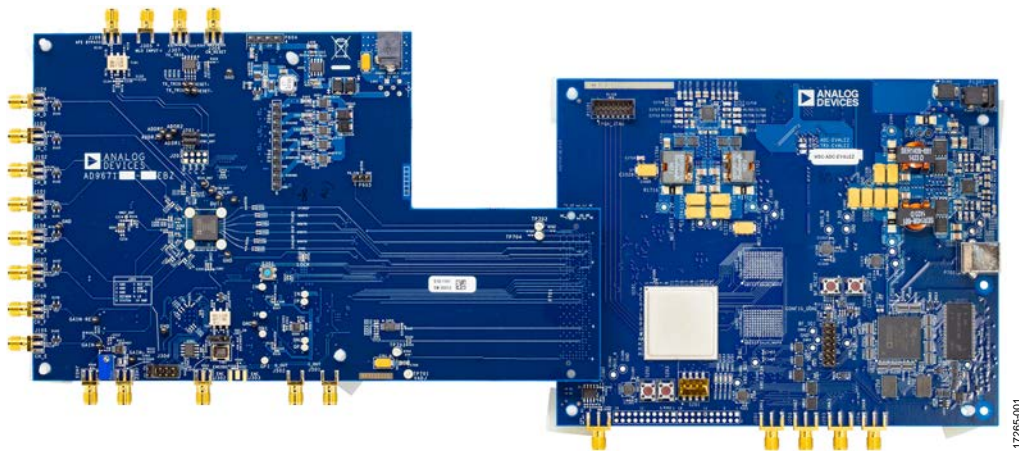


Figure 1.

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**REVISION HISTORY**

1/2019—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

### POWER SUPPLIES

A single switching power supply (6 V, 2.5 A) is needed to power up the AD9671EBZ evaluation board.

### INPUT SIGNALS

The AD9671EBZ evaluation board offers eight SMA connector inputs for the eight AFE channels. The SMA channel inputs maps directly to the low noise amplifier (LNA) input of the [AD9671](#) device. An optional external clock SMA input can be used to bypass the default 40 MHz crystal on the AD9671EBZ evaluation board with a J301 jumper change.

Other SMA inputs include the voltage gain amplifier (VGA)  $GAIN_{\pm}$  control, the continuous wave (CW) doppler  $MLO_{\pm}$  signal, the CW  $RESET_{\pm}$  signal, and an optional  $TX\_TRIG_{\pm}$  input. The  $TX\_TRIG$  signal is provided by the FPGA on the [HSC-ADC-EVALEZ](#) data capture board. A single-ended signal is the default for the VGAIN control although a differential input configuration is also possible.

### OUTPUT SIGNALS

The high speed serial interface (JESD204B) digital output signals are fed to the [HSC-ADC-EVALEZ](#) data capture board via the FPGA mezzanine card (FMC) connector. The J501 and J502 SMA outputs are included for the CW doppler summed I and Q outputs.

## EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

### SOFTWARE INSTALLATION PROCEDURES

Two software programs must be installed first to work with the AD9671EBZ evaluation board. [VisualAnalog](#) is an Analog Devices, Inc. software package that enables data capture and analysis for many Analog Devices analog-to-digital converter (ADC) devices, including the [AD9671](#) ultrasound AFE. [SPIController](#) is another Analog Devices software package that enables interfacing with many Analog Devices devices including the [AD9671](#), and enables serial peripheral interface (SPI) read and write commands to the chip.

#### Installing the [VisualAnalog](#) Software

Visit [www.analog.com/visualanalog](http://www.analog.com/visualanalog) and follow the download and installation instructions.

#### Installing the [SPIController](#) Software

Visit the [SPIController](#) software page at [www.analog.com/spicontroller](http://www.analog.com/spicontroller) and follow the download and installation instructions.

### CONFIGURING THE AD9671EBZ EVALUATION BOARD

Take the following steps to configure the AD9671EBZ evaluation board:

1. Power up the [HSC-ADC-EVALEZ](#) data capture board by connecting it to the USB cable and 12 V adapter, then power up the AD9671EBZ evaluation board by connecting it to the 6 V adapter (see Figure 1).
2. Start [VisualAnalog](#). The software attempts to program the [HSC-ADC-EVALEZ](#) data capture board with the default file associated with the detected AD9671EBZ evaluation board. After the file loads, the CONFIG\_DONE LED illuminates on the [HSC-ADC-EVALEZ](#) data capture board (see Figure 2). Click **Yes**.
3. Select the [AD9671](#) folder on the left side of the window shown in Figure 3 to view the available templates. Select the **Samples** canvas, which shows output vs. sample count. After the **Samples** canvas is selected, the [VisualAnalog](#) task bar opens as shown in Figure 4.

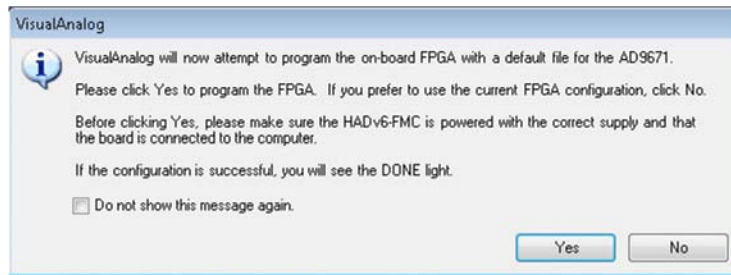


Figure 2. [VisualAnalog](#) FPGA Programming Dialog

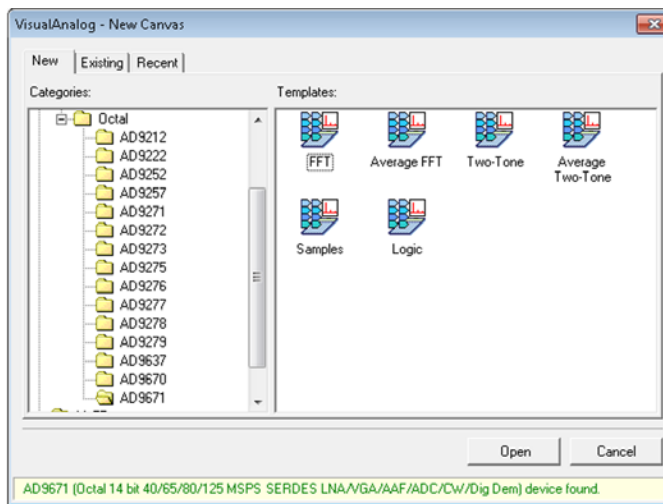


Figure 3. [VisualAnalog](#) Canvas Selection



Figure 4. [VisualAnalog](#) Collapsed Window Mode

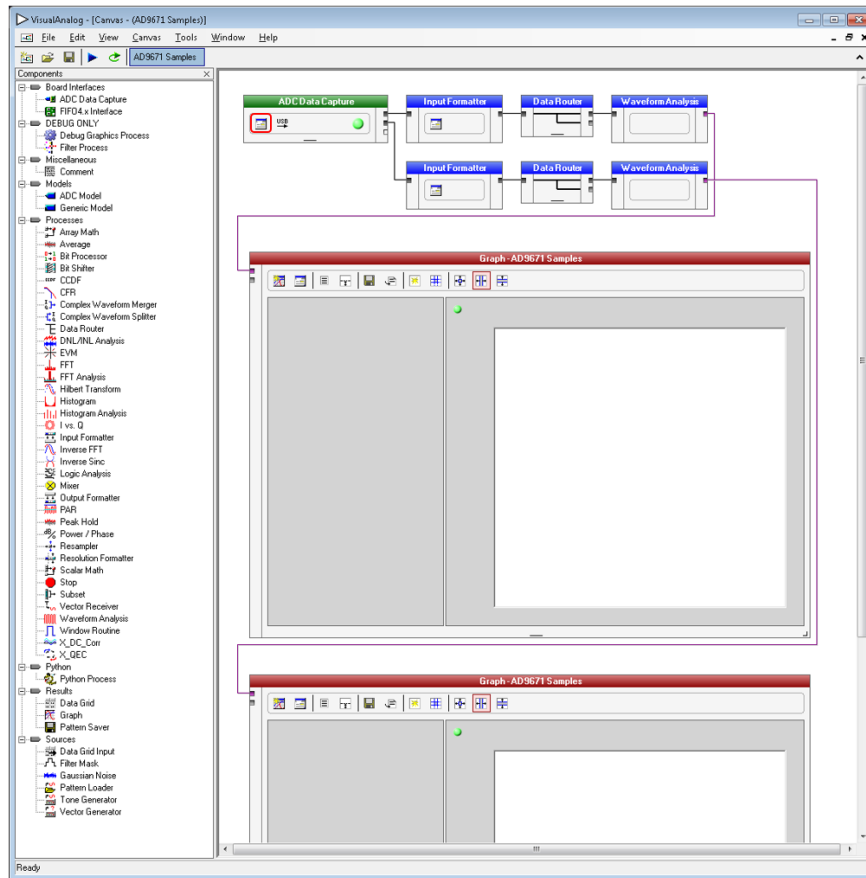


Figure 5. AD9671 Sample Canvas

4. Click the down arrow on the right side of the task bar to expand the canvas and see the signal processing flow shown in Figure 5.
5. To reprogram the FPGA after VisualAnalog starts, click the **Settings** button in the ADC data capture block on any canvas, as marked with the red box in Figure 5. In the **Capture Board** tab in the **ADC Data Capture Settings** window shown in Figure 6, click **Browse**, select the bin file **ad9671\_evalez06132014\_0921am.mcs**, and then click **Program**. After the file loads, the CONFIG\_DONE LED illuminates on the data capture FPGA board. Click **OK** to close the window.
6. Select the correct output mode from the **Device** tab in the **ADC Data Capture Settings** window shown in Figure 7.
7. The default clock crystal on the AD9671EBZ evaluation board is 40 MHz. To use a different speed, connect the external clock source by setting Clock Jumper J301 on the AD9671EBZ evaluation board to off state.
8. Start the **SPIController**. Click the **File** menu, and then click **Cfg Open**. A file **Open** dialog box opens. Select the **AD9671** configuration file, **AD9671\_14bit\_125MSspiR03.cfg** (see Figure 8).

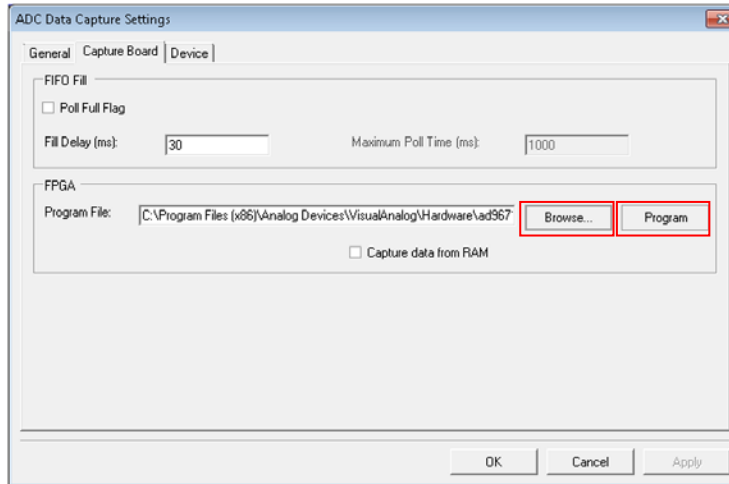


Figure 6. FPGA Programming Section

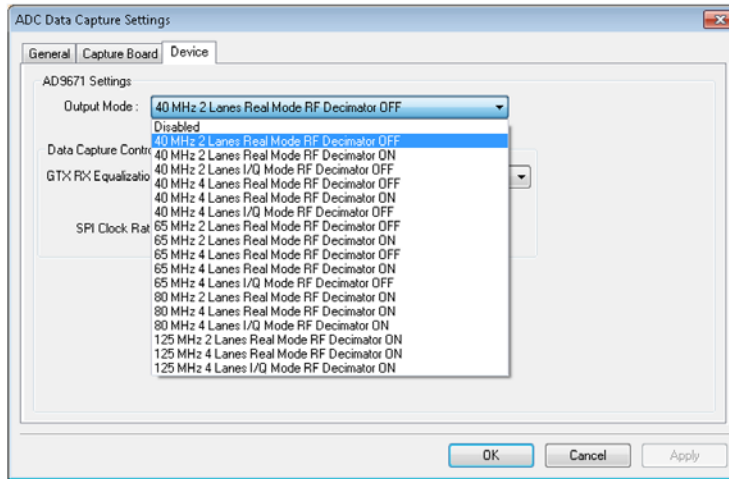


Figure 7. Output Mode Selection Section

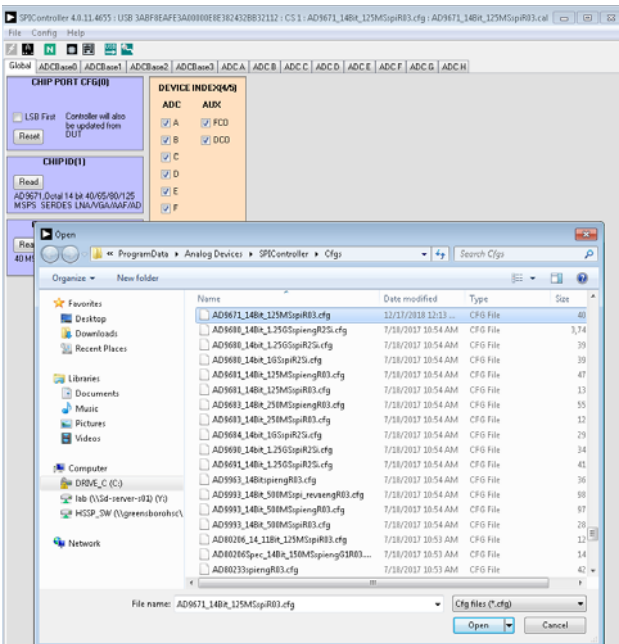


Figure 8. Configuration File Open Dialog Box

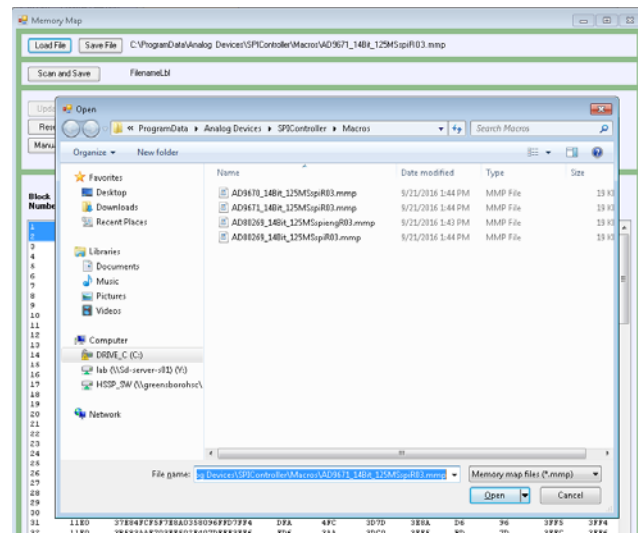


Figure 9. Memory File Select Dialog Box

- On the **Config** menu at the top of the **SPIController** window, click **Launch Memory Map Dialog**. This command starts the memory map shown in Figure 11, as well as a way to select prestored demodulation and decimation profiles. Click **Load File** to open the file **Open** dialog box, and select the **AD9671\_14Bit\_125MSspiR03.mmp** file to load the coefficient and profile memory onto the **AD9671** (see Figure 9).
- In the main **SPIController** window, click **File**, then click the **MacroGroup Open** command, and select the **AD9671\_Test\_Macro\_released.mgp** file (see Figure 10).

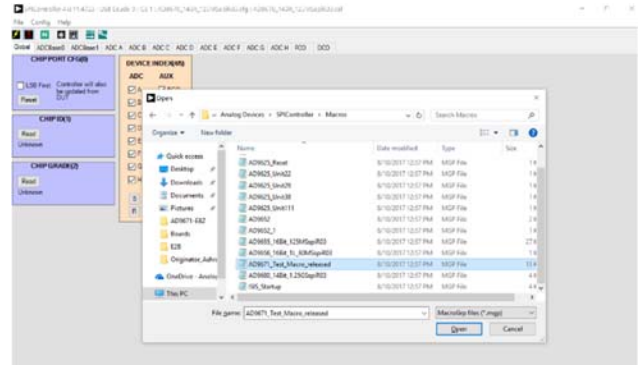


Figure 10. SPI Macro File Select Dialog Box

**UPDATING PROFILE NUMBER  
SELECTS A NEW DECIMATION RATE  
AND COEFFICIENT POINTER**

**DEMODULATION FREQUENCY  
CAN BE CHANGED BY  
UPDATING DEMODULATION FREQUENCY  
AND SAMPLE FREQUENCY**

READS THE MEMORY ON THE DEVICE AND SAVES IT TO A FILE

**Memory Map**

Load File Save File C:\ProgramData\Analog Devices\SPIController\Macros\AD9671\_14Bit\_125MSspiR03.mmp

Scan and Save Filename: Lbl

Update Memory

Reset Defaults

Manual Trigger

Profile # 11

Demod Freq (MHz) 1.0

Sample Freq (MHz) 40.0

Coefficient Pointer 1000

Decimation Rate 2

Gain 16x

HP Filter Bypass Enabled

Profile Value 2000000C00007FFF

**COEFFICIENTS BLOCKS OF SELECTED PROFILE VECTOR**

Block Number	Block Start Address	B13:B0	C7	C6	C5	C4	C3	C2	C1	C0
1	1000	6318K18EABFC1A0726170FF78FE1	18C6	E1B	3AA7	3C1A	1CA	170	3F0E	3FE1
2	1010	7E20EAD7137D041100A200C9FF4	1718	3AD5	3C05	3E2A	104	1A3	1A3	3FF1
3	1020	3DBCA7F1FB024048C106FFABFE8	F6F	AA7	3C7E	3D24	12F	106	3FEA	3FE8
4	1030	4CF05C0F343E4C04280B6FE23FF3	139C	5C0	3C0D	3E4C	10A	B6	3FF8	3FF3
5	1040	5660180F9CBF8401F061007FFFA	1658	180	3E72	3F84	7C	61	1F	3FFA
6	1050	2CA0875F597DC4038C0CBFFBFEF	B28	875	3D65	3DC4	E3	CB	3FE8	3FEF
7	1060	35EC5AAF5ABE6F036C0A1FDF3FF3	D7B	5AA	3D6A	3E5F	DB	A1	3FF4	3FF3
8	1070	3CC4305F7CBF1302A807000BFF8	F31	309	3DF2	3F13	AA	70	2	3FF8
9	1080	40600C9FC47FBE01280420073FFC	1018	C9	3F11	3FBE	4A	42	1C	3FFC
10	1090	46C0DFBEF77C5705A814CFF8FFE4	1170	DFB	3BDD	3C57	16A	14C	3FE3	3FE4
11	10A0	522CA66EF1BD1305A8119FFA3FE9	148B	A66	3BC6	3D13	16A	119	3FE8	3FE9
12	10B0	5C546E7F0B3DF305040DBFFD7FEF	1715	6E7	3C2C	3DF3	141	DB	3FF5	3FEF
13	10C0	638C3B3F497EDA03A809C003BFF5	18E3	3B3	3D25	3EDA	EA	9C	E	3FF5
14	10D0	67480F0FAF3FB0018C06200CBFF9	19D2	F0	3EBC	3F80	63	62	32	3FF9
15	10E0	3934BE6F24FCE70489118FF9FFE8	E4D	BE6	3C93	3CE7	12E	118	3FE7	3FE8
16	10F0	4208969F1D7D6404C40F6FFABFE8	1082	969	3C75	3D64	131	F6	3FEA	3FE8
17	1100	49B06F2F277DFA047C0CDDFC7FEF	126C	6F2	3C9D	3DFA	11F	CD	3FF1	3FEF
18	1110	4FC849A457E9B03CC0A1FFBF4	13F2	49A	3D15	3E9B	F3	A1	3FFF	3FF4
19	1120	5404278F79FF3902B0076004BFF8	1501	278	3DE7	3F39	AC	76	12	3FF8
20	1130	563009CFC53FC8012004E00B3FFA	158C	9C	3F14	3FCB	48	4E	2C	3FFA
21	1140	3078A5AF4FD5204080F3FFABFE8	C1E	ASA	3D13	3D52	102	F3	3FEA	3FE8
22	1150	3710887F3D0FAA041C0DBBFB3FED	DC4	887	3CF7	3DA4	107	DB	3FE8	3FED
23	1160	3CF46B4F417E1503FC0BDFFC3FF0	F3D	684	3D05	3E15	FF	BD	3FF0	3FED
24	1170	41F44EF50FE89039C05DFFDFFF3	107D	4EF	3D43	3E89	E7	9D	3FF7	3FF3
25	1180	4E20345F6DFE02F807D000FFF7	1178	345	3DB7	3EFF	BE	7D	3	3FF7
26	1190	48941C0F993F72020C05D004FFF4	1225	1C0	3E64	3F72	83	5D	13	3FFA
27	11A0	49F006BFD2FFD800DC04100A3FFA	127C	6B	3F4B	3FDB	37	41	28	3FFA
28	11B0	2A08928F5CFDA303880D6FFB7FED	A82	928	3D73	3DA3	E2	D6	3FED	3FED
29	11C0	2F247C3F56BDE5039C0C4FFB7FEF	BC9	7C3	3D6A	3D55	E7	C4	3FED	3FEF
30	11D0	33D065CF573E33038C0AEFFC3FF1	CF4	65C	3D6C	3E33	E3	AE	3FF0	3FF1

Figure 11. Memory Map

**USING THE SOFTWARE FOR TESTING**

Carry out the following steps to test the data capture of the AD9671EBZ evaluation board:

1. The macro file loaded in Step 10 of the Configuring the AD9671EBZ Evaluation Board section is an XML file that lists SPI command macros. Each macro includes SPI writes that configure the AD9671 for a certain operating mode. The **MacroEditor** window in Figure 12 lists all macros under a dropdown list as well as under numerical tabs. The macro file contains six macros. Users can edit the XML macro file to add their own configuration macros and load the edited file onto the macro editor. Table 1 shows an example SPI macro that configures the AD9671.

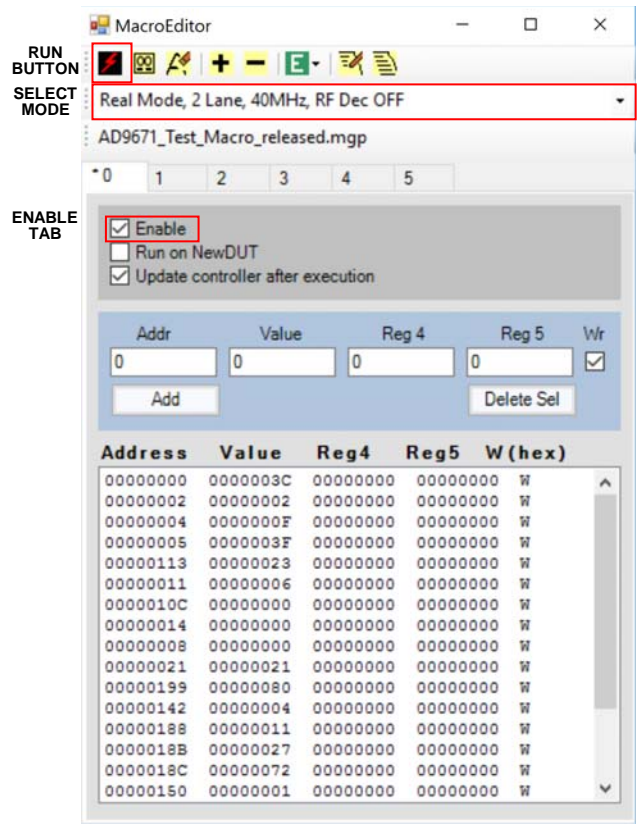
**Table 1. SPI Configuration Macro Example for the AD9671**

Register	Functions
0x00	SPI reset
0x02	Set speed mode
0x04, 0x05	Enable and disable channels
0x113	Enable and bypass digital filters, demodulator, decimator
0x011	LNA and VGA gain settings
0x10C	Set index profile
0x014	Offset binary enable
0x008	Time gain compensation (TGC) run mode
0x021	Set number of bits, set number of lanes
0x199	Enable sample clock counter
0x142	Enable serial initial lane alignment sequence
0x188	Enable start code
0x18B	Set start code word (MSB)
0x18C	Set start code word (LSB)
0x150	Set JESD204B scrambler, set number of lanes
0x182	Set phase-locked loop (PLL) autoconfigure
0x181	Set PLL N divider
0x10C	Set SPI TX_TRIG
0x00F	Filter cutoff frequency, band
0x02B	Set analog LPF and HPF to defaults, tune filters

2. To run one of the macros, select the appropriate tab, 0 to 5, shown in Figure 12, or select the macro from the drop down list. Select the **Enable** checkbox while making sure the internal or external clock matches the speed mode selected, as described in Step 7 of the Configuring the AD9671EBZ Evaluation Board section. See Table 2 for the modes supported by the macro. Click the **Run** button shown in Figure 12 to run the macro.

**Table 2. Real Modes Supported by the Macro**

No. of Lanes	Encode Clock (MHz)	RF Decimation	Channels Per Lane	Speed Mode (MSPS)
2	40	Off	4	40
2	65	On	4	40
2	65	Off	4	65
2	80	On	4	80
4	80	On	2	80
4	125	On	2	125



*Figure 12. Macro Editor Graphical User Interface (GUI)*

3. Click the blue arrow on the upper left side of the **VisualAnalog** toolbar shown in Figure 14 to run the canvas once, or click the green repeat button to set the canvas to run continually. The **Samples** canvas produces two windows that show 8192 time domain samples for Channel A and Channel B, as shown in Figure 13.



### BUTTONS FOR ZOOMING IN AND RESIZING

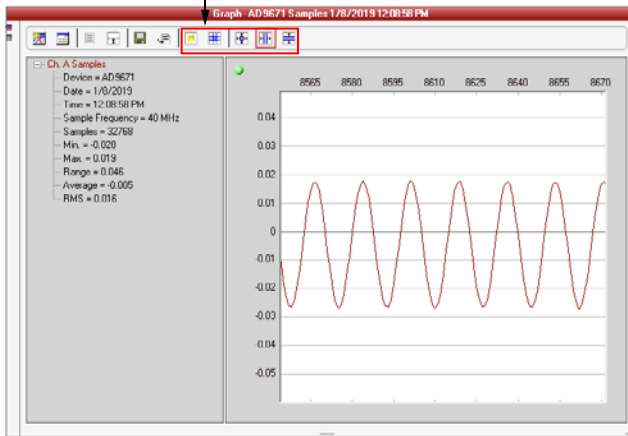


Figure 13. Sample Canvas Output Window

- The AD9671\_Average\_FFT.vac canvas is set up for running and calculating fast Fourier transform (FFT) as shown in Figure 14. The average count is set to five, which means the canvas either needs to be run five times, or left in continuous run mode. The results in Figure 14 show the shaping of the noise floor as a result of the analog filters and the digital high-pass filter.

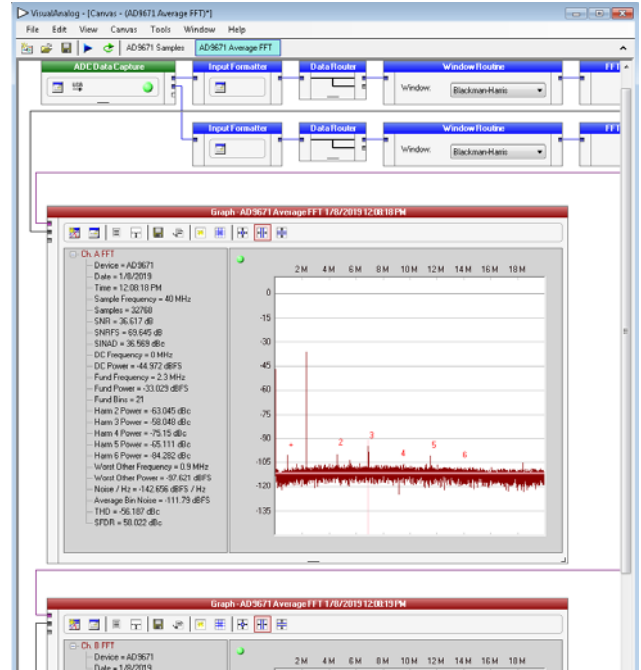


Figure 14. Average FFT Canvas Output Window

EVALUATION BOARD SCHEMATICS

17255-015

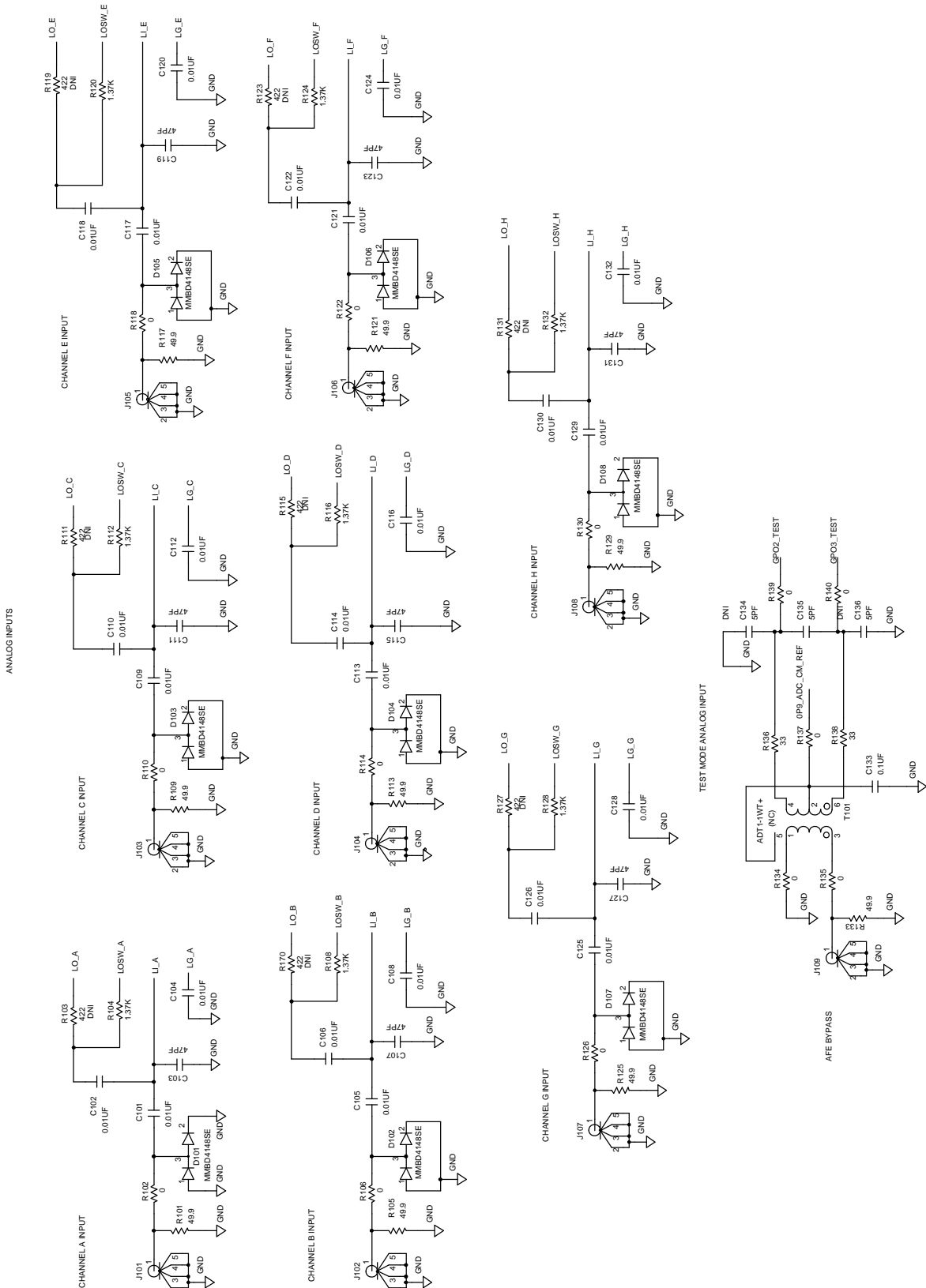


Figure 15. EVAL-AD9671EBZ Schematics Page 1

17265-016

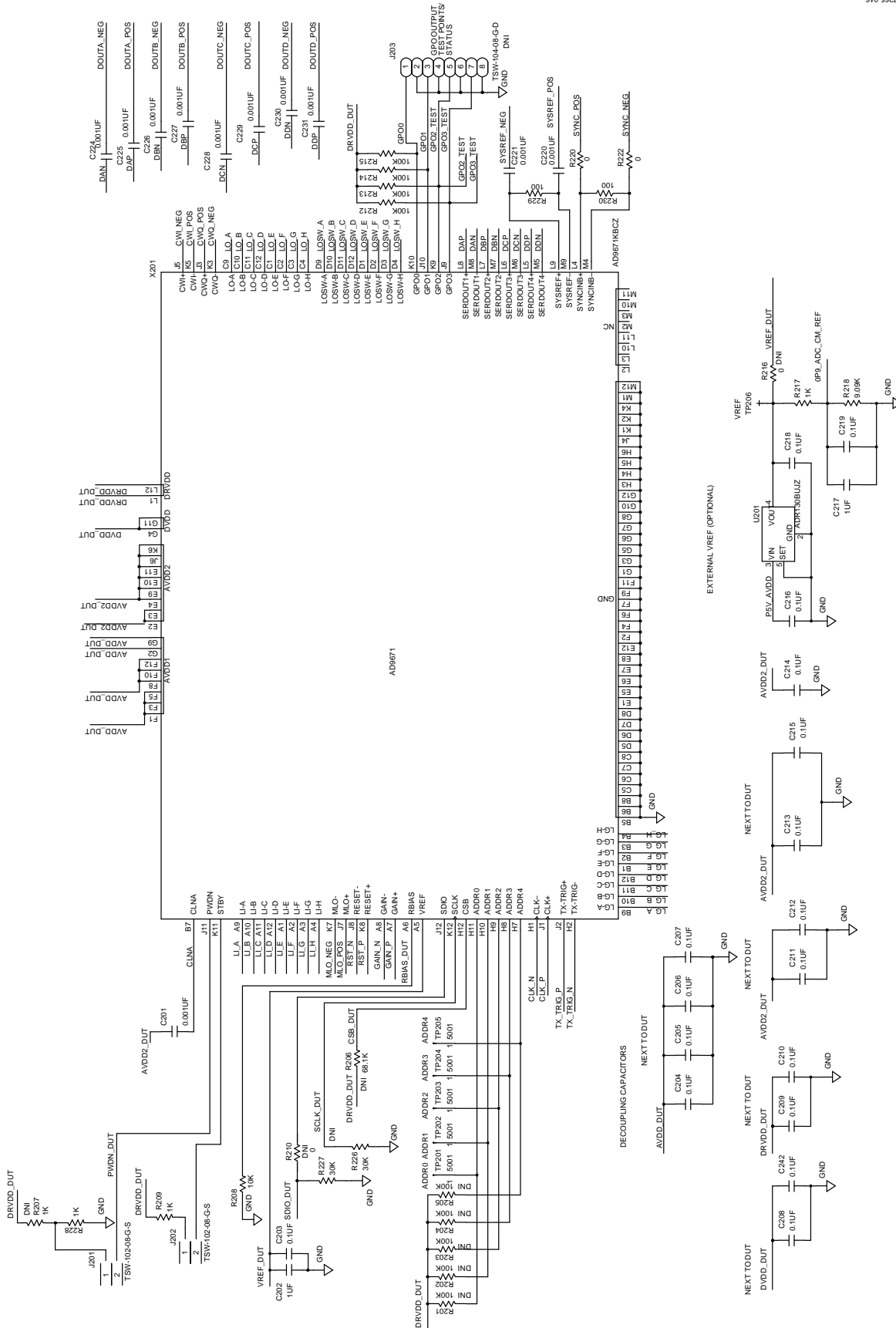


Figure 16. EVAL-AD9671EBZ Schematics Page 2

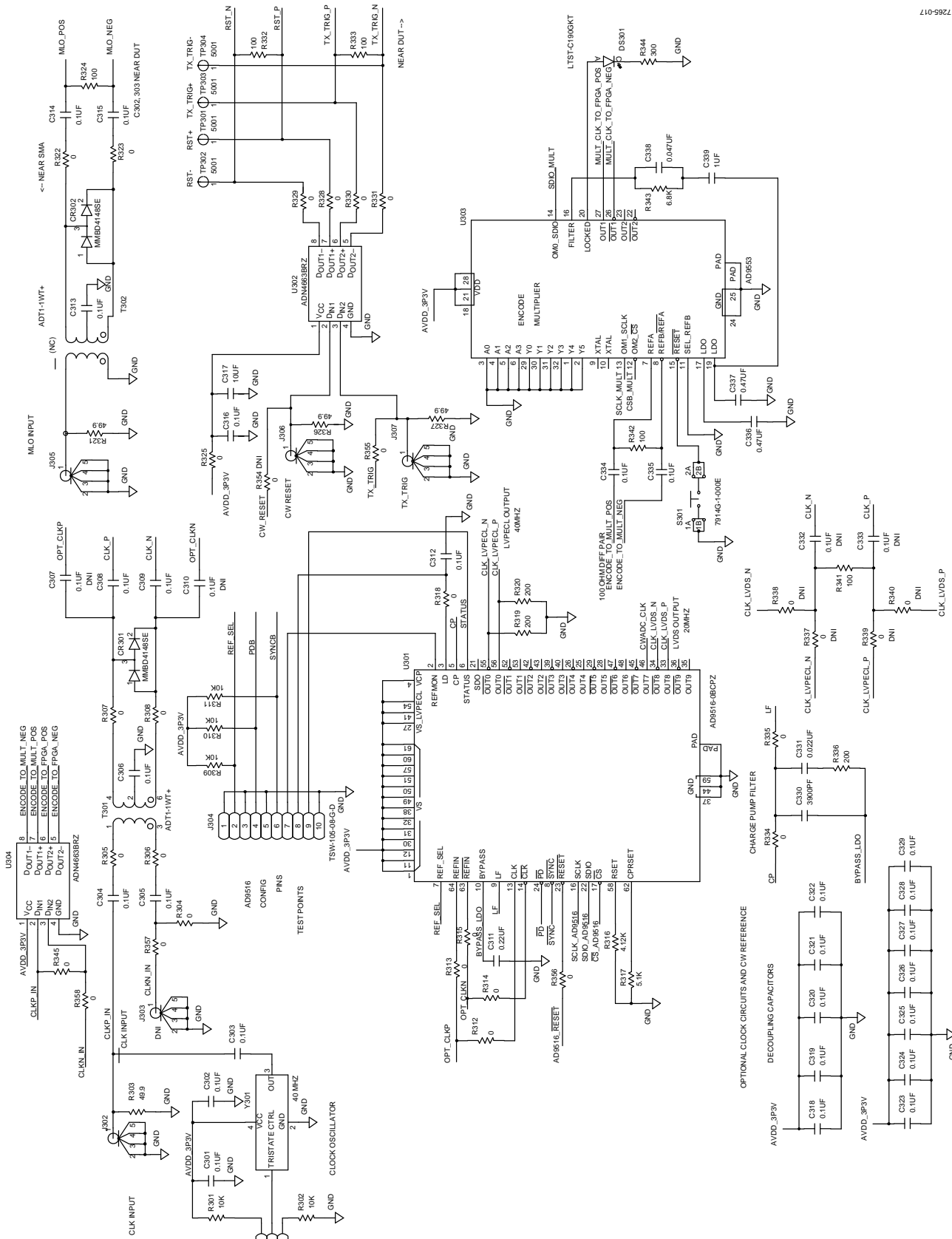


Figure 17. EVAL-AD9671EBZ Schematics Page 3

17265-018

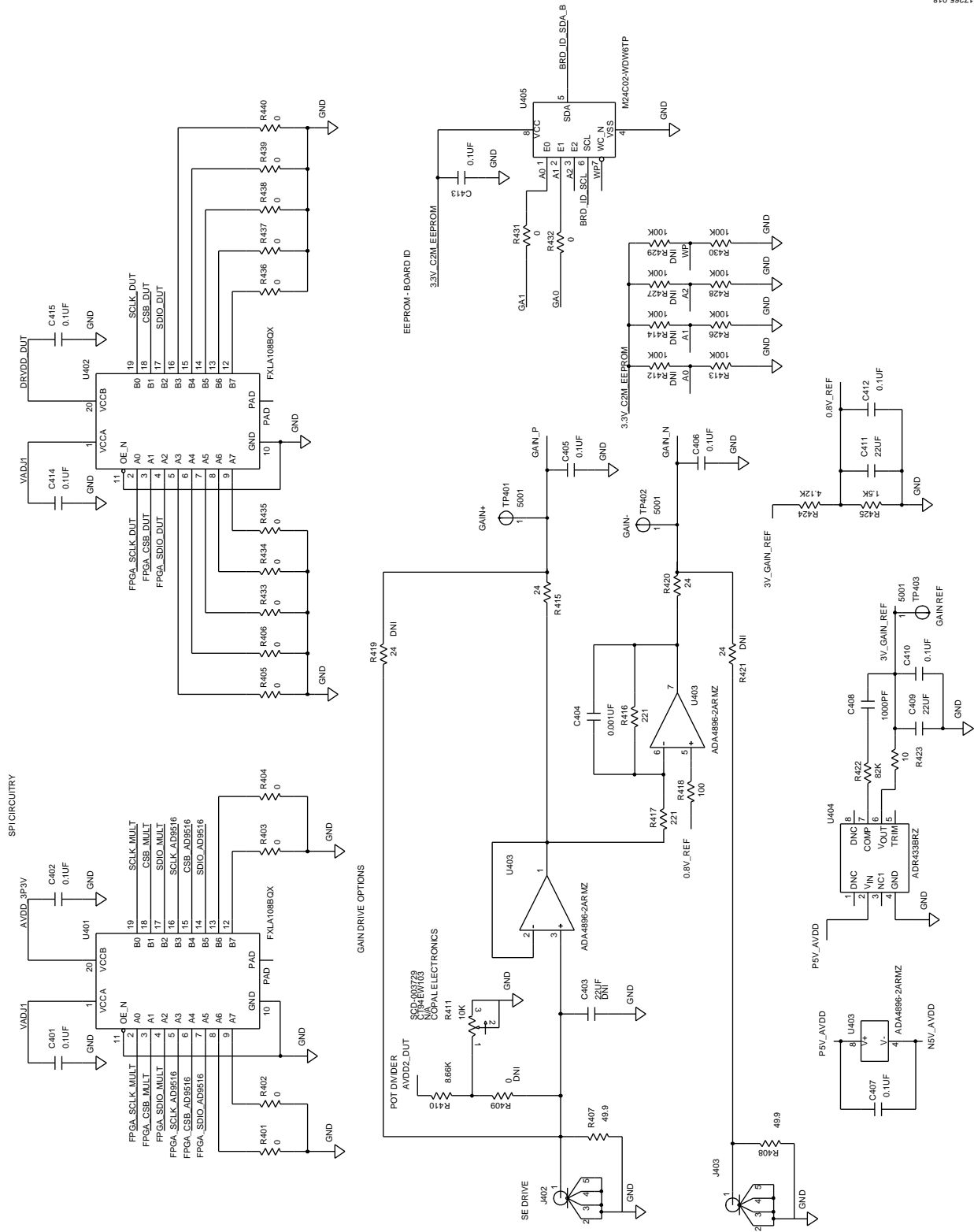


Figure 18. EVAL-AD9671EBZ Schematics Page 4

17265-019

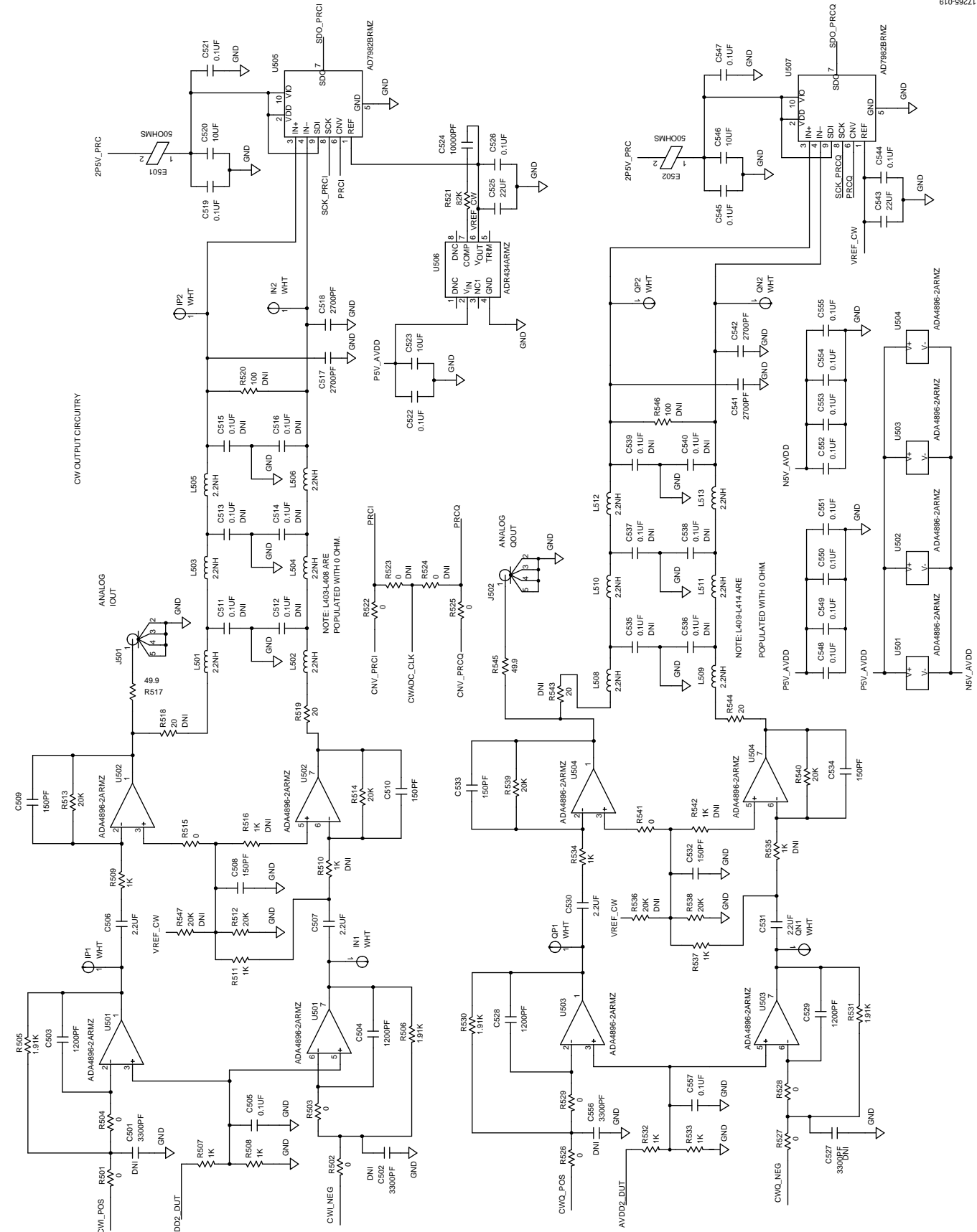


Figure 19. EVAL-AD9671EBZ Schematics Page 5

17265-020

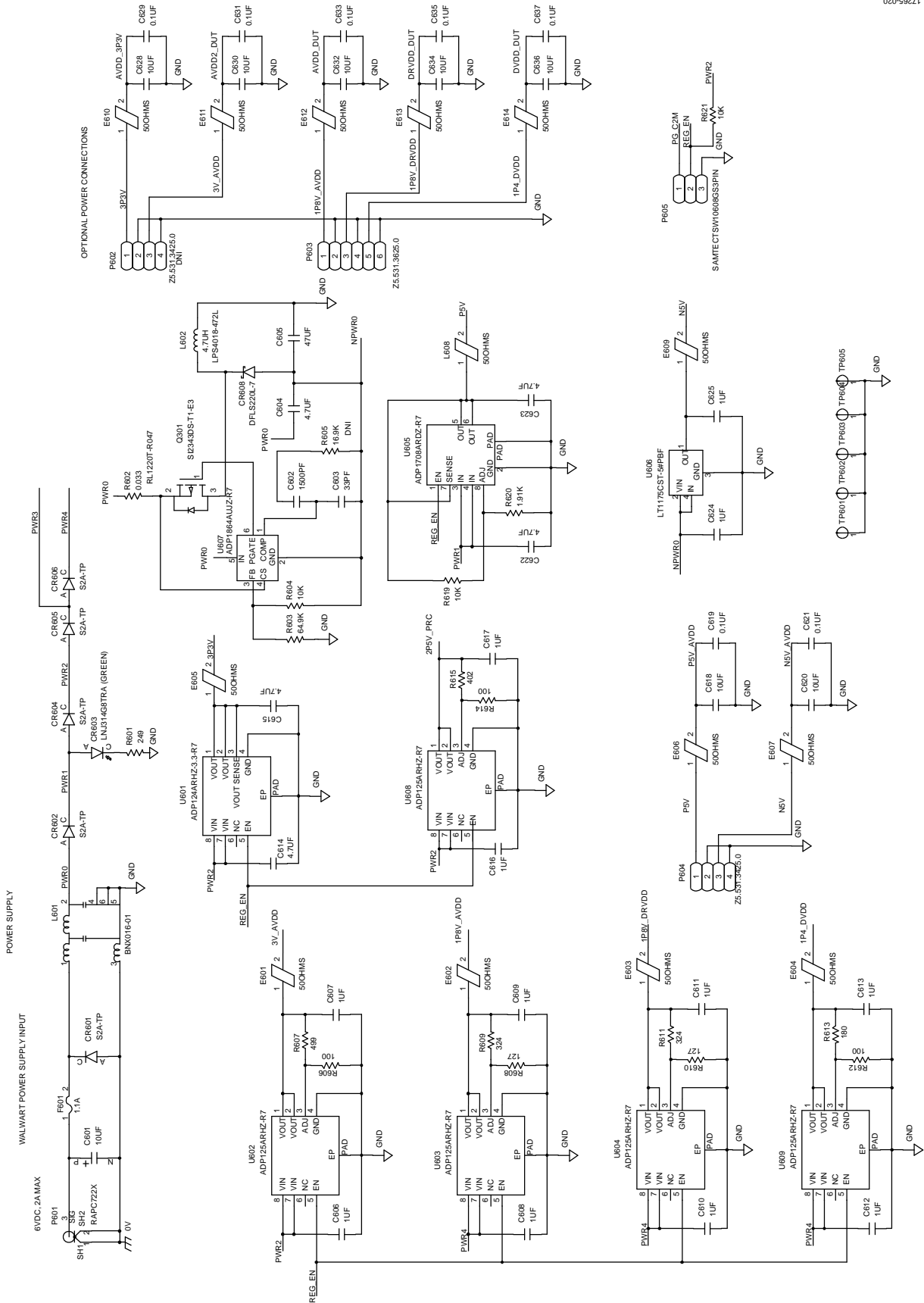


Figure 20. EVAL-AD9671EBZ Schematics Page 6

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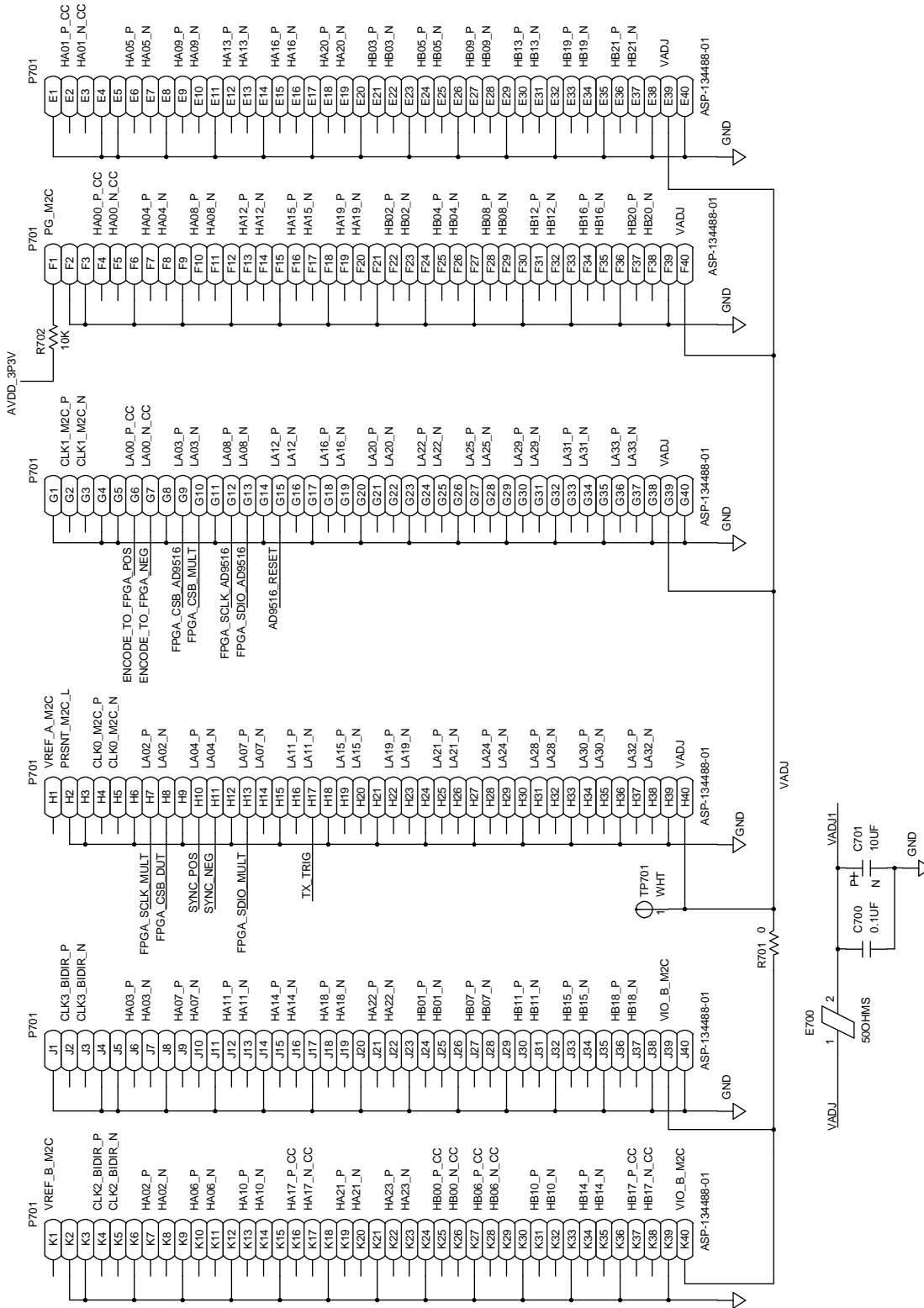


Figure 21. EVAL-AD9671EBZ Schematics Page 7



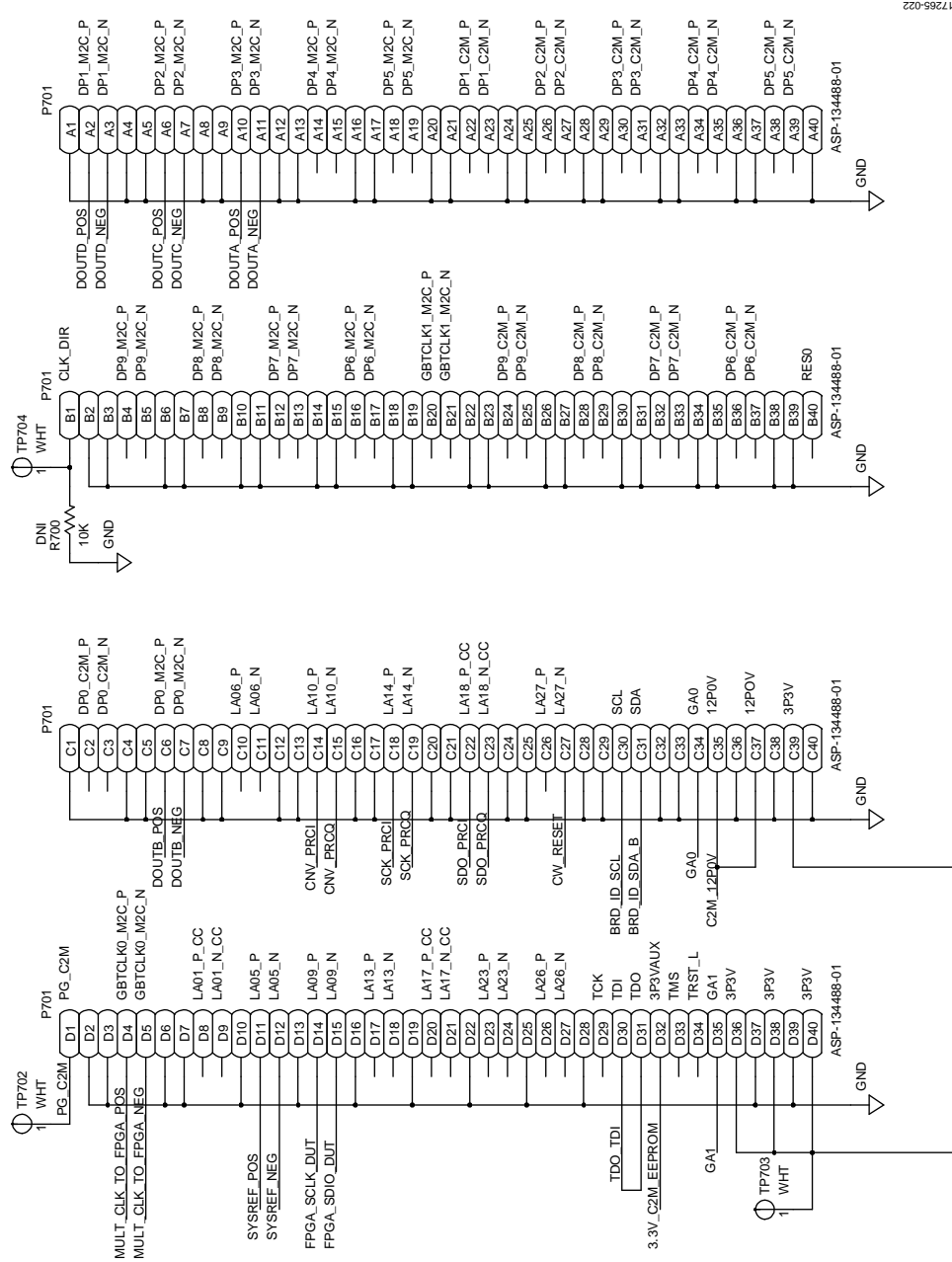


Figure 22. EVAL-AD9671EBZ Schematics Page 8

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Legal Terms and Conditions**

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