ANALOG DEVICES

AD9671EBZ Evaluation Board User Guide
UG-1460

Evaluating the AD9671 JESD204B for Octal Ultrasound AFE with Digital Demodulator

FEATURES

Full featured evaluation board for testing the AD9671
PC software for control of the AD9671 using a USB interface

EQUIPMENT NEEDED

AD9671 evaluation board (AD9671EBZ)
Analog signal source and antialiasing filter
6 V switching power supply, 2.5 A
HSC-ADC-EVALEZ board
12 V switching power supply, 2.5 A, provided with the HSC-ADC-EVALEZ board
CUI EPS060250UH-PHP-SZ, provided
PC running Windows® operating system
PC with USB 2.0 port, recommended (USB 1.1 compatible)
Spectrum analyzer for CW Doppler mode
USB cable, provided with the HSC-ADC-EVALEZ board

DOCUMENTS NEEDED

AD9671 data sheet

SOFTWARE NEEDED

VisualAnalog
SPIController

GENERAL DESCRIPTION

The AD9671EBZ evaluation board enables testing and evaluation of the AD9671 octal ultrasound analog front end (AFE) device. The AD9671EBZ evaluation board offers eight Subminiature Version A (SMA) connector inputs for all eight channels. The AD9671EBZ evaluation board connects to the HSC-ADC-EVALEZ field programmable gate array (FPGA) data capture board, and enables data capture via a USB connection to a PC. SPIController software enables flexible configuration of the AD9671, and VisualAnalog® software offers a powerful data capture as well as signal analysis tools.
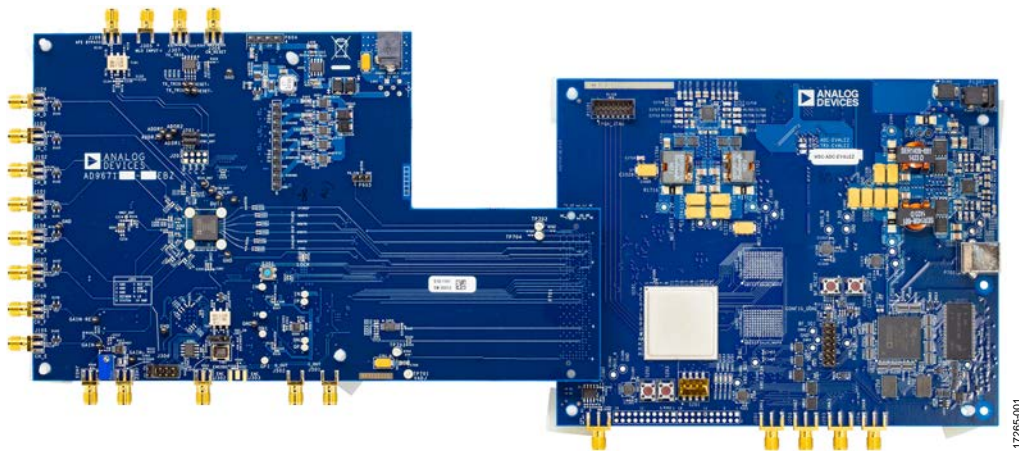
EVALUATION BOARD CONNECTION DIAGRAM

Figure 1.

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REVISION HISTORY

1/2019—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

A single switching power supply (6 V, 2.5 A) is needed to power up the AD9671EBZ evaluation board.

INPUT SIGNALS

The AD9671EBZ evaluation board offers eight SMA connector inputs for the eight AFE channels. The SMA channel inputs maps directly to the low noise amplifier (LNA) input of the AD9671 device. An optional external clock SMA input can be used to bypass the default 40 MHz crystal on the AD9671EBZ evaluation board with a J301 jumper change.

Other SMA inputs include the voltage gain amplifier (VGA) GAIN± control, the continuous wave (CW) doppler MLO± signal, the CW RESET± signal, and an optional TX_TRIG± input. The TX_TRIG signal is provided by the FPGA on the HSC-ADC-EVALEZ data capture board. A single-ended signal is the default for the VGAIN control although a differential input configuration is also possible.

OUTPUT SIGNALS

The high speed serial interface (JESD204B) digital output signals are fed to the HSC-ADC-EVALEZ data capture board via the FPGA mezzanine card (FMC) connector. The J501 and J502 SMA outputs are included for the CW doppler summed I and Q outputs.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

SOFTWARE INSTALLATION PROCEDURES

Two software programs must be installed first to work with the AD9671EBZ evaluation board. VisualAnalog is an Analog Devices, Inc. software package that enables data capture and analysis for many Analog Devices analog-to-digital converter (ADC) devices, including the AD9671 ultrasound AFE. SPIController is another Analog Devices software package that enables interfacing with many Analog Devices devices including the AD9671, and enables serial peripheral interface (SPI) read and write commands to the chip.

Installing the VisualAnalog Software

Visit www.analog.com/visualanalog and follow the download and installation instructions.

Installing the SPIController Software

Visit the SPIController software page at www.analog.comspicontroller and follow the download and installation instructions.

CONFIGURING THE AD9671EBZ EVALUATION BOARD

Take the following steps to configure the AD9671EBZ evaluation board:

1. Power up the HSC-ADC-EVALEZ data capture board by connecting it to the USB cable and 12 V adapter, then power up the AD9671EBZ evaluation board by connecting it to the 6 V adapter (see Figure 1).
2. Start VisualAnalog. The software attempts to program the HSC-ADC-EVALEZ data capture board with the default file associated with the detected AD9671EBZ evaluation board. After the file loads, the CONFIG_DONE LED illuminates on the HSC-ADC-EVALEZ data capture board (see Figure 2). Click **Yes**.
3. Select the **AD9671** folder on the left side of the window shown in Figure 3 to view the available templates. Select the **Samples** canvas, which shows output vs. sample count. After the **Samples** canvas is selected, the VisualAnalog task bar opens as shown in Figure 4.
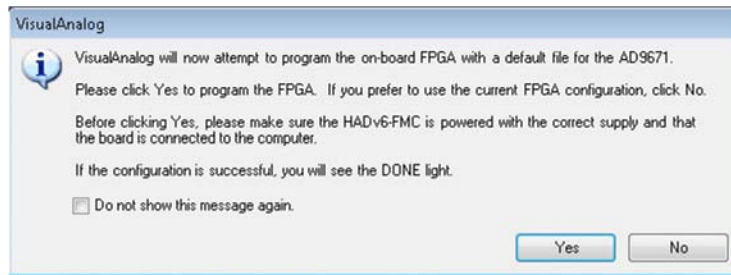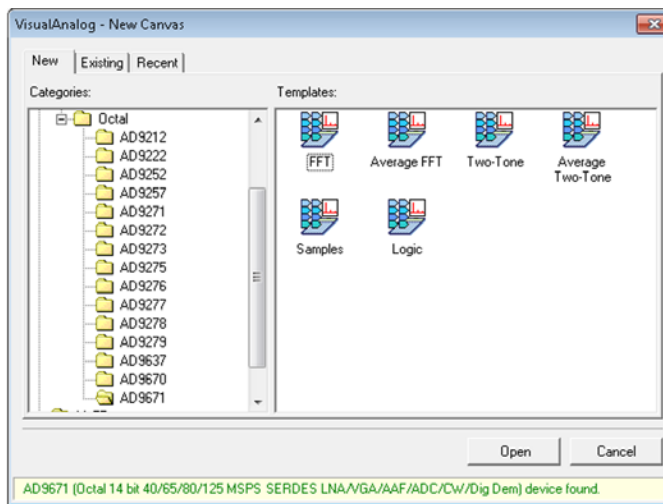

Figure 2. VisualAnalog FPGA Programming Dialog

Figure 3. VisualAnalog Canvas Selection

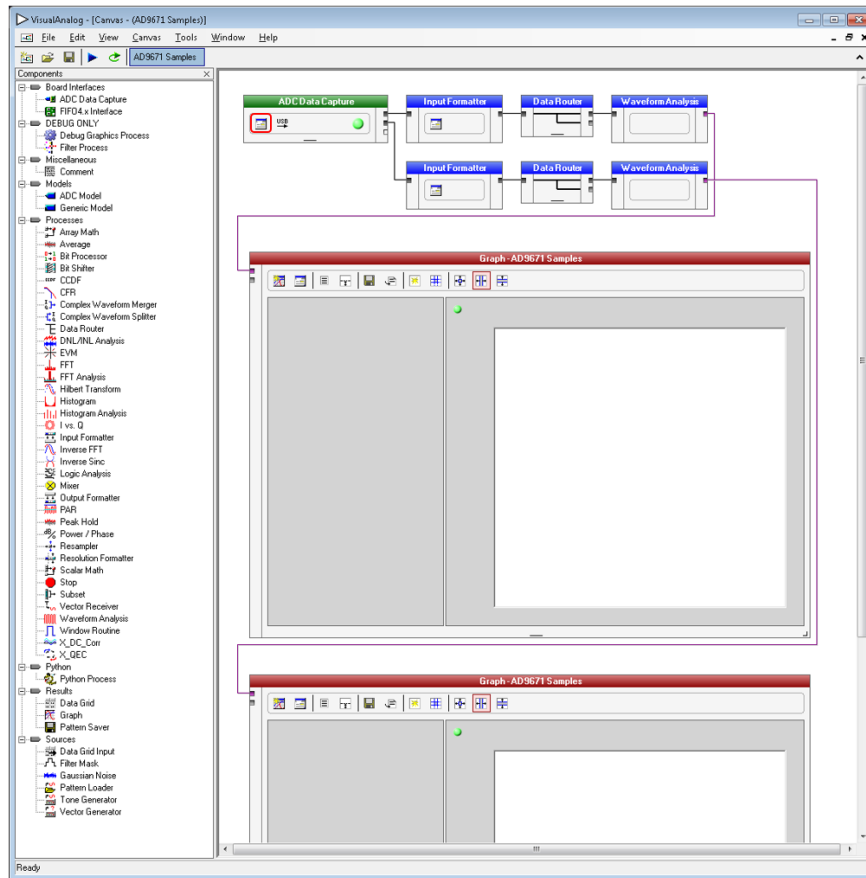*Figure 4. VisualAnalog Collapsed Window Mode*

Figure 5. AD9671 Sample Canvas

4. Click the down arrow on the right side of the task bar to expand the canvas and see the signal processing flow shown in Figure 5.

5. To reprogram the FPGA after VisualAnalog starts, click the **Settings** button in the ADC data capture block on any canvas, as marked with the red box in Figure 5. In the **Capture Board** tab in the **ADC Data Capure Settings** window shown in Figure 6, click **Browse,** select the bin file **ad9671_evalez06132014_0921am.mcs**, and then click **Program**. After the file loads, the CONFIG_DONE LED illuminates on the data capture FPGA board. Click **OK** to close the window.

6. Select the correct output mode from the **Device** tab in the **ADC Data Capture Settings** window shown in Figure 7.

7. The default clock crystal on the AD9671EBZ evaluation board is 40 MHz. To use a different speed, connect the external clock source by setting Clock Jumper J301 on the AD9671EBZ evaluation board to off state.

8. Start the SPIController. Click the **File** menu, and then click **Cfg Open**. A file **Open** dialog box opens. Select the AD9671 configuration file, **AD9671_14bit_125MSspiR03.cfg** (see Figure 8).

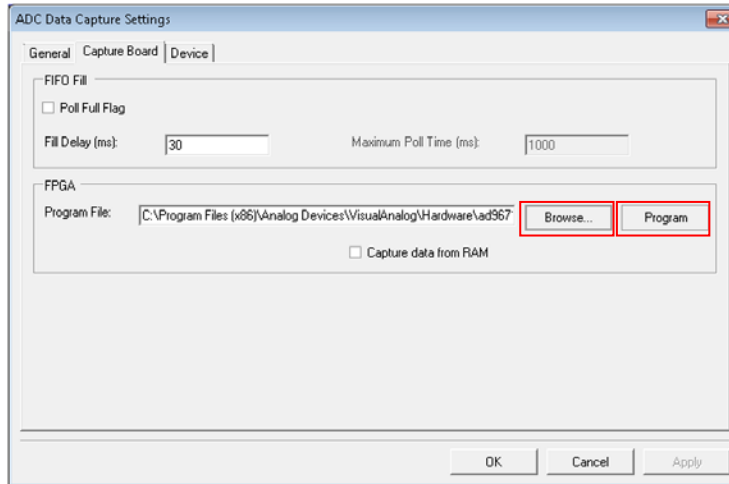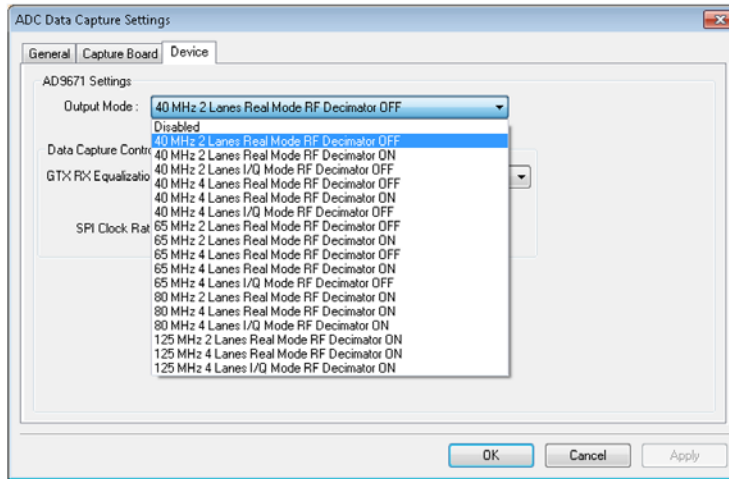*Figure 6. FPGA Programming Section*
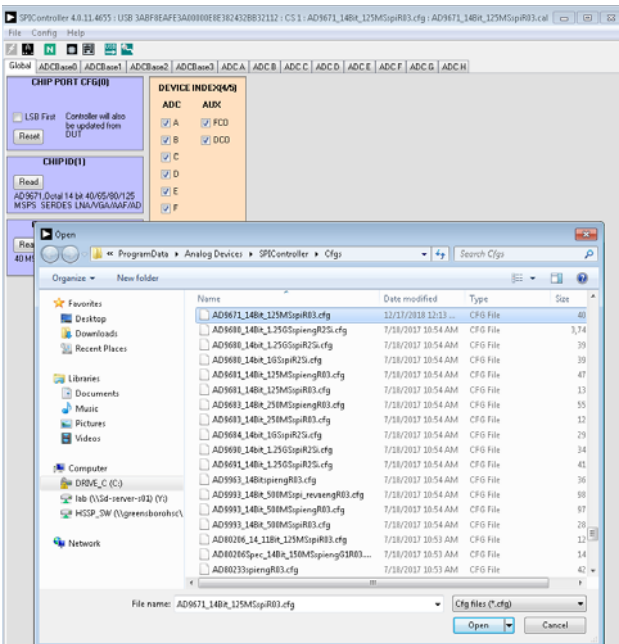

Figure 7.Output Mode Selection Section

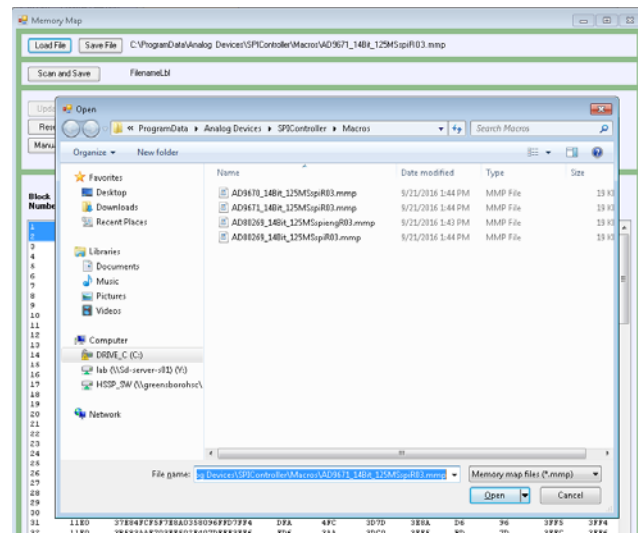*Figure 8. Configuration **File Open** Dialog Box*

*Figure 9. Memory **File Select** Dialog Box*

9. On the **Config** menu at the top of the SPIController window, click **Launch Memory Map Dialog**. This command starts the memory map shown in Figure 11, as well as a way to select prestored demodulation and decimation profiles. Click **Load File** to open the file **Open** dialog box, and select the **AD9671_14Bit_125MSspiR03.mmp** file to load the coefficient and profile memory onto the AD9671 (see Figure 9).

10. In the main SPIController window, click **File**, then click the **MacroGroup Open** command, and select the **AD9671_Test_Macro_released.mgp** file (see Figure 10).

Figure 10. SPI Macro File Select Dialog Box

Figure 11. Memory Map

USING THE SOFTWARE FOR TESTING

Carry out the following steps to test the data capture of the AD9671EBZ evaluation board:

1. The macro file loaded in Step 10 of the Configuring the AD9671EBZ Evaluation Board section is an XML file that lists SPI command macros. Each macro includes SPI writes that configure the AD9671 for a certain operating mode. The **MacroEditor** window in Figure 12 lists all macros under a dropdown list as well as under numerical tabs. The macro file contains six macros. Users can edit the XML macro file to add their own configuration macros and load the edited file onto the macro editor. Table 1 shows an example SPI macro that configures the AD9671.
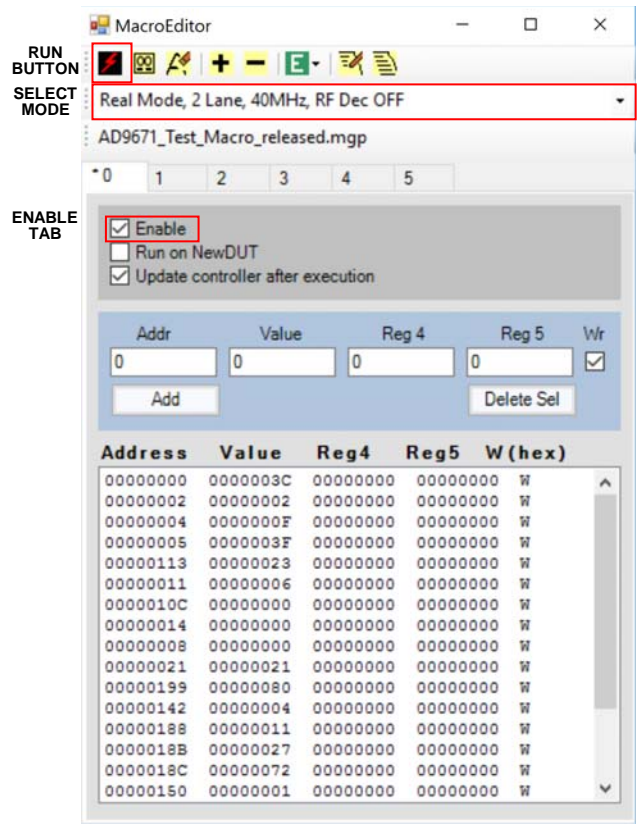
Table 1. SPI Configuration Macro Example for the AD9671

Register	Functions
0x00	SPI reset
0x02	Set speed mode
0x04, 0x05	Enable and disable channels
0x113	Enable and bypass digital filters, demodulator, decimator
0x011	LNA and VGA gain settings
0x10C	Set index profile
0x014	Offset binary enable
0x008	Time gain compensation (TGC) run mode
0x021	Set number of bits, set number of lanes
0x199	Enable sample clock counter
0x142	Enable serial initial lane alignment sequence
0x188	Enable start code
0x18B	Set start code word (MSB)
0x18C	Set start code word (LSB)
0x150	Set JESD204B scrambler, set number of lanes
0x182	Set phase-locked loop (PLL) autoconfigure
0x181	Set PLL N divider
0x10C	Set SPI TX_TRIG
0x00F	Filter cutoff frequency, band
0x02B	Set analog LPF and HPF to defaults, tune filters

2. To run one of the macros, select the appropriate tab, **0** to **5**, shown in Figure 12, or select the macro from the drop down list. Select the **Enable** checkbox while making sure the internal or external clock matches the speed mode selected, as described in Step 7 of the Configuring the AD9671EBZ Evaluation Board section. See Table 2 for the modes supported by the macro. Click the **Run** button shown in Figure 12 to run the macro.

Table 2. Real Modes Supported by the Macro

No. of Lanes	Encode Clock (MHz)	RF Decimation	Channels Per Lane	Speed Mode (MSPS)
2	40	Off	4	40
2	65	On	4	40
2	65	Off	4	65
2	80	On	4	80
4	80	On	2	80
4	125	On	2	125

Figure 12. Macro Editor Graphical User Interface (GUI)

3. Click the blue arrow on the upper left side of the VisualAnalog toolbar shown in Figure 14 to run the canvas once, or click the green repeat button to set the canvas to run continually. The **Samples** canvas produces two windows that show 8192 time domain samples for Channel A and Channel B, as shown in Figure 13.
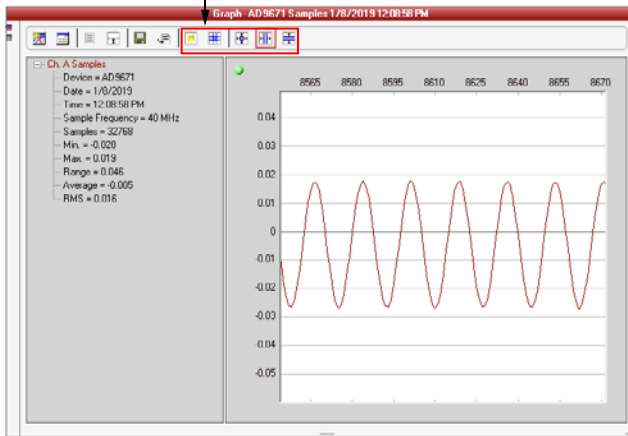
BUTTONS FOR ZOOMING IN AND RESIZING

Figure 13. Sample Canvas Output Window

4. The **AD9671_Average_FFT.vac** canvas is set up for running and calculating fast Fourier transform (FFT) as shown in Figure 14. The average count is set to five, which means the canvas either needs to be run five times, or left in continuous run mode. The results in Figure 14 show the shaping of the noise floor as a result of the analog filters and the digital high-pass filter.

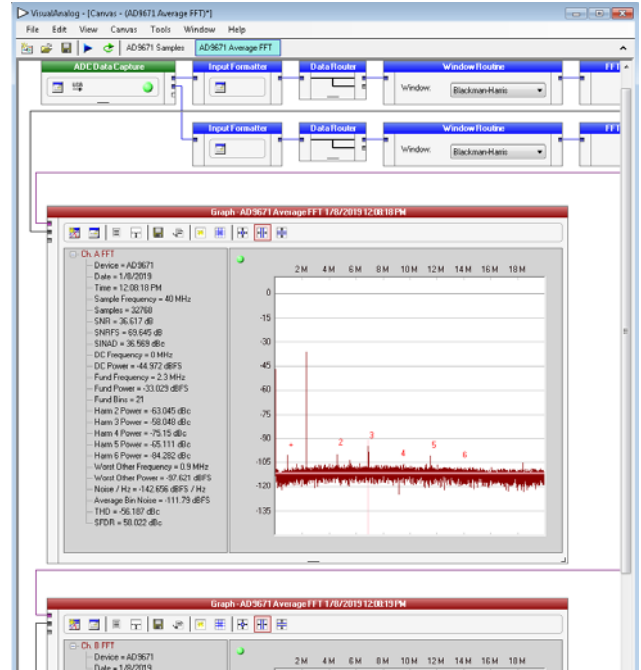

Figure 14. Average FFT Canvas Output Window

EVALUATION BOARD SCHEMATICS

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Figure 15. EVAL-AD9671EBZ Schematics Page 1

Figure 16. EVAL-AD9671EBZ Schematics Page 2

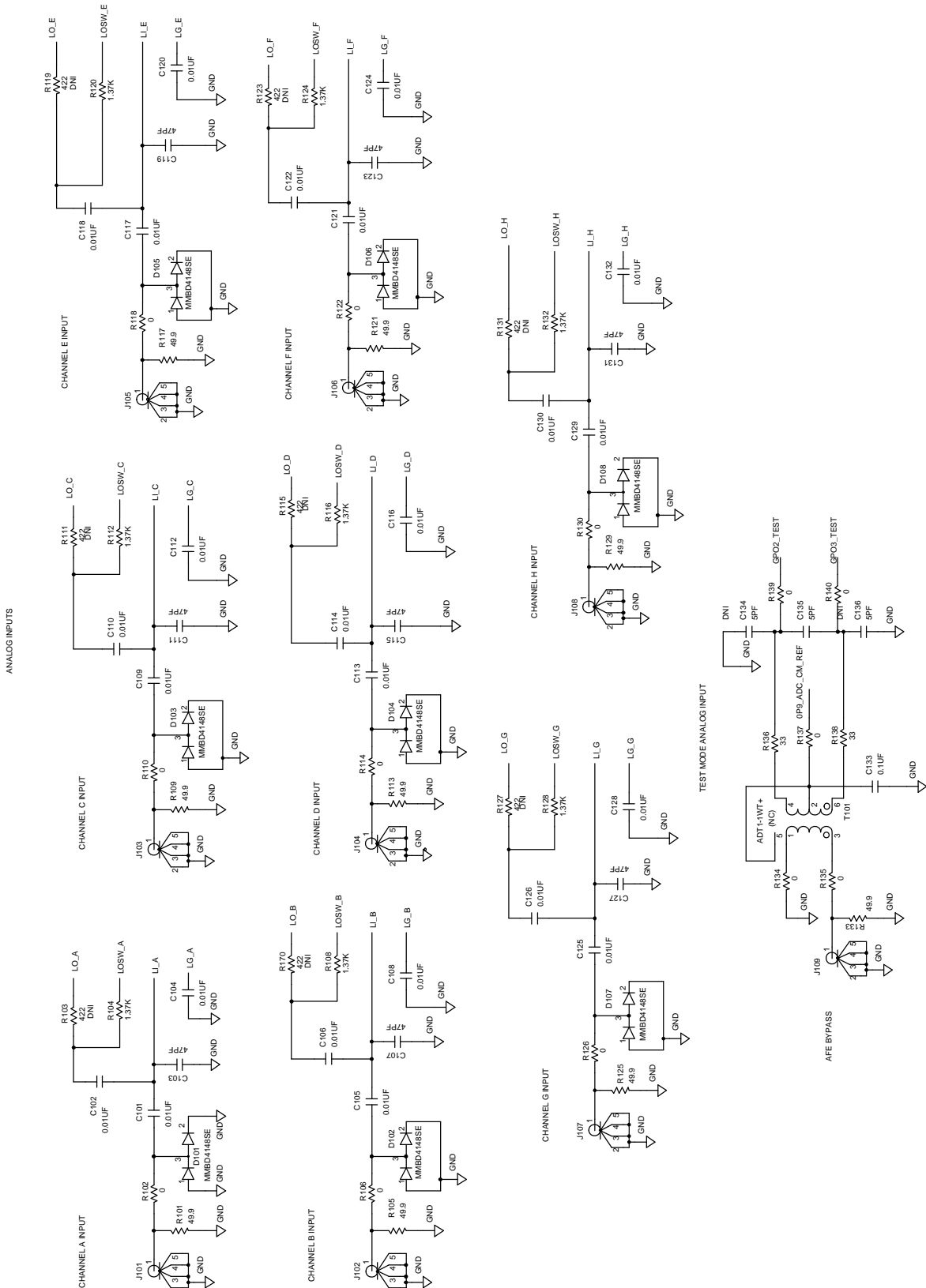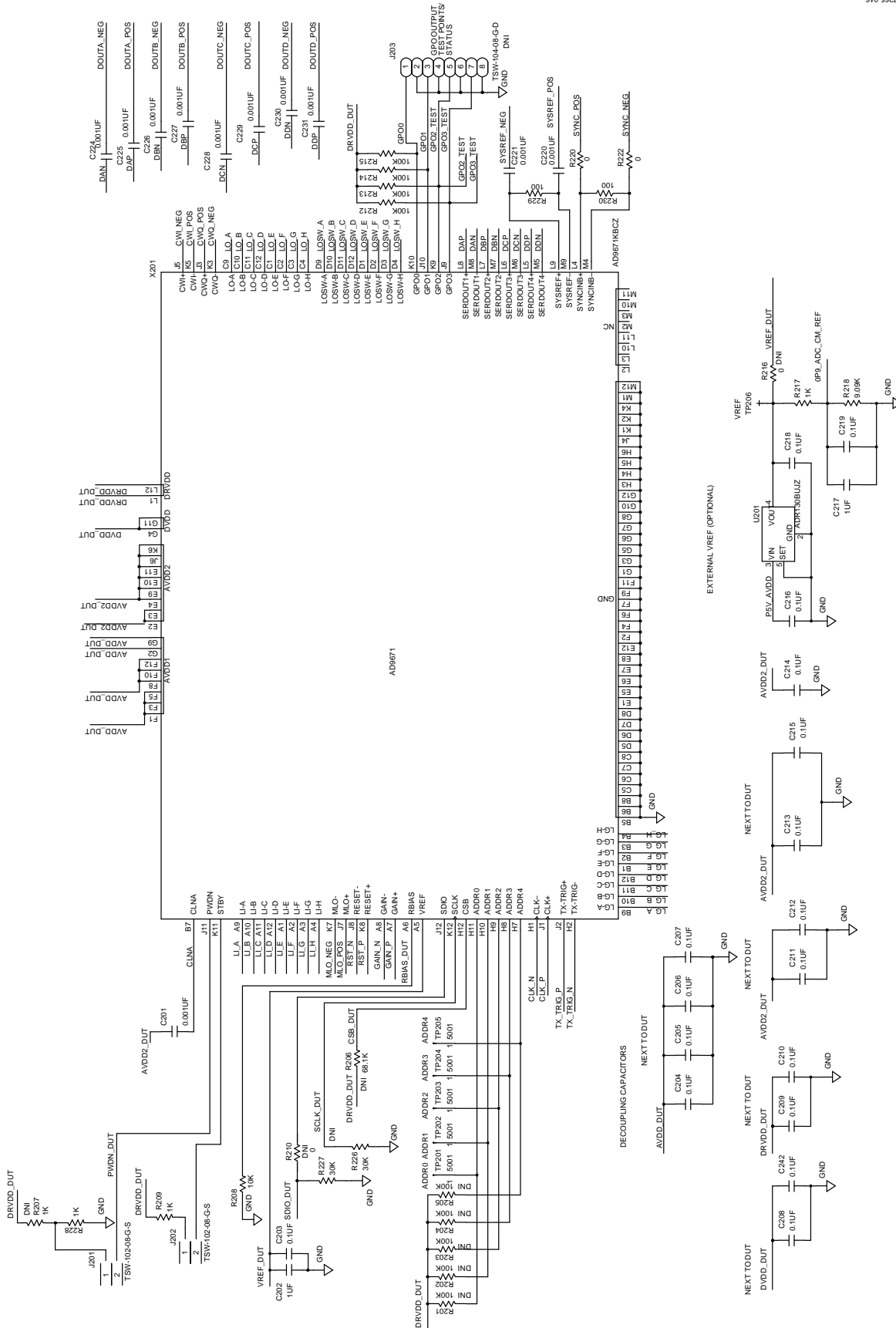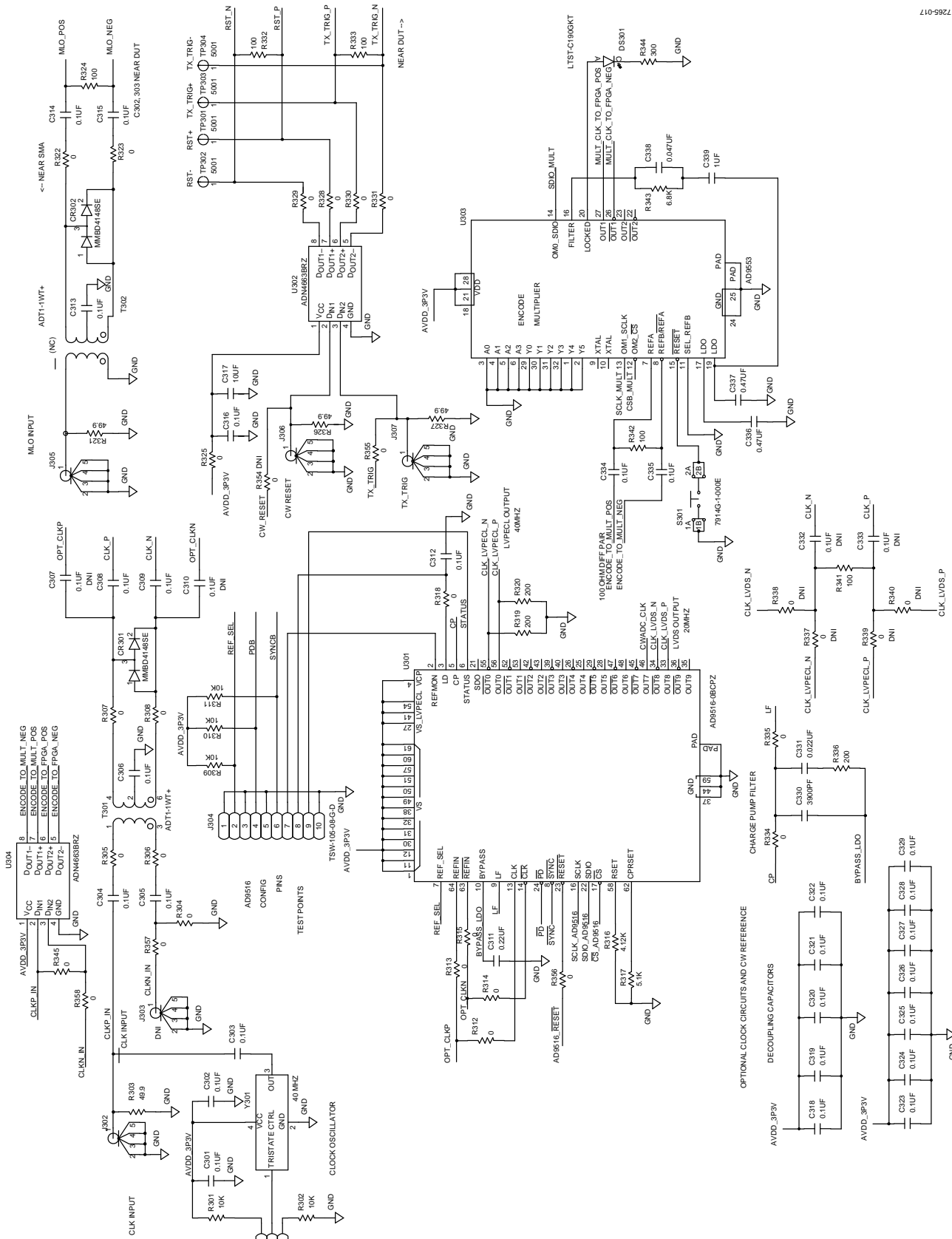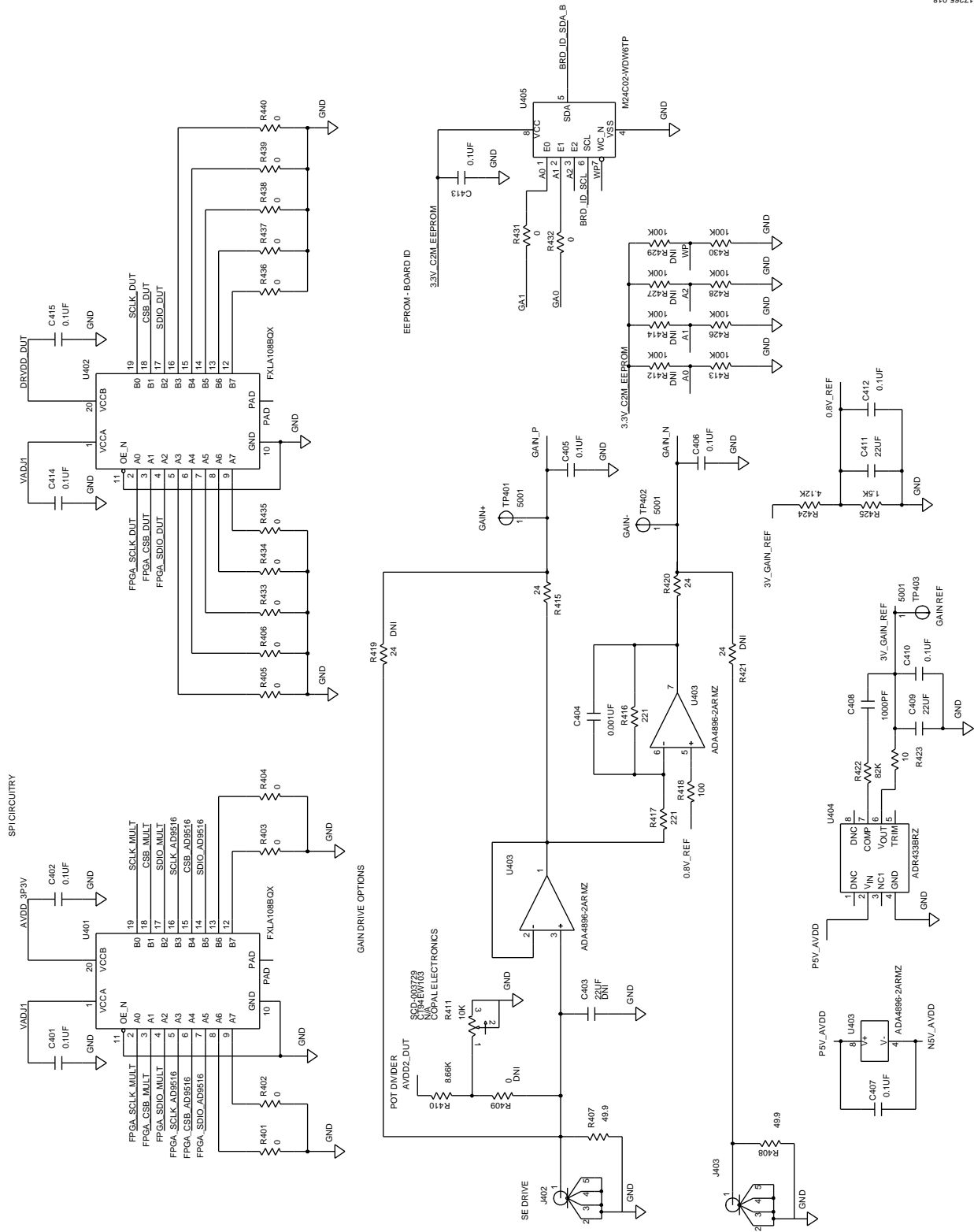*Figure 17. EVAL-AD9671EBZ Schematics Page 3*

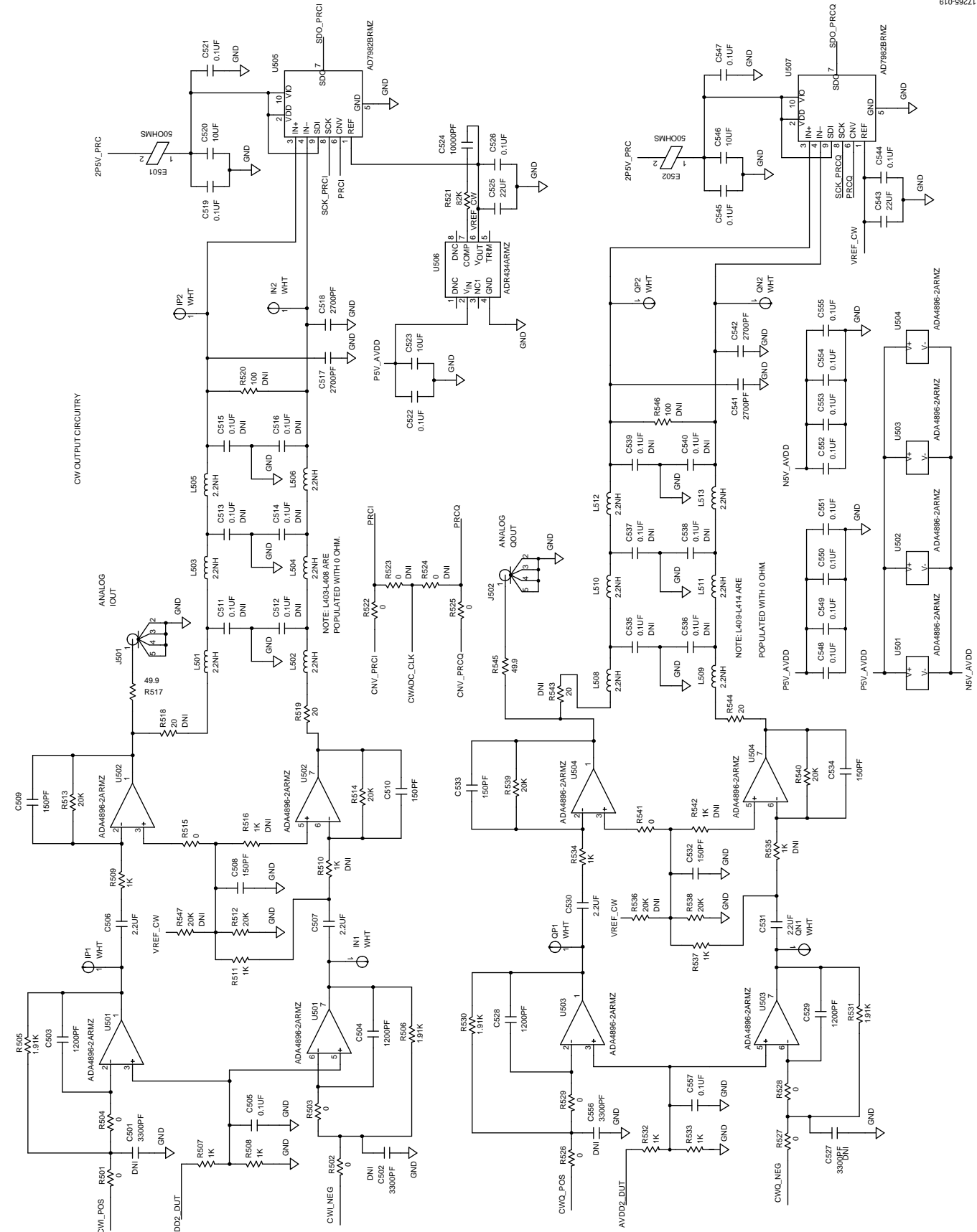*Figure 18. EVAL-AD9671EBZ Schematics Page 4*

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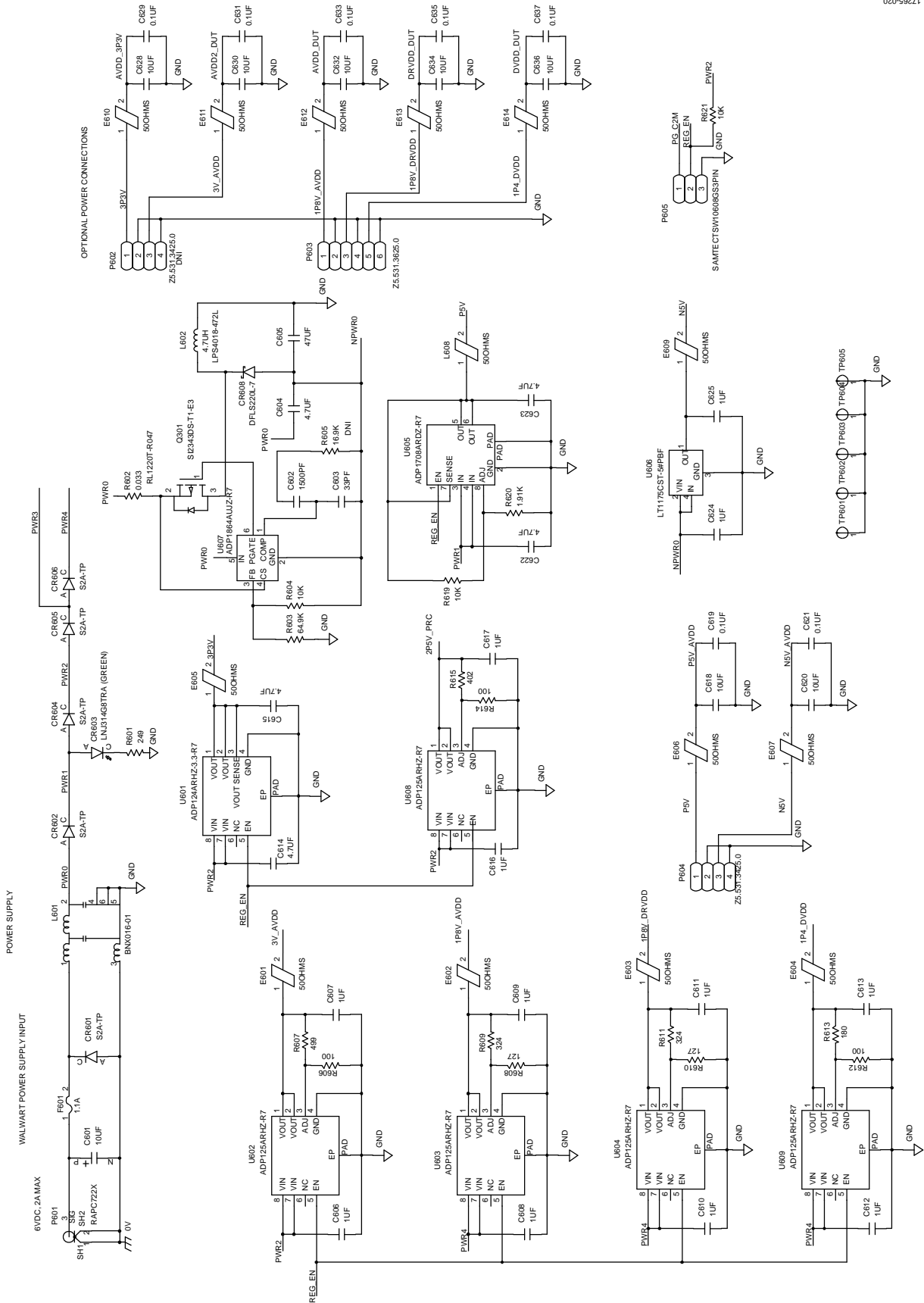*Figure 19. EVAL-AD9671EBZ Schematics Page 5*
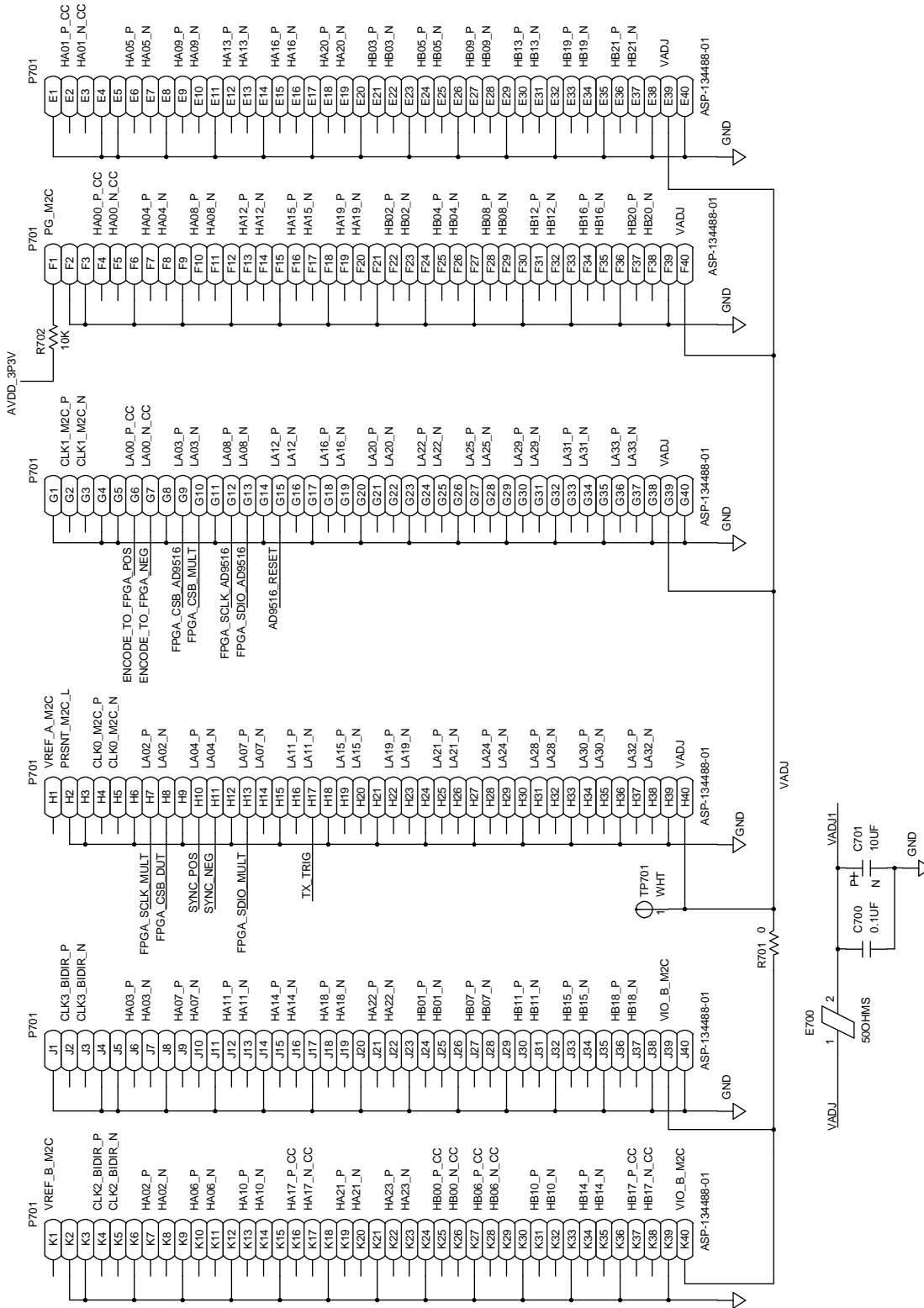
Figure 20. EVAL-AD9671EBZ Schematics Page 6
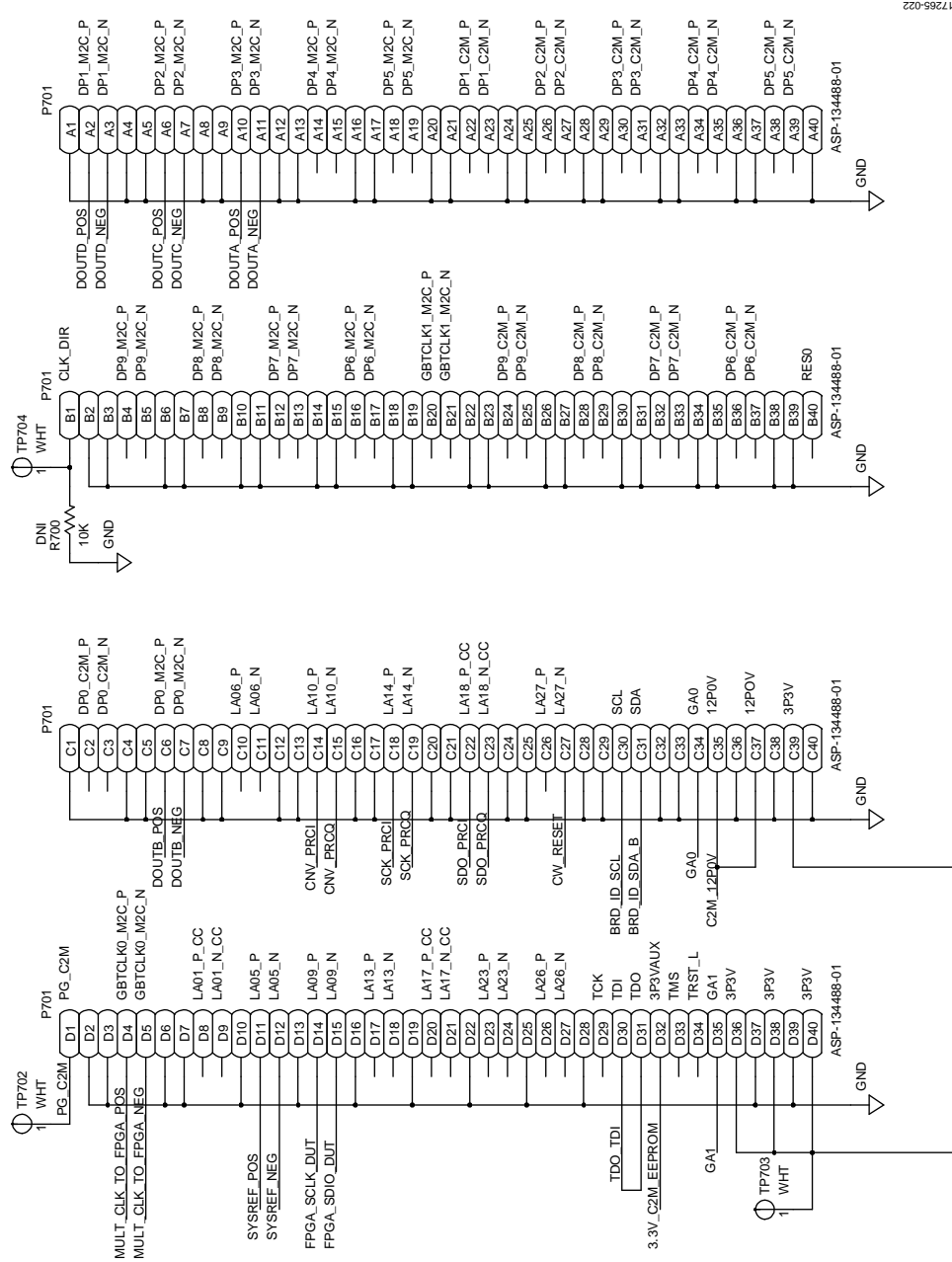
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Figure 21. EVAL-AD9671EBZ Schematics Page 7

Figure 22. EVAL-AD9671EBZ Schematics Page 8

NOTES

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