

LTC6360

High Speed Op Amp with True Zero Output

DESCRIPTION

Demonstration circuit 1639 allows quick setup of the LTC6360 true zero op amp. The op amp is configured as a unity gain buffer, with landing pads provided to make other gains configurable. Ample bypass is provided for both the input supply and for the -0.6V on-chip charge pump. The recommended 10Ω 330pF output compensation is provided on board for unity-gain stability. If this

compensation is removed, gain bandwidth increases but the op amp is stable only in gains of four and higher.

Design files for this circuit board are available at <http://www.linear.com/demo>

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OPERATING PRINCIPLES

Most op amps which operate on single supplies have outputs that cannot get all the way to ground. The saturation of their output devices leave 10's of millivolts of output voltage error when the output tries to swing to

ground. The LTC6360 has an onboard charge pump that creates a -0.6V internal supply for the output stage, so it can swing all the way to ground and even a little below ground.

QUICK START PROCEDURE

Demonstration circuit 1639 is simple to use, with only one jumper provided to allow the shutdown option.

1. Set the power supply to 5V, then turn off the power supply. As shown in Figure 1, connect the +5V lead from the power supply to the V^+ terminal of the demo circuit, and connect the COM side of the supply to the GND terminal of the demo circuit.
2. Turn on the supply. Note that without input excitation the output is very near 0mV, much closer to ground than most op amps can achieve.
3. You are now free to connect a source to the input and exercise the LTC6360. The input range is 0V to about 4.25V. (Under high frequency large signal swing excitation, you may see some odd behavior as the negative charge pump voltage begins to safely collapse.)
4. If you want to set the LTC6360 for some other positive gain, turn off the supply and disconnect the board. Refer to the schematic in Figure 2. Install appropriate resistors at R7 and R6, and install appropriate impedances at C7 and R5 (shorts and/or blocking capacitance). The time domain and frequency responses can be adjusted using a small capacitance at C8.
5. For inverting gain, install J2 and appropriate passives in the path to the $-$ input. For inverting gains, the $+$ input must be biased up at some voltage. Installing R13 connects the $+$ input to the "EXT_VCM" turret which is biased nominally at 2V by R11 and R12, or the turret can be driven with an external supply.
6. **Shutdown:** The LTC6360 can be shut down by moving the shunt on JP1 from the "Enable" position to the "Disable" position. It can also be shut down and reactivated electrically via the $\overline{\text{SHDN}}$ turret, in which case the shunt on JP1 should be removed entirely.

QUICK START PROCEDURE

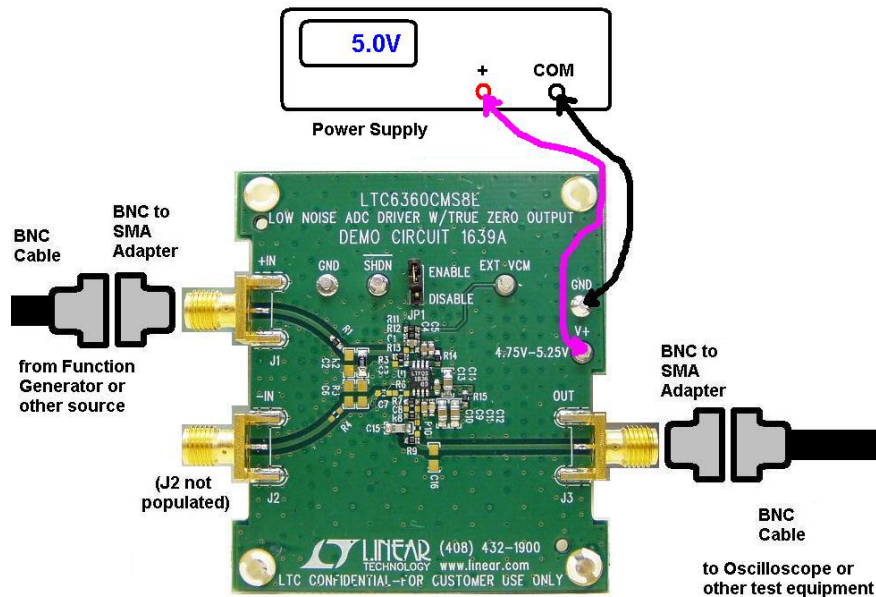


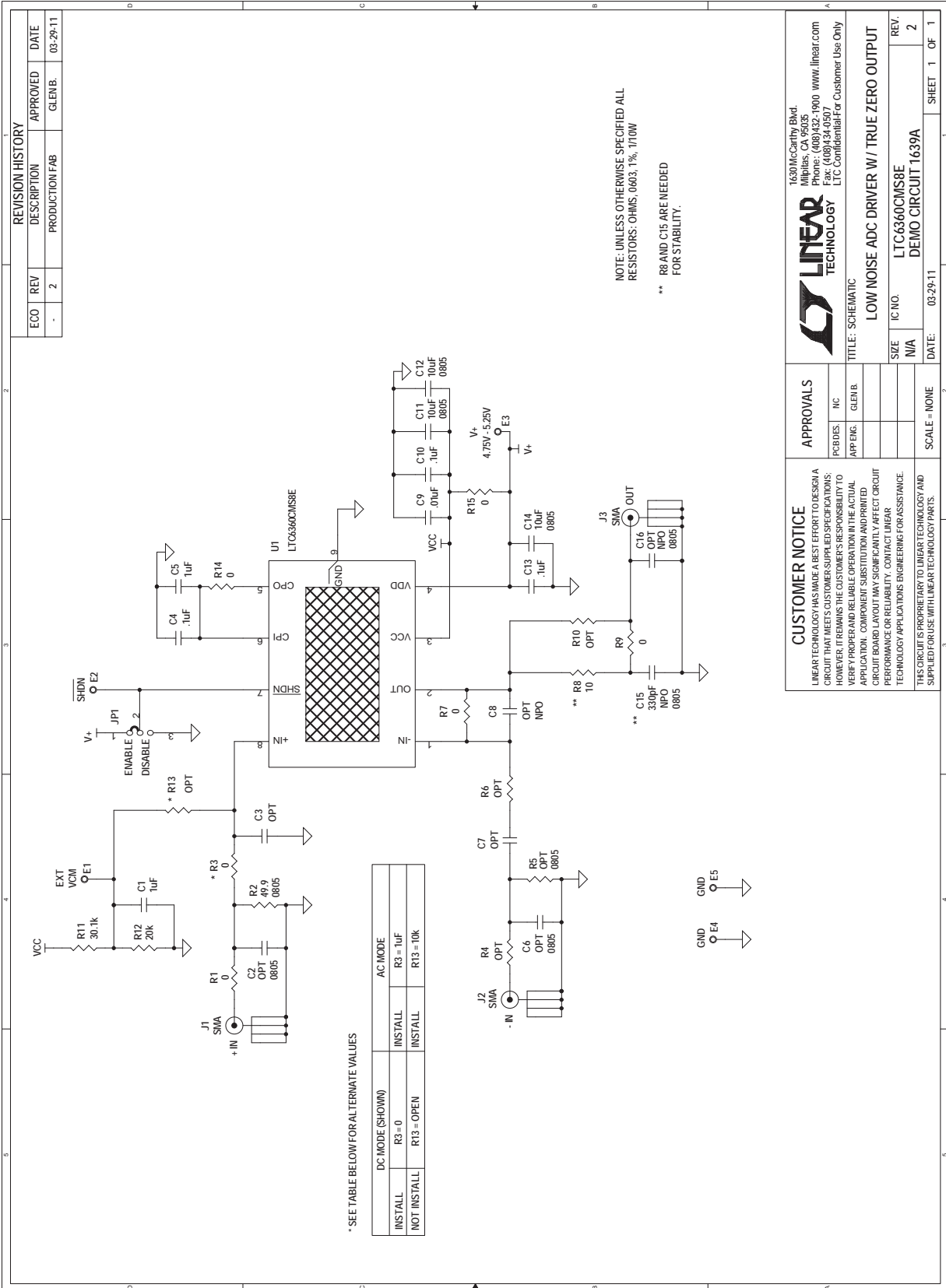
Figure 1. Proper Equipment Setup.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C1, C5	CAP., X7R, 1 μ F, 16V, 10% 0603	AVX, 0603YC105KAT2A
2	0	C2, C6	CAP., 0805	OPT
3	0	C3, C7	CAP., 0603	OPT
4	3	C4, C10, C13	CAP., X7R, 0.1 μ F, 25V, 10% 0603	AVX, 06033C104KAT2A
5	0	C8	CAP., 0603, NPO	OPT
6	1	C9	CAP., X7R, 0.01 μ F, 50V, 10% 0603	AVX, 06035C103KAT2A
7	3	C11, C12, C14	CAP., X5R, 10 μ F, 6.3V, 20% 0805	AVX, 08056D106MAT2A
8	1	C15	CAP., CERM 330pF, 50V, NPO, 0805	AVX, 08055A331JAT2A
9	0	C16	CAP., 0805, NPO	OPT
10	5	E1-E5	TESTPOINT, TURRET, .065" PBF	MILL-MAX, 2308-2-00-80-00-00-07-0
11	1	JP1	HEADER, 3 PINS, 2mm	SAMTEC, TMM-103-02-L-S
12	1	XJP1	SHUNT, 2mm CENTER	SAMTEC, 2SN-BK-G
13	2	J1, J3	CONN, BNC, SMA 50 Ω EDGE-LANCH	E. F. JOHNSON, 142-0701-851
14	0	J2	CONN, BNC, SMA 50 Ω EDGE-LANCH	OPT
15	6	R1, R3, R7, R9, R14, R15	RES., CHIP, 0, 1/10W, 0603	VISHAY, CRCW06030000Z0EA
16	1	R2	RES., CHIP, 49.9, 1/8W, 1% 0805	VISHAY, CRCW080549R9FKEA
17	0	R4, R6, R10, R13	RES., 0603	OPT
18	0	R5	RES., 0805	OPT
19	1	R8	RES., CHIP, 10, 1/10W, 1% 0603	VISHAY, CRCW060310R0FKEA
20	1	R11	RES., CHIP, 30.1k, 1/10W, 1% 0603	VISHAY, CRCW060330K1FKEA
21	1	R12	RES., CHIP, 20k, 1/10W, 1% 0603	VISHAY, CRCW060320K0FKEA
22	4	MH1-MH4 (STAND-OFF)	STAND-OFF, NYLON (SNAP ON), 0.50" TALL	KEYSTONE, 8833(SNAP ON)
23	1	U1	LOW NOISE ADC DRIVER W/TRUE ZERO OUTPUT	LINEAR TECH., LTC6360CMS8E#TRPBF
24	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT #1639A
25	1	STENCIL FOR TOP SIDE	STENCIL	STENCIL 1639A

dc1639f

SCHEMATIC DIAGRAM



REVISION HISTORY				
ECO	REV	DESCRIPTION	APPROVED	DATE
-	2	PRODUCTION FAB	GLENB.	03-29-11

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APPROVALS

PCBIDS:	NC
APP ENG:	GLENB.

TITLE: SCHEMATIC

LOW NOISE ADC DRIVER W/ TRUE ZERO OUTPUT

SIZE:	N/A
IC NO.:	LTC6360CMS8E
REV.:	2

DEMO CIRCUIT 1639A

DATE: 03-29-11

SHEET 1 OF 1

CUSTOMER NOTICE

LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT YOUR LOCAL TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.

THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

Figure 2

DEMO MANUAL DC1639

DEMONSTRATION BOARD IMPORTANT NOTICE

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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