ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4007 & NTE4007T
Integrated Circuit
CMOS, Dual Complementary Pair Plus Inverter

Description:

The NTE4007 (14–Lead DIP) and NTE4007T (SOIC–14) are multipurpose devices consisting of three N–Channel and three P–Channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse–shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

Features:

- Diode Protection on All Inputs
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Ambient Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Stresses exceeding Absolute Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommend Operating Conditions may affect device reliability.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level	V_{IL}									
(V_O = 4.5Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	Vdc
(V_O = 9.0Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	Vdc
(V_O = 13.5Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	Vdc
"1" Level	V_{IH}									
(V_O = 0.5Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	Vdc
(V_O = 1.5Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–5.0	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–1.0	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.5	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–10	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	1.0	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.5	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	10	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.5	–	0.0010	0.5	–	15	µAdc
		15	–	1.0	–	0.0015	1.0	–	30	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Gate, C_L = 50pF, Note 3, Note 4)	I_T	5.0	I_T = (0.7µA/kHz) f + I_{DD}/6							µAdc
		10	I_T = (1.4µA/kHz) f + I_{DD}/6							µAdc
		15	I_T = (2.2µA/kHz) f + I_{DD}/6							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

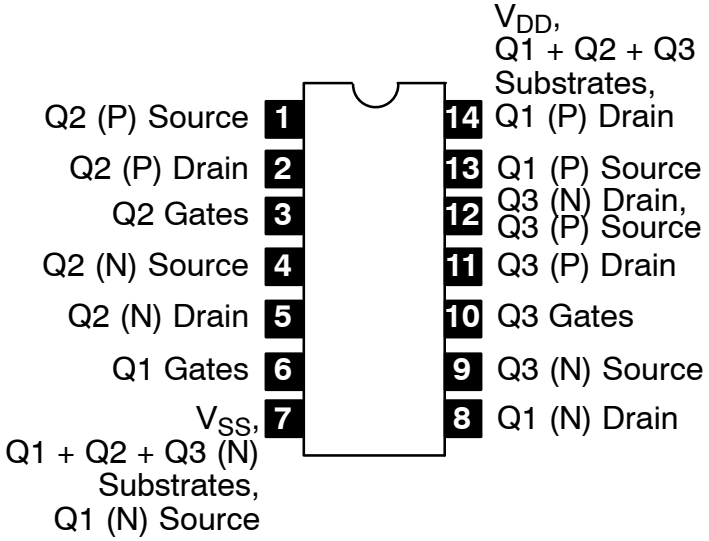
Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2, Note 5)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (1.2ns/pf) C_L + 30ns	t_{TLH}	5.0	–	90	180	ns
t_{TLH} = (0.5ns/pf) C_L + 20ns		10	–	45	90	ns
t_{TLH} = (0.4ns/pf) C_L + 15ns		15	–	35	70	ns
Output Fall Time t_{THL} = (1.2ns/pf) C_L + 15ns	t_{THL}	5.0	–	75	150	ns
t_{THL} = (0.5ns/pf) C_L + 15ns		10	–	40	80	ns
t_{THL} = (0.4ns/pf) C_L + 10ns		15	–	30	60	ns
Turn−Off Delay Time t_{PLH} = (1.5ns/pf) C_L + 35ns	t_{PLH}	5.0	–	60	125	ns
t_{PLH} = (0.2ns/pf) C_L + 20ns		10	–	30	75	ns
t_{PLH} = (0.15ns/pf) C_L + 17.5ns		15	–	25	55	ns
Turn−On Delay Time t_{PHL} = (1.0ns/pf) C_L + 10ns	t_{PHL}	5.0	–	60	125	ns
t_{PHL} = (0.3ns/pf) C_L + 15ns		10	–	30	75	ns
t_{PHL} = (0.2ns/pf) C_L + 15ns		15	–	25	55	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 5. The formulas given are for the typical characteristics only. Switching specifications are for devices connected as an inverter.

Pin Connection Diagram



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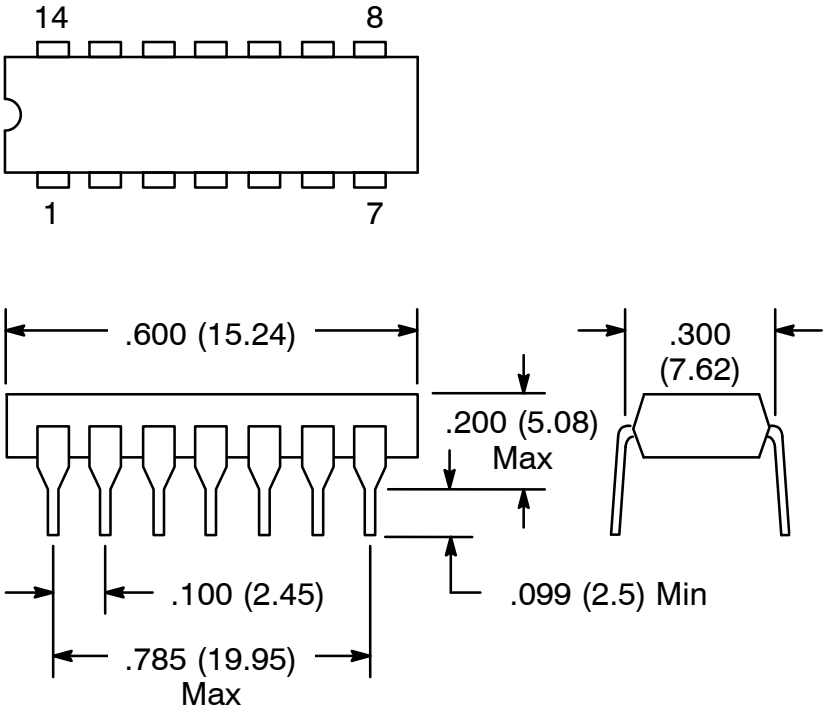

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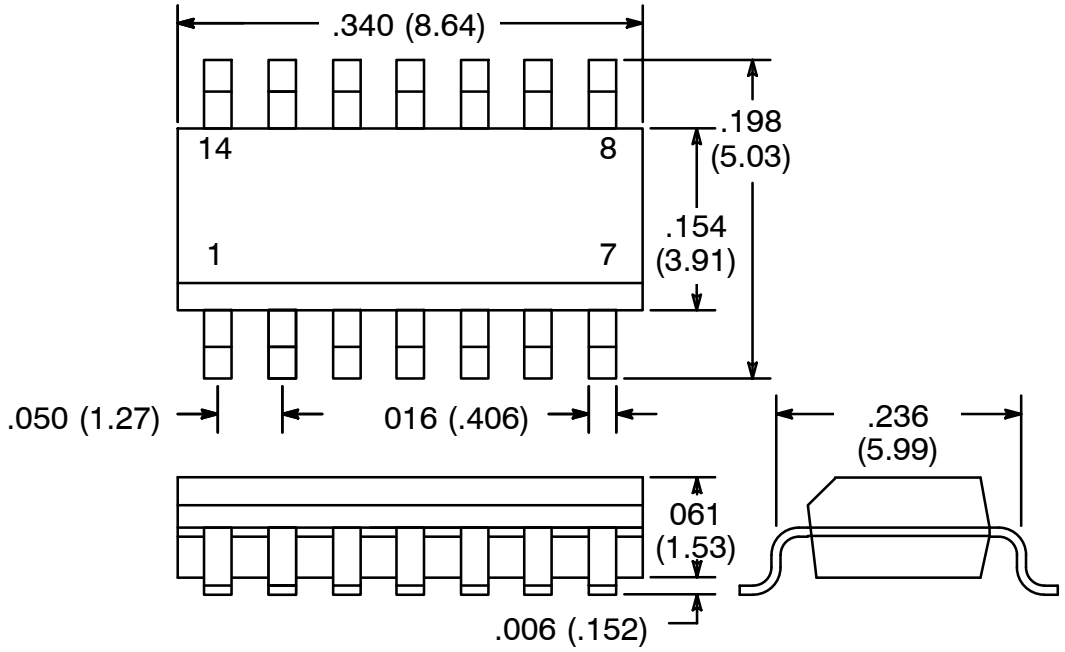

NOTE: Pin1 on Beveled Edge