Revision History
8GB eMMC 153ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Release	Dec. 2021
Rev 1.1	Corrections in Table.5, 6 & 15	Jan. 2022
Rev 1.2	Product revision "PRV" revised from 0x01 to 0x0A	Apr. 2022
Rev 1.3	Corrections on Enhance Mode Support functions References updated to JEDEC Spec JESD84-B51 Added Appendix : V_{CCQ} Power-Off Sequence	Nov. 2022

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1 Product Overview

1.1 Product Description

Alliance Memory's 8GB eMMC device (AS08FC) is a high performance embedded MMC solution designed for embedded NAND flash applications. It supports eMMC/JEDEC 5.1 industry standard and is backward compatible with eMMC 4.5 & 5.0 version.

AS08FC device contains both MLC NAND flash and eMMC controller. A single 3V supply voltage is for the NAND area (VCC) with internal regulator and Dual supply voltages 1.8V or 3V (VCCQ) for eMMC controller. Customers find it easy to use AS08FC without having to consider any changes inside device such as Flash, leading to easier & faster development of applications (fast time to market).

Alliance Memory's featured embedded flash management software or FTL(Flash Transition Layer) of eMMC manages high reliability with noticeable Wear Leveling, Bad Block Management and strong ECC and achieves high performance.

1.2 Product Ordering Information

Table 1. Ordering Information

Capacities (GB)	Part Number	eMMC Version	NAND Die	Temperature	Package Size (mm)	Package Type
8	**ASFC8G31M-51BIN**	5.1	64Gb x 1	Industrial Grade -40^{O}C ~ 85^{O}C	11.5x13.0x1.0	153ball FBGA

Note1. HS200/HS400 can be supported at only V_{CCQ} 1.8V

1.3 Key Features

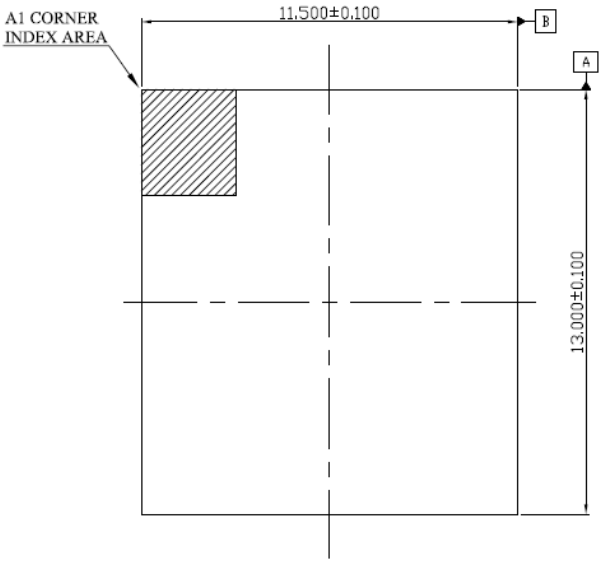
- Supports features of eMMC5.1 which are defined in JEDEC Standard
  - Supported Features : Boot, RPMB, Write Protection, DDR, HS200, Multi-partitioning, Secure Erase/Trim, Trim, HPI, Background operation, Discard, Sanitize, Security features, Partition types, Packed commands Real time clock, Dynamic device capacity, Power off notification, Thermal spec, Cache, HS400, Field Firmware Update, Security Removal type, Device Health Report, Enhanced Strobe, Command Queuing, Secure Write protection
  - Non-supported Features : Large Sector Size (4KB)

- Full backward compatibility with previous eMMC 4.41/4.5/5.0 specification and MultiMediaCard system specification
- Programmable bus width : 1bit (Default), 4bit and 8bit Data bus.
- MMC I/F Clock Frequency : 0 ~ 200MHz
- MMC I/F Boot Frequency : 0 ~ 52MHz
- Operating Temperature : -40^{O}C ~ 85^{O}C
- Storage Temperature : -40^{O}C ~ 85^{O}C
- Operating Power Supply
  - V_{CC} : 2.7V ~ 3.6V (for NAND Flash Memory)
  - V_{CCQ} : 1.7V ~ 1.95V or 2.7V ~ 3.6V (for Interface)

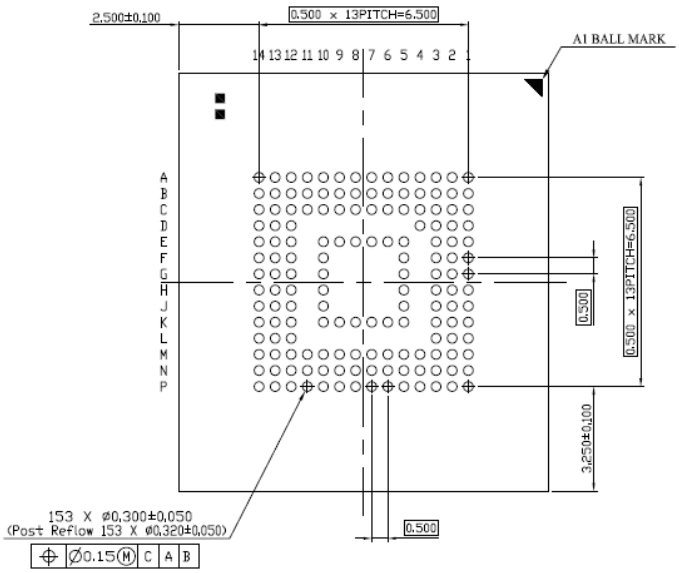
2 Package Information

2.1 Package Dimension

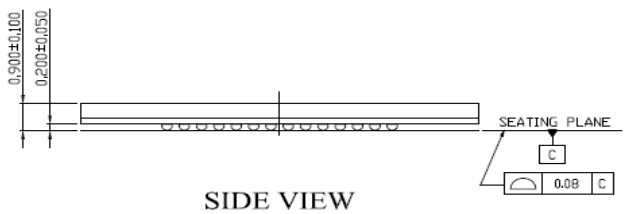
Figure 1. **11.5 x 13.0 x 1.0 (mm) Package Dimension**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE :
1. ALL DIMENSION ARE IN MILLIMETERS.
2. ⚠1 POST REFLOW SOLDER BALL DIAMETER.
(Pre Reflow diameter : 0.30±0.02)
3. ⚠2 TOLERANCE INCLUDES WARPAGE.

2.2 Ball & Signal Assignment

Figure 2. **eMMC Package Ball Assignment**

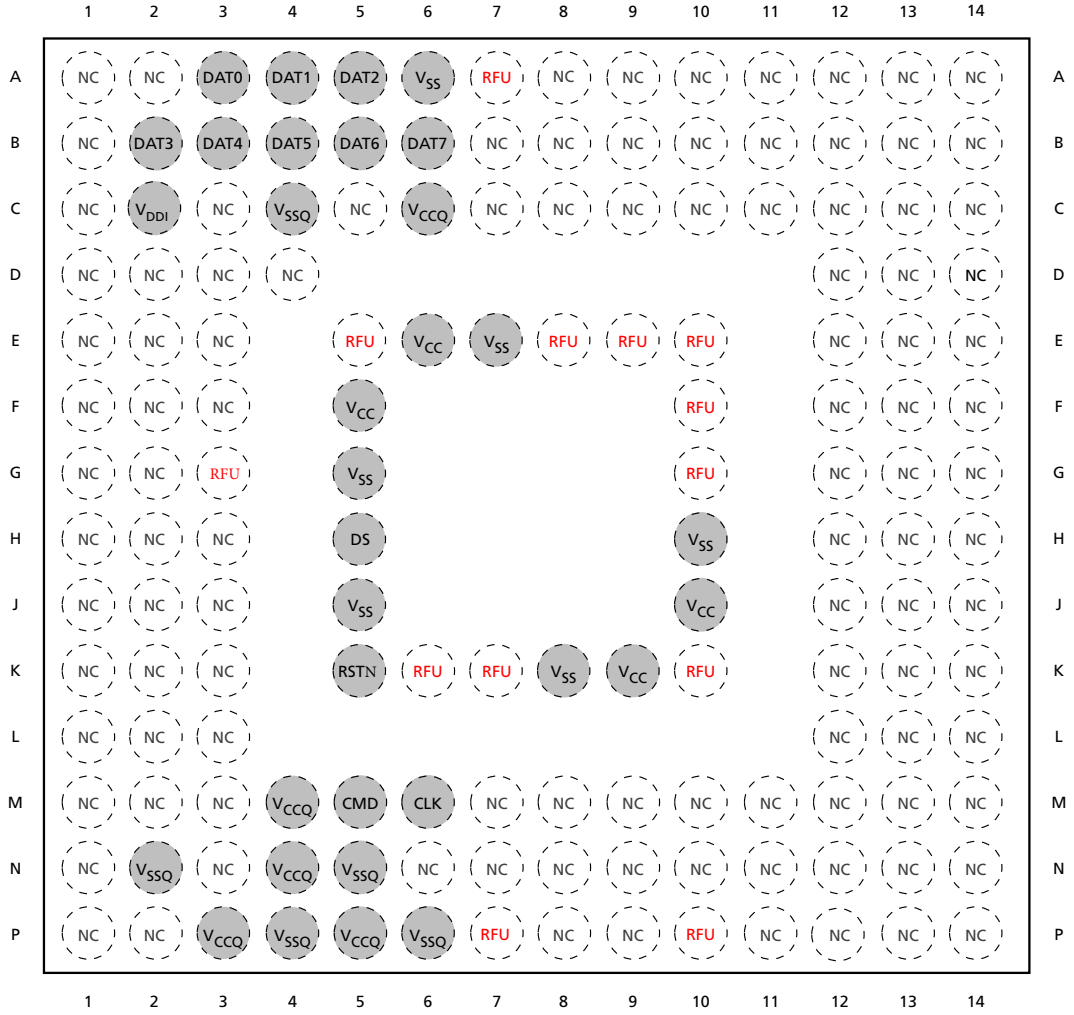


Table 2. Ball & Signal Assignment

No	Signal	Type	Description
A3	DAT0	I/O	Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		

B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers. Command operates in two modes, open-drain for initialization and push-pull for fast command transfer.
M6	CLK	I	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RSTN		Hardware reset signal pin
H5	Data Strobe	O	Data Strobe
E6	V_{CC}	P	Flash I/O and memory power supply
F5	V_{CC}		
J10	V_{CC}		
K9	V_{CC}		
C6	V_{CCQ}	P	Memory controller core and MMC I/F I/O power supply
M4	V_{CCQ}		
N4	V_{CCQ}		
P3	V_{CCQ}		
P5	V_{CCQ}		
E7	V_{SS}	P	Flash I/O and memory ground connection
G5	V_{SS}		
H10	V_{SS}		
K8	V_{SS}		
A6	V_{SS}		
J5	V_{SS}		
C4	V_{SSQ}	P	Memory controller core and MMC I/F ground connection
N2	V_{SSQ}		
N5	V_{SSQ}		
P4	V_{SSQ}		
P6	V_{SSQ}		
C2	V_{DDi}		Internal power node. Connect 0.1uF capacitor from VDDi to ground

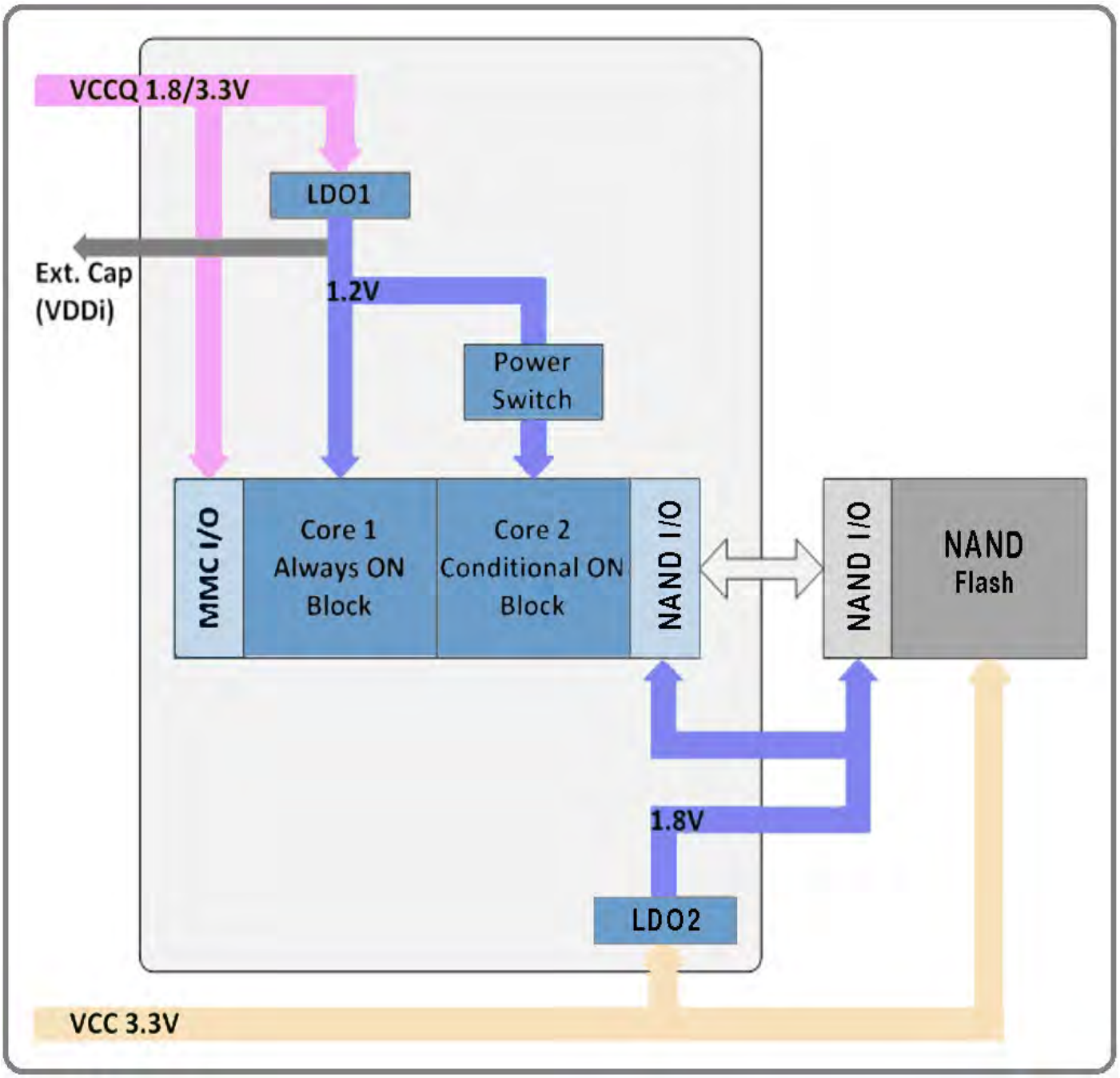
NOTE

I/O = Bi-direction, I = Input, O = Output, P = Power/Analog, RFU = Reserved for Future Use

2.3 Product Architecture

eMMC consists of NAND Flash and Controller. V_{CCQ} is for Controller power and V_{CC} is for Flash power

Figure 3. **ASFC8G31M-51BIN Block Diagram**



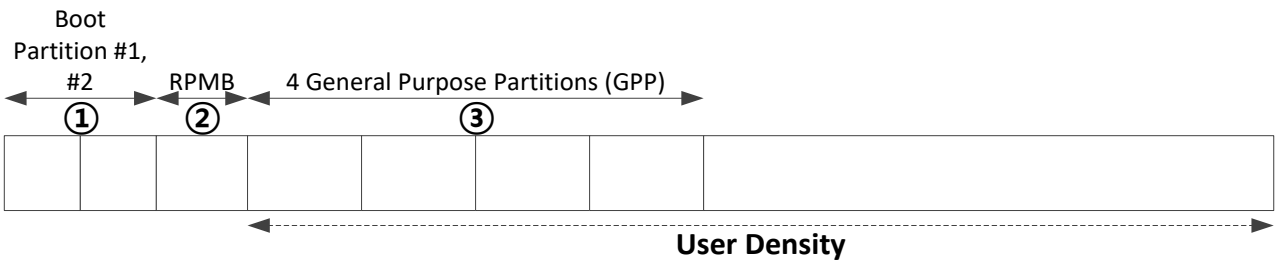
3 Technical Notes

3.1 HS400 Interface

Support HS400 DDR interface timing mode to achieve a bus speed of 400 MB/s at 200MHz clock frequency with 8bit bus width only and the 1.7 ~ 1.95V V_{CCQ} option. At this mode, the host may need to have an adjustable sampling point to reliably receive the incoming data, due to the speed. Please refer to JESD84-B51 standard for additional information.

3.2 Partition Management

The device initially consists of two Boot partitions, RPMB(Replay Protected Memory Block) partition and User Data Area. Both Boot and RPMB area have fixed size of area and can't be adjusted.



3.2.1 Boot Area Partition and RPMB Area Partition

The device has fixed size of Boot and RPMB area.

Boot partition size is calculated as (128KB * BOOT_SIZE_MULT)

The size of Boot Area Partition 1 and 2 cannot be set independently. It is set as same value.

RPMB partition size is calculated as (128KB * RPMB_SIZE_MULT).

In RPMB partition, CMD 0, 6, 8, 12, 13, 15, 18, 23, 25 are admitted.

Access Size of RPMB partition is defined as the below:

Table 3. Setting sequence of Boot Area Partition size and RPMB Area Partition size

REL_WR_SEC_C	Description
REL_WR_SEC_C = 1	Access sizes 256B and 512B supported to RPMB partition
REL_WR_SEC_C > 1	Access sizes up to REL_WR_SEC_C * 512B supported to RPMB partition with 256B granularity

Any undefined set of parameters or sequence of commands results in failure access.

If the failure is in data programming case, the data is not programmed.

If the failure occurs in data read case, the read data is '0x00'.

Table 4. Capacity according to partition

Device	Boot partition 1 [KB]	Boot partition 2 [KB]	RPMB [KB]
8GB	4,096	4,096	4,096

3.2.2 User Density

This table defines the user density size

Table 5. User Density Size

Device	LBA [Hex]	LBA [Dec.]	User Partition Size
8GB	0xE18000	14,778,368	7,216MB

3.3 Boot operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

Figure 4. embedded MultiMediaCard state diagram (boot mode)

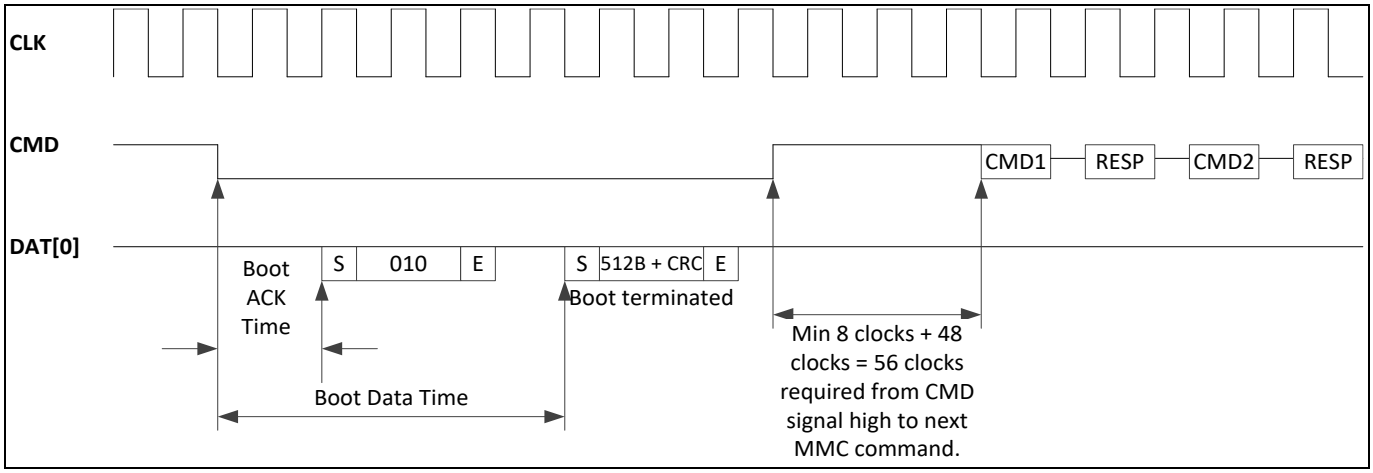


Figure 5. embedded MultiMediaCard state diagram (alternative boot mode)

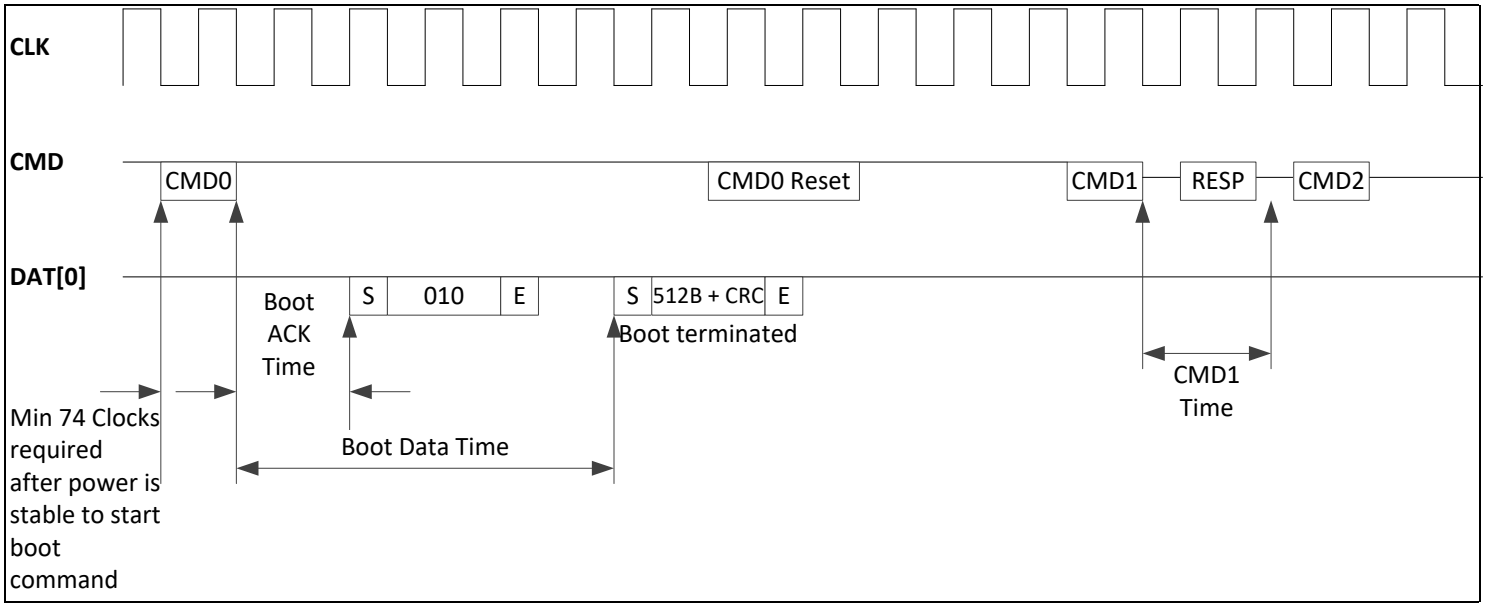


Table 6. Boot ack, boot data and initialization Time

Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 1 sec
(3) Initialization Time	< 1 sec

NOTE

1) The value for this initialization time is for such case which includes partition setting also. For details, please refer to INI_TIMEOUT_AP in Extended CSD Register of JESD84-B51.

Normal initialization time (without partition setting) is completed within 1sec

3.4 Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) is for customer's FW updating in field for those cases of debugging, enhancing and adding new features of FW itself. The host can download a new version of the firmware into the eMMC device by this mechanism and whole FFU process can happen without affecting any user/OS data, even in parallel with Host's performing other operations.

Refer to JEDEC Standards No. JESD84-B51 for additional information.

3.5 Cache

This device supports 128KB of volatile memory as an eMMC cache for performance improvement of both sequential and random access. For additional information please refer to JESD84-B51 standard.

3.6 Packed Commands

This device supports packed commands feature of eMMC standard version 5.1 and allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus, which leads reducing overall bus overheads and thus, enables optimal system performance.

Please refer to JESD84-B51 for information details.

3.7 Secure Delete

3.7.1 Sanitize

The device supports Sanitize operation for removing data from the unmapped user address space in the device, physically. Device keeps the sanitize operation until one of the following events occurs, with keeping busy asserted,

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

No data should exist in the unmapped host address space after the sanitize operation is completed.

3.7.2 Secure Erase

This device supports the optional Secure Erase command, which is for backward compatibility reasons, as well as standard erase command. Host will erase provided range of LBAs and ensure no older copies of this data exist in the flash with this command.

Please refer to JEDEC Standards No. JESD84-B51 for more information.

3.7.3 Secure Trim

This device supports Secure Trim command which is similar to the Secure Erase command but different in that performs a secure purge operation on write blocks instead of erase groups. This is for backward compatibility reasons.

The secure trim command is performed in two steps:

1) Mark the LBA range as candidate for erase.
2) Do Erase the marked address range and then, ensure no old copies are left within that range. .

For additional information refer to JEDEC Standards No. JESD84-B51.

3.8 High Priority Interrupt (HPI)

This device supports High Priority Interrupt and prevent problem of Host being stalled due to too much delayed Write operation by new paging request of operating system, by user. It will delay the request for new paging until currently going write operation is completed.

Please refer to JEDEC Standards No. JESD84-B51 for more information.

3.9 Device Health

This device supports Device Health Report feature which is featured by each bytes of DEVICE_LIFE_TIME_EST_TYP_B[269].

It can be queried by standard MMC command for getting Extended CSD structure. Please refer to below and JEDEC Standards No. JESD84-B51 for details.

DEVICE_LIFE_TIME_EST_TYP_B[269], The host may use it to query health information of other partition area.

3.10 Auto Power Saving Mode

This device supports Auto Power Saving Mode which can save power consumption. Device will enter this mode if host does not issue any command during 20ms, after completion of previously issued command.

Any newly issued commands during this mode will be carried normally.

Table 7. Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no command is issued during a certain time.	If Host issues any command

Table 8. Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
NAND Power	ON	ON/OFF
GotoSleep Time	< 100ms	< 52.43ms

3.11 Performance

Table 9. Sustained Sequential Performance

Capacity (GB)	Sequential Read (MB/s)	Sequential Write (MB/s)
8	140	80

NOTE

Test Condition: Bus width x8, HS400, 512KB data transfer, Packed Off, Cache On,

w/o file system overhead, measured on Alliance's internal board at Clean Case(WAI=1)

4 Register Value

Following sections are for describing all register value of eMMC device at its default in the AS08FC. And these values here may be updated in later version without notice.

There are defined total six registers in this section: OCR, CID, CSD, EXT_CSD, RCA and DSR. All of them has its own commands corresponded and for details, please refer JEDEC Standards No. JESD84-B51 for details. The OCR, CID and CSD registers has information of device and content, while the RCA and DSR registers are for configuring parameters of device. For the EXT_CSD register, it contains both device specific information and actual configuration parameters.

4.1 OCR Register

The operation conditions register (OCR) contains: VCC voltage profile of the device, access mode indication, status information bit. The status bit is set when the device finished its power up procedure.
All eMMC devices shall have this register implemented.

Table 10. OCR Register

OCR bit	V_{CCQ} Voltage Window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 ~ 1.95	1b
[14:8]	2.0 ~ 2.6	000 0000b
[23:15]	2.7 ~ 3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) -[2GB] 10b (sector mode) -[*Higher than 2GB only]
[31]	e-MMC power up status bit (busy)[1]	

NOTE

1) This bit is set to LOW if the e-MMC has not finished the power up routine.
2) The voltage for internal flash memory(V_{CC}) should be 2.7 ~ 3.6V regardless of OCR register value.

4.2 CID Register

The device Identification (CID) register is 128bits wide. It contains the device identification information used during the device identification phase (e-MMC protocol). e-MMC device shall have a unique identification number.

Users can define their own CID register and the CID contents will be programmed into the eMMC device when firmware fusing process. After the programming is complete, end users cannot change CID, unless the whole foundry production program is re-done. Users can install the new downloaded firmware into the device by using FFU (Field Firmware Update) mode.

Table 11. CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x52
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	0x52
Product name	PNM	48	[103:56]	8GB :" AS08FC" 0x415330384643
Product revision	PRV	8	[55:48]	0x0A
Product serial number	PSN	32	[47:16]	---[3]
Manufacturing date	MDT	8	[15:8]	---[4]
CRC7 checksum	CRC	7	[7:1]	---[5]
not used, always '1'	-	1	[0:0]	---

NOTE

1),4),5) description are same as e.MMC JEDEC standard

2) PRV is composed of the revision count of controller and the revision count of F/W patch

3) A 32 bits unsigned binary integer. (Random and Manufacture Number)

4.2.1 Product name table (In CID Register)

Table 12. Product name table

Part Number	Density (GB)	Product Name in CID Register (PNM)	PKG Type
ASFC8G31M-51BIN	8	AS08FC	11.5x13.0x1.0

4.3 RCA Register

The writable 16-bit relative device address (RCA) register carries the device address assigned by the host during the device identification. This address is used for the addressed host-device communication after the device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all devices into the Stand-by State with CMD7.

4.4 CSD Register

The device Specific Data (CSD) register provides information on how to access the device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E) can be changed by CMD27.

The CSD register defines the behavior or of eMMC devices. The eMMC behavior is related to the controller design. The following table shows a typical CSD definition of ASFC8G31M-51BIN based eMMC. If users need to add on more features, firmware or hardware modifications may be necessary.

※Note that the register values are preliminary data and may be updated in a later version. And the updated value will be supported by specified application note later.

Table 13. ASFC8G31M-51BIN Typical CSD Register

Name	Field	Bit	Type	Slice	Value	Note
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h	
System specification version	SPEC_VERS	4	R	[125:122]	4h	
Reserved	-	2	R	[121:120]	-	
Data read access-time 1	TAAC	8	R	[119:112]	27h	
Data read access-time 2 in CLK cycles (NSAC x 100)	NSAC	8	R	[111:104]	01h	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h	
Device command classes	CCC	12	R	[95:84]	0F5h	
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h	
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h	
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h	
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h	
DSR implemented	DSR_IMP	1	R	[76:76]	0h	
Reserved	-	2	R	[75:74]	-	
Device size	C_SIZE	12	R	[73:62]	FFFh	
Max read current@VCCQ min	VCCQ_R_CURR_MIN	3	R	[61:59]	7h	
Max read current@VCCQ max	VCCQ_R_CURR_MAX	3	R	[58:56]	7h	
Max write current@VCCQ min	VCCQ_W_CURR_MIN	3	R	[55:53]	7h	
Max write current@VCCQ max	VCCQ_W_CURR_MAX	3	R	[52:50]	7h	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h	
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh	
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh	
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh	

Name	Field	Bit	Type	Slice	Value	Note
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h	
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h	
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h	
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h	
Reserved	-	4	R	[20:17]	-	
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h	
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h	
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h	
File format	FILE_FORMAT	2	R/W	[11:10]	0h	
ECC code	ECC	2	R/W/E	[9:8]	0h	
CRC	CRC	7	R/W/E	[7:1]	-	
Not used, always '1'	-	1	-	[0:0]	-	

NOTE

: The type of the CSD Registry entries in the Table 13 is coded as follows.

R: Read only

W: One time programmable and not readable

R/W: One time programmable and readable

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

4.5 Extended CSD Register (EXT_CSD)

The Extended CSD register defines the additional behavior of eMMC devices due to limited CSD information. The following table shows a typical extended CSD definition of ASFC8G31M-51BIN based eMMC. If users need to add on more features, firmware or hardware modifications may be necessary.

–Note that the register values are preliminary data and may be updated in a later version. And the updated value will be supported by specified application note later.

Table 14. ASFC8G31M-51BIN Typical EXT_CSD Register

Name	Field	Byte	Type	Slice	Value	Note
Reserved	-	6	-	[511:506]	-	
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0h	
Supported command sets	S_CMD_SET	1	R	[504]	1h	Allocated by MMCA
HPI features	HPI_FEATURES	1	R	[503]	1h	HPI type CMD13
Background operations support	BKOPS_SUPPORT	1	R	[502]	1h	BKOPS supported
Max packed read commands	MAX_PACKED_READS	1	R	[501]	3Fh	Max. 63 commands in a packed cmd
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	3Fh	Max. 63 commands in a packed cmd
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	1h	Support Data Tag
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0h	
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0h	
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	78h	Max Tag Size = 8*2 = 16MB Max_Context ID = 8
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	1h	1MB*2=2MB
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	3h	Support "System code" and "Non-persistent"
Supported modes	SUPPORTED_MODES	1	R	[493]	1h	FFU is supported
FFU features	FFU_FEATURES	1	R	[492]	0h	
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	17h	(2^23)*100us = 838.86s
FFU Argument	FFU_ARG	4	R	[490:487]	FFFAFFF0h	

Barrier support	BARRIER_SUPPORT	1	R	[486]	1h	Support barrier
Reserved	-	177	-	[485:309]	-	
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	1h	Support CMDQ
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	1Fh	32 CMDQ_DEPTH
Reserved	-	1	-	[306]		
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0000h	
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	TBD	
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	1h	
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	1h	not supported
Pre EOL information	PRE_EOL_INFO	1	R	[267]	1h	
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	40h	
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	40h	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	7h	
Device version	DEVICE_VERSION	2	R	[263:262]	3805h	
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	TBD	
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0h	
Cache size	CACHE_SIZE	4	R	[252:249]	0400h	128KB (depending on 16KB*CE)
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	5h	5x10ms = 50ms
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	64h	100x10ms = 1000ms
Background operations status	BKOPS_STATUS	1	R	[246]	0h	No operations required
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0h	Run Time update
First initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0Ah	Initial time out 1s
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	1h	Support cache flushing policy
Power class for 52MHz, DDR at V_{CC} = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0h	RMS 100mA, Peak 200mA

Power class for 52MHz, DDR at V_{CC} = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0h	RMS 65mA, Peak 130mA
Power class for 200MHz at V_{CCQ} =1.95V, V_{CC} = 3.6V	PWR_CL_200_195	1	R	[237]	0h	
Power class for 200MHz, at V_{CCQ}=1.3V, V_{CC}=3.6V	PWR_CL_200_130	1	R	[236]	0h	
Minimum write performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0h	For devices not reaching the 4.8MB/s value
Minimum read performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0h	For devices not reaching the 4.8MB/s value
Reserved	-	1	-	[233]	-	
TRIM multiplier	TRIM_MULT	1	R	[232]	02h	Trim time out 300ms
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	55h	1. Support the secure and insecure trim operations. 2. Support the automatic secure purge operation on retired defective portions of the array. 3. Secure purge operations are supported.
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	FFh	
Secure Trim Multiplier	SEC_TRIM_MULT	1	R	[229]	FFh	
Boot information	BOOT_INFO	1	R	[228]	7h	
Reserved	-	1	-	[227]	-	
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	20h	32 x 128KB = 4MB

Access size	ACC_SIZE	1	R	[225]	6h	super page size = 64 x 512B = 32KB
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	1h	high capacity erase group size 1 x 512KB
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	2h	
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	1h	
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	10h	
Sleep current (VCC)	S_C_VCC	1	R	[220]	7h	VCC < 128uA for sleep
Sleep current (VCCQ)	S_C_VCCQ	1	R	[219]	7h	VCCQ < 128uA for sleep
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	17h	(2^23)*100us = 838.86s
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	13h	(2^19)*100ns =52.43ms
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0Ch	(2^12)*10us = 40.960ms
Sector count	SEC_COUNT	4	R	[215:212]	→	8GB :00E18000h
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	1h	Support Secure write protect
Minimum write performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0h	
Minimum read performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0h	
Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0h	
Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0h	
Minimum write performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0h	

Minimum read performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0h	
Reserved	-	1	-	[204]	-	
Power class for 26 MHz at 3.6 V 1 R	PWR_CL_26_360	1	R	[203]	0h	
Power class for 52 MHz at 3.6 V 1 R	PWR_CL_52_360	1	R	[202]	0h	
Power class for 26 MHz at 1.95 V 1 R	PWR_CL_26_195	1	R	[201]	0h	
Power class for 52 MHz at 1.95 V 1 R	PWR_CL_52_195	1	R	[200]	0h	
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	6h	6x10ms = 60ms
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	5h	5x10ms = 50ms
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	1Fh	Support Type0/Type1/Type2 /Type3/Type4
Device type	DEVICE_TYPE	1	R	[196]	57h	
Reserved	-	1	-	[195]	-	
CSD STRUCTURE	CSD_STRUCTURE	1	R	[194]	2h	
Reserved	-	1	-	[193]	-	
Extended CSD revision	EXT_CSD_REV	1	R	[192]	8h	Support JEDEC eMMC v5.1
Command set	CMD_SET	1	R/W/E_P	[191]	0h	
Reserved	-	1	-	[190]	-	
Command set revision	CMD_SET_REV	1	R	[189]	0h	
Reserved	-	1	-	[188]	-	
Power class	POWER_CLASS	1	R/W/E_P	[187]	0h	
Reserved	-	1	-	[186]	-	
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0h	
Strobe Support	STROBE_SUPPORT	1	R	[184]	0h	
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0h	
Reserved	-	1	-	[182]	-	
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0h	
Reserved	-	1	-	[180]	-	

Partition configuration	PARTITION_CONFIG	1	R/W/E R/W/E_P	[179]	0h	
Boot configuration protection	BOOT_CONFIG_PROT	1	R/W R/W/C_P	[178]	0h	
Boot bus conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0h	
Reserved	-	1	-	[176]	-	
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0h	
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0h	
Boot area write protection register	BOOT_WP	1	R/W R/W/C_P	[173]	0h	
Reserved	-	1	-	[172]	-	
User area write protection register	USER_WP	1	R/W R/W/C_P R/W/E_P	[171]	0h	
Reserved	-	1	-	[170]	-	
FW configuration	FW_CONFIG	1	R/W	[169]	0h	
RPMB size	RPMB_SIZE_MULT	1	R	[168]	20h	
Write reliability setting register	WR_REL_SET	1	R/W	[167]	1Fh	Use 1Fh for SPOR; Use 00h for performance
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	15h	
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0h	
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0h	
Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	[163]	0h	
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0h	
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0h	
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	7h	
Max enhanced area size	MAX_ENH_SIZE_MULT	3	R	[159:157]	1C3h	Not support

Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0h	
Partitioning setting	PARTITION_SETTING_ COMPLETED	1	R/W	[155]	0h	
General purpose partition size	GP_SIZE_MULT	12	R/W	[154:143]	0h	
Reserved		3	R/W	[142:140]	0h	
Reserved		4	R/W	[139:136]	0h	
Reserved		1	-	[135]	-	
Secure bad block management	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0h	
Production state awareness	PRODUCTION_STATE_AWA RENESS	1	R/W/E	[133]	0h	
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0h	
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0h	
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_ SUPPORT	1	R	[130]	0h	
Reserved	-	2	TBD	[129:128]	-	
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	3700C8h	
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	1h	4KB
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0h	
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0h	Default 512B
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0Ah	100ms*10=1000 ms
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0h	
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0h	
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	00h	1. URGENT_BKOPS status bit is support 2. DYNCAP_NEEDED status bit is support 3. SYSPOOL_EXHAUSTED status bit is support 4. PACKED_FAILURE status bit is support

Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	00h	Device Run Time update
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	00h	
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	00h	
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0h	Device Run Time update
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0h	Device Run Time update
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0h	
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0h	
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0h	
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0h	
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0h	
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0h	
Reserved	-	1	TBD	[28:27]	-	
FFU status	FFU_STATUS	1	R	[26]	0h	
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0h	
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	E18000h	
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	01h	Manual mode only
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	3Bh	
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0h	Enable by CMDQ process
Reserved	-	15	-	[14:0]	-	

NOTE

1. The definitions of cell types are shown as follows: R: Read only.

W: One time programmable and not readable. R/W: One time programmable and readable.

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and H/W rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

2. Reserved bits should be read as “0”.

5 AC Parameter

5.1 Timing Parameter

Table 15. Timing Parameter

Timing Paramter		Max. Value
Initialization Time (tINIT)	Normal [1)]	1 sec
	After partition setting [2)]	1sec
Read Timeout		150ms
Write Timeout		600ms
Erase Timeout		600ms
Force Erase Timeout		3 min
Secure Erase Timeout		153 sec
Secure Trim step Timeout		1536 sec
Trim Timeout		600 ms
Partition Switching Timeout (after Init)		60ms
Power Off Notification (Short) Timeout		50ms
Power Off Notification (Long) Timeout		1000ms

NOTE

1) Normal Initialization Time without partition setting

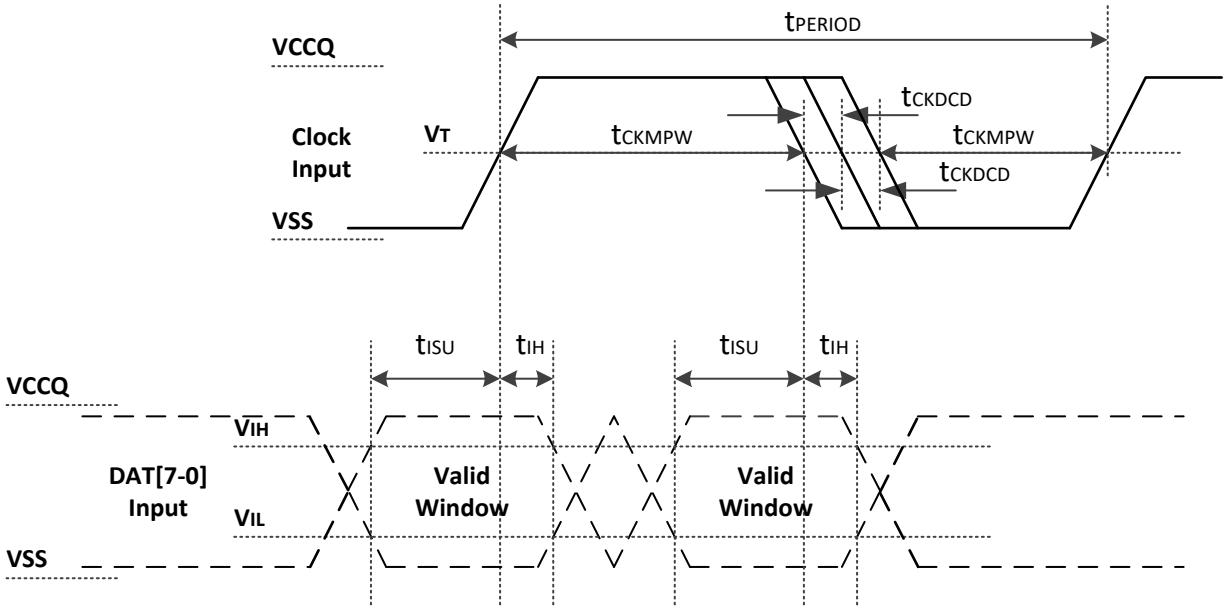
2) For the Initialization Time after partition setting, refer to INI_TIMEOUT_AP in 6.4 EXT_CSD register

3) All those Timeout Values specified in the above Table are only for testing purposes under specific test case only and it can vary in real cases. Also, it may be affected may vary due to user environment.

5.2 Bus Timing Specification in HS400 mode

5.2.1 HS400 Device Input Timing

Figure 6. **HS400 Device Input Timing Diagram**



NOTE

1) t_{ISU} and t_{IH} are measured at V_{IL} (max) and V_{IH} (min).

2) V_{IH} denotes V_{IH} (min) and V_{IL} denotes V_{IL} (max)

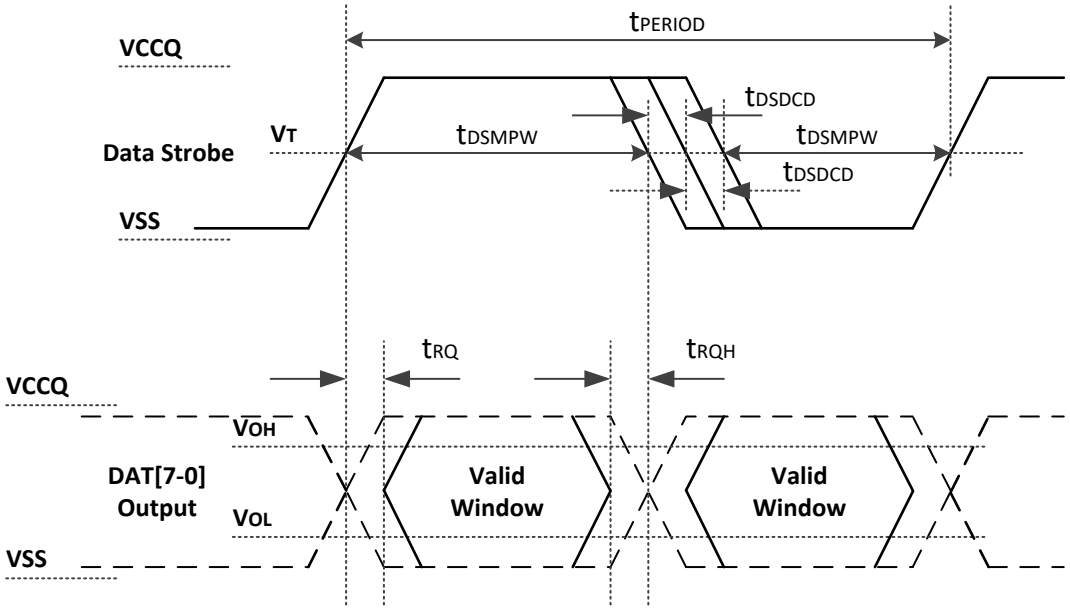
Table 16. HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5	-	ns	200MHz(Max), between rising edges with respect to V_T.
Slew rate	SR	1.125	-	V/ns	
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	
Minimum pulse width	t_{CKMPW}	2.2	-	ns	
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4	-	ns	
Input hold time	t_{IHddr}	0.4	-	ns	
Slew rate	SR	1.125	-	V/ns	

5.2.2 HS400 Device Output Timing

Data Strobe is used to read data (data read and CRC status response read) in HS400 mode. The device output value of Data Strobe is “High-Z” when the device is not in outputting data(data read, CRC status response). Data Strobe is toggled only during data read period.

Figure 7. **HS400 Device Output Timing Diagram**



NOTE

1) V_{OH} denotes V_{OH} (min) and V_{OL} denotes V_{OL} (max).

Table 17. HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5	-	ns	200MHz(max), between rising edges with respect to V_T.
Slew rate	SR	1.125	-	V/ns	
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	
Minimum pulse width	t_{DSMPW}	2.0	-	ns	
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}	
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}	
Output DAT (referenced to Data Strobe)					
Output skew	t_{RQ}	-	0.4	ns	
Output hold skew	t_{RQH}	-	0.4	ns	
Slew rate	SR	1.125	-	V/ns	

5.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

***Figure 8*. Bus Signal Levels**

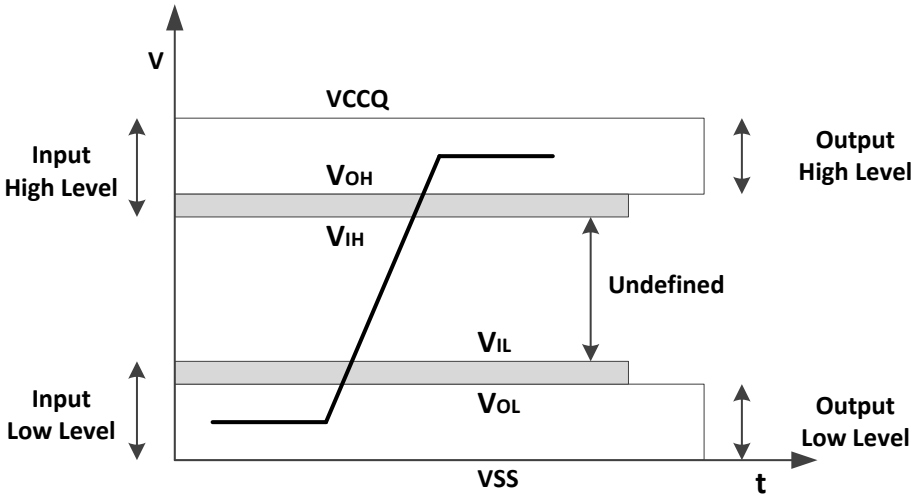


Table 18. Bus Signal Levels

Parameter	Symbol	Min	Max	Unit	Remark
Open-drain mode					
Output HIGH voltage	V_{OH}	V_{CCQ} – 0.2	-	V	-
Output LOW voltage	V_{OL}	-	0.3	V	I_{OL} = 2mA
Push-pull mode (High-voltage eMMC)					
Output HIGH voltage	V_{OH}	0.75 x V_{CCQ}	-	V	I_{OH} = –100uA @ V_{CCQ} min
Output LOW voltage	V_{OL}	-	0.125 x V_{CCQ}	V	I_{OL} = 100uA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 x V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.25 x V_{CCQ}	V	
Push-pull mode (1.70 ~ 1.95 V)					
Output HIGH voltage	V_{OH}	V_{CCQ} – 0.45	-	V	I_{OH} = –2mA
Output LOW voltage	V_{OL}	-	0.45	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 x V_{CCQ} [1)]	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.35 x V_{CCQ} [2)]	V	

NOTE

1) Because V_{OH} depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet V_{OH} Min value.

2) 0.7 x V_{CCQ} for MMC4.3 and older revisions.

3) 0.3 x V_{CCQ} for MMC4.3 and older revisions.

6 DC Parameter

6.1 Power Consumption

Table 19. Active Power Consumption during operation

Density (GB)	NAND Type (MLC)	CTRL (Max RMS,mA)	NAND (Max RMS,mA)
8	64Gb x 1	120	120

NOTE

* Power Measurement conditions: Bus configuration =x8 @200MHz DDR

* Typical value is measured at Vcc=3.3V, Vccq=1.8V, TA=25°C. Not 100% tested.

* The measurement for max RMS current is the average RMS current consumption over a period of 100ms

Table 20. Standby Power Consumption in auto power saving mode and standby state

Density (GB)	NAND Type (MLC)	CTRL (Ave. RMS, uA)		NAND (Ave. RMS, uA)	
		25°C (Typ)	85°C	25°C (Typ)	85°C
8	64Gb x 1	130	600	40	50

NOTE

* Power Measurement conditions: Bus configuration =x8, No CLK

* Typical value is measured at Vcc=3.3V,Vccq=1.8V TA=25°C. Not 100% tested.

Table 21. Sleep Power Consumption in Sleep State

Density (GB)	NAND Type (MLC)	CTRL (uA)		NAND (uA)
		25°C (Typ)	85°C	
8	64Gb x 1	130	600	TBD *1

NOTE

* Power Measurement conditions: Bus configuration =x8, No CLK

* Typical value is measured at Vcc=3.3V, VccQ=1.8V, TA=25°C. Not 100% tested.

*1) In auto power saving mode, NAND power can not be turned off, However in sleep mode NAND power can be turned off. If NAND power is alive, NAND power is same with that of the Standby state.

6.2 Supply Voltage

Table 22. Supply Voltage

Symbol	Min (V)	Max (V)
V_{CCQ} (Low)	1.7	1.95
V_{CCQ} (High)	2.7	3.6
V_{CC}	2.7	3.6
V_{SS}	- 0.5	0.5

6.3 Bus Signal Line Load

The total capacitance CL of each line of the e-MMC bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CDEVICE of the e-MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Table 23. Bus Signal Line Load

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			6	pF	
Maximum signal line inductance				16	nH	f_{PP} <= 52 MHz

Table 24. Capacitance and Resistance for HS400 mode

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	C_L			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	KOhm	

7 Power Domains

Alliance 8GB eMMC has three power domains assigned to V_{CCQ}, V_{CC} and V_{DDi}, as shown below.

Table 25. Power Domains

Symbol	Power Domain	Comments
V_{CCQ}	Host Interface	Interface Power 1.70V ~ 1.95V or 2.7V ~ 3.6V
V_{CC}	Memory	NAND Flash Power 2.7V ~ 3.6V
V_{DDi}	Internal	V_{DDi} is the internal regulator connection to an external decoupling capacitor.

Appendix : VCCQ Power – off Sequence

This section describes the power on/off sequence requirements of system power design. The system power design should consider the following descriptions to ensure the eMMC controller and internal POR(power-on reset)circuits are operated correctly.

1. POR Circuit

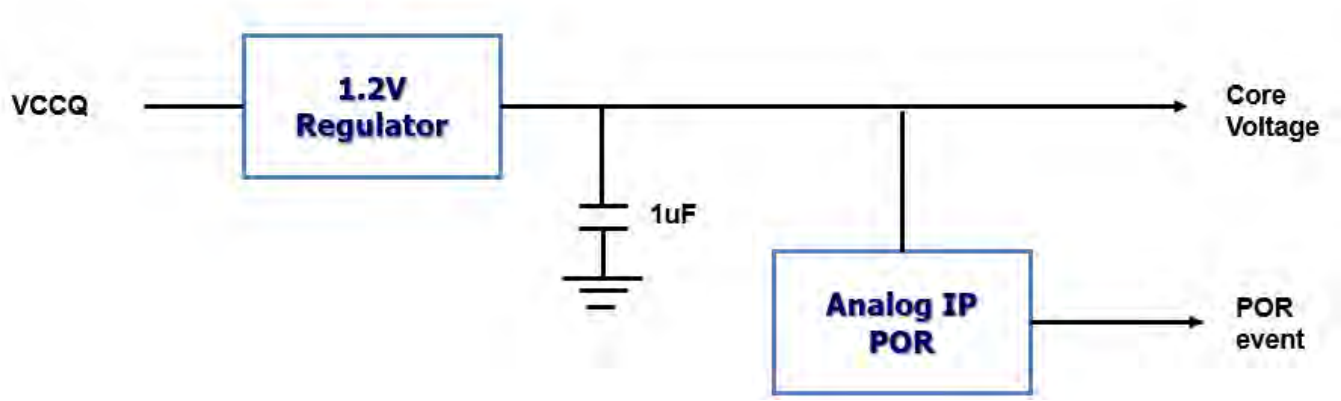


Figure Appendix 1. SM2736 POR Circuit Block Diagram

2. POR Component Specifications

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Input power voltage	0	1.2	1.32	V
VRR	The rise threshold voltage		0.94		V
VFR1	The fall threshold voltage		0.84		V
VRR-delay	Delay time for VRR	1.66	2.08	2.69	us
VFR1-delay	Delay time for VFR1	2.68	3.12	3.58	us
VFR2-delay	Delay time for VFR2	2.7	3.1	3.54	us
Current	Power Consumption	4.15	4.88	6.02	uA

Note: VRR/VFR process variation s about +/-15% regarding temperature and SS/FF

3. Requirements of Power–off and Recovery

To prevent improper VCCQ power off sequence which results in the POR components abnormally reset the SM2736 logic, a monotonic VCCQ power off curve is required.

During a power-on sequence, a power-off sequence, or during an error recovery sequence, the voltage range varied between 0.95V to 0.4V may trigger ambiguous operation of POR cell. To avoid this situation, power rail transitions should be monotonic within the range(0.4V~0.95V)during the voltage rising/falling.

The system power rail(VCCQ) must stay below 0.4V for at least 50us before fully power-up. This is to ensure the power reset is triggered solidly.

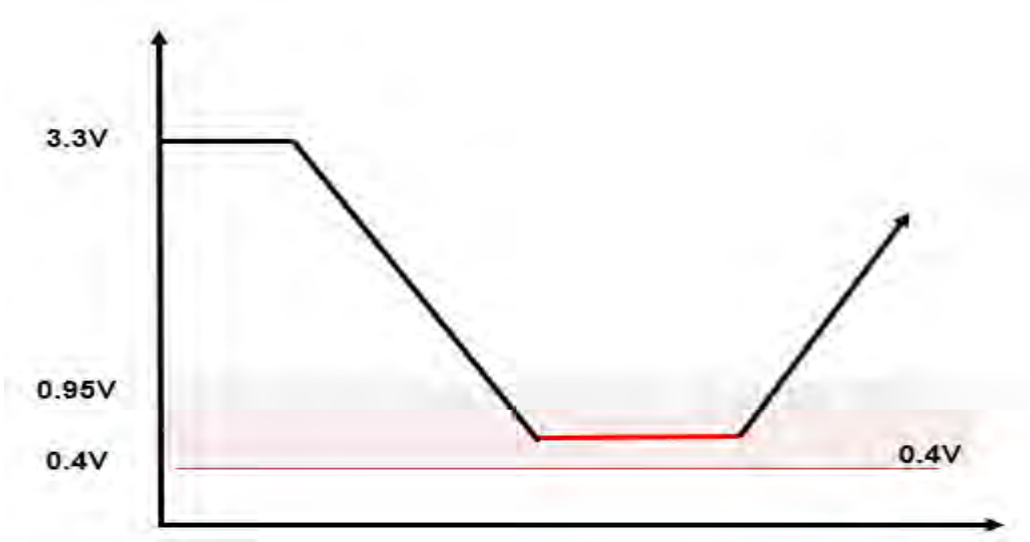


Figure Appendix 2. BAD VCCQ power-off and Recovery Curve

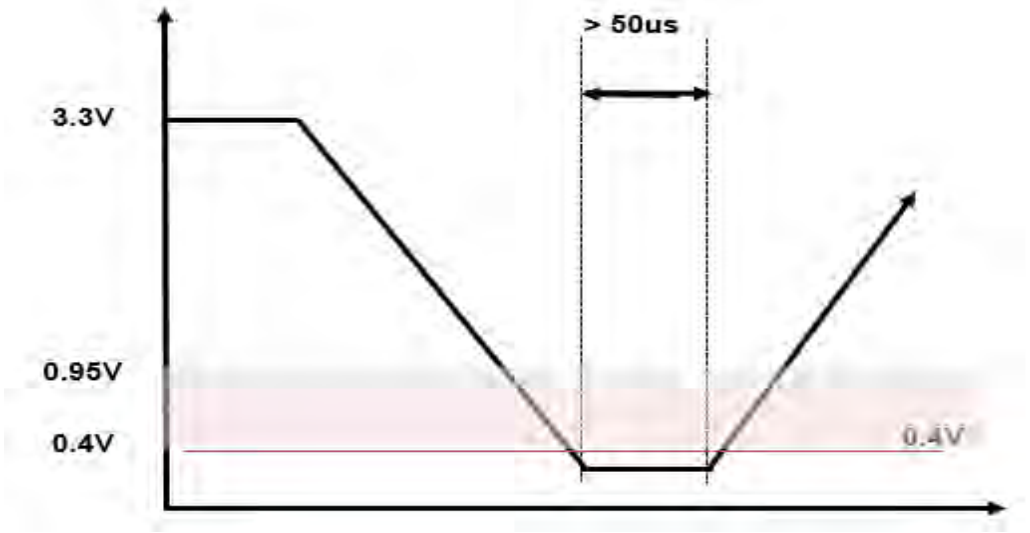


Figure Appendix 3. Recommended VCCQ power-off and Recovery Curve

8 Part number system

Table 26. Part number system

AS	FC	8G	3	1	M	X	-51	B	I	N	XX
Alliance Memory	eMMC Series (Flash + Controller)	Density 4G=4GB 8G=8GB 16G= 16GB	Flash Voltage 3=3.3V 1=1.8V	NAND Die 1=Single 2=Dual Die	NAND Type S = SLC M = MLC	Generation Code Blank = rev0 A = revA B = revB	eMMC Version 51 = 5.1	Package Type B = 153b FBGA (11.5x13mm)	Operating Temperature I = Industrial (-40°C~85°C)	ROHS Compliant	Packing Type None:Tray TR:Reel

Alliance Memory, Inc.
12815 NE 124th St STE#D
Kirkland, WA 98034, USA
Tel: +1(425)898-4456
Fax +1(425)896-8628

www.alliancememory.com