

PCN# 20180209000

Obsolete 8MB NOR Flash on:

MityDSP-L138(F), MitySOM-1808(F), and MitySOM-1810(F) Modules

Date: February 09, 2018

To: Purchasing Agents & Design Engineers

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact the Hardware Manager Bill Halpin (bill.halpin@critiallink.com).

Sincerely,

Critical Link, LLC

Phone: (315) 425-4045

Fax: (315) 425-4048



**PCN Number:** 20180402000

**PCN Date:** February 09, 2018

**Title:** Obsolete 8MB NOR Flash

**Contact:** Bill Halpin

**Phone:** (315) 425-4045

**EOL Date:** 10/01/2019

## **Overview**

Changes to MityDSP-L138(F) MitySOM-1808(F), and MitySOM-1810(F) System on Modules are identified in the following sections

## **1 Replace Obsolete 8MB NOR Flash with 16MB NOR flash**

### **1.1 Description of Change**

Production for MityDSP and MitySOM variants using 8MB NOR will be discontinued as of October 1, 2019.

### **1.2 Reason for Change**

On 12/5/16 Micron announced it was discontinuing production of 8MB NOR, moving to 45nm high density NOR Flash products (PCN 32162).

Critical Link will migrate the MityDSP, MitySOM family to the 16MB NOR. The current 8MB variants will have a planned last time buy date of October 1, 2019\*. See Table 2.

\*- Orders placed prior to this date are subject to inventory status. Early orders are recommended.

### **1.3 Anticipated Impact on Form, Fit, Function (positive / negative)**

Functionally, the memory will be expanded from 64Mbits to 128 Mbits. The new 128 Mbit part is organized with the same-sized sectors (64 Kbytes), but increases the number of available sectors from 128 to 256. The new 128 Mbit part command set is backward compatible with the current 64 Mbit part. Additional commands, such as subsector erase, are supported with the 128 Mbit part. The JEDEC Read Identification Data sequence, which is used to identify the part over the SPI bus, has changed.

There is no impact on the hardware design, the electrical SPI bus interface has not changed.

The software impact is primarily associated with any software set that reads the JEDEC identification data. The following sections outline the impact for the following categories of code: First Stage Bootloader (OMAP-L138 ROM Loader), Second Stage Bootloader (UBL), Third Stage Bootloader (U-Boot), Operating System (Linux), Operating System (other), Applications / NOR partitioning. A summary of the impact is listed in Table 1.

**Table 1 SW Impact Summary**

Software Category	Impact	Recommendation
First Stage / ROM Bootloader	None	No Action
Second Stage Bootloader (UBL)	None	No Action
Third Stage Bootloader(U-Boot)	Yes – New JEDEC code needed.	No action if you don't reprogram factory provided U-Boot. Otherwise, upgrade to latest U-Boot from support site.
Operating System (Linux)	Yes – New JEDEC code needed.	No action if the SPI NOR is not accessed from Linux. Otherwise, upgrade kernel to properly identify 16 MB NOR and gain access to it.
Operating System (other)	Contact Supplier	Contact OS Supplier for further detail.
Applications	None	Partition sizes are the same. Upgrade required only if access to additional space on 16MB NOR parts is necessary.

**First Stage Bootloader (OMAP-L138 ROM Loader)**

OMAP-L138 ROM Loader reads the Second Stage Bootloader (the UBL) from a fixed offset in the SPI NOR device by using commands that are compatible with both the 64 and 128 Mbit NOR FLASH. The OMAP-L138 ROM Loader does not query the JEDEC ID code. There is no impact on the OMAP-L138 ROM Loader code. It will support either device without modification.

**Second Stage Bootloader (UBL)**

The User Bootloader (UBL) reads the uBoot application from a fixed offset in the SPI NOR device by using commands that are compatible with both the 64 and 128 Mbit NOR FLASH. The UBL does not query the JEDEC ID code. There is no impact on the UBL code. It will support either device without modification.

**Third Stage Bootloader (U-Boot)**

The U-Boot application queries the JEDEC ID code in order to determine the sector format of the SPI device attached. This information is necessary to support erase/write operations. The sector information is stored in a compiled-in lookup table keyed by the JEDEC ID. The U-Boot application delivered on older modules or compiled prior to 2017-12-25 does not contain a table entry for the 128 Mbit device. Version TBS of the U-Boot code, available on the git repository for customer access, includes the necessary patches to support the 128 Mbit device. The uBoot application delivered on future modules will be updated to include the patch.

There is no impact for customers that use the factory installed U-Boot for their end applications.

Customers that install their own version of U-Boot must incorporate the following patch outlined by the commit items as listed below.

[abfcd79c2716ab088f61a503ec5a5f0bf3656ca0: Add support for Micron versions of 64 and 128 Mbit SPI NOR flash.](#)

**Operating System (Linux)**

Prior to 2017-12-25, the officially supported versions of the Linux kernel by Critical Link (versions 2.6.34 and 3.2) hardcoded the SPI NOR FLASH ID to the 64 Mbit device by defining the "type" field in the SPI flash configuration



data in the board-mityomapl138.c file. Customers using these versions of the kernel with modules having the 256 Mbit device installed will only be able to access the first 8 MB of flash area (only because the sector sizes and command sets are compatible between the 64 Mbit and 128 Mbit device), and the kernel will not correctly identify the device during the boot process. Critical Link has included a patch set to introduce the new 128 Mbit part data in the kernel lookup table, as well as instruct the kernel to use the JEDEC ID code from the part to determine which device is installed and support it appropriately. The patches are available on the Critical Link support site.

There is no impact for customers that do not use the SPI NOR flash device under Linux.

Customers that access the SPI NOR flash devices under Linux should update their kernel version to include the patches listed below in order to correctly identify the device and access the upper 8 MB of FLASH memory on the 128 Mbit device.

Master Branch:

[52861c73d2a9c2c4d1358605e8f18a8adf72c0c1: Auto-probe the SPI NOR flash type using JEDEC ID 7b261b1903eef9a8f23286e3d8dbba36982d213a: Add micron JEDEC IDs and block sizes to support newer NOR FLASH devices.](#)

mitydsp-linux-v3.2 Branch:

[e752a55281883c9ea1d688dd0db4404c1a97839a: Auto-probe the SPI NOR flash type using JEDEC ID. 27a97bd689bb76496658d0c47a98eee93ab2a672: Add micron JEDEC IDs and block sizes to support newer NOR FLASH devices.](#)

### **Operating System (other)**

Customers that use operating system software such as embedded windows or QNX should contact their OS provider for details. Customers developing with Starterware or writing bare metal applications and are using the SPI NOR flash device must assess the impact, if any, of the device change on their application software. Contact Critical Link if further assistance is required.

### **Applications / NOR Partitioning**

Because both devices use 64 Kbyte sectors, there is no need to alter the NOR partitioning on a working / fielded application. No impact is anticipated on application software.

### **1.4 Anticipated Impact on Quality or Reliability (positive / negative)**

There is no impact to Quality or Reliability.

## 2 Products Affected

Details regarding the full revision history can be located in the MityDSP-L138 Revision History section on the Critical Link support site.

[https://support.criticallink.com/redmine/projects/arm9-platforms/wiki/Module\\_Product\\_Change\\_Notifications](https://support.criticallink.com/redmine/projects/arm9-platforms/wiki/Module_Product_Change_Notifications)

The hardware update for the new firmware will be tracked by Lot Code. Starting Lot Code of updated hardware will be listed at a later date.

**Table 2 Products Affected**

Model Number	Starting PCA	Replacement Model	Replacement PCA
1808-FX-225-RC	80-000307RC-6		Contact Critical Link
1810-DX-225-RC	Contact Critical Link		Contact Critical Link
L138-FX-225-RC	80-000325RC-6	L138-FX-325-RC	80-001103RC-6
L138-DX-225-RI	Contact Critical Link		Contact Critical Link
1808-FG-225-RC	Contact Critical Link		Contact Critical Link
1808-DG-225-RI	Contact Critical Link		Contact Critical Link
1810-DG-225-RI	Contact Critical Link		Contact Critical Link
L138-DI-225-RI	80-000419RI-6	L138-DI-325-RI	80-001112RI-6
L138-DG-225-RI	80-000316RI-6	L138-DG-325-RI	80-001115RI-6
L138-DG-225-RI-1	80-000420RI-6	L138-DG-325-RI-1	80-001117RI-6
L138-DG-225-RI-CR	80-000637RI-1	L138-DG-325-RI-CR	80-001118RI-1
L138-FG-225-RC	80-000333RC-6	L138-FG-325-RC	80-001105RC-6
L138-FI-225-RC	80-000354RC-6	L138-FI-325-RC	80-001108RC-6
L138-FI-236-RC	Contact Critical Link		Contact Critical Link
L138-FI-236-RL	80-000381RL-6	L138-FI-336-RL	80-001110RL-6
L138-FG-226-RC	80-000631RC-6	L138-FG-326-RC	80-001114RC-6

See the [MityDSP-L138F Carrier Board Design Guide](#) and the [MityDSP-L138 Carrier Board Design Guide](#) for migration options across the MityDSP-L138F family.

## 3 Document Revision History

Date	Version	Change Description
09-Feb-2018	1.0	Initial Version