PRTR5V0U2AX-Q

Ultra low capacitance double rail-to-rail ESD protection diode

3 May 2022 Product data sheet

1. General description

Ultra low capacitance double rail-to-rail ElectroStatic Discharge (ESD) protection diode in a small SOT143B Surface-Mounted Device (SMD) plastic package.

The device is designed to protect two high-speed data lines or high-frequency signal lines from the damage caused by ESD and other transients.

PRTR5V0U2AX integrates two ultra low capacitance rail-to-rail diodes and one additional ESD protection diode to ensure signal line protection even if no supply voltage is available.

2. Features and benefits

- ESD protection of two high-speed data lines or high frequency signal lines
- Ultra low input/output to ground capacitance: $C_{(I/O\text{-}GND)}$ = 1.8 pF
- ESD protection up to 12 kV
- IEC 61000-4-2, level 4 (ESD)
- Very low clamping voltage due to an integrated additional ESD protection diode
- Very low reverse current
- Small SMD plastic package
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- USB 2.0 ports
- Digital Video Interface (DVI)
- High-Definition Multimedia Interface (HDMI)
- Mobile phones
- Digital cameras
- WAN/LAN systems
- PCs, notebooks, printers and other PC peripherals

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
$C_{(I/O\text{-}GND)}$	input/output to ground capacitance	f = 1 MHz; $V_{(I/O\text{-}GND)}$ = 0 V; T_{amb} = 25 °C	[1]	-	1.8	-	pF
C_{sup}	supply pin to ground capacitance	f = 1 MHz; V_{CC} = 0 V; T_{amb} = 25 °C	[2]	-	16	-	pF

[1] Measured from pin 2 and 3 to ground
[2] Measured from pin 4 to ground

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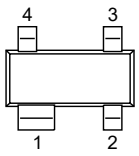
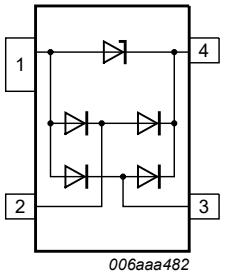
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND	ground	 SOT143B	 006aaa482
2	I/O 1	input/output 1		
3	I/O 2	input/output 2		
4	V_{CC}	supply voltage		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PRTR5V0U2AX-Q	SOT143B	plastic, surface-mounted package; 4 leads; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT143B

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PRTR5V0U2AX-Q	%AE

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	ambient temperature			-40	125	°C
T_{stg}	storage temperature			-55	125	°C
ESD standards compliance						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; level 4 (ESD)		-	12	kV

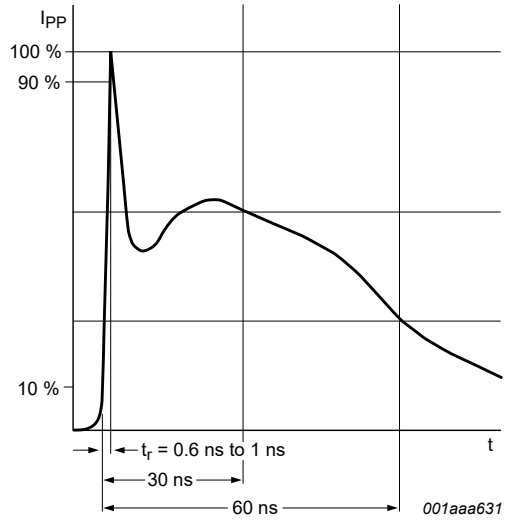


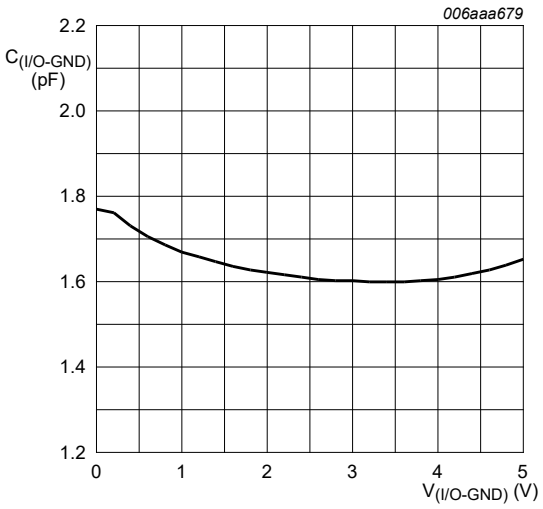
Fig. 1. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

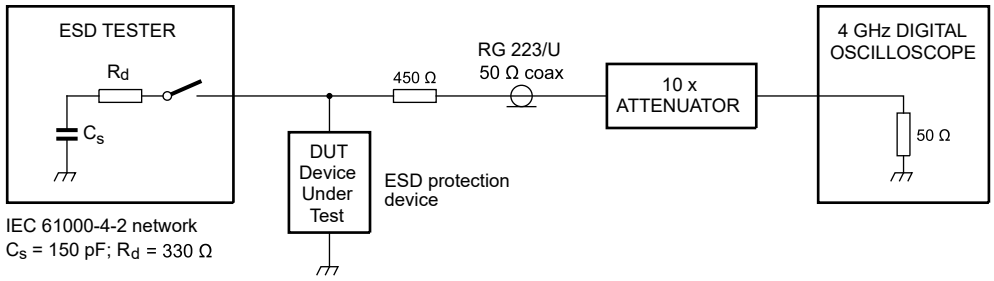
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_R	reverse current	V_R = 3 V; T_{amb} = 25 °C	[1]	-	1	100	nA
$C_{(I/O-GND)}$	input/output to ground capacitance	f = 1 MHz; $V_{(I/O-GND)}$ = 0 V; T_{amb} = 25 °C	[2]	-	1.8	-	pF
V_F	forward voltage	I_F = 1 mA; T_{amb} = 25 °C		-	0.7	-	V
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
V_{BR}	breakdown voltage		[3]	6	-	9	V
C_{sup}	supply pin to ground capacitance	f = 1 MHz; V_{CC} = 0 V; T_{amb} = 25 °C	[3]	-	16	-	pF

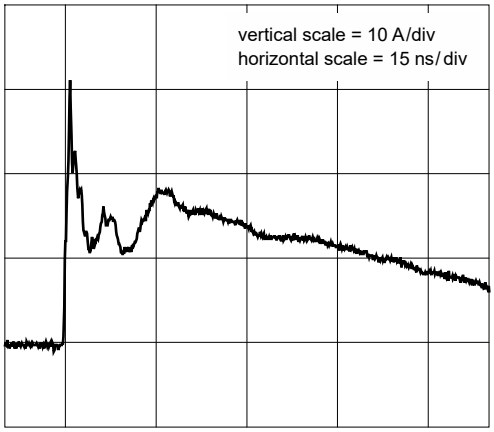
[1] Measured from pin 2, 3 and 4 to ground
[2] Measured from pin 2 and 3 to ground
[3] Measured from pin 4 to ground



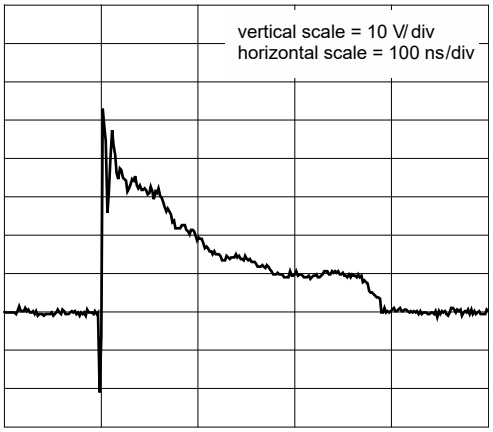
f = 1 MHz; T_{amb} = 25 °C

Fig. 2. Input/output to ground capacitance as a function of input/output to ground voltage; typical values

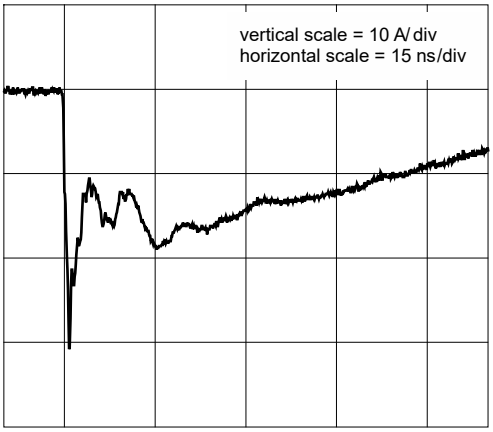




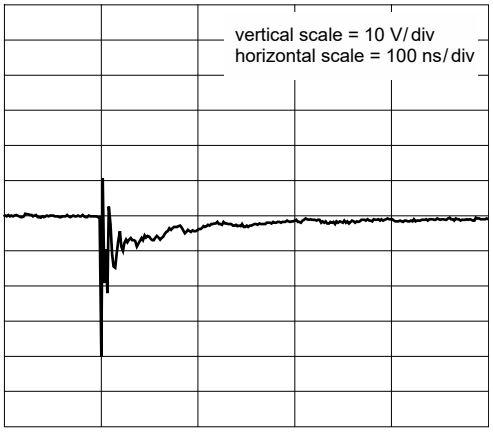
unclamped +8 kV ESD pulse waveform
(IEC 61000-4-2 network)



clamped +8 kV ESD voltage waveform
(IEC 61000-4-2 network), pin I/O to GND



unclamped -8 kV ESD pulse waveform
(IEC 61000-4-2 network)



clamped -8 kV ESD pulse waveform
(IEC 61000-4-2 network), pin I/O to GND

006aaa680

Fig. 3. ESD clamping test setup and waveforms

10. Application information

Handling data rates up to 480 Mbit/s, USB 2.0 interfaces require ESD protection devices with an extremely low line capacitance in order to avoid signal distortion.

With a capacitance of only 1.8 pF, the device offers IEC 61000-4-2, level 4 compliant ESD protection.

The device integrates two ultra-low capacitance rail-to-rail ESD protection diodes and an additional ESD protection diode in a small 4-lead SOT143B package.

The additional ESD protection diode connected between ground and V_{CC} prevents charging of the supply.

To achieve the maximum ESD protection level, no additional external capacitors are required.

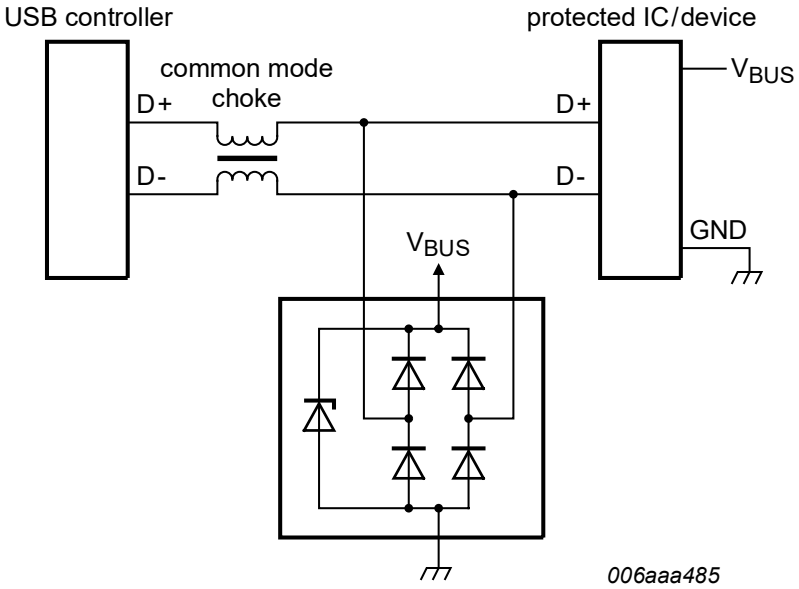


Fig. 4. Application diagram: USB 2.0

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

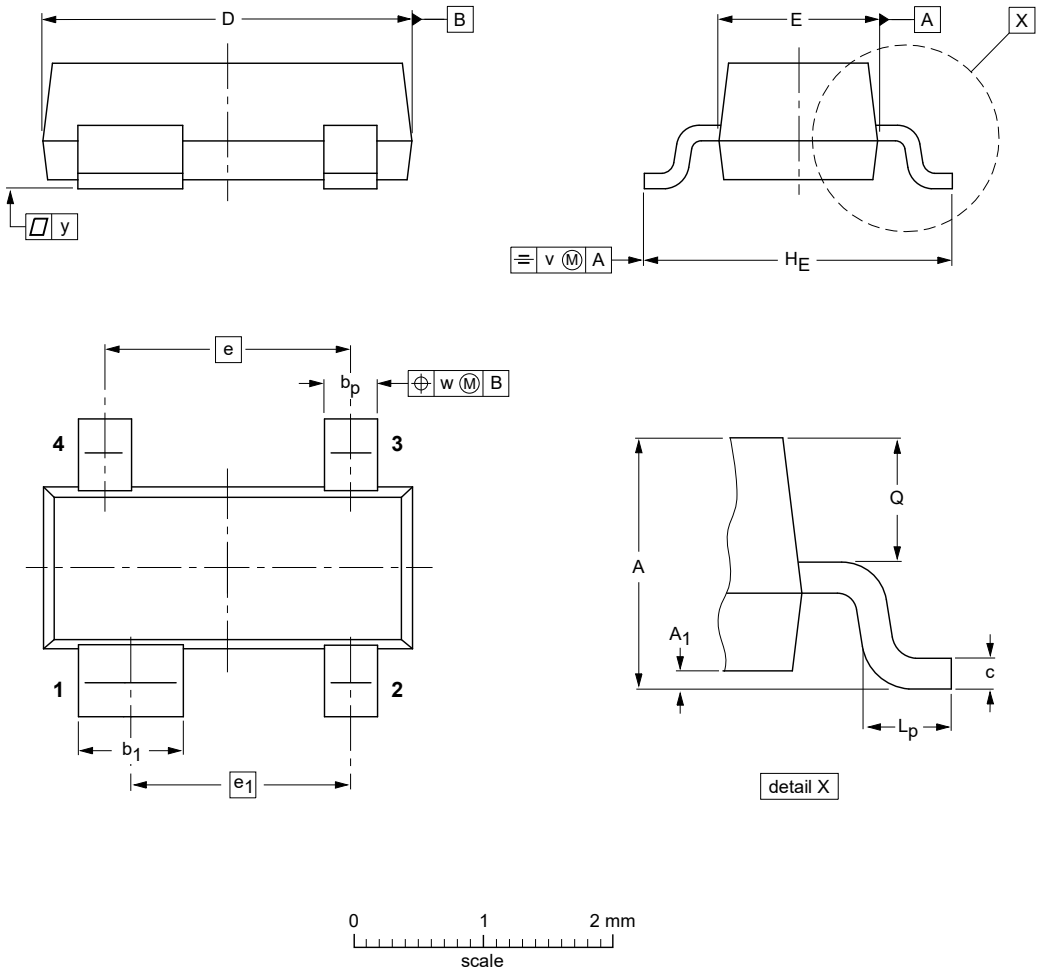
11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

Plastic surface-mounted package; 4 leads **SOT143B**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143B						~~04-11-16~~ 06-03-16

Fig. 5. Package outline SOT143B

13. Soldering

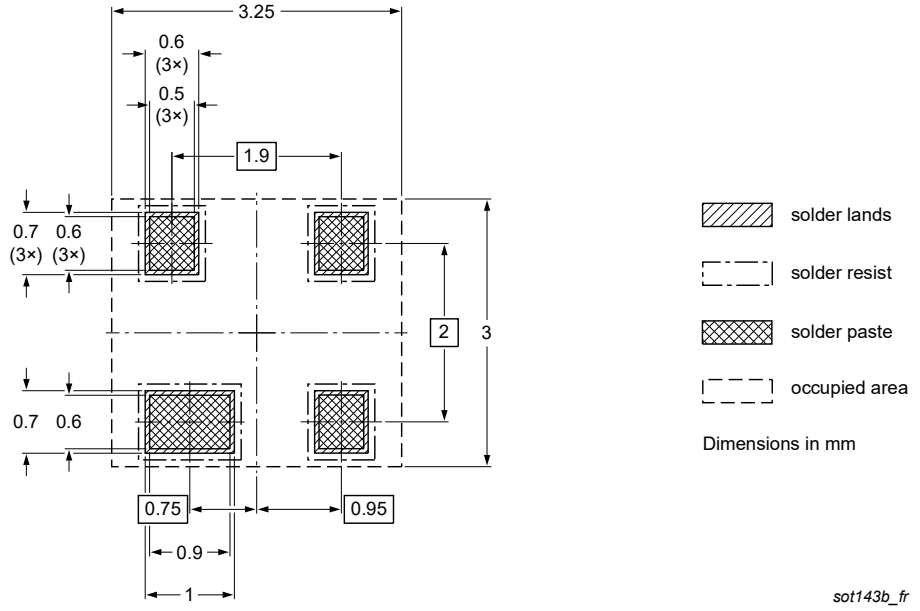


Fig. 6. Reflow soldering footprint for SOT143B

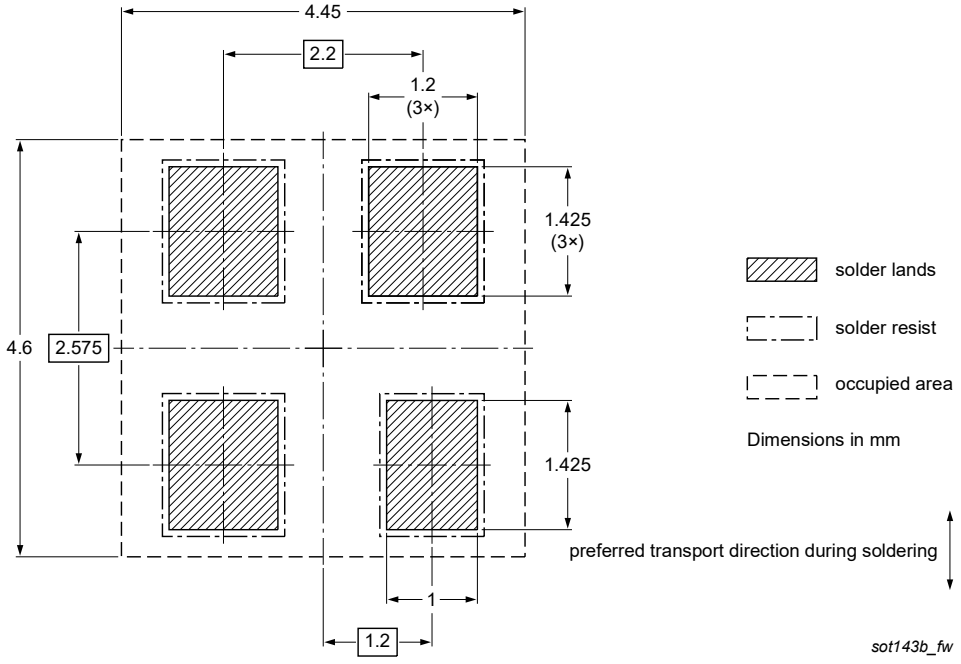


Fig. 7. Wave soldering footprint for SOT143B

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PRTR5V0U2AX-Q v.1	20220503	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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