MLX90291

Datasheet

1. Features and Benefits

- Programmable Hall effect sensor
  - 12-bit 125Hz PWM output signal proportional to the magnetic flux density
  - Switch function
- Measurement range from ±15mT to ±400mT
- Low noise output signal (PWM jitter)
- Programmable through the connector (supply, ground & output)
- 16 bit customer ID number (48 bit MLX ID for traceability purposes)
- SOIC8 package RoHS compliant
- Lead free component, suitable for lead free soldering profile 260°C

2. Application Examples

- Rotary position sensor
- Linear position sensor
- Contactless switch

3. Description

The MLX90291 is a monolithic programmable linear hall sensor IC, which can provide a PWM output signal proportional to the externally applied magnetic flux density or act as a switch with a programmable threshold level. The transfer characteristic of the MLX90291 is fully programmable (offset, gain, clamping levels …).

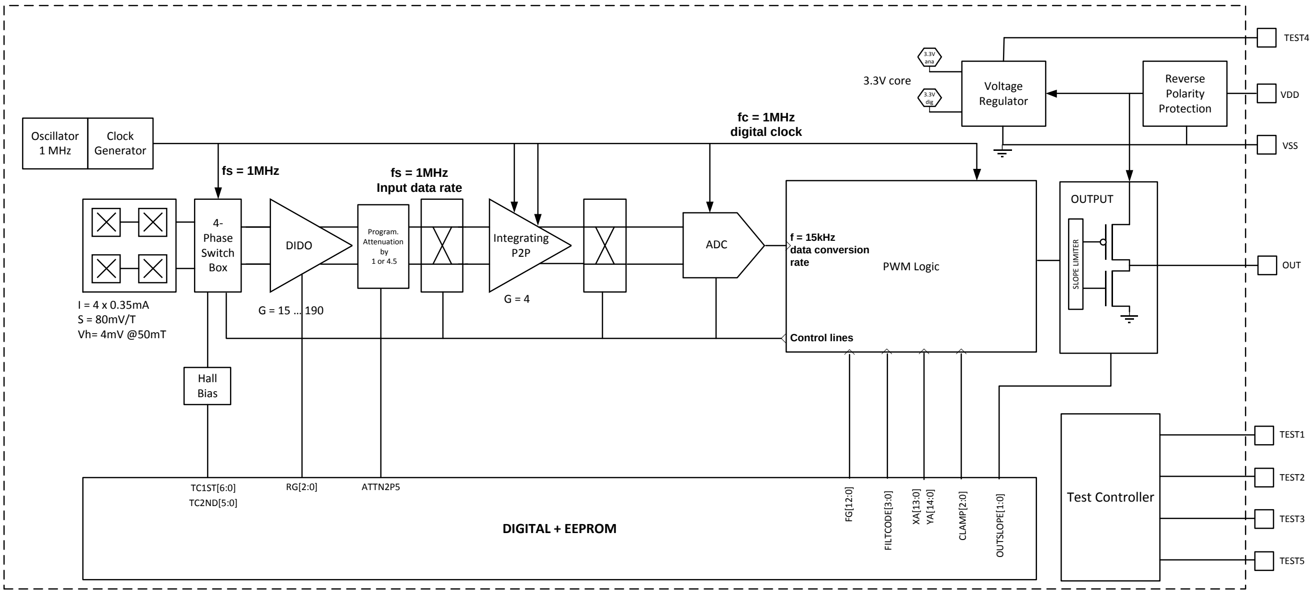

Figure 1

Contents

4. Ordering Information

Product	Temperature	Package	Option Code	Packing Form	Definition
MLX90291	K (-40°C to 125°C)	DC	BCA-000	RE	

Legend:

Temperature Code:	K: from -40°C to 125°C
Package Code:	“DC” for SOIC-8 package
Option Code:	BCA-000
Packing Form:	“RE for Reel”
Ordering Example:	“ML90291KDC-BCA-000-RE” For SOIC package, delivered in Reel.

Table 1

5. Glossary of Terms

Gauss (G), Tesla (T)	Units for the magnetic flux density – 1 mT = 10 G
TC	Temperature Coefficient (in ppm/Deg.C.)
NC	Not Connected
PWM	Pulse Width Modulation
%DC	Duty Cycle of the output signal i.e. TON /(TON + TOFF)
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
LSB	Least Significant Bit
MSB	Most Significant Bit
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
PTC	Programming Through Connector
POR	Power On Reset

Table 2

6. Pin Definitions and Descriptions

Pin #	Name	Description
1	VDD	Supply Voltage
2	VSS	Ground Voltage
3	TEST4	MLX Test and factory calibration
4	OUT	Sensor output signal
5	TEST5	MLX Test and factory calibration
6	TEST3	MLX Test and factory calibration
7	TEST2	MLX Test and factory calibration
8	TEST1	MLX Test and factory calibration

Table 3 Pin definition and description – SOIC8 pacakage

Pins Input and Test are internally grounded in application. For optimal EMC behaviour connect the unused pins (Not Used) to the Ground.

6.1. Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Positive Supply Voltage (over-voltage)	Vdd	20	V
Reverse Supply Voltage Protection		-10 -14 (200s max, TA = +25°C)	V
Positive Output Voltage		+10 +14 (200s max, TA = +25°C)	V
Output Current	Iout	20	mA
Reverse Output Voltage(1)		-5	V
Reverse Output Current(1)		-50	mA
Operating Ambient Temperature Range	T_A	-40 to +125	°C
Storage Temperature Range	T_S	-55 to +150	°C

Parameter	Symbol	Value	Units
Magnetic Flux Density		± 10	T

Table 4
(1) Realized through an on-chip resistor along the output line

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

7. General Electrical Specifications

Operating Parameters TA = -40°C to 125°C, Vdd = 5.0 V, using recommended application diagram, unless otherwise specified.

Electrical Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Nominal Supply Voltage	VDD		4.5	5	5.5	V
Supply Current	IDD			8	10	mA
Peak Supply Current	IDD_{peak}	During power-up and PWM switching			15	mA
Reset Voltage (POR)	V_{POR}		2.2		2.7	V
POR Threshold Hysteresis	$V_{PORHYST}$			0.3		V
Operating Threshold (rising)	$V_{OPERATING}$			3.3	3.8	V
Under-Voltage Threshold (falling)	V_{UNDER}	Immediate diagnostic low without reset in case of recovery	2.7	3		V
Operating / Under-Voltage Threshold Hysteresis	V_{HYST}			0.1		V
Programming Voltage	V_{PROG}	Not Locked Part Output = High Impedance	6.7	7.4	7.7[1]	V
Overvoltage detection	V_{OVER}	Output = High Impedance	7.5[1]	8.5		V
Resistance range (Pull-up/down)	RL	Pull-up OUT to 5V	2	4.7	kΩ	
Load Capacitor range	CL	Between OUT and GND		10		nF

Electrical Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Saturation Voltage Push Pull Mode	$V_{SATPPHI}$	IOUT = + 2mA	VDD – 0.3			V
	$V_{SATPPLO}$	IOUT = – 2 mA			0.3	V
Output Saturation Voltage Open Drain Mode	V_{SATOD}	IOUT = – 2 mA Output = Low (Driver ON)			0.3	V
	I_{LEAKOD}	VOUT = + 5 V Output = High (Driver OFF)			0.3	V
Output Short Circuit Current	$I_{OUTSCGND}$	Current limitation fully ON	+ 15		+ 28	mA
	$I_{OUTSCVDD}$	Current limitation fully ON	– 28		– 15	mA

Table 5

(1) No overlap possible between programming voltage and overvoltage thresholds at the same temperature

8. Magnetic Specification

Operating Parameters TA = -40°C to 125°C, Vdd = 5.0 V, unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Magnetic Flux Density range	B		±15	±40	±400	mT

Table 6

9. Timing Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Up Sequence	t_{ON1}	$0 < VDD < V_{POR}$		$F(V_{DDSR})$		ms
	t_{ON2}	$V_{POR} < VDD < V_{OPERATING}$		$F(V_{DDSR})$		ms

	t_{ON3}	VDD > $V_{OPERATING}$		1		Cycle
Power Supply Slw rate (external)	V_{DDSR}		0.0005		5	V/µs
EEPROM Check	t_{EEPROM}	EEPROM dump + CRC check		0.5	1	ms
Main Oscillator Frequency	F_{OSC}	Tolerance +/- 10%	921	1024	1127	kHz
Tick Time	t_{TICK}			0.98		µs
PWM Cycle Duration	$Cycle_{PWM}$	2^{13} t_{TICK}		8		Ms
PWM Output Frequency	F_{PWM}	$F_{OSC}/2^{13}$		125		Hz
Sampling Frequency	F_{SAMPLE}	Analog sampling		F_{osc}		
Conversion Rate @ F_{OSC} = 1024 kHz	F_{CONV}	Measurement: 40 analog samples Conversion (ADC): 25 µs		70		µs
Low pass filtering (First order filter) @ F_{OSC} = 1024 kHz @ -3 dB	F_{FILTER}	FILTCODE = 9 FILTCODE = 8 FILTCODE = 7 FILTCODE = 6 FILTCODE = 5 FILTCODE = 4 FILTCODE = 3 FILTCODE = 2		4 9 17 35 70 139 279 557		Hz
Output Slope current generator	I_{SLOPE}	OUTSLOPE = 0 OUTSLOPE = 1 OUTSLOPE = 2 OUTSLOPE = 3		4 6 11 20		mA

Table 7 Timing specification of the analog output

10. PWM output specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PWM Output Clamping Ssetting sets both upper & lower clamp.	SCG_{PWM}	CLAMP = 0 CLAMP = 1 CLAMP = 2 CLAMP = 3 CLAMP = 4 CLAMP = 5 CLAMP = 6	1 4 5 6 7 8 9		99 96 95 94 93 92 91	%DC
PWM Output Offset	PWM_{OQ}	Programming Range	0		100	%DC
PWM Output Offset Resolution	PWM_{OQRES}	Programming Resolution		0.025		%DC
PWM Output Slope	S	10%-90% Swing	0.1	1	6.4	%DC/mT
PWM Output Slope Resolution	S_{RES}	% of Slope target value (fine gain)		0.025		%
PWM Resolution	LSB_{PWM}	12 bits		0.0125		%DC
SWITCH Low Level Threshold range	$SWITCH_{LOW}$	Switch mode Programming range	0		100	%
SWITCH High Level Threshold range	$SWITCH_{HIGH}$	Switch mode Programming range	0		100	%
SWITCH Programming resolution	$SWITCH_{RES}$	Switch mode Resolution		0.025		%
PWM Linearity	DNL_{PWM} INL_{PWM}	13 bits resolution 40 mT – 1%DC/mT	-1 -2		1 2	LSB_{PWM}
PWM Jitter	JIT_{PWM}	S = 1% DC/mT F_{PWM} = 125 Hz Filter setting: m=32	-2		2	LSB_{PWM}
PWM Clamping Accuracy	$Clamp_{ACC}$		– 2		+ 2	LSB_{PWM}

Intrinsic Offset Thermal Drift	Δ^TOffset	25 °C to - 40 °C 25 °C to 125 °C	– 0.1		+ 0.1	mT
Thermal Sensitivity Drift	Δ^TS	After calibration @ MLX full temperature range	– 150	0	+ 150	ppm/°C
Sensitivity thermal coefficient resolution	RES	Incremental TC Adjust 5 bits over ± 800ppm/°C		50		ppm/°C

Table 8 PWM output specification

11. Fault Modes

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output signal in Fault state	$Fault_{OUT}$	EEPROM parity fail Pull resistor = 5K	4		-	V
Parity Fail Criterion	n_{PARITY}	Successive CRC fails before Diagnostic is set	-	2	-	Count
Broken VSS	VBR_{VSS}	Pull-Up resistor = 5K	4			V
Broken VDD	VBR_{VDD}	Pull-Up resistor = 5K	4			V

Table 9 Fault Modes

12. Programmable Items

12.1. Parameter Table

Parameter	Bits	Comment
OUTMODE	1	Push pull or open drain output drive
ROUGHGAIN	3	Rough gain preamplifier
FINEGAIN	13	Digital fine gain adjustment from -3.999 to +3.999
XA	14	Offset before gain
YA	15	Offset after gain, (Xa,Ya) defines the zero Gauss point
CLAMP	3	Clamp high and clamp low level
FILTCODE	4	Digital output filter
OUTSLOPE	2	Output Slope Control
DCDEF	1	PWM Duty Cycle Definition
TC1ST	7	Sensitivity temperature drift correction 1^{st} order
TC2ND	6	Sensitivity temperature drift correction 2^{nd} order
OFFDRIFT	6	Residual Offset Correction
SWITCH	1	PWM/Switch mode
PLATEPOL	1	Invert Sensitivity Sign
ATTN2P5	1	Attenuator block switch
CSTID	16	Melexis ID

Table 10 Customer programmable items

12.2. Output mode configuration (OUTMODE)

OUTMODE configures the output driver.

OUTMODE	Output Driver
0	PWM Open-drain
1	PWM Push-pull

Table 11 Output configuration

12.3. Sensitivity programming (ROUGHGAIN, FINEGAIN)

ROUGHGAIN[2:0]

This 3-bit register controls the gain of the pre-amplifier.

- The Most Significant Bits enables the PREAMP block, which gives an gain of 4.3 . Enabling this PREAMP uses 2mA extra supply current on top of the specified IDD.
- The 2 LSB control the gain of the MAINAMP

Value	Typical Gain
0	15.0
1	21.6
2	31.1
3	44.8
4	64.5
5	92.9
6	133.7
7	192.6

Table 12 ROUGHGAIN versus amplifier gain

FINEGAIN[12:0]

Value defines the digital gain adjustment

- The code 1024 corresponds to a gain of 1
- The MSB is the sign bit which acts as a polarity bit
- FINEGAIN gain range is from -3.9999 to +3.99999

12.4. Offset / output quiescent voltage programming (XA, YA)

XA[13:0]

PWM mode: Offset trimming before FINEGAIN block

Switch mode: Threshold for the output to switch

YA[14:0]

PWM mode: Offset trimming after FINEGAIN block

Switch mode: Hysteresis for the output to switch

Both parameters together define the zero Gauss point in PWM mode

In switch mode, XA is used to set the threshold and YA to set the hysteresis

Case YA > 0	Case YA < 0	Output State
ADC < 4.XA – 16.YA	ADC < 4.XA	Set to Zero
ADC > 4.XA	ADC > 4.XA - 16.YA	Set to One
Otherwise	Otherwise	Unchanged

Table 13 Output state as function of XA and YA in switch mode

12.5. Clamping level programming (CLAMP)

CLAMP[2:0] defines the clamping level of the PWM output

CLAMP	Minimal output [%DC]	Maximal output [%DC]
0	1	99
1	4	96
2	5	95
3	6	94
4	7	93
5	8	92
6	9	91
7	10	90

Table 14 CLAMP parameter versus output.

12.6. Bandwidth and filter programming (FILTCODE)

FILTCODE[3:0] allows adjusting the internal bandwidth of the sensor in order to optimize for speed or resolution.

FILTCODE	Cutt off frequency [Hz]	Attenuation [dB]	Tau [ms]
2	557	-8.0	0.29
3	279	-11.2	0.57
4	139	-14.4	1.14
5	70	-18.1	2.29
6	35	-22.4	4.57
7	17	-27.1	9.14
8	9	-32.3	18.29
9	4	-38.1	36.57

Table 15: FILTCODE settings PWM mode

12.7. Current limitation (OUTSLOPE)

2 Bit register to set the current limitation for slew rate control

OUTSLOPE	Current limitation [mA]
0	4
1	6
2	11
3	20

Table 16 Current limitation

12.8. PWM Mode duty cycle definition (DCDEF)

The PWM duty cycle definition is as follows.

DCDEF	PWM duty cycle definition
0	tLow / (tLow + tHigh)
1	tHigh / (tLow + tHigh)

Table 17 PWM duty cycle definition

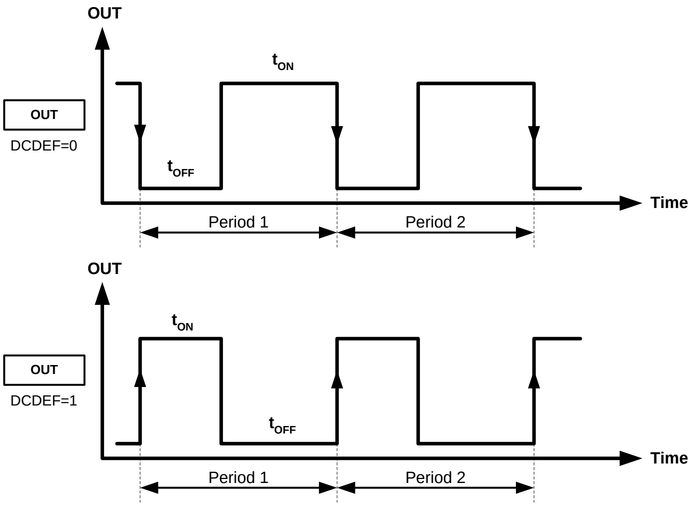

Figure 1: Two different PWM modes

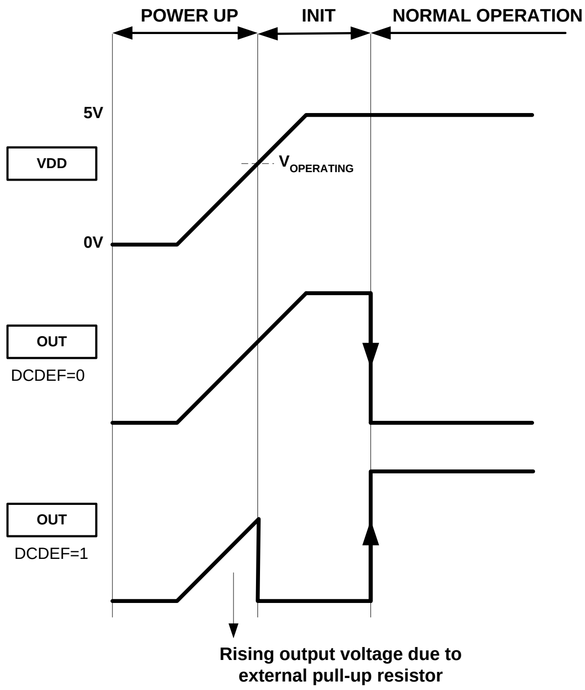

Figure 2: Power-on behavior of the two different modes

12.9. Sensitivity and temperature drift programming (TC1ST, TC2ND)

TC1ST[6:0]

Programming first order sensitivity temperature drift

Value	Typical 1st order TC
0	+2740ppm/°C
63 or 64	0ppm/°C
127	-2950ppm/°C

Table 18 : TC1ST parameter

TC2ND[5:0]

Programming second order sensitivity temperature drift

Value	Typical 2nd order TC
0 or 32	0 ppm/°C²
31	+6.8 ppm/°C²
63	-6.1 ppm/°C²

Table 19 : TC2ND parameter

12.10. Offset temperature drift programming (OFFDRIFT)

OFFDRIFT[5:0] parameter defines the offset behaviour over temperature (1st order)

Value	Offset drift correction
0 or 32	0 mV/°C
31	+0.9 mV/°C
63	-0.9 mV/°C

Table 20 : OFFDRIFT parameter versus correction

12.11. Functional Mode (SWITCH)

Value	Mode
0	PWM output mode
1	Switch output mode

Table 21 : SWITCH parameter

12.12. Polarity (PLATEPOL)

PLATEPOL parameter changes the sign of the measured sensitivity
Default value = 0

12.13. Attenuator (ATTN2P5)

Switch to control the attenuation block in the signal path. Enabling this block reduces the signal by a factor of 4.5. Enabling this attenuator together with the PREAMP block gives the lowest noise at a cost of 2mA with the full signal amplification to be the same.

Value	ATTN2P5
0	Attenuation factor = 1
1	Attenuation factor = 4.5

Table 22 : Attenuation settings

12.14. Customer ID (CSTID)

16-bit customer programmable ID

13. Recommended Application Diagrams

13.1. Resistor and Capacitor Values

CLAMP[2:0] defines the clamping level of the PWM output

Part	Description	Value	Unit
C1	Decoupling, EMI, ESD	10	nF

C2	Supply capacitor, EMI, ESD	100	nF
R1	Pull up or pull down resistor	4.7	kΩ

Table 23 : Resistive and capacitive values for the recommended application diagrams.

13.2. Pull down resistor for diagnostic low

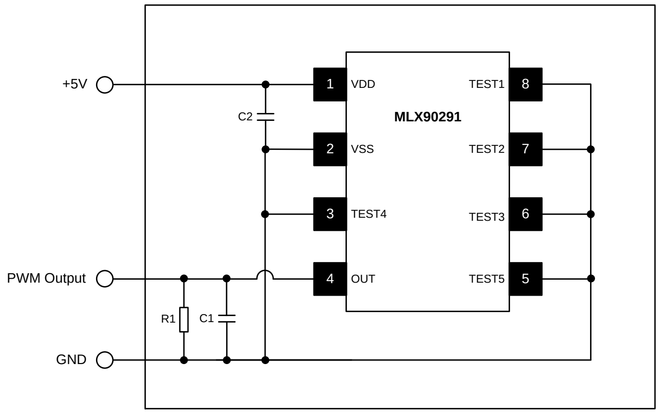

Figure 3: Diagnostic low

13.3. Pull up resistor for diagnostic high

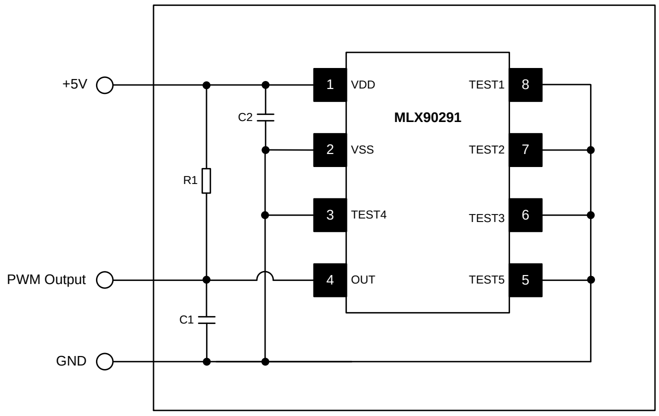

Figure 4: Diagnostic high

14. Package Information

14.1. SOIC8 Package Dimensions

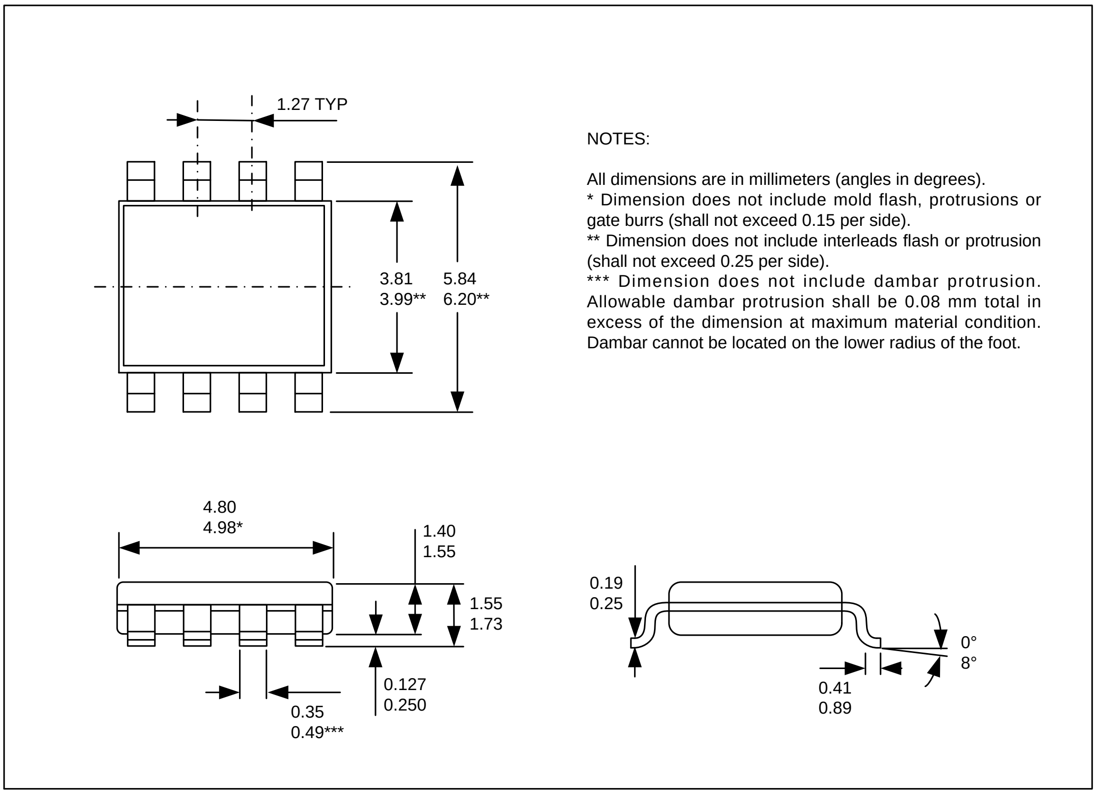

Figure 5: Package dimensions

14.2. SOIC8 Pin Out and Marking

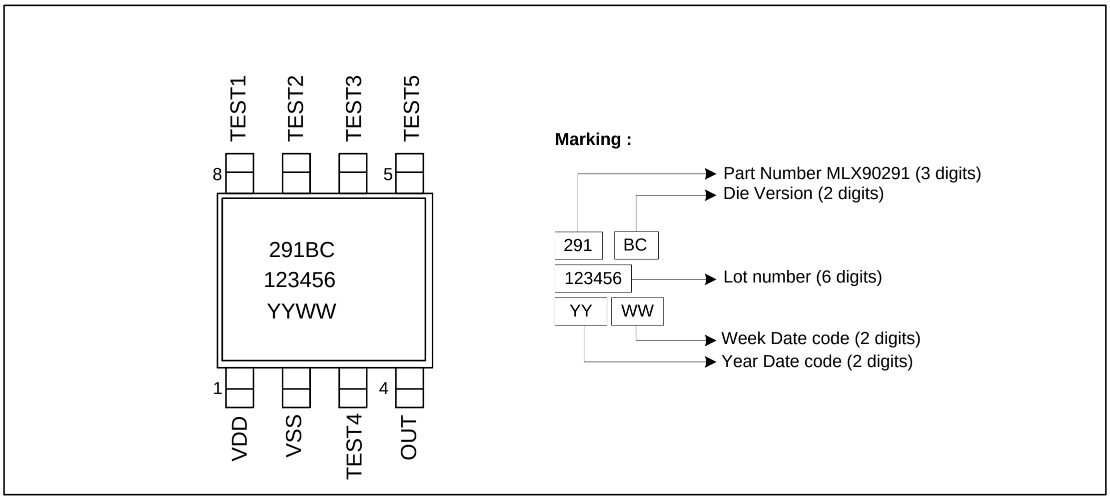

Figure 6: Pin out and marking

14.3. SOIC8 Hall plate positioning

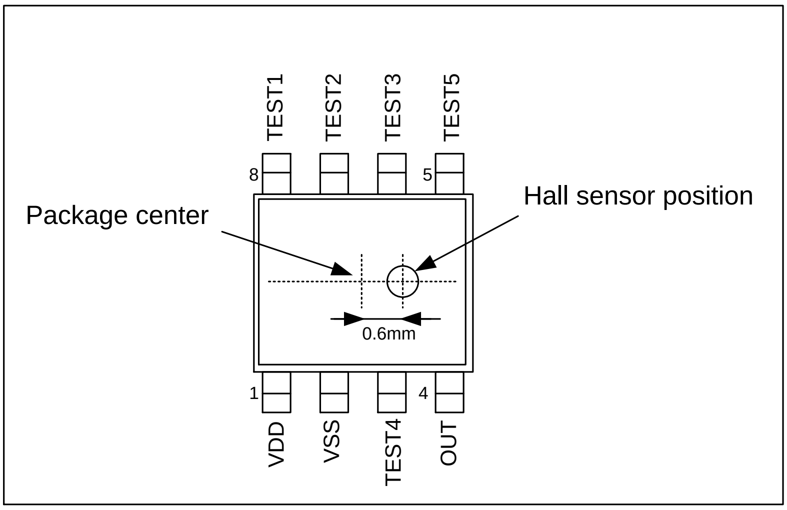

Figure 7: Hall Plate positioning

15. Standard Information

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation. For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile etc), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends to consult the dedicated trim&form recommendation application note: lead trimming and forming recommendations

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/en/quality-environment

16. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

17. Revision History Table

06/10/2016	New template

Table 24

18. Contact

For the latest version of this document, go to our website at www.melexis.com.

For additional information, please contact our Direct Sales team and get help for your specific needs:

Europe, Africa	Telephone: +32 13 67 04 95
	Email : sales_europe@melexis.com
Americas	Telephone: +1 603 223 2362
	Email : sales_usa@melexis.com
Asia	Email : sales_asia@melexis.com

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