



megaAVR[®] 0-series Errata

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General Notes

The megaAVR[®] 0-series devices that you have received conform functionally to the current Device Data Sheet that are available online at <https://www.microchip.com/8-bit/microchip-avr-mcus>, except for the anomalies described in this document.

The errata described in this document are likely be addressed in future revisions of the silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Note: If you are unable to extract the silicon revision level, contact your local Microchip sales office for assistance.

1. Silicon Errata

Symbols

- Erratum not applicable
- X** Erratum is applicable
- * This die revision was for internal use/sampling only

1.1 ADC

1.1.1 One Extra Measurement Performed After Disabling ADC Free Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN Fix/
Workaround: Write ADCn.CTRLA.ENABLE.

Work around

Write ADCn.CTRLA.ENABLE to zero to stop the free running mode immediately.

Affected Silicon Revisions

Device	rev.A	rev.B					
ATmega3209/4809	*	X					
ATmega3208/4808-A/M	*	X					
ATmega3208/4808-X	*	X					

1.1.2 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work around

Clear ADC.EVCTRL.STARTEI and wait for conversion to complete before disabling the ADC.

Affected Silicon Revisions

Device	rev.A	rev.B					
ATmega3209/4809	*	X					
ATmega3208/4808-A/M	*	X					
ATmega3208/4808-X	*	X					

1.1.3 ADC - Functionality Cannot be Guaranteed With ADCCLK Above 1.5 MHz for All Conditions

The ADC functionality cannot be guaranteed if ADCCLK > 1.5 MHz with ADCn.CALIB.DUTYCYC set to 1. The ADC functionality cannot be guaranteed if ADCCLK > 1.5 MHz and VDD < 2.7V.

Work around

If ADC is operated with ADCCLK > 1.5 MHz and VDD > 2.7V, ADCn.CALIB.DUTYCYC must be set to zero (50% duty cycle). Do not use ADC at ADCCLK > 1.5 MHz and VDD < 2.7V

Affected Silicon Revisions

Device	rev.A	rev.B					
ATmega3209/4809	*	X					
ATmega3208/4808-A/M	*	X					
ATmega3208/4808-X	*	X					

1.2 CCL

1.2.1 D-Latch is Not Functional

The CCL D-latch is not functional.

Work around

None.

Affected Silicon Revisions

Device	rev.A	rev.B					
ATmega3209/4809	*	X					
ATmega3208/4808-A/M	*	X					
ATmega3208/4808-X	*	X					

1.3 RTC

1.3.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the RTC and PIT prescaler.

Work around

None.

Affected Silicon Revisions

Device	rev.A	rev.B					
ATmega3209/4809	*	X					
ATmega3208/4808-A/M	*	X					
ATmega3208/4808-X	*	X					

1.4 TCA

1.4.1 Restart Command Does Not Work in Single Slope Down-Counting Mode

Issuing a restart command when in single slope down-counting mode will reset TCA_n.CNT and clear the direction bit causing the timer to count up.

Work around

None.

Affected Silicon Revisions

Device	rev.A	rev.B					
ATmega3209/4809	*	X					
ATmega3208/4808-A/M	*	X					
ATmega3208/4808-X	*	X					

1.5 TCB

1.5.1 TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is only restarted after a TCA OVF.

Work around

None.

Affected Silicon Revisions

Device	rev.A	rev.B					
ATmega3209/4809	*	X					
ATmega3208/4808-A/M	*	X					
ATmega3208/4808-X	*	X					

2. Revision History

2.1 Document Rev.A - 02/2018

Initial version.

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