ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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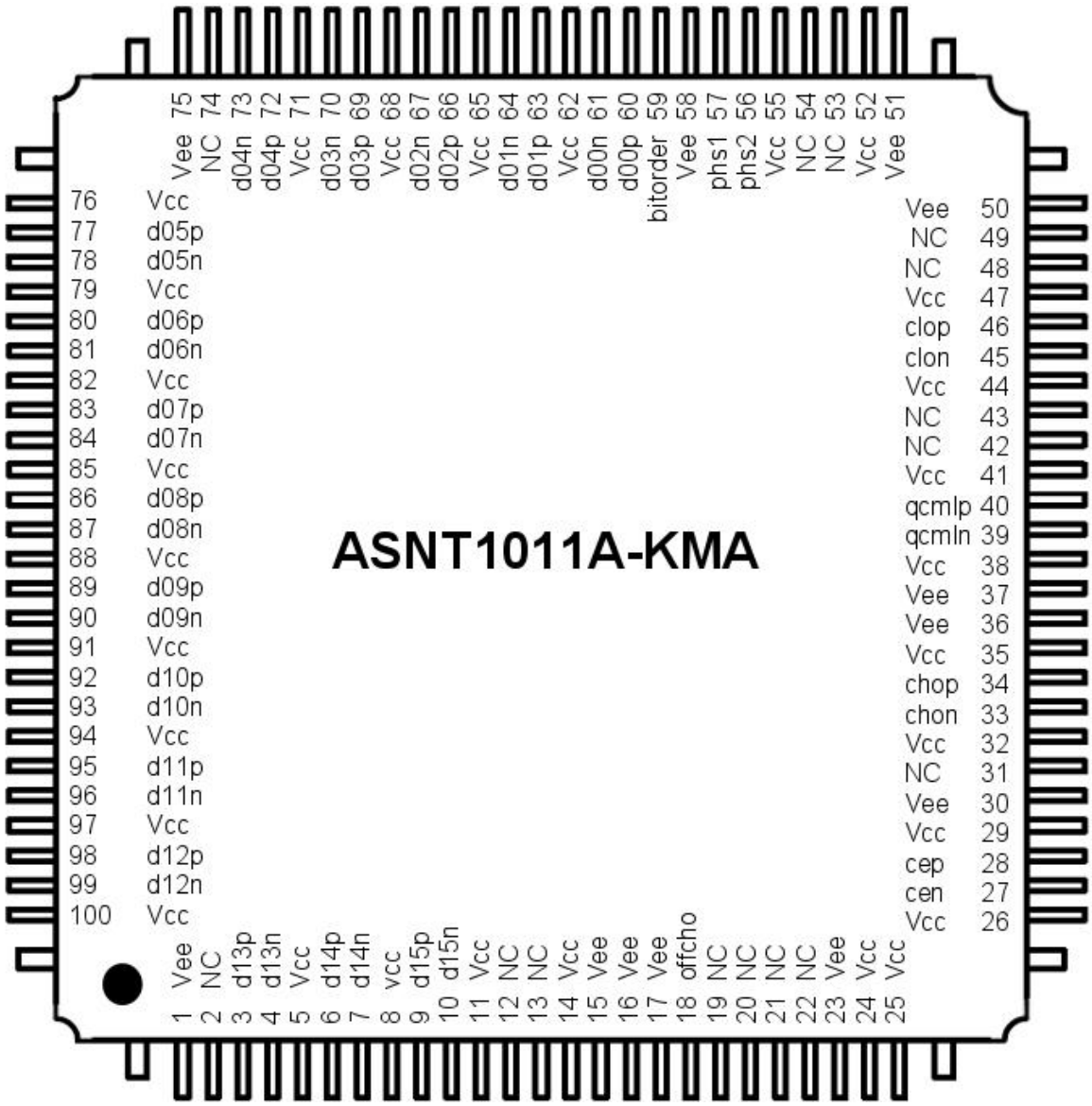
# ASNT1011A-KMA
# DC-to-17*Gbps* Digital Multiplexer 16:1 / Serializer

- Broadband digital serializer 16 to 1 operating seamlessly from DC to 17*Gbps*
- LVDS compliant input data buffers
- Full-rate clock output
- Clock divided-by-16 LVDS output buffer with 90°-step phase selection
- Single +3.3*V* power supply
- Industrial temperature range
- Low power consumption of 660*mW* at 17*Gbps*
- Custom 100-pin CQFP package (12*mm* x 12*mm*)



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# DESCRIPTION

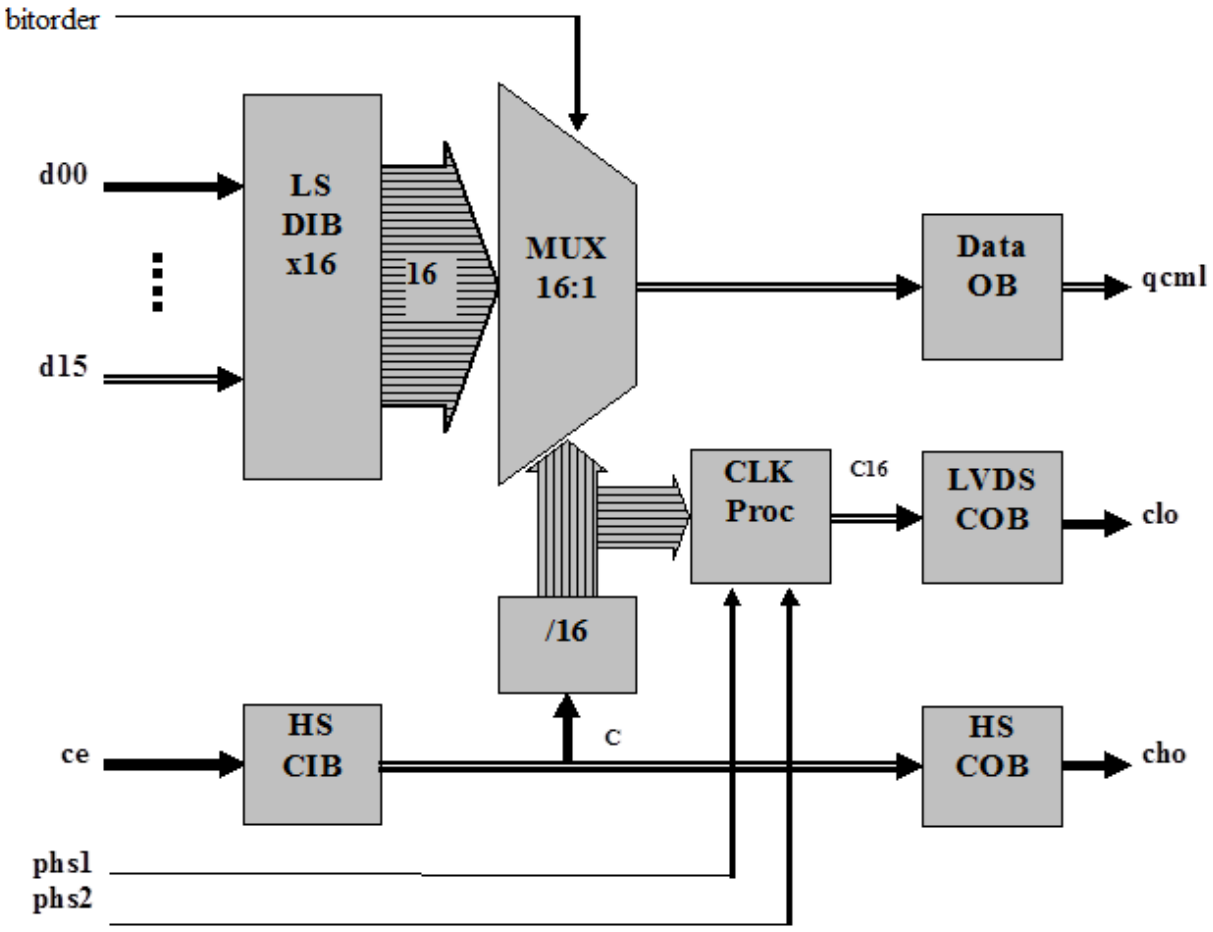


*Fig. 1. Functional Block Diagram*

ASNT1011A-KMA is a low power and high-speed digital 16-to-1 multiplexer (MUX) / serializer IC. The IC shown in Fig. 1 functions seamlessly over data rates ($f_{bit}$) ranging from DC to 17*Gbps*.

The main function of the IC is to multiplex 16 parallel data channels running at a bit rate of $f_{bit}/16$ into a high speed serial bit stream running at $f_{bit}$. It provides a high-speed output data channel for point-to-point data transmission over a controlled impedance media of 50*Ohm*. The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

During normal operation, the serializer's low-speed input buffer (LS DIBx16) accepts external 16-bit wide parallel data words d00p/d00n-d15p/d15n through 16 differential LVDS inputs and delivers them to the multiplexer's core (MUX16:1) for serialization. A full rate clock must be provided by an external source cep/cen to the high-speed clock input buffer (HS CIB) where it is routed to the high speed clock output buffer (HS COB) and the internal divider-by-16 (/16). The divider provides signaling for MUX16:1 and produces a full rate clock divided-by-16 "C16" for the low speed LVDS compliant clock output buffer (LVDS COB).The phase of clop/clon can be modified by 90° increments by utilizing pins phs1 and phs2 and the clock processing block (CLK Proc).

By utilizing pin bitorder, the serializer can designate either d00p/d00n or d15p/d15n as the MSB thus simplifying the interface between ASNT1011A-KMA and a proceeding ASIC.

The serialized words are transmitted as 2-level signals qcmlp/qcmln by a differential CML output buffer (Data OB). A full-rate clock is transmitted by HS COB in parallel with the high-speed data. The clock and data outputs are well phase matched to each other resulting in very little relative skew over the operating temperature range of the device. Both output stages are back terminated with on-chip 50*Ohm* resistors.

The serializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

## LS DIBx16

The Low-Speed Data Input Buffer (LS DIBx16) consists of 16 proprietary universal input buffers (UIBs) that exceed the LVDS IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 standards. UIB is designed to accept differential signals with amplitudes above 60*mV* peak-to-peak (p-p), DC common mode voltage variation between the negative vee and positive vcc supply rails, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes above 60*mV*p-p and threshold voltages between vee and vcc. The input termination impedance is set to 100*Ohm* differential.

## HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process an external CML clock signal cep/cen with frequencies from DC to 17*GHz*. It can also accept a single-ended signal to cep/cen with a threshold voltage applied to the unused cen/cep pin. HS CIB can handle input signal amplitudes between 200*mV* and 1.2*V* p-p differential or single-ended. The buffer utilizes on-chip single-ended termination of 50*Ohm* to vcc for each input line.

## /16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The high-speed clock "C" is fed into the first divide-by-2 circuit that generates half rate clock "C2". "C2" is routed internally to the next divide-by-two circuit and outside of the block to MUX16:1. Other divided down clock signals are formed and routed to MUX16:1 in similar fashion. "C16" is passed on to LVDS COB to become the output low speed clock signal clop/clon.

## MUX16:1

The 16 to 1 Multiplexer (MUX16:1) utilizes a tree type architecture that latches the incoming data on the negative edge of the "C16" clock signal that is supplied by /16. The 16-bit wide data word is subsequently multiplexed and delivered to Data OB as a single serial data stream running at a data rate up to 17*Gbps*. The latency of this circuit block is equal to roughly one period of "C16". The input MSB corresponds to d00p/d00n when bitorder = 0 (default), or to d15p/d15n when bitorder = 1.

## Data OB

The Data Output Buffer (Data OB) receives high-speed serial data from MUX16:1 and converts it into the CML output signal qcmlp/qcmln with a single ended swing of 600*mV*. The buffer requires 50*Ohm* external termination resistors connected between vcc and each output to match its internal 50*Ohm* resistors and can operate at a data rate up to 17G*bps*.

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## HS COB

The High Speed Clock Output Buffer (HS COB) utilizes the same termination scheme as Data OB and can operate at a frequency up to 17*GHz* while producing a single-ended CML output swing of 600*mV*. The buffer can be enabled or disabled by the external 2-state control signal offcho. The logic "0" state provides a full-rate clock output signal while the logic "1" state disables the buffer completely to save power.

## CLK Proc

By utilizing the CMOS control pins phs1 and phs2, the phase of clop/clon can be altered in accordance with Table 1.

*Table 1. Output Clock Phase Selection*

| phs1 | phs2 | C16 phase |
|---|---|---|
| vee (default) | vee (default) | 270° |
| vee | vcc | 180° |
| vcc | vee | 90° |
| vcc | vcc | 0° |

## LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives "C16" and converts it into an LVDS output signal clop/clon. The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2.0*GHz* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 standards.

## Output Timing

The phase relation between the output data qcmlp/qcmln and the full rate output clock chop/chon is specified in Table 2 and illustrated by Fig. 2.

*Table 2. Output Data-to-Clock Phase Difference*

| Junction temperature, *°C* | $\tau$,*ps* | |
|---|---|---|
| | Min. | Max. |
| -25 | 77 | 80 |
| 50 | 82 | 86 |
| 125 | 87 | 91 |

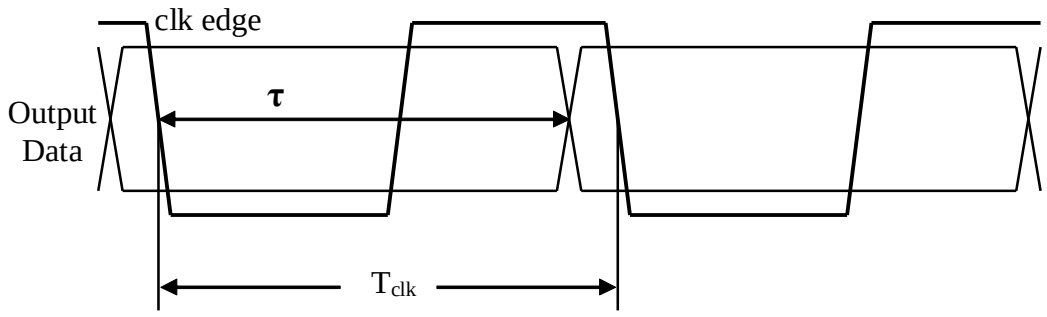


*Fig. 2. Output Timing Diagram*

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# ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

*Table 3. Absolute Maximum Ratings*

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply Voltage (vcc) | | +3.6 | *V* |
| Power Consumption | | 0.72 | *W* |
| RF Input Voltage Swing (SE) | | 1.0 | *V* |
| Case Temperature | | +90 | *ºC* |
| Storage Temperature | -40 | +100 | *ºC* |
| Operational Humidity | 10 | 98 | *%* |
| Storage Humidity | 10 | 98 | *%* |

# TERMINAL FUNCTIONS

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| **Name** | **No.** | **Type** | |
| **High-Speed I/Os** | | | |
| cep | 28 | Input | CML differential external clock inputs with internal SE 50*Ohm* termination to vcc |
| cen | 27 | | |
| chop | 34 | Output | CML differential clock outputs. Require external SE 50*Ohm* termination to vcc |
| chon | 33 | | |
| qcmlp | 40 | Output | CML differential data outputs. Require external SE 50*Ohm* termination to vcc |
| qcmln | 39 | | |
| **Controls** | | | |
| phs1 | 57 | LS In., CMOS | Low-speed output clock phase selection (default: both low) |
| phs2 | 56 | | |
| offcho | 18 | LS In., CMOS | HS COB control (active: high, buffer is disabled; default: low, full-rate output clock) |
| bitorder | 59 | LS IN., CMOS | Input bit order selection (active: high, d15p/d15n is serialized first; default: low, d00p/d00n is serialized first) |

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| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| Name | No. | Type | |
| **Low-Speed I/Os** | | | |
| clop | 46 | Output | LVDS clock outputs. Can transmit four different clock phases as defined by phs1 and phs2 |
| clon | 45 | | |
| d00p | 60 | Input | LVDS data inputs |
| d00n | 61 | | |
| d01p | 63 | | |
| d01n | 64 | | |
| d02p | 66 | | |
| d02n | 67 | | |
| d03p | 69 | | |
| d03n | 70 | | |
| d04p | 72 | | |
| d04n | 73 | | |
| d05p | 77 | | |
| d05n | 78 | | |
| d06p | 80 | | |
| d06n | 81 | | |
| d07p | 83 | | |
| d07n | 84 | | |
| d08p | 86 | | |
| d08n | 87 | | |
| d09p | 89 | | |
| d09n | 90 | | |
| d10p | 92 | | |
| d10n | 93 | | |
| d11p | 95 | | |
| d11n | 96 | | |
| d12p | 98 | | |
| d12n | 99 | | |
| d13p | 3 | | |
| d13n | 4 | | |
| d14p | 6 | | |
| d14n | 7 | | |
| d15p | 9 | | |
| d15n | 10 | | |

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| Supply and Termination Voltages | | |
|---|---|---|
| **Name** | **Description** | **Pin Number** |
| vcc | Positive power supply (+3.3*V*) | 5, 8, 11, 14, 24, 25, 26, 29, 32, 35, 38, 41, 44, 47, 52, 55, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100 |
| vee | Negative power supply (GND or 0*V*) | 1, 15, 16, 17, 23, 30, 36, 37, 50, 51, 58, 75 |
| NC | Unconnected pin | 2, 12, 13, 19, 20, 21, 22, 31, 42, 43, 48, 49, 53, 54, 74 |

# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| vcc | +3.14 | +3.3 | +3.47 | *V* | ±5% |
| vee | | 0.0 | | *V* | |
| Power consumption | | 660 | | *mW* | |
| Junction temperature | -25 | 50 | 125 | *°C* | |
| **LS Input Data (d00p/d00n-d15p/d15n)** | | | | | |
| Data Rate | 0.0 | | 1063 | *Mbps* | |
| Differential Swing | 0.06 | | 0.8 | *V* | Peak-to-peak |
| CM Voltage Level | vee | | vcc | *V* | |
| **HS Input Clock (cep/cen)** | | | | | |
| Frequency | 0.0 | | 17 | *GHz* | |
| Swing (Diff or SE) | 0.2 | | 1.2 | *V* | Peak-to-peak |
| CM Voltage Level | vcc -0.8 | | vcc | *V* | |
| Duty Cycle | 40% | 50% | 60% | | |
| **HS Output Data (qcmlp/qcmln)** | | | | | |
| Data Rate | 0.0 | | 17 | *Gbps* | |
| Logic “1” level | | vcc | | *V* | |
| Logic “0” level | | vcc -0.6 | | *V* | |
| Jitter | | 12 | | *ps* | Peak-to-peak @12.5*Gb/s* |
| **HS Output Clock (chop/chon)** | | | | | |
| Frequency | 0.0 | | 17 | *GHz* | |
| Logic “1” level | | vcc | | *V* | |
| Logic “0” level | | vcc -0.6 | | *V* | |
| Jitter | | 6 | | *ps* | Peak-to-peak @12.5*GHz* |
| Duty Cycle | | 50% | | | |
| **LS Output Clock (clop/clon)** | | | | | |
| Frequency | 0.0 | | 1063 | *MHz* | |
| Interface | | LVDS | | | Meets the IEEE Std. |
| **CMOS Control Inputs** | | | | | |
| Logic “1” level | vcc -0.4 | | | *V* | |
| Logic “0” level | | | vee +0.4 | *V* | |

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# PACKAGE INFORMATION

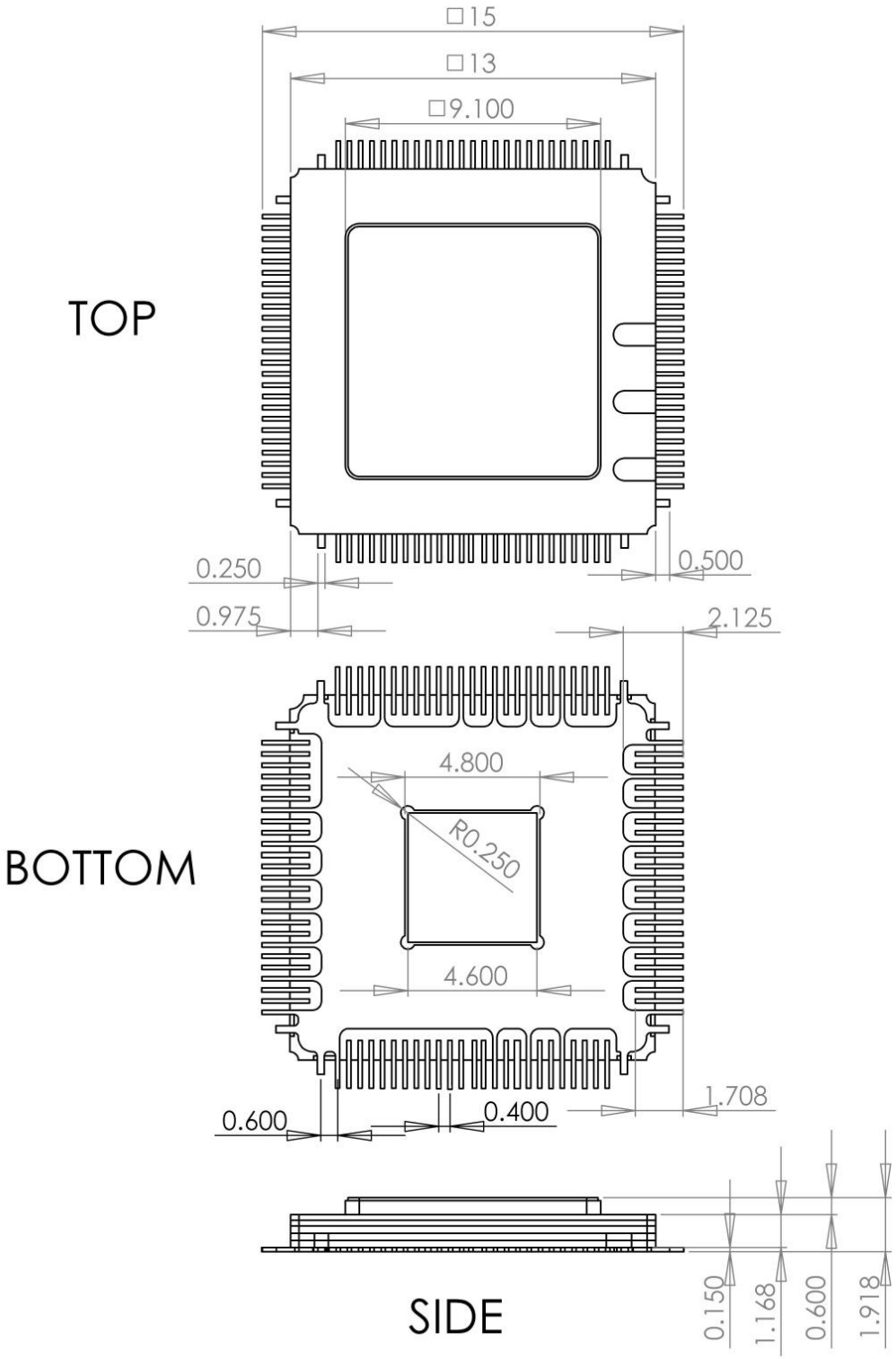


*Fig. 3. Package Drawing*

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The chip die is housed in a custom 100-pin CQFP package. The dimensioned drawings are shown in Fig. 3. The package's leads will be trimmed to a length of 1.0mm. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is power for a positive supply.

The part's identification label is ASNT1011A-KMA. The first 9 digits of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

# REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 2.3.2 | 01-2020 | Updated Package Information |
| 2.2.2 | 07-2019 | Letterhead Updated |
| 2.2.1 | 05-2015 | Corrected Absolute Maximum Ratings section<br>Revised Package Information section<br>Updated format |
| 2.1 | 02-2012 | Revised Description section<br>Revised Package Information section |
| 2.0 | 01-2012 | Revised Electrical Characteristics section<br>Revised Package Information section<br>Added Absolute Maximums Rating table<br>Added Pin Diagram |
| 1.0 | 01-2011 | First release |