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U\_A-Headers  
A-Headers.SchDoc



U\_Analog  
Analog.SchDoc



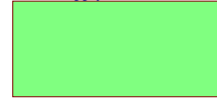
U\_DDR3-RAM  
DDR3-RAM.SchDoc



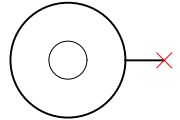
U\_USB-PHY  
USB-PHY.SchDoc



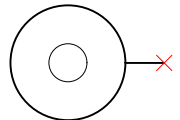
U\_PowerSupply  
PowerSupply.SchDoc



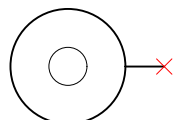
U\_FTDI  
FTDI.SchDoc



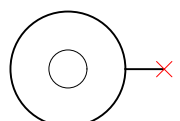
Mount.Hole 3.2mm (unplated)



Mount.Hole 3.2mm (unplated)



Mount.Hole 3.2mm (unplated)

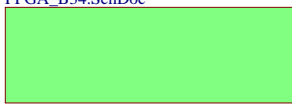


Mount.Hole 3.2mm (unplated)

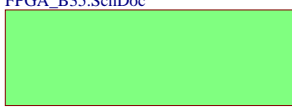
A

A

U\_FPGA\_B34  
FPGA\_B34.SchDoc



U\_FPGA\_B35  
FPGA\_B35.SchDoc



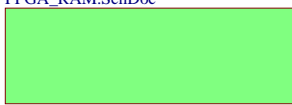
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B

U\_FPGA\_MIO  
FPGA\_MIO.SchDoc



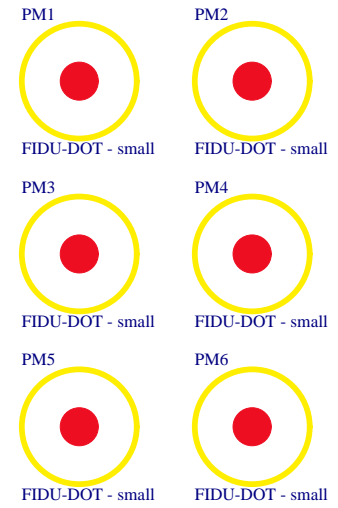
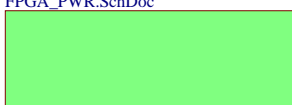
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FPGA\_RAM.SchDoc



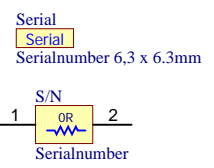
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C

U\_FPGA\_PWR  
FPGA\_PWR.SchDoc



LOGO1  
TE Logo PRINT Layer  
LOGO PRINT



Title: <b>TE0723</b>		
A4	Number: <b>TE0723 TE0723-M</b>	Rev. <b>03</b>
Date: <b>2016-07-15</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page1 of 13
Filename: <b>TE0723.SchDoc</b>		

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D

D

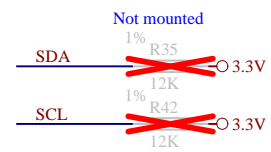
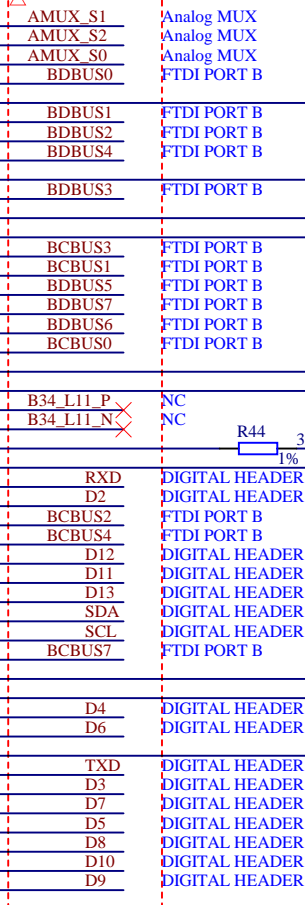
U1A

**BANK 34**

IO_L1P_T0_34	G11	AMUX_S1	Analog MUX
IO_L1N_T0_34	H12	AMUX_S2	Analog MUX
IO_L2P_T0_34	G12	AMUX_S0	Analog MUX
IO_L2N_T0_34	H13	BDBUS0	FTDI PORT B
IO_L3P_T0_DQS_PUDC_B_34	G14	BDBUS1	FTDI PORT B
IO_L3N_T0_DQS_34	J15	BDBUS2	FTDI PORT B
IO_L4P_T0_34	K15	BDBUS4	FTDI PORT B
IO_L4N_T0_34	J13		
IO_L5P_T0_34	J14	BDBUS3	FTDI PORT B
IO_L5N_T0_34	H11		
IO_L6P_T0_34	J11		
IO_L6N_T0_VREF_34	N13	BCBUS3	FTDI PORT B
IO_L7P_T1_34	N14	BCBUS1	FTDI PORT B
IO_L7N_T1_34	L15	BDBUS5	FTDI PORT B
IO_L8P_T1_34	M15	BDBUS7	FTDI PORT B
IO_L8N_T1_34	L14	BDBUS6	FTDI PORT B
IO_L9P_T1_DQS_34	M14	BCBUS0	FTDI PORT B
IO_L9N_T1_DQS_34	M14	BCBUS0	FTDI PORT B
IO_L10P_T1_34	K13		
IO_L10N_T1_34	L13		
IO_L11P_T1_SRCC_34	K11	B34_L11_P	NC
IO_L11N_T1_SRCC_34	K12	B34_L11_N	NC
IO_L12P_T1_MRCC_34	L12		
IO_L12N_T1_MRCC_34	M12		
IO_L13P_T2_MRCC_34	N11	RXD	DIGITAL HEADER
IO_L13N_T2_MRCC_34	N12	D2	DIGITAL HEADER
IO_L15P_T2_DQS_34	P15	BCBUS2	FTDI PORT B
IO_L15N_T2_DQS_34	R15	BCBUS4	FTDI PORT B
IO_L16P_T2_34	P11	D12	DIGITAL HEADER
IO_L16N_T2_34	R11	D11	DIGITAL HEADER
IO_L17P_T2_34	R12	D13	DIGITAL HEADER
IO_L17N_T2_34	R13	SDA	DIGITAL HEADER
IO_L18P_T2_34	P13	SCL	DIGITAL HEADER
IO_L18N_T2_34	P14	BCBUS7	FTDI PORT B
IO_L19P_T3_34	M9		
IO_L19N_T3_VREF_34	R7	D4	DIGITAL HEADER
IO_L20P_T3_34	R8	D6	DIGITAL HEADER
IO_L20N_T3_34	M10		
IO_L21P_T3_DQS_34	M11	TXD	DIGITAL HEADER
IO_L21N_T3_DQS_34	N7	D3	DIGITAL HEADER
IO_L22P_T3_34	N8	D7	DIGITAL HEADER
IO_L22N_T3_34	P8	D5	DIGITAL HEADER
IO_L23P_T3_34	P9	D8	DIGITAL HEADER
IO_L23N_T3_34	P10	D10	DIGITAL HEADER
IO_L24P_T3_34	R10	D9	DIGITAL HEADER
IO_L24N_T3_34	R10	D9	DIGITAL HEADER

XC7Z010-1CLG225C

B34



Title: TE0723 - FPGA B34		
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Filename: FPGA_B34.SchDoc		

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A

A

B

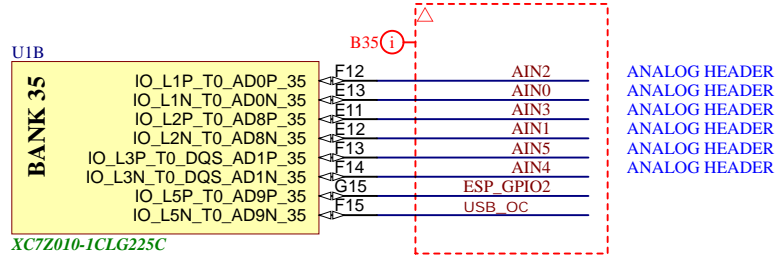
B


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C

D

D



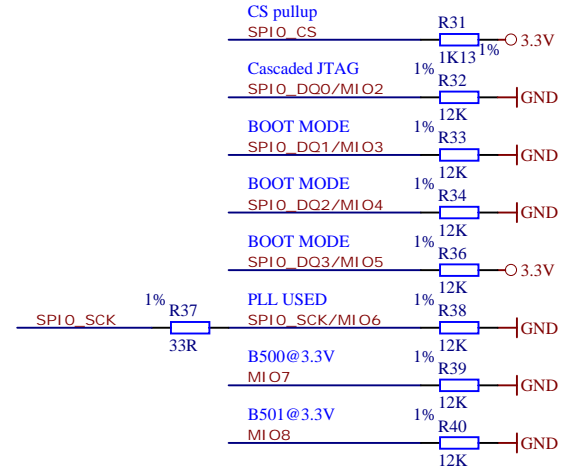
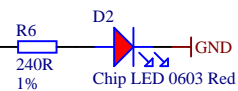
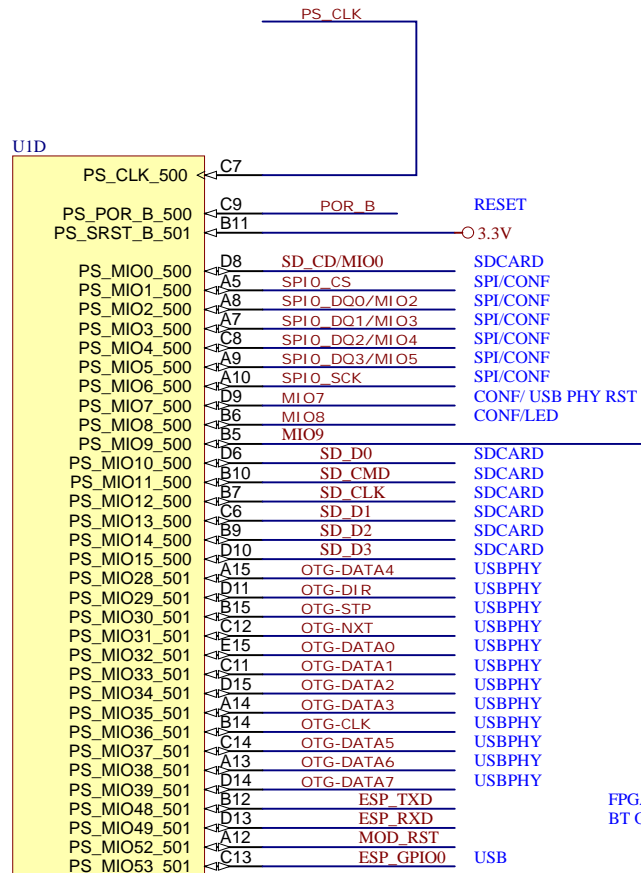
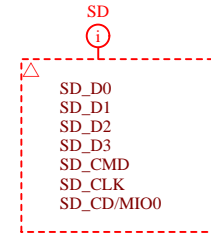
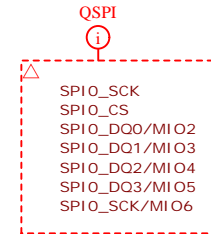
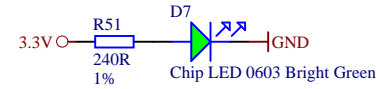
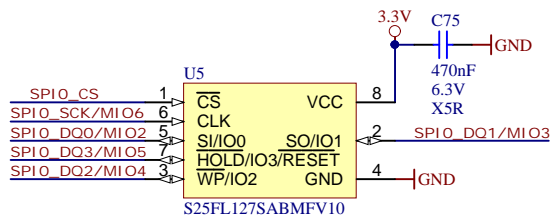
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	A4	Number: <b>TE0723 TE0723-M</b>	Rev. <b>03</b>
	Date: <b>2016-07-15</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>3</b> of <b>13</b>
	Filename: <b>FPGA_B35.SchDoc</b>		

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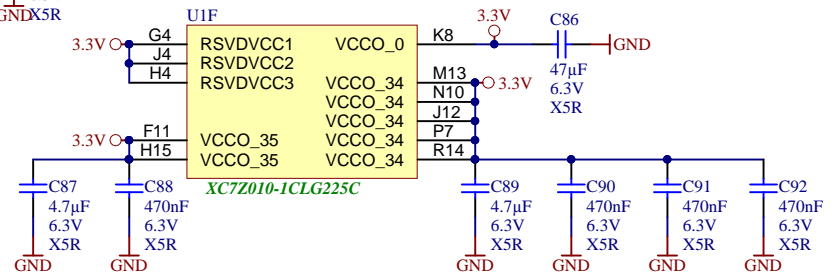
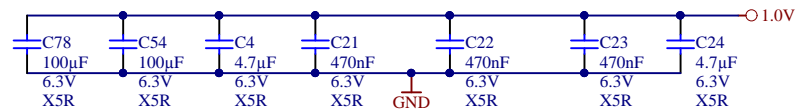
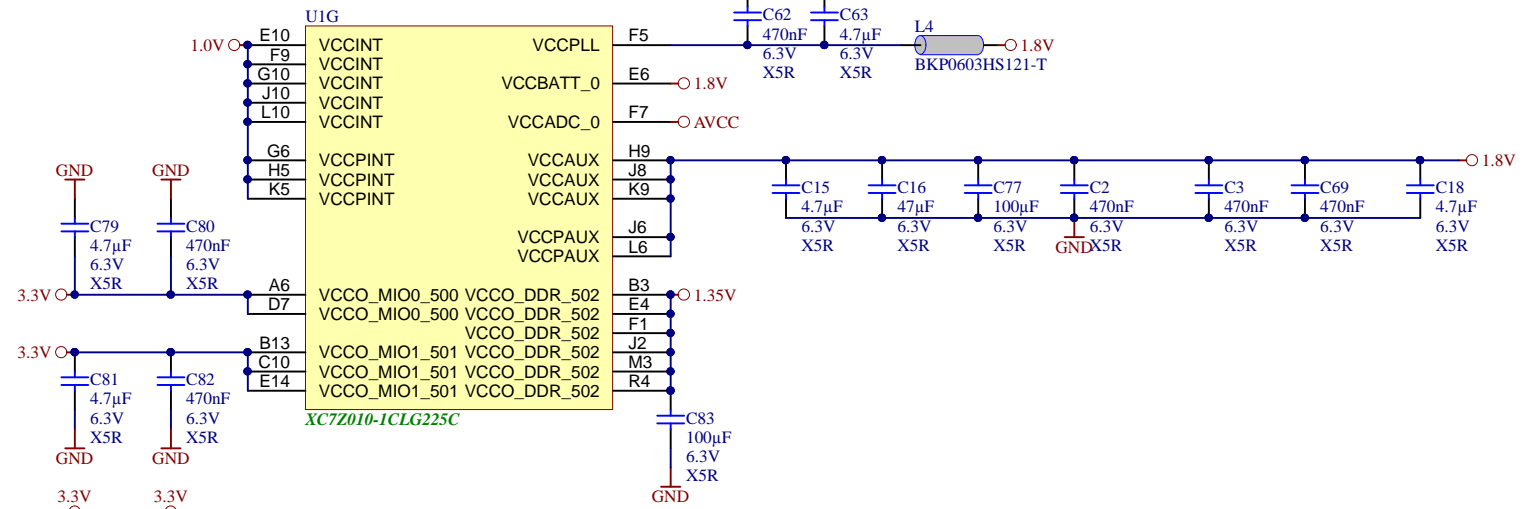
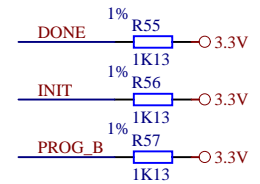
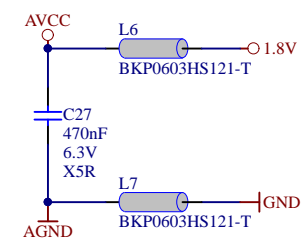
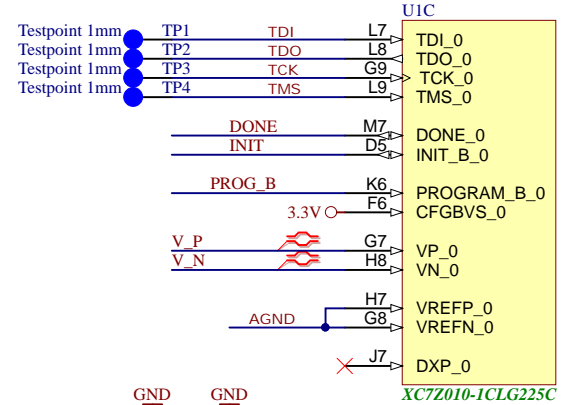
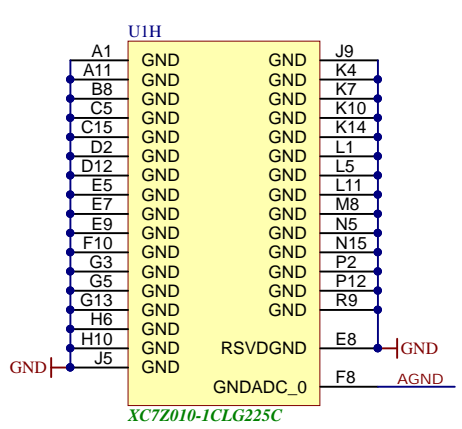


FPGA OUT -> BT IN  
BT OUT -> FPGA IN

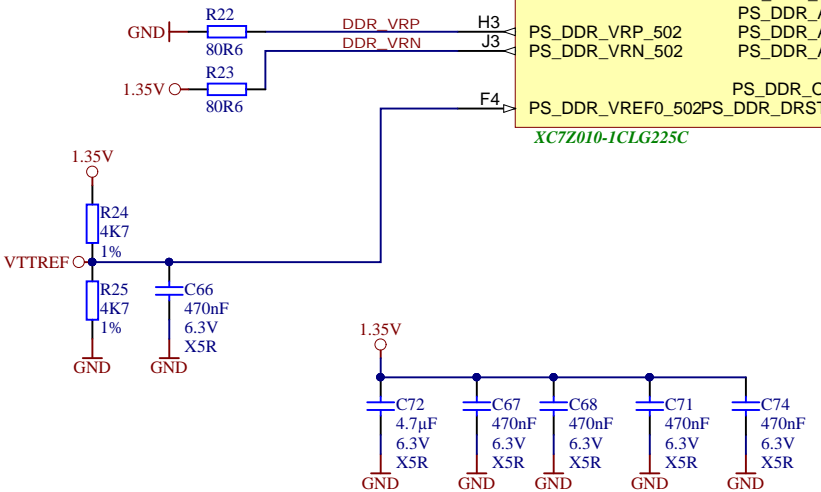
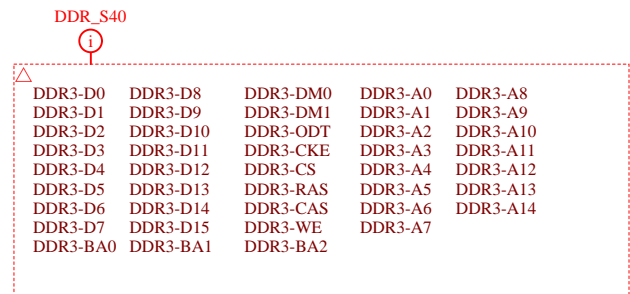
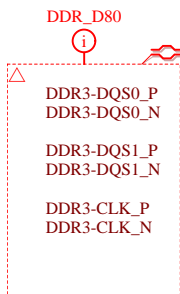
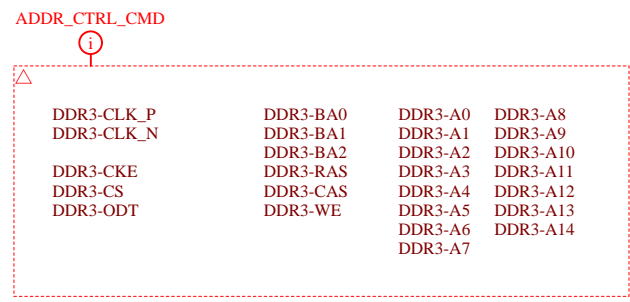
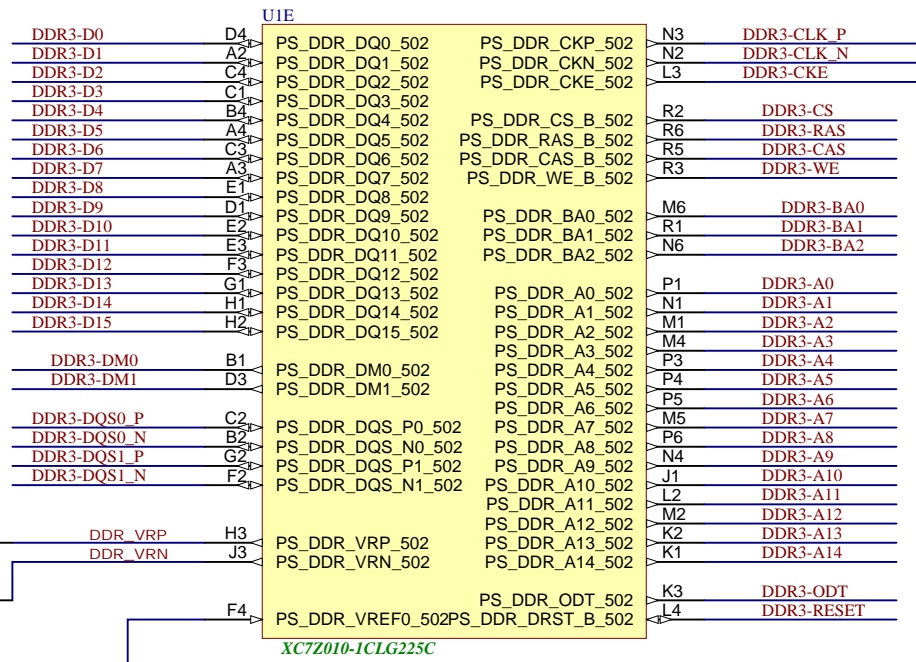


Title: TE0723 - FPGA MIO		
A4	Number: TE0723 TE0723-M	Rev. 03
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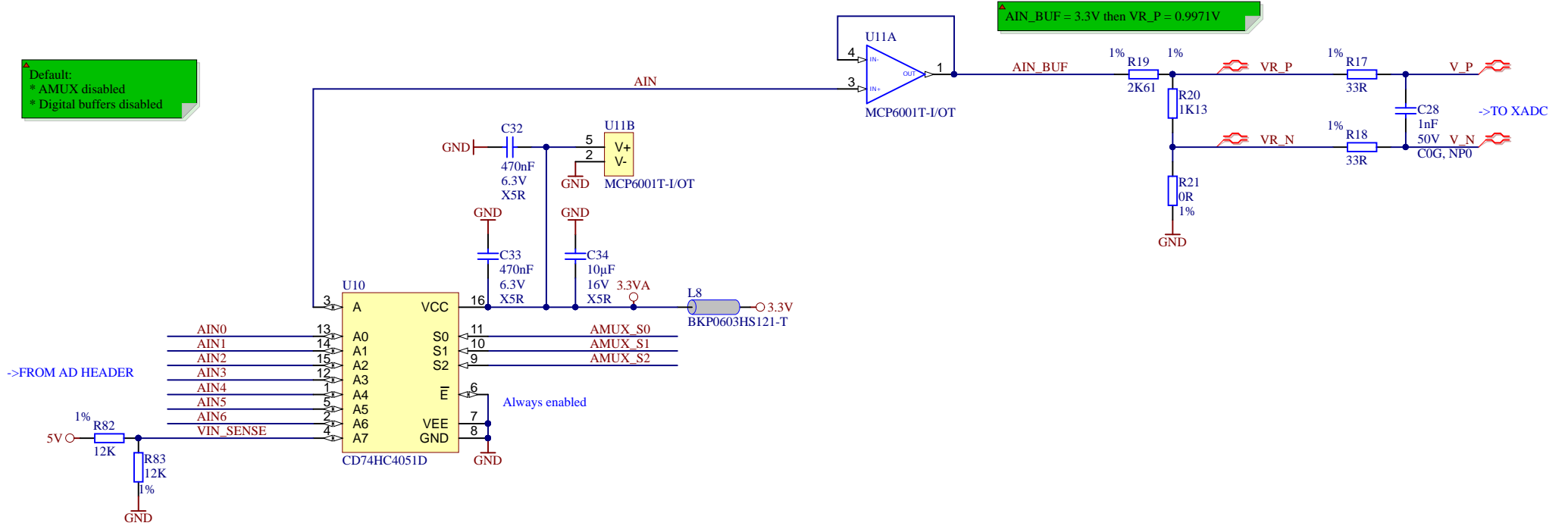
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A4	Number: TE0723 TE0723-M	Rev. 03
Date: 2016-07-15	Copyright: Trenz Electronic GmbH	Page5 of 13
Filename: FPGA_PWR.SchDoc		




		Title: TE0723 - FPGA RAM	
		A4 Number: TE0723 TE0723-M	Rev. 03
Date: 2016-07-15		Copyright: Trenz Electronic GmbH	
Filename: FPGA_RAM.SchDoc		Page 6 of 13	

Default:  
 \* AMUX disabled  
 \* Digital buffers disabled

AIN\_BUF = 3.3V then VR\_P = 0.9971V



	Title: TE0723 - Analog Input		
	A4	Number: TE0723 TE0723-M	Rev. 03
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	Filename: Analog.SchDoc		

A

A

B

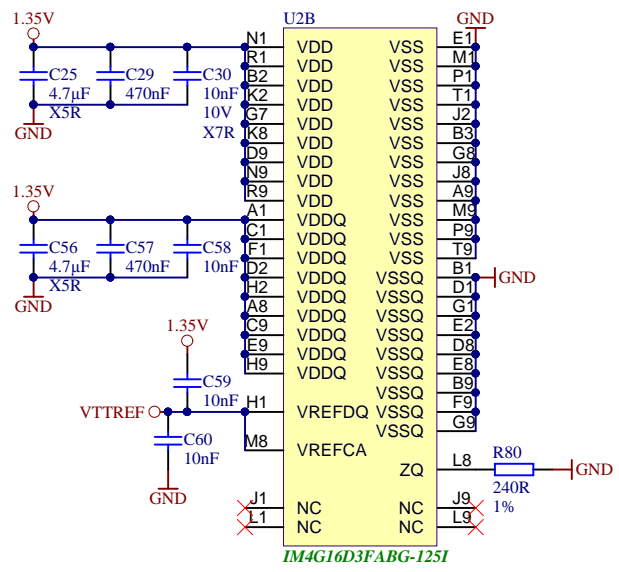
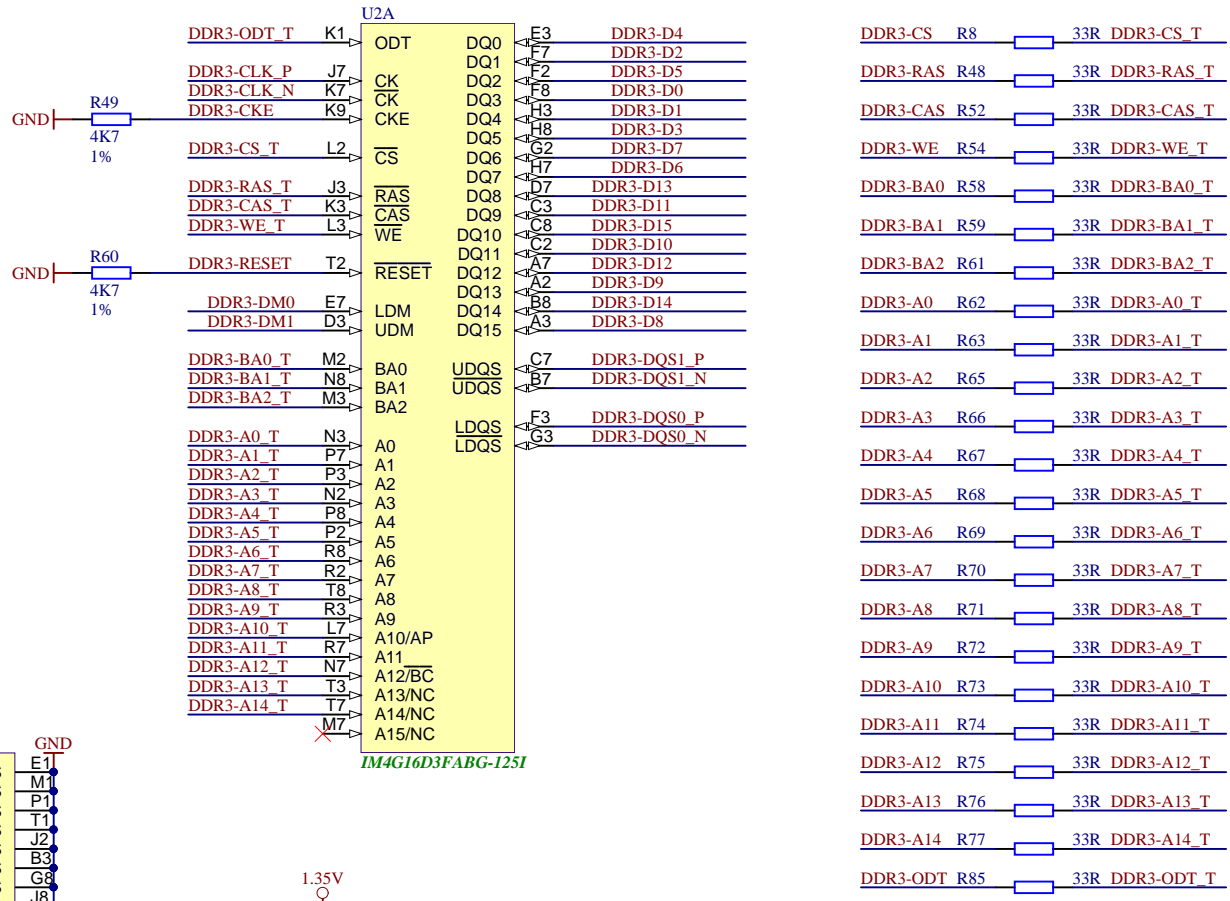
B

C

C

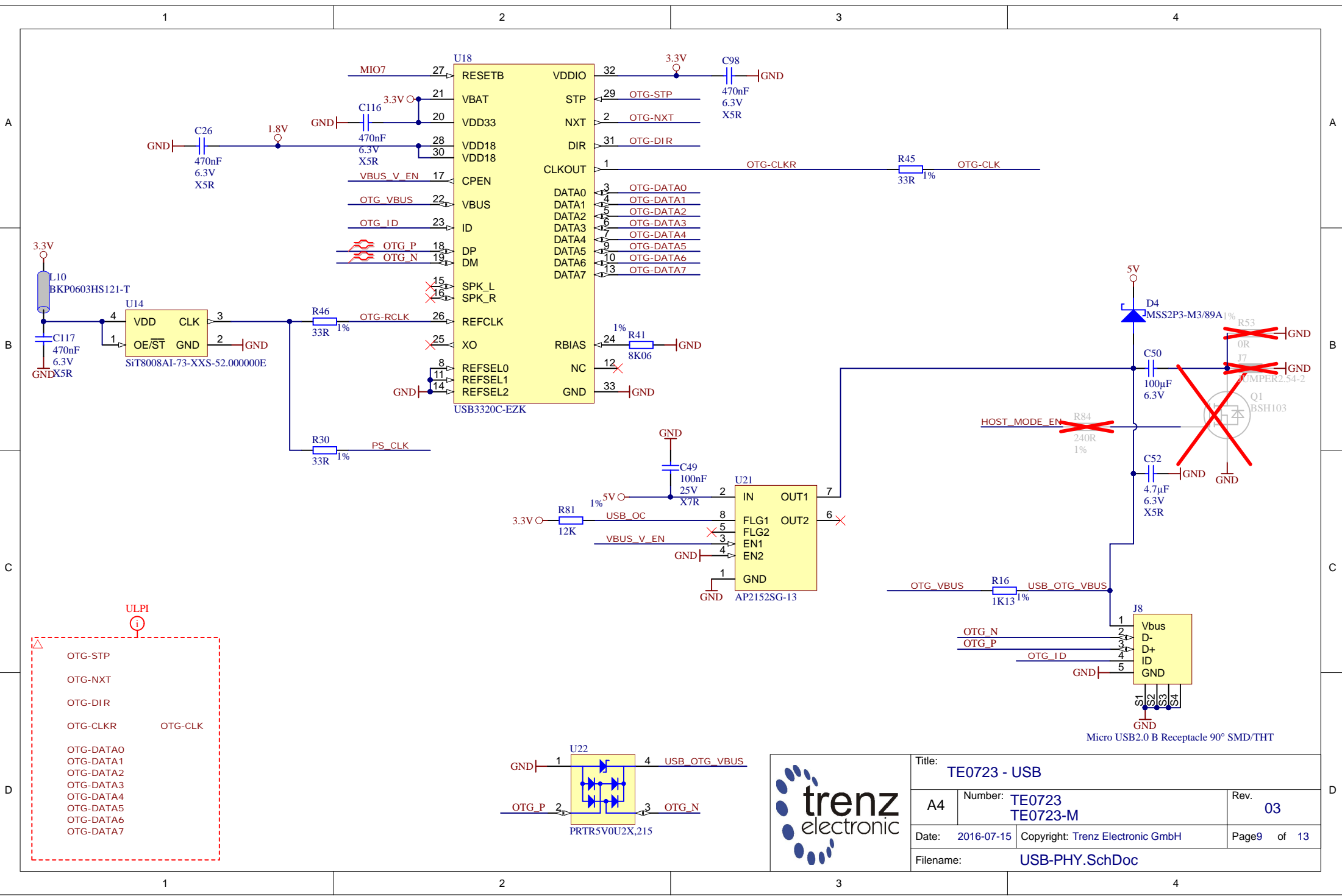
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D

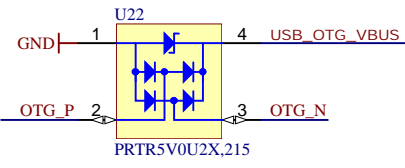


Title: TE0723 - DDR Memory		
A4	Number: TE0723 TE0723-M	Rev. 03
Date: 2016-07-15	Copyright: Trenz Electronic GmbH	Page 8 of 13
Filename: DDR3-RAM.SchDoc		





- ULPI
- OTG-STP
  - OTG-NXT
  - OTG-DIR
  - OTG-CLKR      OTG-CLK
  - OTG-DATA0
  - OTG-DATA1
  - OTG-DATA2
  - OTG-DATA3
  - OTG-DATA4
  - OTG-DATA5
  - OTG-DATA6
  - OTG-DATA7



Title: <b>TE0723 - USB</b>		
A4	Number: <b>TE0723 TE0723-M</b>	Rev. <b>03</b>
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Filename: <b>USB-PHY.SchDoc</b>		

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A

A

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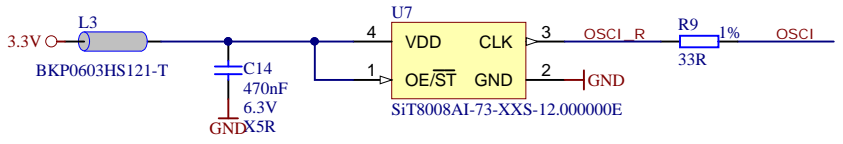
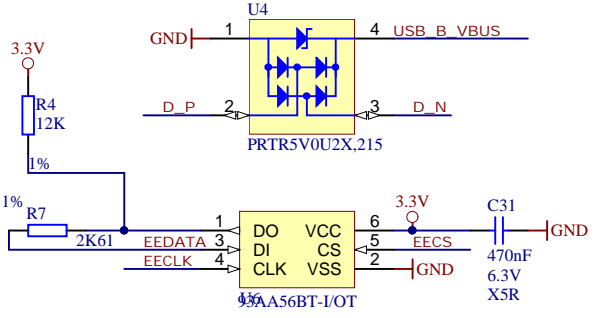
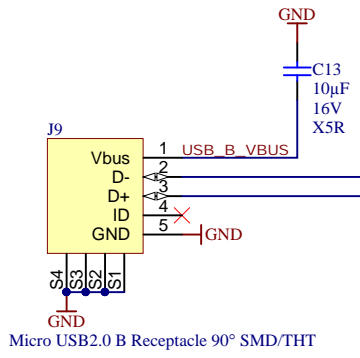
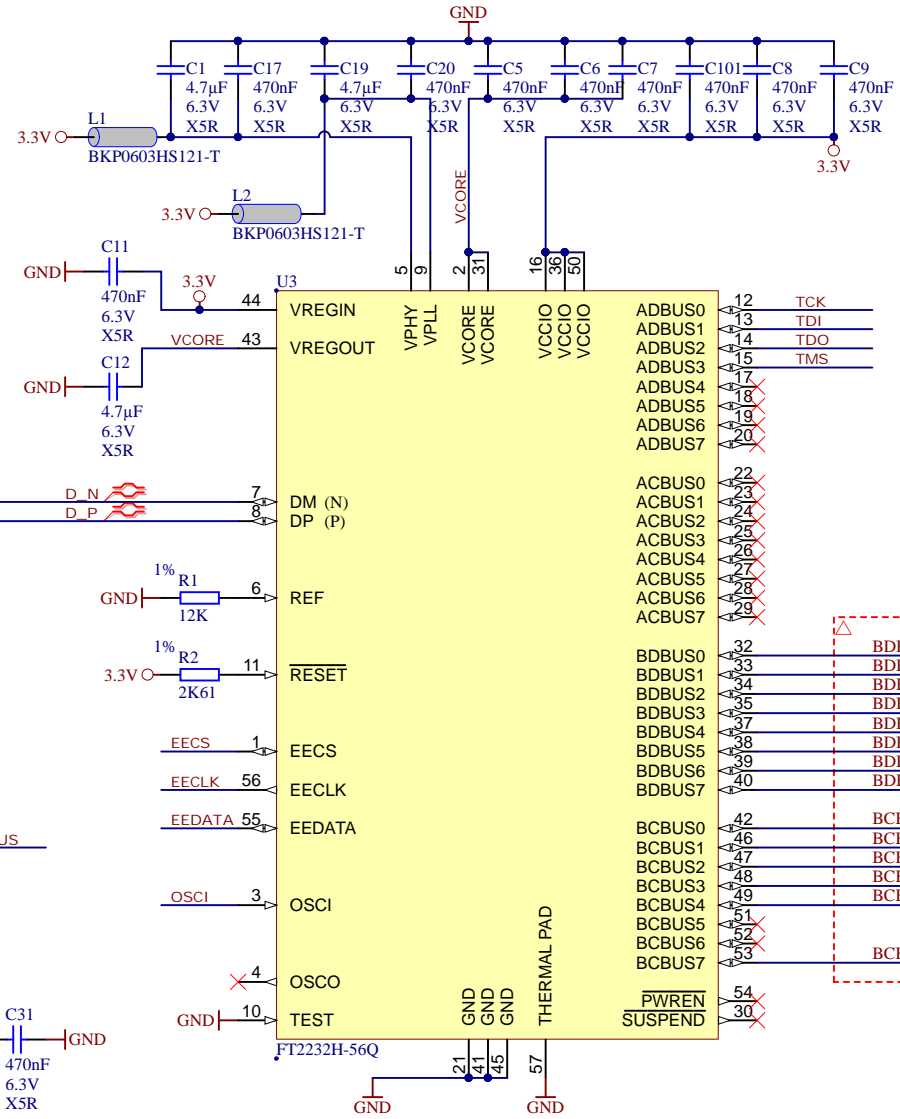
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D



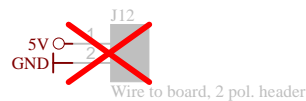
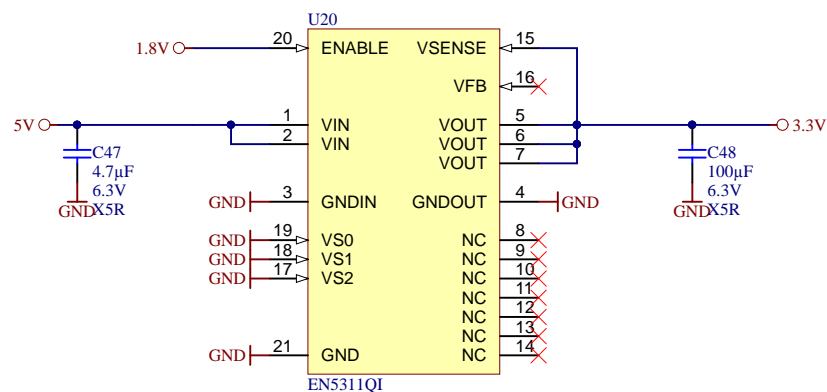
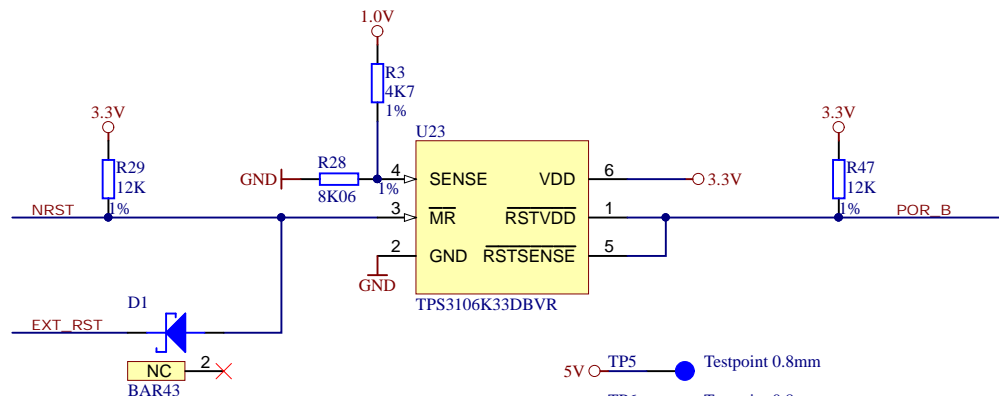
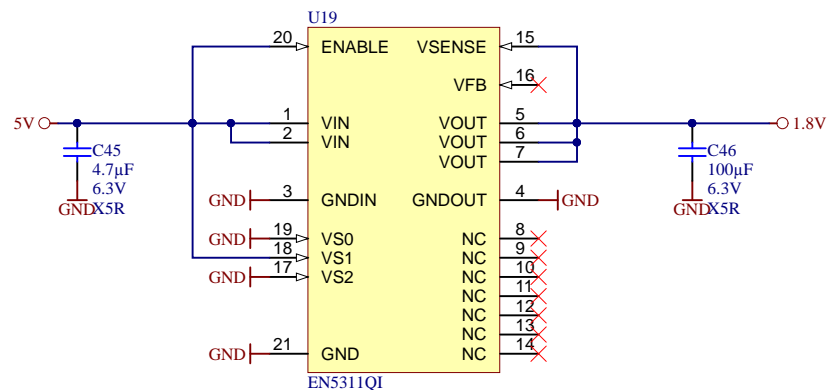
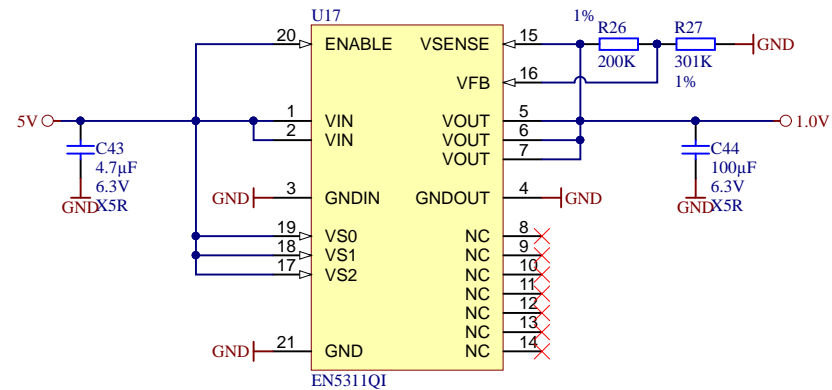
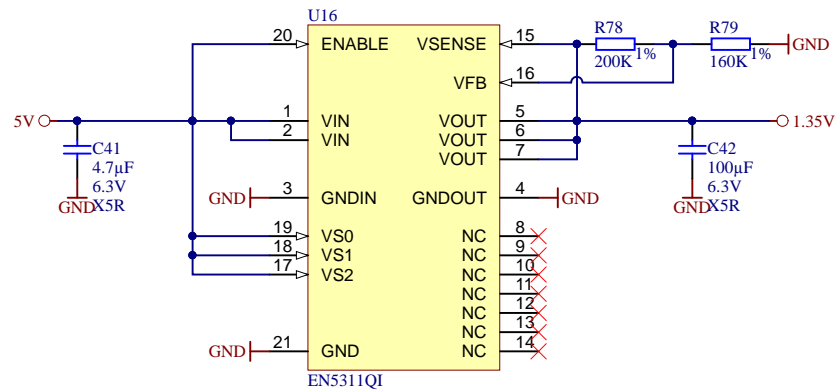
Title: TE0723 - FTDI		
A4	Number: TE0723 TE0723-M	Rev. 03
Date: 2016-07-15	Copyright: Trenz Electronic GmbH	Page 10 of 13
Filename: FTDI.SchDoc		

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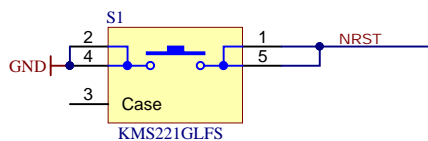
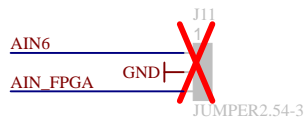
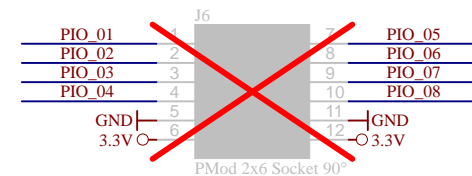
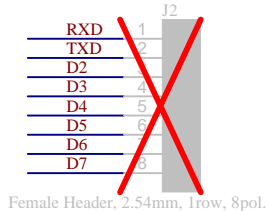
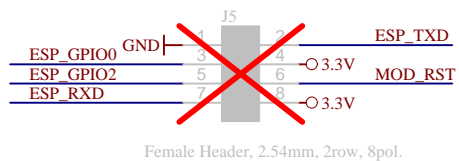
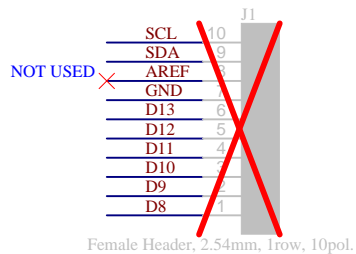
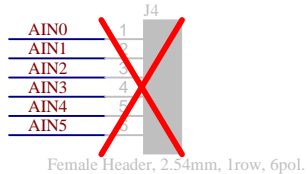
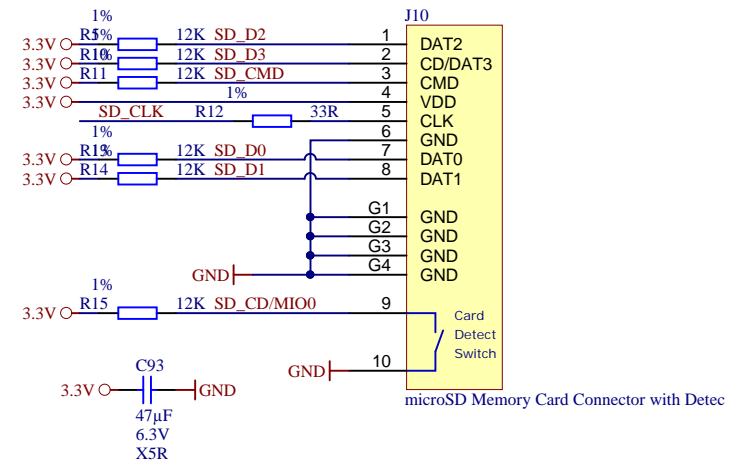
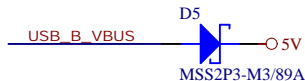
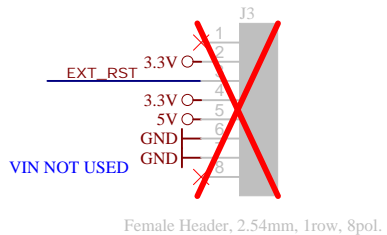
4



- 5V ○ TP5 ● Testpoint 0.8mm
- 3.3V ○ TP6 ● Testpoint 0.8mm
- 1.8V ○ TP7 ● Testpoint 0.8mm
- 1.35V ○ TP8 ● Testpoint 0.8mm
- 1.0V ○ TP9 ● Testpoint 0.8mm
- GND | TP10 ● Testpoint 0.8mm
- GND | TP11 ● Testpoint 0.8mm
- GND | TP12 ● Testpoint 0.8mm
- GND | TP13 ● Testpoint 0.8mm



Title: TE0723 - PowerSupply		
A4	Number: TE0723 TE0723-M	Rev. 03
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Title: TE0723 - Connectors		
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CHANGES REV02 to REV03

- 1) changed FTDI-chip on 56pins package
- 2) changed micro-USB connectors
- 3) optimized BOM
- 4) update footprints, full update lib
- 5) added serial number (traceability pad)

A

A

B

B

C

C

D

D



Title: <b>TE0723 - Changes list</b>		
A4	Number: <b>TE0723</b> <b>TE0723-M</b>	Rev. <b>03</b>
Date: <b>2016-07-15</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>13</b> of <b>13</b>
Filename: <b>Revision_Changes.SchDoc</b>		

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