200730830-Si5397/96 Datasheet with 7x7 Substrate and Reduce Max Jitter Spec

PCN Issue Date: 7/30/2020 **Effective Date:** 11/5/2020

PCN Type: Datasheet

Description of Change

Silicon Labs is announcing an update to the Si5397/96 datasheet to revision 1.1. Changes include
1. The substrate for the Si5396 7x7 LGA package
2. The maximum Phase Jitter specification is reduced from 140 fs to 125 fs.
Please see change reason for additional details.

Reason for Change

The single center pad on the 7x7 mm 44-LGA Package is divided by soldermask into nine pads (3x3 grid array) to increase mechanical support to the center of the package. Reduced maximum Phase jitter spec from 140 fs to 125 fs based on additional characterization data

Impact on Form, Fit, Function, Quality, Reliability

A review of the SMT stencil apertures on all designs that use Si539xJ/K/L/M/E-grade devices in 44-pin
LGA packages must be performed by customers. The stencil design will need to match the respective ground pads as shown in the Package outline. The stencil aperture to land pad size recommendation is 70% paste coverage.

Product Identification

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Existing Part #
SI5396A-A-GM
SI5396J-A-GM
SI5397A-A10084-GM
SI5397A-A-GM
SI5397B-A-GM
SI5397B-A-GMR
SI5397C-A-GM
SI5397J-A11023-GM
SI5397J-A-GM
SI5397K-A-GM
SI5397L-A-GM
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Last Date of Unchanged Product: 11/5/2020

Qualification Samples

Available upon request

Customer Response

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change, Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.

Customers may approve early PCN acceptance by emailing approval, along with PCN # to PCNEarlyAcceptance@silabs.com

User Registration

Register today to create your account on Silabs.com. Your personalized profile allows you to receive technical document updates, new product announcements, “how-to” and design documents, product change notices (PCN) and other valuable content available only to registered users. **http://www.silabs.com/profile**

Qualification Data

See attached

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Si5371/72/92/94/96 Embedded Crystal Qualification Report

Part Rev A, TSMC Fabrication, ASECL Assembly except as noted

Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group A – Accelerated Environment Stress Tests							
HAST	JA110		Q043892	0/26	1, 2		
	110°C, 85%RH	3 lots, N=>25	Q043273	0/26	1, 2	3 lots	Pass
	Vcc=3.63V, 264 hours		Q043331	0/26	1, 2	0/78	
Temp Cycle	JA104		Q046294	0/25	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q046295	0/25	1	3 lots	Pass
	500 cycles		Q046296	0/25	1	0/75	
HTSL	JA103		Q043889	0/26	1, 2		
	150°C, 1000hr	3 lots, N=>25	Q043111	0/26	1, 2	3 lots	Pass
			Q043332	0/26	1, 2	0/78	
Test Group B – Accelerated Lifetime Simulation Tests							
HTOL	JA108		Q041587	0/79	3, 4		
	T_J ≥ 125°C, Dynamic	3 lots, N=>77	Q037081	0/80	3, 4	3 lots	Pass
	Vcc=3.63V, 1000 hours		Q038677	0/80	3, 4	0/239	
LTOL	JA108						
	T_A = -10°C, Dynamic	1 lot, N=>32	Q035769	0/34	3	1 lots	Pass
	Vcc=3.63V, 1000 hours					0/34	
ELFR	JA108		Q041720	0/356	3		
	T_J ≥ 125°C, Dynamic	3 lots, N=>500	Q041819	0/66	3	5 lots	Pass
	Vcc=3.63V, 48 hours		Q037086	0/504	3		
			Q037468	0/514	3		
			Q037808	0/504	3	0/1944	
Test Group C – Package Assembly Integrity Tests							
Mechanical Shock	JESD22-B104		Q043090	0/40	2		
	Cond. B (1500g)	3 lots, N=>39	Q043292	0/40	2	3 lots	Pass
			Q043461	0/40	2	0/120	
Variable Vibration Frequency	JESD22-B103		Q043105	0/40	2		
	Service Cond. 1 (20g)	3 lots, N=>39	Q043350	0/40	2	3 lots	Pass
			Q043511	0/40	2	0/120	
Constant Acceleration	MIL-STD-883		Q043125	0/40	2		
	Method 2001.3	3 lots, N=>39	Q043385	0/40	2	3 lots	Pass
	Cond. B (10000g)		Q043556	0/40	2	0/120	

Prepared on: 28-Jul-2020 by N. Arguello

Si5371/72/92/94/96 Embedded Crystal Qualification Report

Part Rev A, TSMC Fabrication, ASECL Assembly except as noted							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group E – Electrical Verification							
ESD-HBM	JS-001	1 lot, N=>3	Q041588		3	3 kV	Class 2
ESD-CDM	JESD22-C101	1 lot, N=>3	Q043902			1000 V	Class IV
Latch Up	JESD78 ±100mA Overvoltage = 5.1975V	1 lot, N=>3	Q041590	85 °C	3		Pass

Notes:
1. Parts are Pre-conditioned at MSL3/260°C
2. Leveraged package family qualification data
3. Leveraged die family qualification data
4. Lot stressed to 2,000 hours

This report applies to the following part numbers:				
Si5371J-A-GM/R	Si5371J-Axxxxx-GM/R	Si5372J-A-GM/R	Si5372J-Axxxxx-GM/R	Si5392E-A-GM/R
Si5392E-Axxxxx-GM/R	Si5392J-A-GM/R	Si5392J-Axxxxx-GM/R	Si5392K-A-GM/R	Si5392K-Axxxxx-GM/R
Si5392L-A-GM/R	Si5392L-Axxxxx-GM/R	Si5392M-A-GM/R	Si5392M-Axxxxx-GM/R	Si5394E-A-GM/R
Si5394E-Axxxxx-GM/R	Si5394J-A-GM/R	Si5394J-Axxxxx-GM/R	Si5394K-A-GM/R	Si5394K-Axxxxx-GM/R
Si5394L-A-GM/R	Si5394L-Axxxxx-GM/R	Si5394M-A-GM/R	Si5394M-Axxxxx-GM/R	Si5396J-A-GM/R
Si5396J-Axxxxx-GM/R	Si5396K-A-GM/R	Si5396K-Axxxxx-GM/R		

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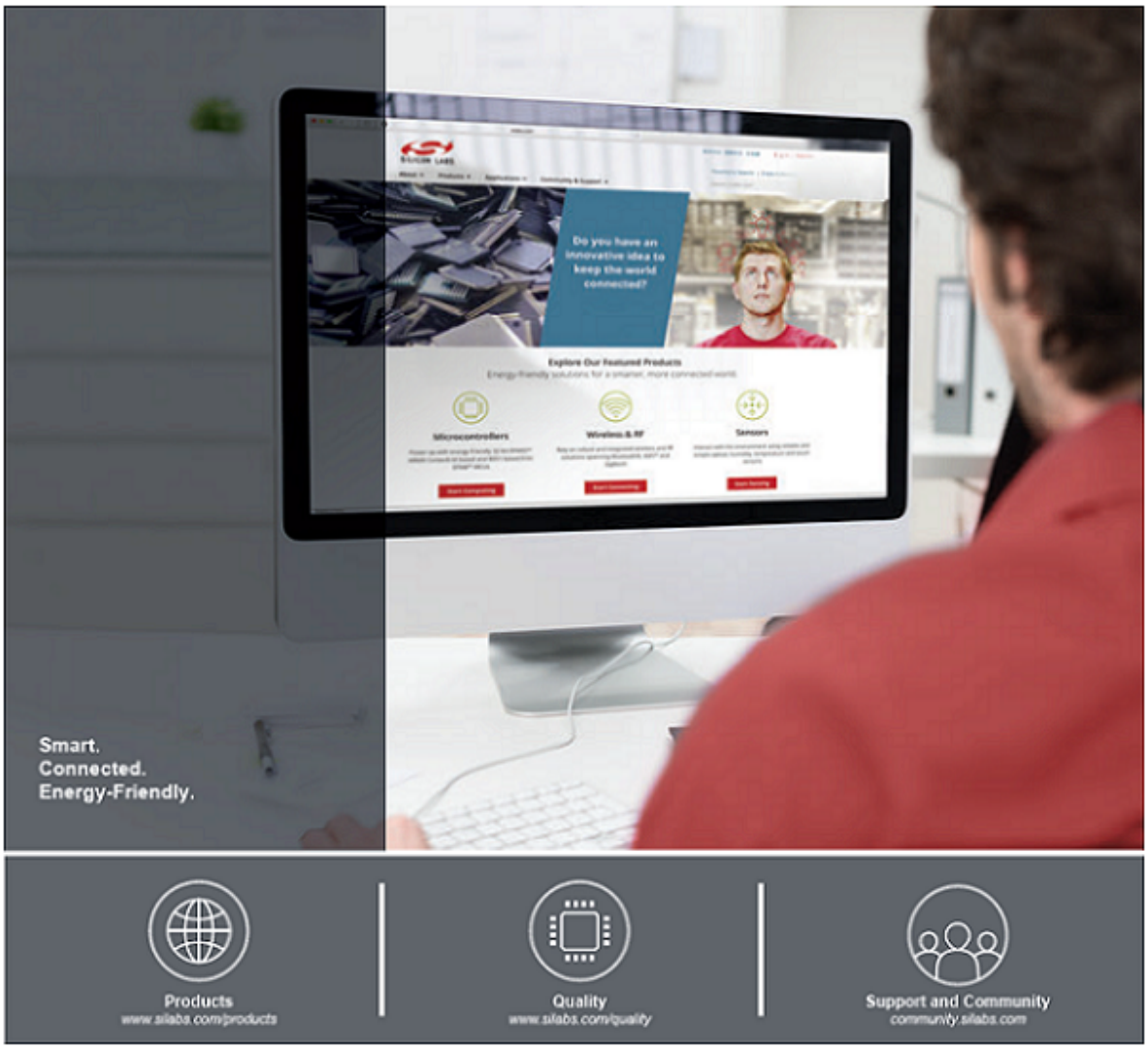

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