MIXED SIGNAL MICROCONTROLLER

FEATURES

- **Low Supply Voltage Range 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption**
  - **Active Mode: 220 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.5 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Five Power-Saving Modes**
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%**
  - **Internal Very Low-Power Low-Frequency Oscillator**
  - **32-kHz Crystal** (1)
  - **External Digital Clock Source**
- **16-Bit Timer_A With Two Capture/Compare Registers**
- **16-Bit Sigma-Delta A/D Converter With Differential PGA Inputs and Internal Reference** (2)
- **Universal Serial Interface (USI) Supporting SPI and I2C**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **On-Chip Emulation Logic With Spy-Bi-Wire Interface**
- **2KB + 256B Flash Memory; 128B RAM**
- **Available in a 16-Pin QFN Package**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extended (–40°C/125°C) Temperature Range** (3)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Crystal oscillator cannot be operated beyond 105°C.
(2) ADC performance characterized up to 105°C only.
(3) Custom temperature ranges available

DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

The MSP430F2013 is an ultra-low-power mixed signal microcontroller with a built-in 16-bit timer and ten I/O pins. In addition, the MSP430F2013 has a built-in communication capability using synchronous protocols (SPI or I2C) and a 16-bit sigma-delta A/D converter.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand alone RF sensor front end is another area of application.

Table 1. ORDERING INFORMATION(1)

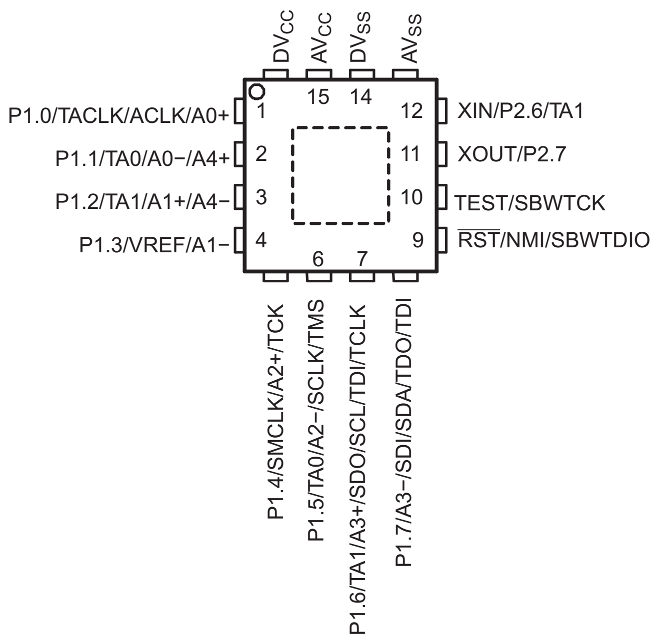
T_A	PACKAGE(2)	ORDERABLE PART NUMBER	VID NUMBER
-40°C to 125°C	QFN (RSA)	MSP430F2013QRSATEP	V62/11613-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

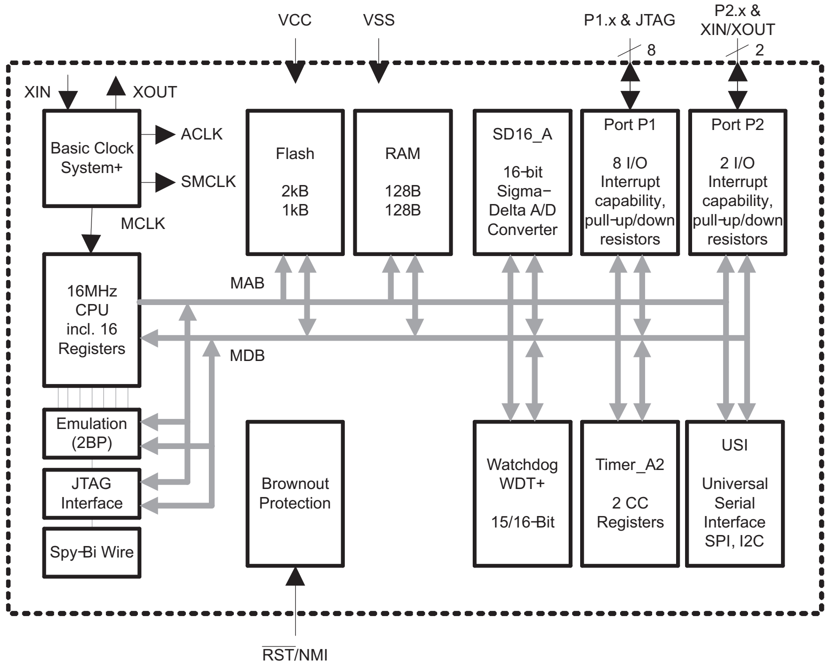
Device Pinout

See port schematics section for detailed I/O information.

RSA PACKAGE
(TOP VIEW)



Functional Block Diagram



NOTE: See port schematics section for detailed I/O information.

Table 2. Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
P1.0/TACLK/ACLK/A0+	1	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal output SD16_A positive analog input A0
P1.1/TA0/A0-/A4+	2	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output SD16_A negative analog input A0 SD16_A positive analog input A4
P1.2/TA1/A1+/A4-	3	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output SD16_A positive analog input A1 SD16_A negative analog input A4
P1.3/VREF/A1-	4	I/O	General-purpose digital I/O pin Input for an external reference voltage/internal reference voltage output (can be used as mid-voltage) SD16_A negative analog input A1
P1.4/SMCLK/A2+/TCK	5	I/O	General-purpose digital I/O pin SMCLK signal output SD16_A positive analog input A2 JTAG test clock, input terminal for device programming and test
P1.5/TA0/A2-/SCLK/TMS	6	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output SD16_A negative analog input A2 USI: external clock input in SPI or I2C mode; clock output in SPI mode JTAG test mode select, input terminal for device programming and test
P1.6/TA1/A3+/SDO/SCL/ TDI/TCLK	7	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1B input, compare: Out1 output SD16_A positive analog input A3 USI: Data output in SPI mode; I2C clock in I2C mode JTAG test data input or test clock input during programming and test
P1.7/A3-/SDI/SDA/ TDO/TDI [1]	8	I/O	General-purpose digital I/O pin SD16_A negative analog input A3 USI: Data input in SPI mode; I2C data in I2C mode JTAG test data output terminal or test data input during programming and test
XIN/P2.6/TA1	12	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer_A, compare: Out1 output
XOUT/P2.7	11	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin [2]
$\overline{\text{RST}}$/NMI/SBWTDIO	9	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	10	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DV_{CC}	16		Digital supply voltage
AV_{CC}	15		Analog supply voltage
DV_{SS}	14		Digital ground reference
AV_{SS}	13		Analog ground reference
QFN Pad	Pad	NA	QFN package pad. Connection to VSS is recommended.

(1) TDO or TDI is selected via JTAG instruction.
(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

SHORT-FORM DESCRIPTION

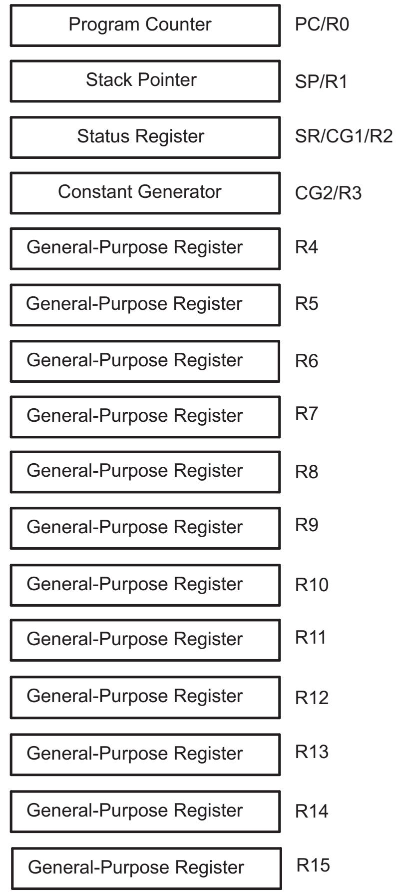
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

Table 3. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 4. Address Mode Descriptions

ADDRESS MODE	S (1)	D (1)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 --> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) --> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2--> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed) the CPU goes into LPM4 immediately after power-up.

Table 5. Interrupt Sources

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Timer+ Flash key violation PC out-of-range (1)	PORIFG RSTIFG WDTIFG KEYV See (2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (2)(3)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	30
			0FFFAh	29
			0FFF8h	28
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer_A2	TACCR0 CCIFG (4)	maskable	0FFF2h	25
Timer_A2	TACCR1 CCIFG.TAIFG (2)(4)	maskable	0FFF0h	24
			0FFEEh	23
			0FFECh	22
SD16_A	SD16CCTL0 SD16OVIFG, SD16CCTL0 SD16IFG (2)(4)	maskable		
USI	USIIFG, USISTTIFG (2)(4)	maskable	0FFE8h	20
I/O Port P2 (two flags)	P2IFG.6 to P2IFG.7 (2)(4)	maskable	0FFE6h	19
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (5)			0FFDEh to 0FFC0h	15 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
	(shaded)	SFR bit is not present in device.

Table 6. Interrupt Enable Register 1 and 2

Address	7	6	5	4	3	2	1	0
00h			**ACCVIE**	**NMIIE**			**OFIE**	**WDTIE**
			rw-0	rw-0			rw-0	rw-0

WDTIE Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE Oscillator fault interrupt enable

NMIIE (Non)maskable interrupt enable

ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h								

Table 7. Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				**NMIIFG**	**RSTIFG**	**PORIFG**	**OFIFG**	**WDTIFG**
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault.

PORIFG Power-On Reset interrupt flag. Set on V_{CC} power-up.

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.

NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h								

Memory Organization

Table 8. Memory Organization

		MSP430F200x	MSP430F201x
Memory Main: interrupt vector Main: code memory	Size Flash Flash	1KB Flash 0FFFFh-0FFC0h 0FFFFh-0FC00h	2KB Flash 0FFFFh-0FFC0h 0FFFFh-0F800h
Information memory	Size Flash	256 Byte 010FFh - 01000h	256 Byte 010FFh - 01000h
RAM	Size	128 Byte 027Fh - 0200h	128 Byte 027Fh - 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh - 0100h 0FFh - 010h 0Fh - 00h	01FFh - 0100h 0FFh - 010h 0Fh - 00h

Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430F2xx Family User's Guide.*

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally-controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

Table 9. DCO Calibration Data (Provided From Factory in Flash Information Memory Segment A)

DCO FREQUENCY	CALIBRATION REGISTER	SIZE	ADDRESS
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh
8 MHz	CALBC1_8MHZ	byte	010FDh
	CALDCO_8MHZ	byte	010FCh
12 MHz	CALBC1_12MHZ	byte	010FBh
	CALDCO_12MHZ	byte	010FAh
16 MHz	CALBC1_16MHZ	byte	010F9h
	CALDCO_16MHZ	byte	010F8h

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There is one 8-bit I/O port implemented—port P1—and two bits of I/O port P2:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and the two bits of port P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

Watchdog Timer (WDT+)

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A2

Timer_A2 is a 16-bit timer/counter with two capture/compare registers. Timer_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 10. Timer_A2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PW, N	RSA					PW, N	RSA
2 - P1.0	1 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
2 - P1.0	1 - P1.0	TACLK	INCLK				
3 - P1.1	2 - P1.1	TA0	CCI0A	CCR0	TA0	3 - P1.1	2 - P1.1
7 - P1.5	6 - P1.5	ACLK (internal)	CCI0B			7 - P1.5	6 - P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
4 - P1.2	3 - P1.2	TA1	CCI1A	CCR1	TA1	4 - P1.2	3 - P1.2
8 - P1.6	7 - P1.6	TA1	CCI1B			8 - P1.6	7 - P1.6
		V_{SS}	GND			13 - P2.6	12 - P2.6
		V_{CC}	V_{CC}				

USI

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

SD16_A

The SD16_A module supports 16-bit analog-to-digital conversions. The module implements a 16-bit sigma-delta core and reference generator. In addition to external analog inputs, internal V_{CC} sense and temperature sensors are also available.

Peripheral File Map

Table 11. Peripherals With Word Access

SD16_A	General Control	SD16CTL	0100h
	Channel 0 Control	SD16CCTL0	0102h
	Interrupt vector word register	SD16IV	0110h
	Channel 0 conversion memory	SD16MEM0	0112h
Timer_A	Capture/compare register	TACCR1	0174h
	Capture/compare register	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control	TACCTL1	0164h
	Capture/compare control	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

Table 12. Peripherals With Byte Access

SD16_A	Channel 0 Input Control	SD16INCTL0	0B0h
	Analog Enable	SD16AE	0B7h
USI	USI control 0	USICTL0	078h
	USI control 1	USICTL1	079h
	USI clock control	USICKCTL	07Ah
	USI bit counter	USICNT	07Bh
	USI shift register	USISR	07Ch
Basic Clock System+	Basic clock system control 3	BCSCTL3	053h
	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P2	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

Absolute Maximum Ratings[(1)]

	Voltage applied at V_{CC} to V_{SS}		-0.3 V to 4.1 V
	Voltage applied to any pin[(2)]		-0.3 V to V_{CC} + 0.3 V
	Diode current at any device terminal		±2 mA
T_{stg}	Storage temperature[(3)]	Unprogrammed device	-55°C to 150°C
		Programmed device	-40°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

THERMAL INFORMATION

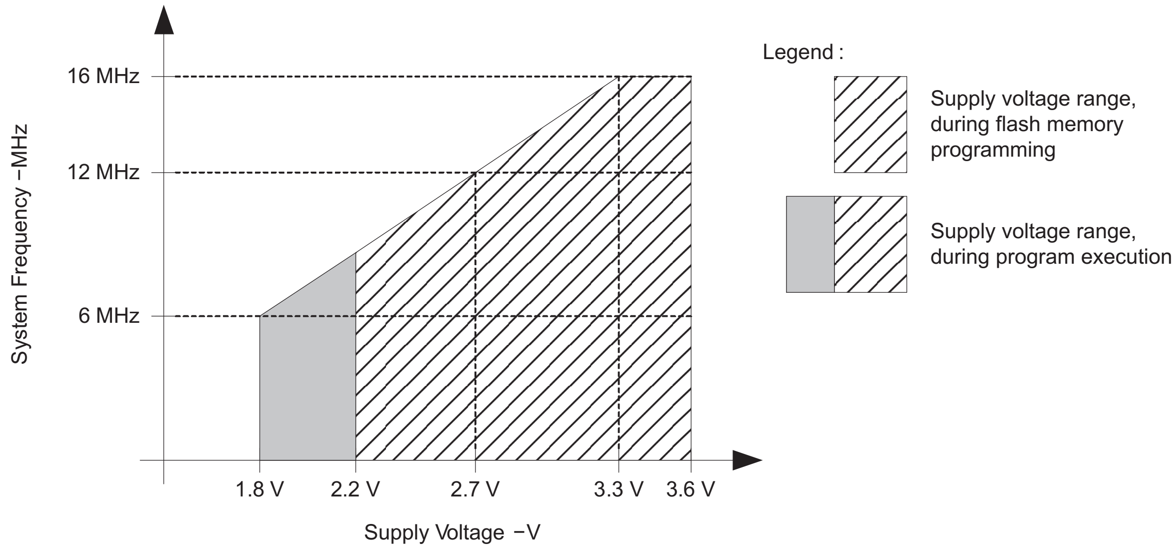
THERMAL METRIC[(1)]		MSP430F2013-EP RSA 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[(2)]	38.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[(3)]	26	
θ_{JB}	Junction-to-board thermal resistance[(4)]	7.5	
ψ_{JT}	Junction-to-top characterization parameter[(5)]	0.3	
ψ_{JB}	Junction-to-board characterization parameter[(6)]	5.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[(7)]	1.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Recommended Operating Conditions

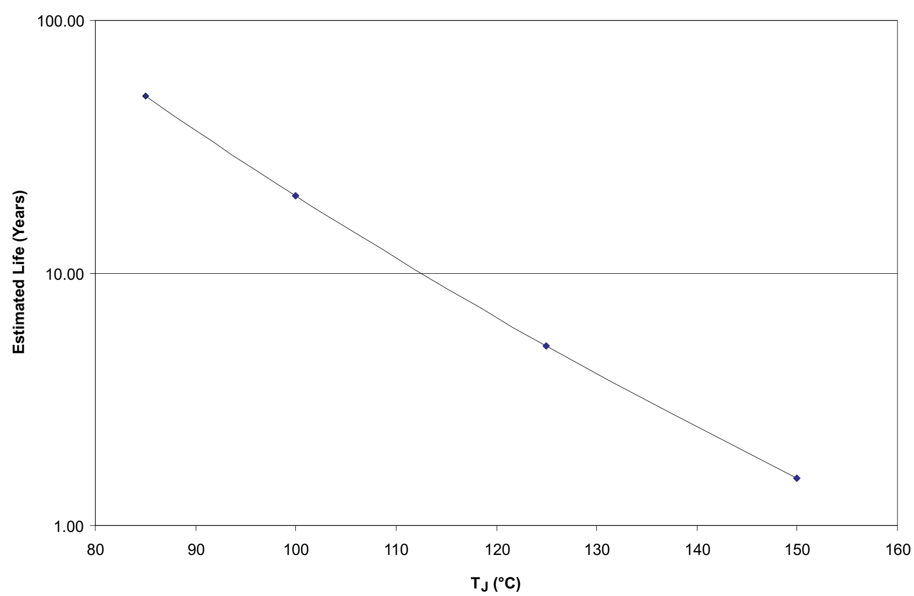
			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution	1.8		3.6	V
		During flash program/erase	2.2		3.6	
V_{SS}	Supply voltage			0		V
T_A	Operating free-air temperature		-40		125	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)[(1)(2)]	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc		12	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ± 10%	dc		16	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Safe Operating Area



(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 110°C junction temperture (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 2. Operating Life Derating Chart

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		220	280	µA
				3 V		310	380	
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		190		µA
				3 V		265		
$I_{AM,4kHz}$	Active mode (AM) current (4 kHz)	$f_{MCLK} = f_{SMCLK} = f_{ACLK}$ = 32768 Hz/8 = 4096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		1.2	3	µA
			125°C	2.2 V			6	
			-40°C to 85°C	3 V		1.6	4	
			125°C	3 V			7	
$I_{AM,100kHz}$	Active mode (AM) current (100 kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)}$ ≈ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		37	50	µA
			125°C	2.2 V			65	
			-40°C to 85°C	3 V		40	55	
			125°C	3 V			70	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) External crystal not used. The currents are characterized with a clock derived from alternate external clock source.

Typical Characteristics - Active Mode Supply Current (Into V_{CC})

ACTIVE MODE CURRENT
vs
V_{CC}
(T_A = 25°C)

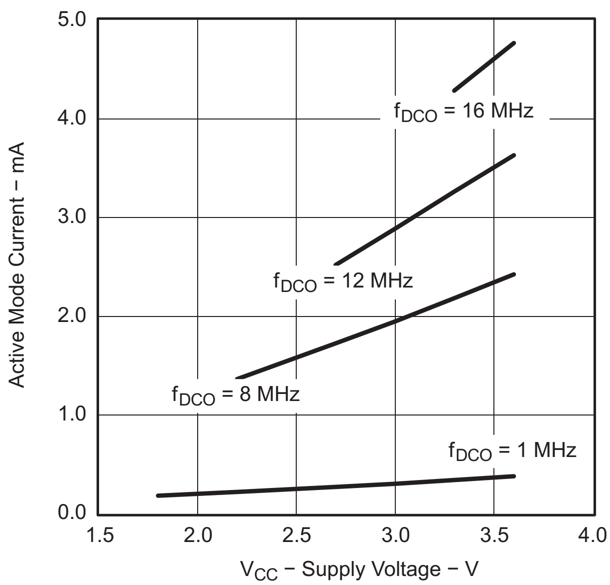


Figure 3.

ACTIVE MODE CURRENT
vs
DCO FREQUENCY

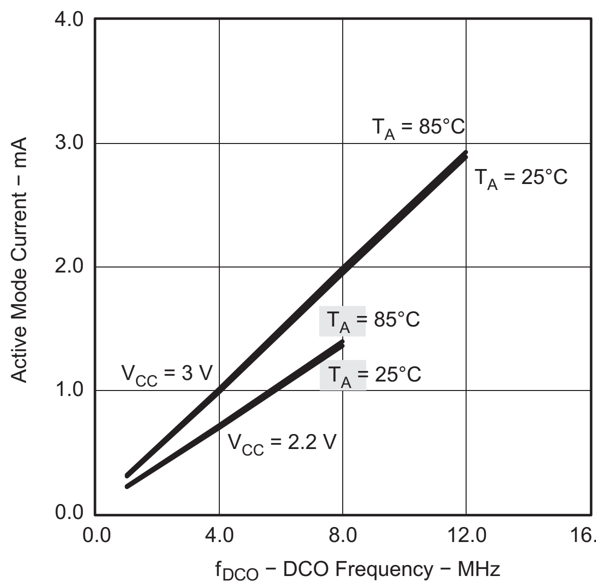


Figure 4.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		65	86	µA
				3 V		85	108	
$I_{LPM0,100kHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = $f_{DCO(0, 0)}$ ≈ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1		2.2 V		37	52	µA
				3 V		41	56	
I_{LPM2}	Low-power mode 2 (LPM2) current(4)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		22	29	µA
			125°C				34	
			-40°C to 85°C	3 V		25	32	
			125°C				37	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current(3)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.7	1.2	µA
			25°C			0.7	1	
			85°C			1.4	2.3	
			125°C			3	6.5	
			-40°C	3 V		0.9	1.2	
			25°C			0.9	1.2	
			85°C			1.6	2.8	
			125°C			3	7.6	
$I_{LPM3,VLO}$	Low-power mode 3 (LPM3) current(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.4	0.7	µA
			25°C			0.5	0.7	
			85°C			1	1.6	
			125°C			2	5.5	
			-40°C	3 V		0.5	0.9	
			25°C			0.6	0.9	
			85°C			1.3	1.8	
			125°C			2.5	6.5	
I_{LPM4}	Low-power mode 4 (LPM4) current(5)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V/3 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			0.8	1.5	
			125°C			2	4.4	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) External crystal not used. The currents are characterized with a clock derived from alternate external clock source.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

Schmitt-Trigger Inputs (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			2.2 V	1.00		1.65	
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			2.2 V	0.55		1.20	
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} - V_{IT-})		2.2 V	0.2		1.0	V
			3 V	0.3		1.0	
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

Inputs (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag[1]	2.2 V/3 V	25			ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

Leakage Current (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	See [1] and [2]	2.2 V/3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = -1.5 mA (1)	2.2 V	V_{CC} - 0.25		V_{CC}	V
		$I_{(OHmax)}$ = -6 mA (2)	2.2 V	V_{CC} - 0.6		V_{CC}	
		$I_{(OHmax)}$ = -1.5 mA (1)	3 V	V_{CC} - 0.25		V_{CC}	
		$I_{(OHmax)}$ = -6 mA (2)	3 V	V_{CC} - 0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA (1)	2.2 V	V_{SS}		V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 6 mA (2)	2.2 V	V_{SS}		V_{SS} + 0.6	
		$I_{(OLmax)}$ = 1.5 mA (1)	3 V	V_{SS}		V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA (2)	3 V	V_{SS}		V_{SS} + 0.6	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±12 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ (1) (2)	2.2 V			10	MHz
			3 V			12	
$f_{Port°CLK}$	Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C_L = 20 pF (2)	2.2 V			12	MHz
			3 V			16	

(1) A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics - Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

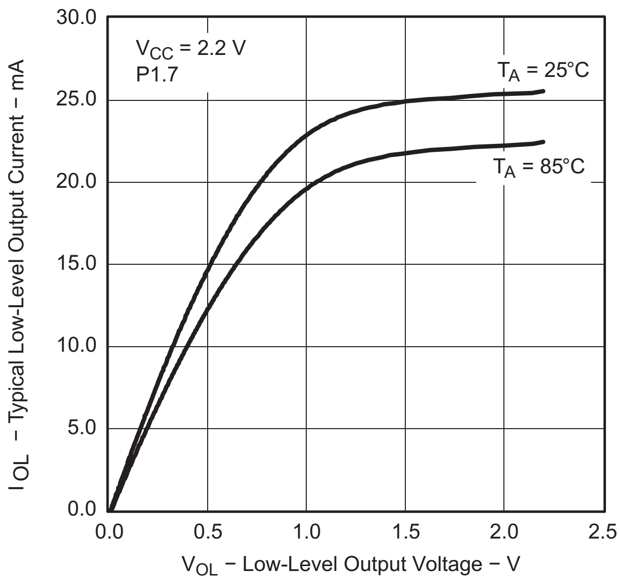


Figure 5.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

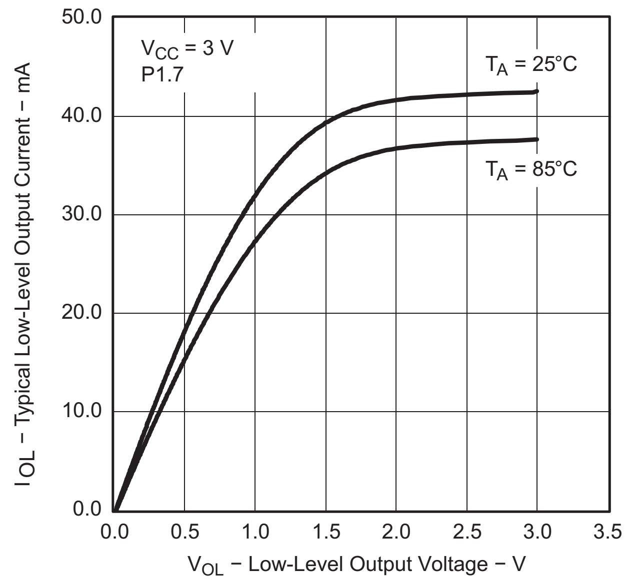


Figure 6.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

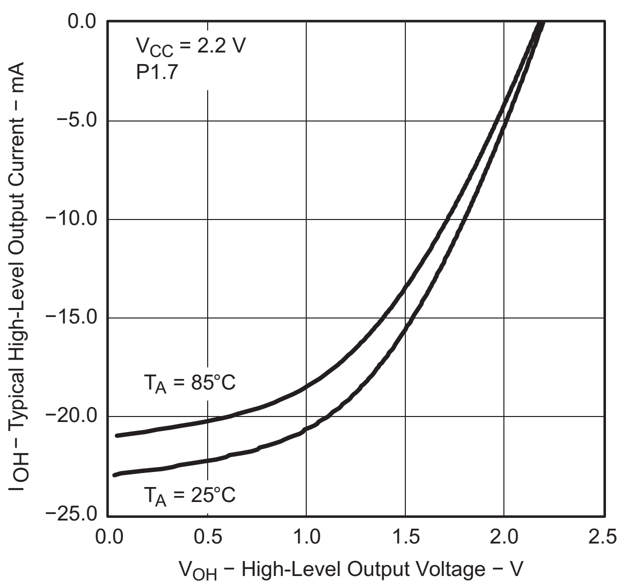


Figure 7.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

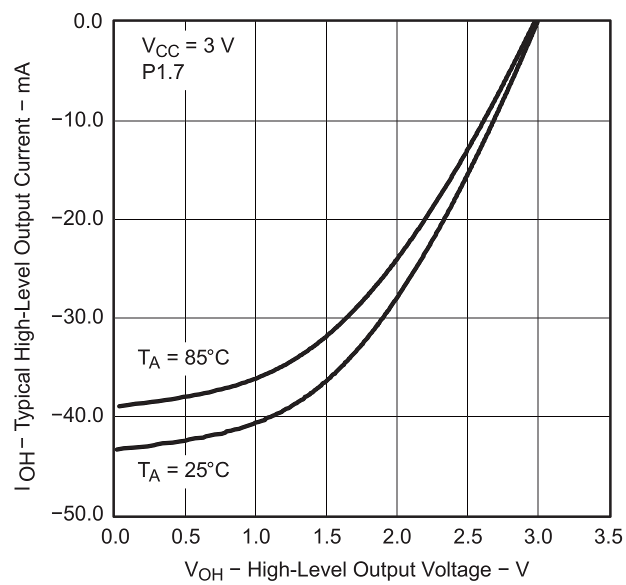


Figure 8.

POR/Brownout Reset (BOR)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 9	$dV_{CC}/dt \le 3$ V/s			0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 9 through Figure 11	$dV_{CC}/dt \le 3$ V/s				1.71	V
$V_{hys(B\_IT-)}$	See Figure 9	$dV_{CC}/dt \le 3$ V/s		70	155	210	mV
$t_{d(BOR)}$	See Figure 9(2)					2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally(2)		2.2 V/3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)}$ + $V_{hys(B\_IT-)}$ is ≤ 1.8 V.
(2) Minimum and maximum parameters are characterized up to T_A = 105°C unless otherwise noted.

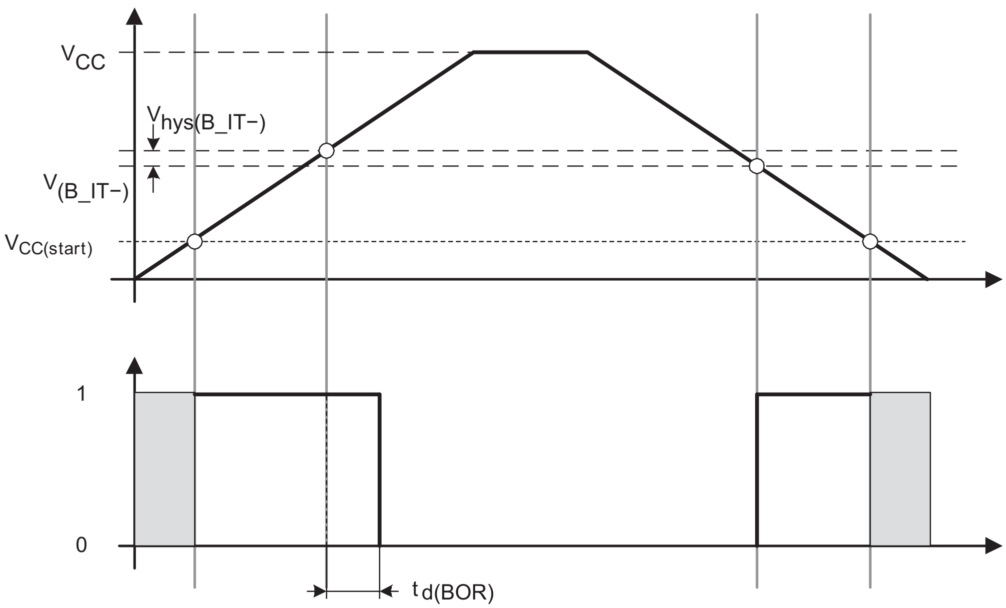


Figure 9. POR/Brownout Reset (BOR) vs Supply Voltage

Typical Characteristics - POR/Brownout Reset (BOR)

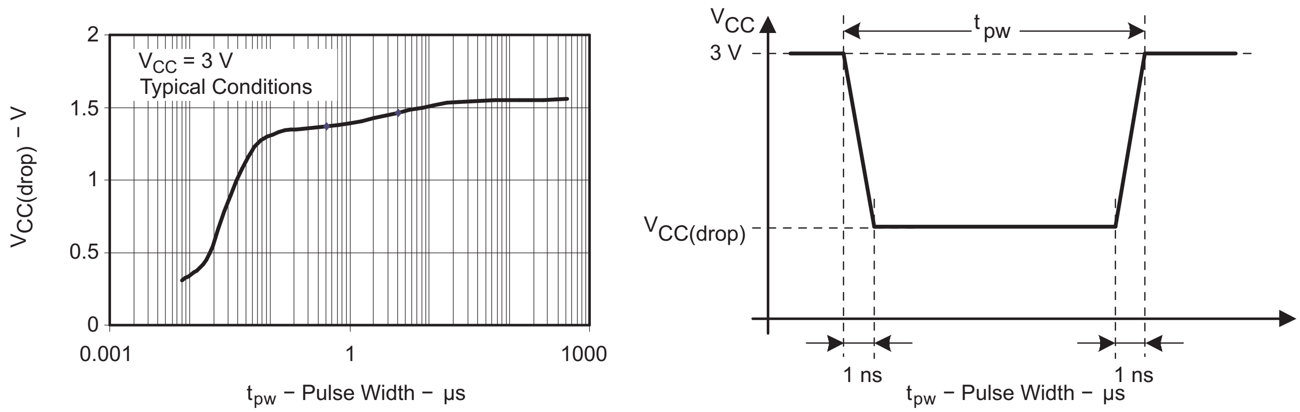


Figure 10. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

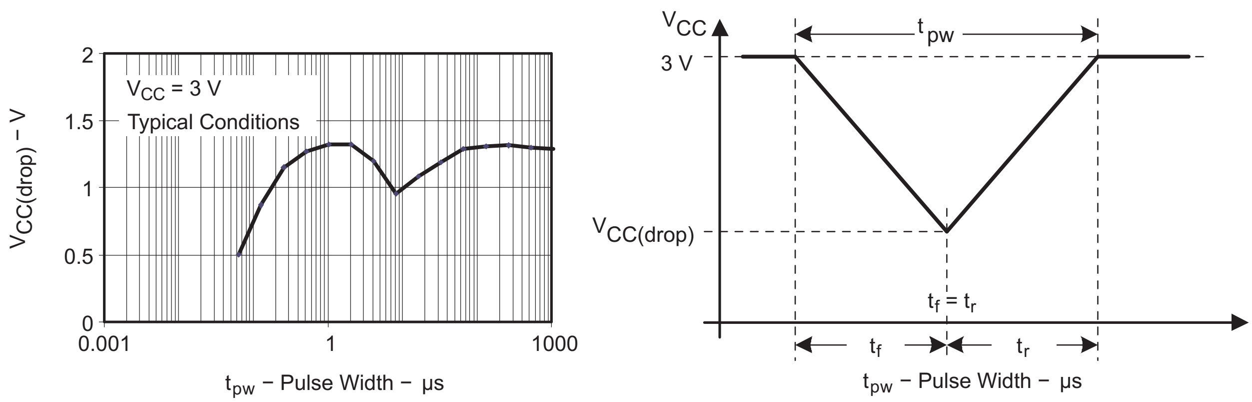


Figure 11. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V			1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.03	1.08	1.14	
	Duty cycle	Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

Calibrated DCO Frequencies - Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	Frequency tolerance at calibration		25°C	3 V	-1	±0.2	+1	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

Calibrated DCO Frequencies - Tolerance Over Temperature -40°C to 125°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over temperature		-40°C to 125°C	3 V	-2.5	±1.25	+2.5	%
	8-MHz tolerance over temperature		-40°C to 125°C	3 V	-5	±1.25	+5	%
	12-MHz tolerance over temperature		-40°C to 125°C	3 V	-5	±1.25	+2.5	%
	16-MHz tolerance over temperature		-40°C to 125°C	3 V	-6.25	±2.0	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	-40°C to 125°C	2.2 V	0.97	1	1.03	MHz
				3 V	0.975	1	1.025	
				3.6 V	0.97	1	1.03	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	-40°C to 125°C	2.2 V	7.6	8	8.4	MHz
				3 V	7.6	8	8.4	
				3.6 V	7.6	8	8.4	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	-40°C to 125°C	2.2 V	11.6	12	12.3	MHz
				3 V	11.6	12	12.3	
				3.6 V	11.6	12	12.3	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	-40°C to 125°C	3 V	15	16	16.48	MHz
				3.6 V	15	16	16.48	

Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
	8-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
	12-MHz tolerance over V_{CC}		25°C	2.2 V to 3.6 V	-4	±2	+3	%
	16-MHz tolerance over V_{CC}		25°C	3 V to 3.6 V	-6.25	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.97	1	1.03	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.76	8	8.24	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V to 3.6 V	15	16	16.48	MHz

Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance overall		1.8 V to 3.6 V	-5	±2.5	+5	%
	8-MHz tolerance overall		1.8 V to 3.6 V	-5	±2.5	+5	%
	12-MHz tolerance overall		2.2 V to 3.6 V	-5	±2.5	+5	%
	16-MHz tolerance overall		3 V to 3.6 V	-6.25	±3	+6.25	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	1.8 V to 3.6 V	0.95	1	1.05	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	1.8 V to 3.6 V	7.6	8	8.4	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	2.2 V to 3.6 V	11.4	12	12.6	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	3 V to 3.6 V	15	16	17	MHz

Typical Characteristics - Calibrated 1-MHz DCO Frequency

CALIBRATED 1-MHz FREQUENCY vs TEMPERATURE

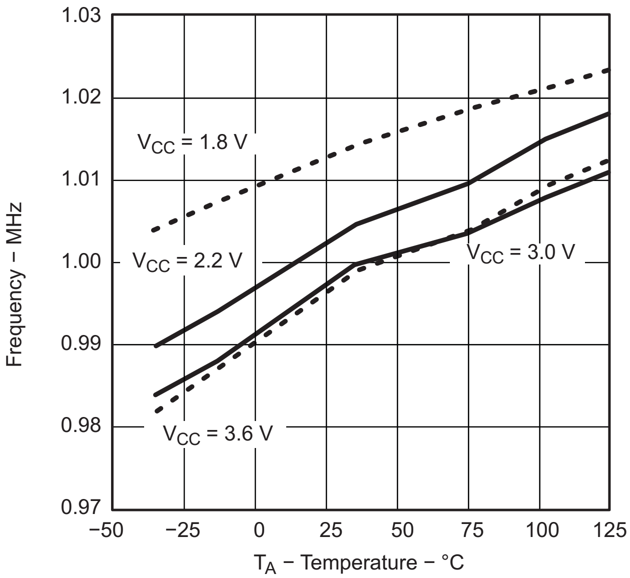


Figure 12.

CALIBRATED 1-MHz FREQUENCY vs SUPPLY VOLTAGE

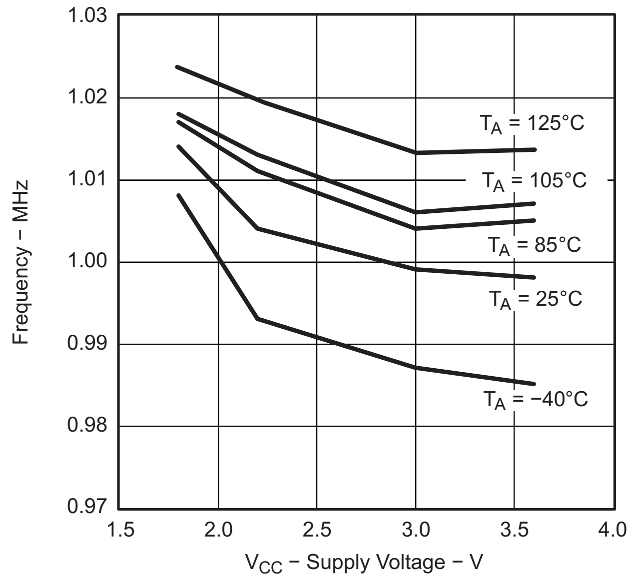


Figure 13.

Wake-Up From Lower-Power Modes (LPM3/4)(1)

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4(2)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V/3 V			2	μs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ				1.5	
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ				1	
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4(3)				$1 / f_{MCLK} + t_{Clock,LPM3/4}$		

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.
(2) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(3) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics - DCO Clock Wake-Up Time From LPM3/4

DCO WAKE-UP TIME FROM LPM3 vs DCO FREQUENCY

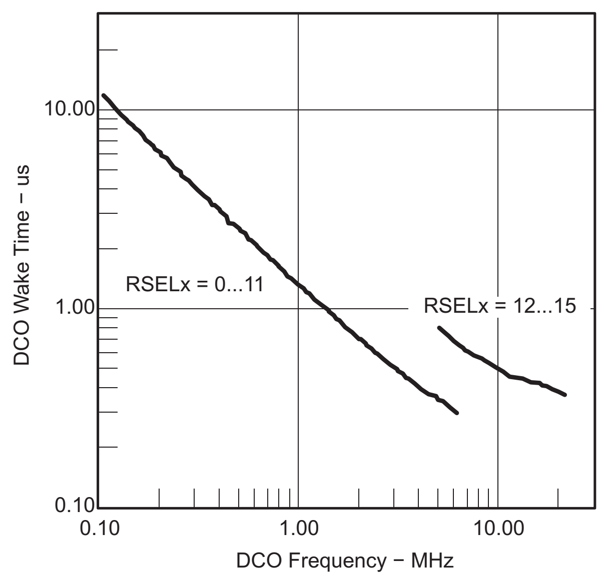


Figure 14.

Crystal Oscillator, XT1, Low-Frequency Mode(1)(2)

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(3)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P1.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(4)	XTS = 0, LFXT1Sx = 3(5)	2.2 V/3 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  (a) Keep the trace between the device and the crystal as short as possible.
  (b) Design a good ground plane around the oscillator pins.
  (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Crystal oscillator cannot be operated beyond 105°C. Parameters are characterized up to T_A = 105°C unless otherwise noted.
(3) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(4) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(5) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	-40°C to 85°C	2.2 V/3 V	4	12	20	kHz
		125°C				22	
df_{VLO}/dT	VLO frequency temperature drift(1)	-40°C to 125°C	2.2 V/3 V		0.68		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift(2)	25°C	1.8 V to 3.6 V		4		%/V

(1) Calculated using the box method:
(MAX(-40 to 125°C) - MIN(-40 to 125°C)) / MIN(-40 to 125°C) / (125°C - (-40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) - MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V - 1.8 V)

Timer_A

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
			3 V			16	
$t_{TA,cap}$	Timer_A capture timing(1)	TA0, TA1	2.2 V/3 V	20			ns

(1) Parameter characterized up to T_A = 105°C unless otherwise noted.

USI, Universal Serial Interface (1)

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USI}	USI clock frequency	External: SCLK, Duty cycle = 50% ±10%, SPI slave mode	2.2 V			10	MHz
			3 V			16	
$V_{OL,I2C}$	Low-level output voltage on SDA and SCL	USI module in I2C mode, $I_{(OLmax)}$ = 1.5 mA	2.2 V/3 V	V_{SS}		V_{SS} + 0.4	V

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.

Typical Characteristics, USI Low-Level Output Voltage on SDA and SCL

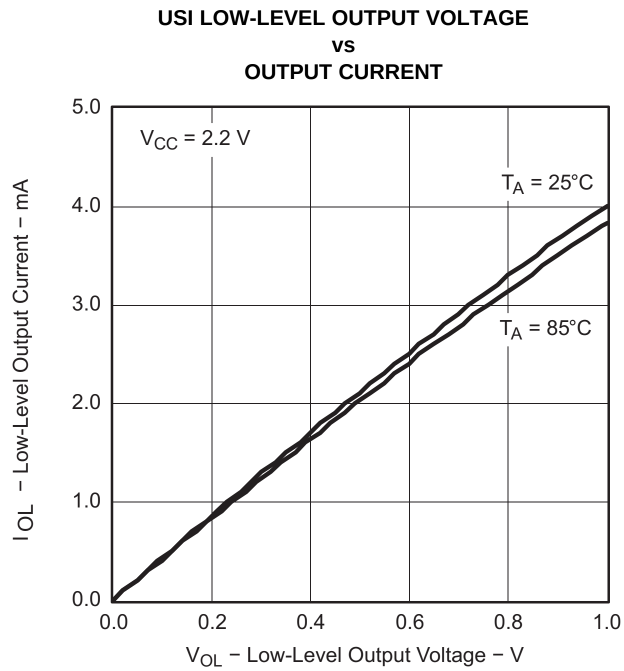


Figure 15.

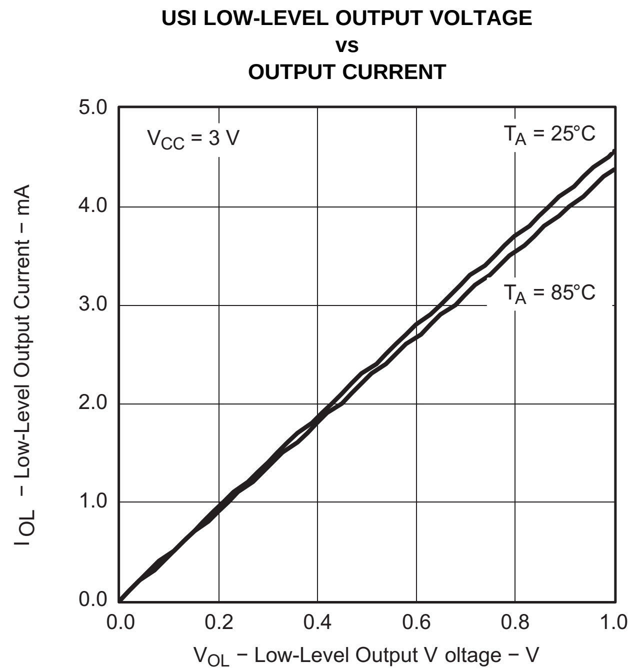


Figure 16.

SD16_A, Power Supply and Recommended Operating Conditions(1)

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage range	$AV_{CC} = DV_{CC} = V_{CC}$, $AV_{SS} = DV_{SS} = V_{SS}$ = 0 V				2.5		3.6	V
I_{SD16}	Analog supply current including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	GAIN: 1,2	-40°C to 85°C	3 V		730	1050	µA
				105°C				1170	
			GAIN: 4,8,16	-40°C to 85°C			810	1150	
				105°C				1300	
			GAIN: 32	-40°C to 85°C			1160	1700	
				105°C				1850	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	GAIN: 1	-40°C to 85°C			720	1030	
				105°C				1160	
			GAIN: 32	-40°C to 85°C			810	1150	
				105°C				1300	
f_{SD16}	SD16 input clock frequency	SD16LP = 0 (Low power mode disabled)			3 V	0.03	1	1.1	MHz
		SD16LP = 1 (Low power mode enabled)				0.03	0.5		

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.

SD16_A, Input Range(1)

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{ID,FSR}$	Differential full scale input voltage range(2)	Bipolar mode, SD16UNI = 0			$-(V_{REF}/2)$/GAIN		$+(V_{REF}/2)$/GAIN	mV
		Unipolar mode, SD16UNI = 1			0		$+(V_{REF}/2)$/GAIN	
V_{ID}	Differential input voltage range for specified performance(2)	SD16REFON = 1	SD16GAINx = 1			±500		mV
			SD16GAINx = 2			±250		
			SD16GAINx = 4			±125		
			SD16GAINx = 8			±62		
			SD16GAINx = 16			±31		
			SD16GAINx = 32			±15		
Z_I	Input impedance (one input pin to AV_{SS})	f_{SD16} = 1 MHz	SD16GAINx = 1	3 V		200		kΩ
			SD16GAINx = 32			75		
Z_{ID}	Differential input impedance (IN+ to IN-)	f_{SD16} = 1 MHz	SD16GAINx = 1	3 V	300	400		kΩ
			SD16GAINx = 32		100	150		
V_I	Absolute input voltage range				AV_{SS} - 0.1		AV_{CC}	V
V_{IC}	Common-mode input voltage range				AV_{SS} - 0.1		AV_{CC}	V

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.
(2) The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)$/GAIN and $V_{FSR-} = -(V_{REF}/2)$/GAIN. The analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}.

SD16_A, SINAD Performance (f_{SD16} = 1 MHz, SD16OSRx = 1024, SD16REFON = 1)[(1)]

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	UNIT
$SINAD_{1024}$	Signal-to-noise + distortion ratio (OSR = 1024)	SD16GAINx = 1, Signal amplitude: V_{IN} = 500 mV, Signal frequency: f_{IN} = 100 Hz	3 V	86	87	dB
		SD16GAINx = 2, Signal amplitude: V_{IN} = 250 mV, Signal frequency: f_{IN} = 100 Hz		82	83	
		SD16GAINx = 4, Signal amplitude: V_{IN} = 125 mV, Signal frequency: f_{IN} = 100 Hz		78	79	
		SD16GAINx = 8, Signal amplitude: V_{IN} = 62 mV, Signal frequency: f_{IN} = 100 Hz		73	74	
		SD16GAINx = 16, Signal amplitude: V_{IN} = 31 mV, Signal frequency: f_{IN} = 100 Hz		68	69	
		SD16GAINx = 32, Signal amplitude: V_{IN} = 15 mV, Signal frequency: f_{IN} = 100 Hz		62	63	

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.

SD16_A, SINAD Performance (f_{SD16} = 1 MHz, SD16OSRx = 256, SD16REFON = 1)[(1)]

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	UNIT
$SINAD_{256}$	Signal-to-noise + distortion ratio (OSR = 256)	SD16GAINx = 1, Signal amplitude: V_{IN} = 500 mV, Signal frequency: f_{IN} = 100 Hz	3 V	82	83	dB
		SD16GAINx = 2, Signal amplitude: V_{IN} = 250 mV, Signal frequency: f_{IN} = 100 Hz		76	77	
		SD16GAINx = 4, Signal amplitude: V_{IN} = 125 mV, Signal frequency: f_{IN} = 100 Hz		71	72	
		SD16GAINx = 8, Signal amplitude: V_{IN} = 62 mV, Signal frequency: f_{IN} = 100 Hz		67	68	
		SD16GAINx = 16, Signal amplitude: V_{IN} = 31 mV, Signal frequency: f_{IN} = 100 Hz		63	64	
		SD16GAINx = 32, Signal amplitude: V_{IN} = 15 mV, Signal frequency: f_{IN} = 100 Hz		57	58	

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.

Typical Characteristics, SD16_A SINAD Performance Over OSR

SINAD PERFORMANCE
vs
OSR
(f_{SD16} = 1 MHz, SD16REFON = 1,SD16GAINx = 1)

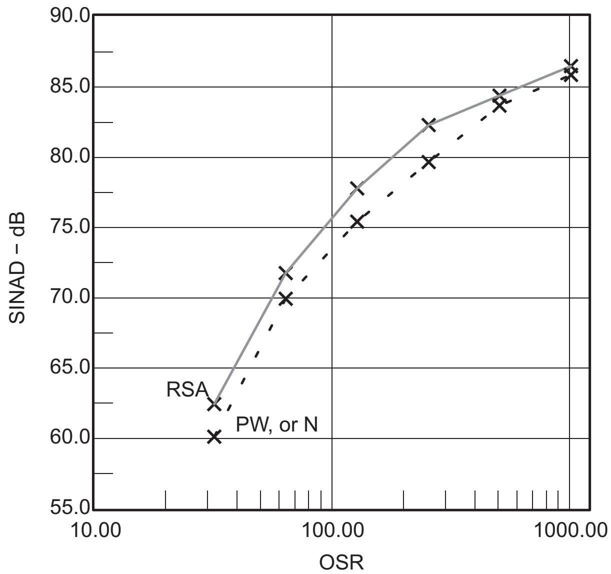


Figure 17.

SD16_A, Performance (f_{SD16} = 1 MHz, SD16OSRx = 256, SD16REFON = 1)(1)

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
G	Nominal gain	SD16GAINx = 1	3 V	0.97	1.00	1.02	
		SD16GAINx = 2		1.90	1.96	2.02	
		SD16GAINx = 4		3.76	3.86	3.96	
		SD16GAINx = 8		7.36	7.62	7.84	
		SD16GAINx = 16		14.56	15.04	15.52	
		SD16GAINx = 32		27.20	28.35	29.76	
ΔG/ΔT	Gain temperature drift	SD16GAINx = 1(2)	3 V		15		ppm/°C
E_{OS}	Offset error	SD16GAINx = 1	3 V			±0.2	%FSR
		SD16GAINx = 32				±1.5	
$\Delta E_{OS}/\Delta T$	Offset error temperature coefficient	SD16GAINx = 1	3 V		±4	±20	ppm FSR/°C
		SD16GAINx = 32			±20	±100	
CMRR	Common-mode rejection ratio	SD16GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz, 100 Hz	3 V		>90		dB
		SD16GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz, 100 Hz			>75		
DC PSR	DC power supply rejection	SD16GAINx = 1, V_{IN} = 500 mV, V_{CC} = 2.5 V to 3.6 V(3)	2.5 V to 3.6 V		0.35		%/V
AC PSRR	AC power supply rejection ratio	SD16GAINx = 1, V_{CC} = 3 V ± 100 mV, f_{IN} = 50 Hz	3 V		>80		dB

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.
(2) Calculated using the box method: (MAX(-40°C to 85°C) - MIN(-40°C to 85°C)) / MIN(-40°C to 85°C) / (85°C - (-40°C))
(3) Calculated using the ADC output code and the box method:
(MAX-code(2.5 V to 3.6 V) - MIN-code(2.5 V to 3.6 V)) / MIN-code(2.5 V to 3.6 V) / (3.6 V - 2.5 V)

SD16_A, Built-In Voltage Reference[1]

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD16REFON = 1, SD16VMIDON = 0		3 V	1.14	1.20	1.26	V
I_{REF}	Reference supply current	SD16REFON = 1, SD16VMIDON = 0	-40°C to 85°C	3 V		190	280	μA
			105°C	3 V			295	
TC	Temperature coefficient	SD16REFON = 1, SD16VMIDON = 0		3 V		18	50	ppm/°C
C_{REF}	V_{REF} load capacitance	SD16REFON = 1, SD16VMIDON = 0[2]				100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD16REFON = 1, SD16VMIDON = 0		3 V			±200	nA
t_{ON}	Turn-on time	SD16REFON = 0 → 1, SD16VMIDON = 0, C_{REF} = 100 nF		3 V		5		ms
DC PSR	DC power supply rejection $\Delta V_{REF}/\Delta V_{CC}$	SD16REFON = 1, SD16VMIDON = 0, V_{CC} = 2.5 V to 3.6 V		2.5 V to 3.6 V		100		μV/V

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.
(2) There is no capacitance required on V_{REF}. However, a capacitance of at least 100 nF is recommended to reduce any reference voltage noise.

SD16_A, Reference Output Buffer[1]

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF,BUF}$	Reference buffer output voltage	SD16REFON = 1, SD16VMIDON = 1		3 V		1.2		V
$I_{REF,BUF}$	Reference supply + reference output buffer quiescent current	SD16REFON = 1, SD16VMIDON = 1	-40°C to 85°C	3 V		385	600	μA
			105°C				660	
$C_{REF(O)}$	Required load capacitance on V_{REF}	SD16REFON = 1, SD16VMIDON = 1			470			nF
$I_{LOAD,Max}$	Maximum load current on V_{REF}	SD16REFON = 1, SD16VMIDON = 1		3 V			±1	mA
	Maximum voltage variation vs load current	$\lvert I_{LOAD} \rvert$ = 0 to 1 mA		3 V	-15		+15	mV
t_{ON}	Turn on time	SD16REFON = 0 → 1, SD16VMIDON = 1, C_{REF} = 470 nF		3 V		100		μs

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.

SD16_A, External Reference Input[1]

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD16REFON = 0	3 V	1	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.

SD16_A, Temperature Sensor(1)(2)

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient			1.18	1.32	1.46	mV/°C
$V_{Offset,Sensor}$	Sensor offset voltage			-100		100	mV
V_{Sensor}	Sensor output voltage (3)	Temperature sensor voltage at T_A = 85°C	3 V	435	475	515	mV
		Temperature sensor voltage at T_A = 25°C		355	395	435	
		Temperature sensor voltage at T_A = 0°C		320	360	400	

(1) Values are not based on calculations using TC_{Sensor} or $V_{Offset,sensor}$ but on measurements.
(2) Parameters are characterized up to T_A = 105°C unless otherwise noted.
(3) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A$ = 0°C) [mV]

Flash Memory(1)(2)

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time (3)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/erase endurance	-40°C ≤ T_J ≤ 105°C		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See (4)			30		t_{FTG}
$t_{Block,\ 0}$	Block program time for first byte or word	See (4)			25		t_{FTG}
$t_{Block,\ 1-63}$	Block program time for each additional byte or word	See (4)			18		t_{FTG}
$t_{Block,\ End}$	Block program end-sequence wait time	See (4)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	See (4)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	See (4)			4819		t_{FTG}

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.
(2) Additional flash retention documentation located in application report (SLAA392).
(3) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(4) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM(1)

over recommended ranges of supply voltage and up to operating free-air temperature T_A = 105°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (2)	CPU halted	1.6		V

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.
(2) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V/3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length[(1)]	2.2 V/3 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge[(2)])	2.2 V/3 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time	2.2 V/3 V	15		100	µs
f_{TCK}	TCK input frequency[(3)]	2.2 V	0		5	MHz
		3 V	0		10	MHz
$R_{Internal}$	Internal pulldown resistance on TEST	2.2 V/3 V	25	60	90	kΩ

(1) Parameters are characterized up to T_A = 105°C unless otherwise noted.
(2) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
(3) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse[(1)]

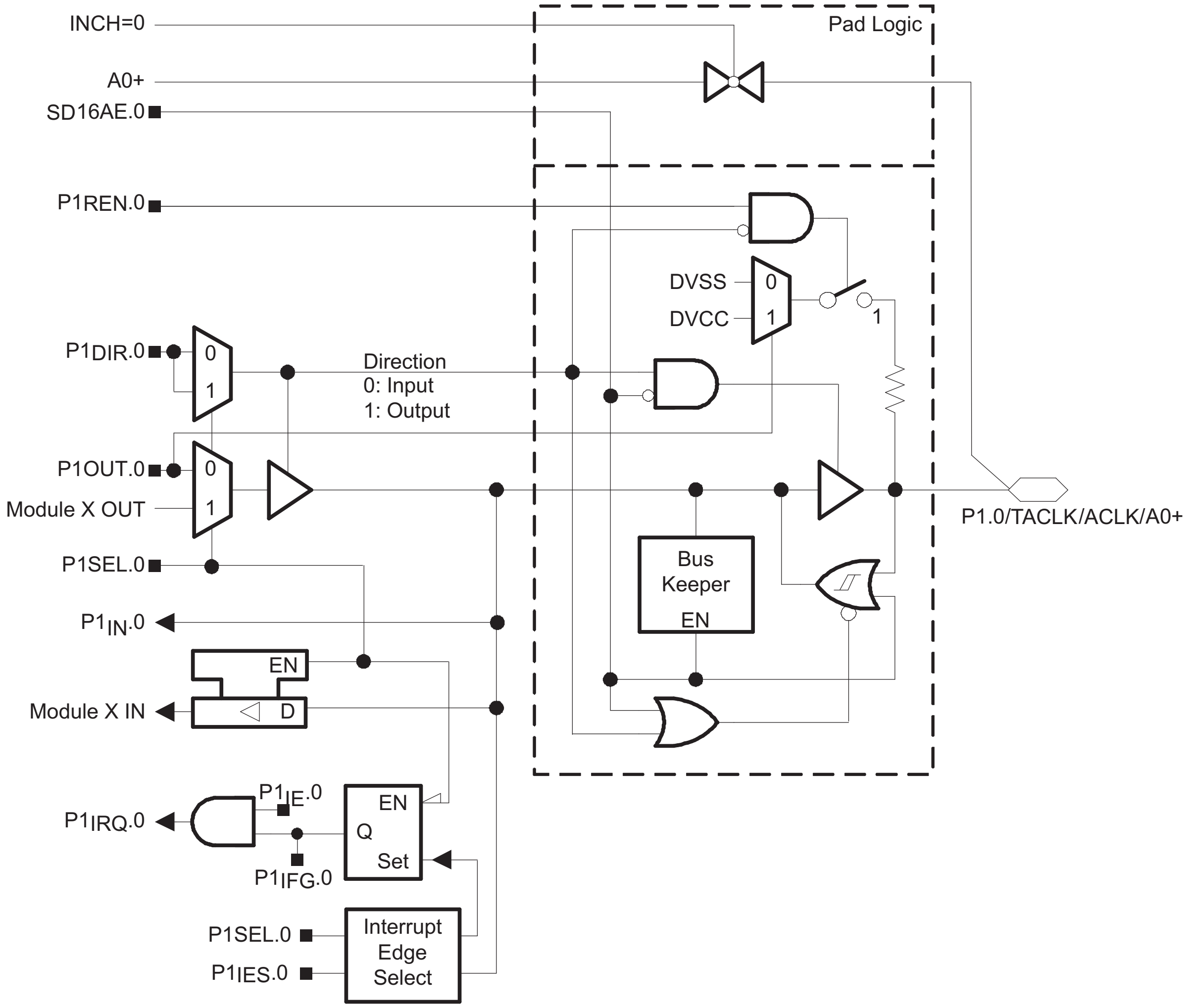
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

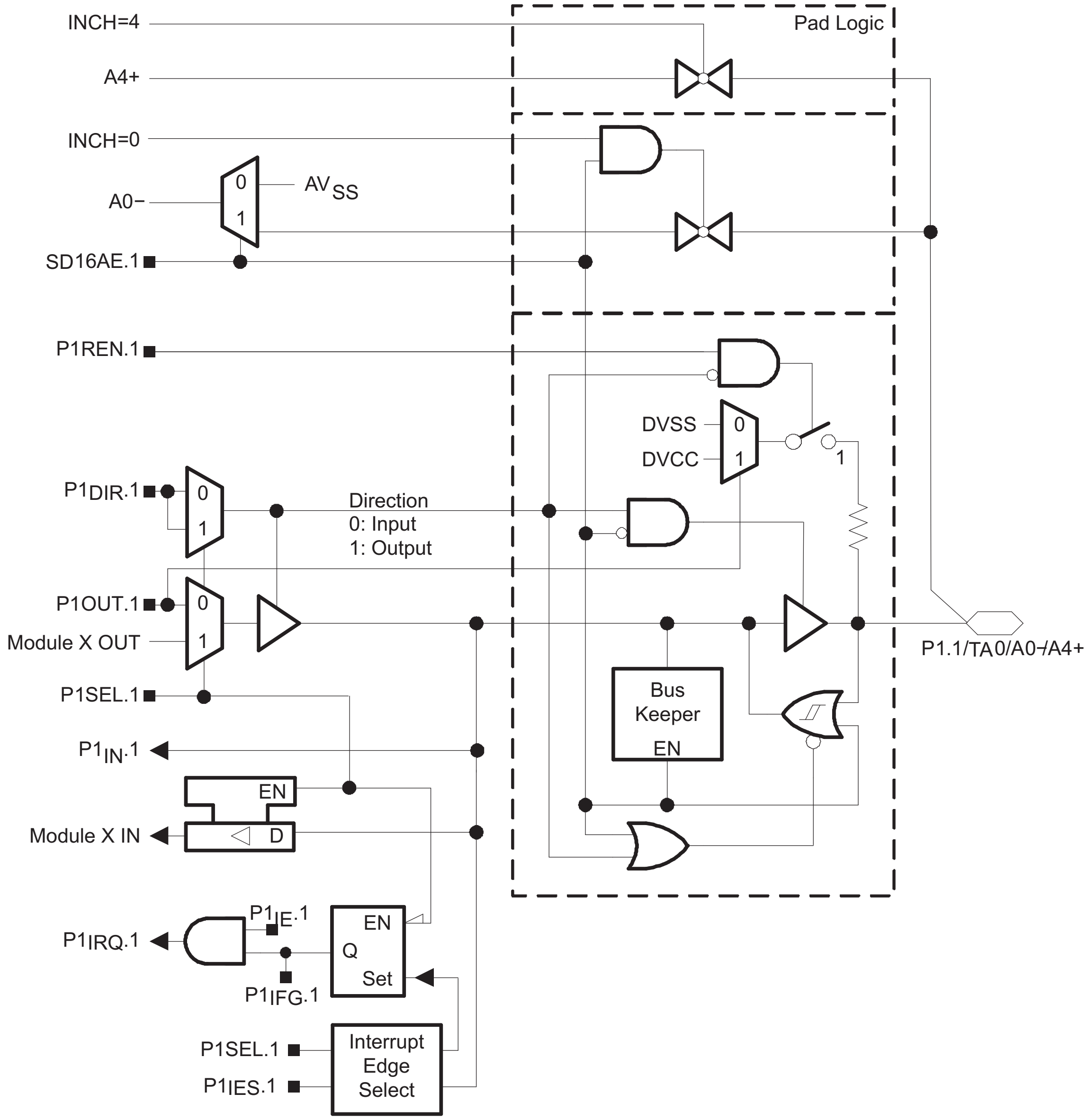
(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

APPLICATION INFORMATION

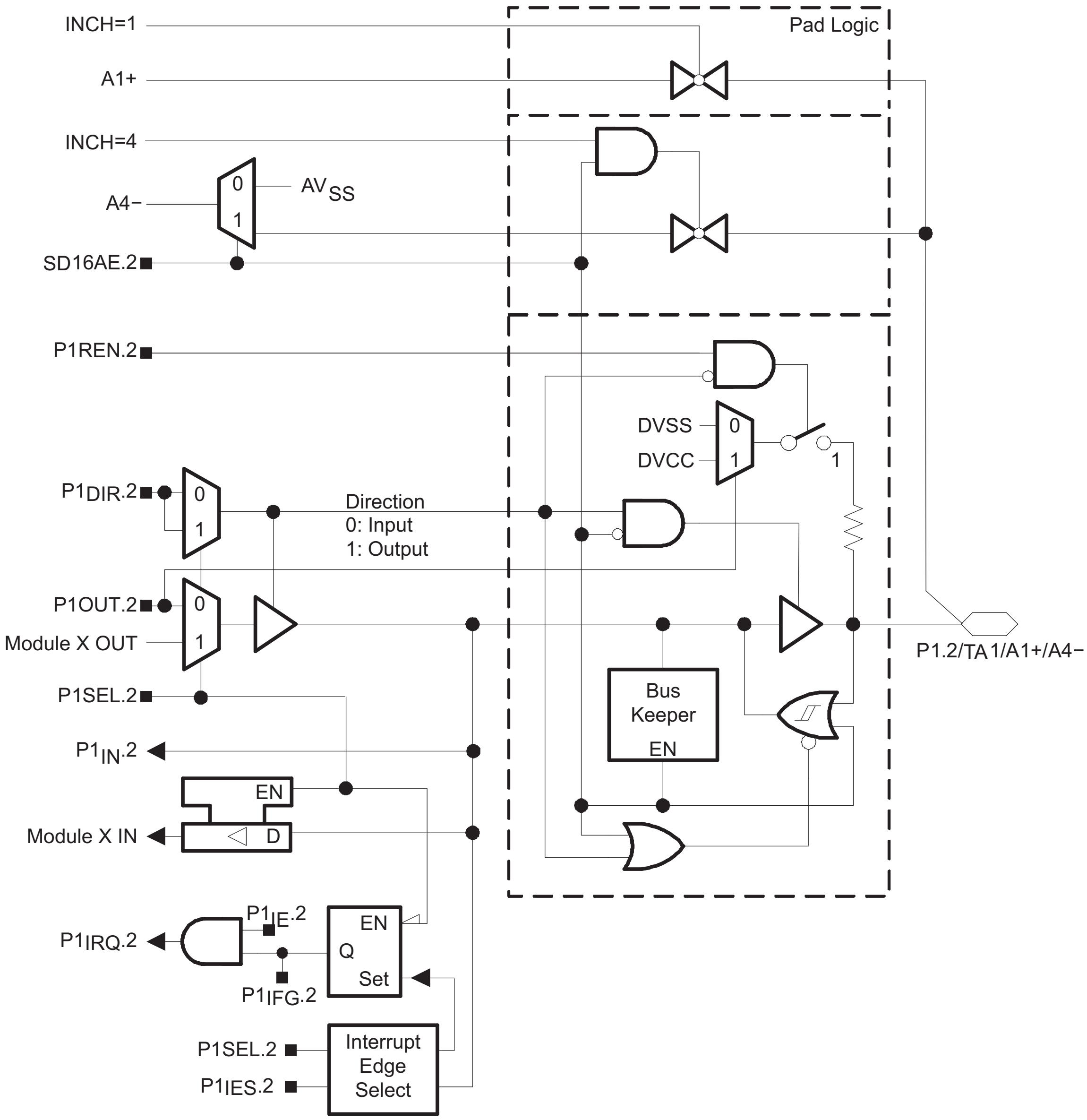
Port P1 (P1.0) Pin Schematics



Port P1 (P1.1) Pin Schematics



Port P1 (P1.2) Pin Schematics



Port P1 (P1.3) Pin Schematics

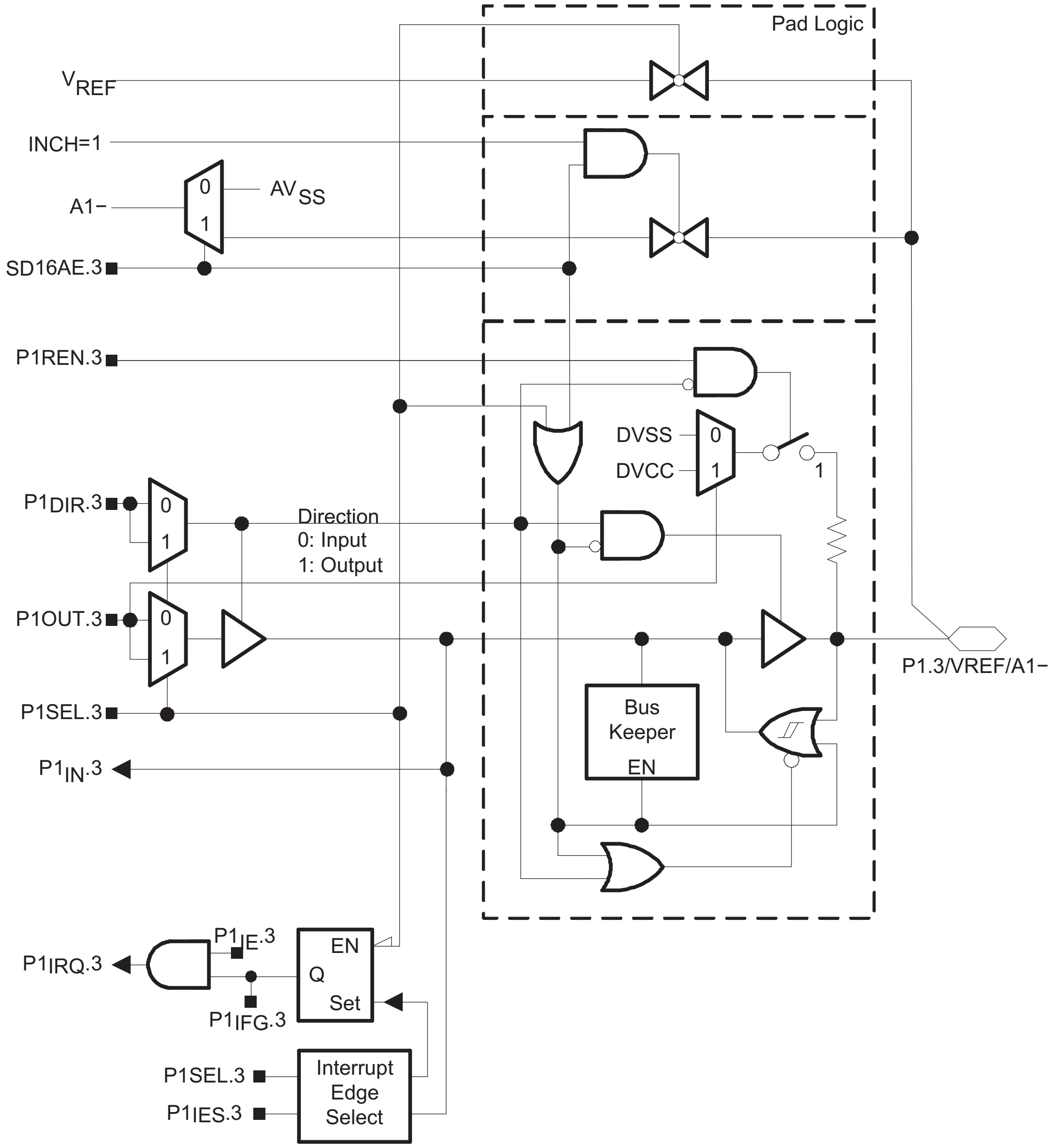
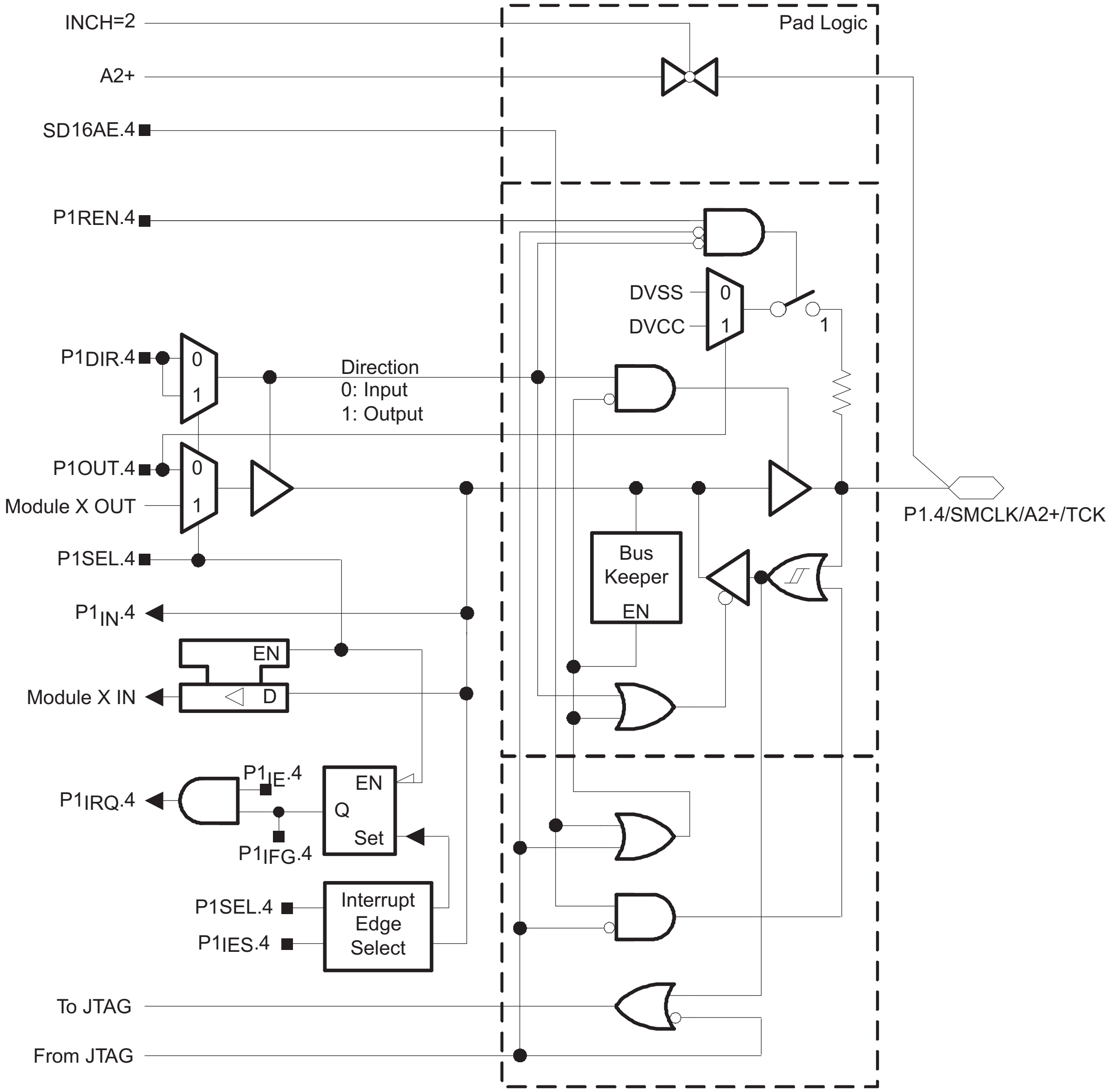


Table 13. Port P1 (P1.0 to P1.3) Pin Functions

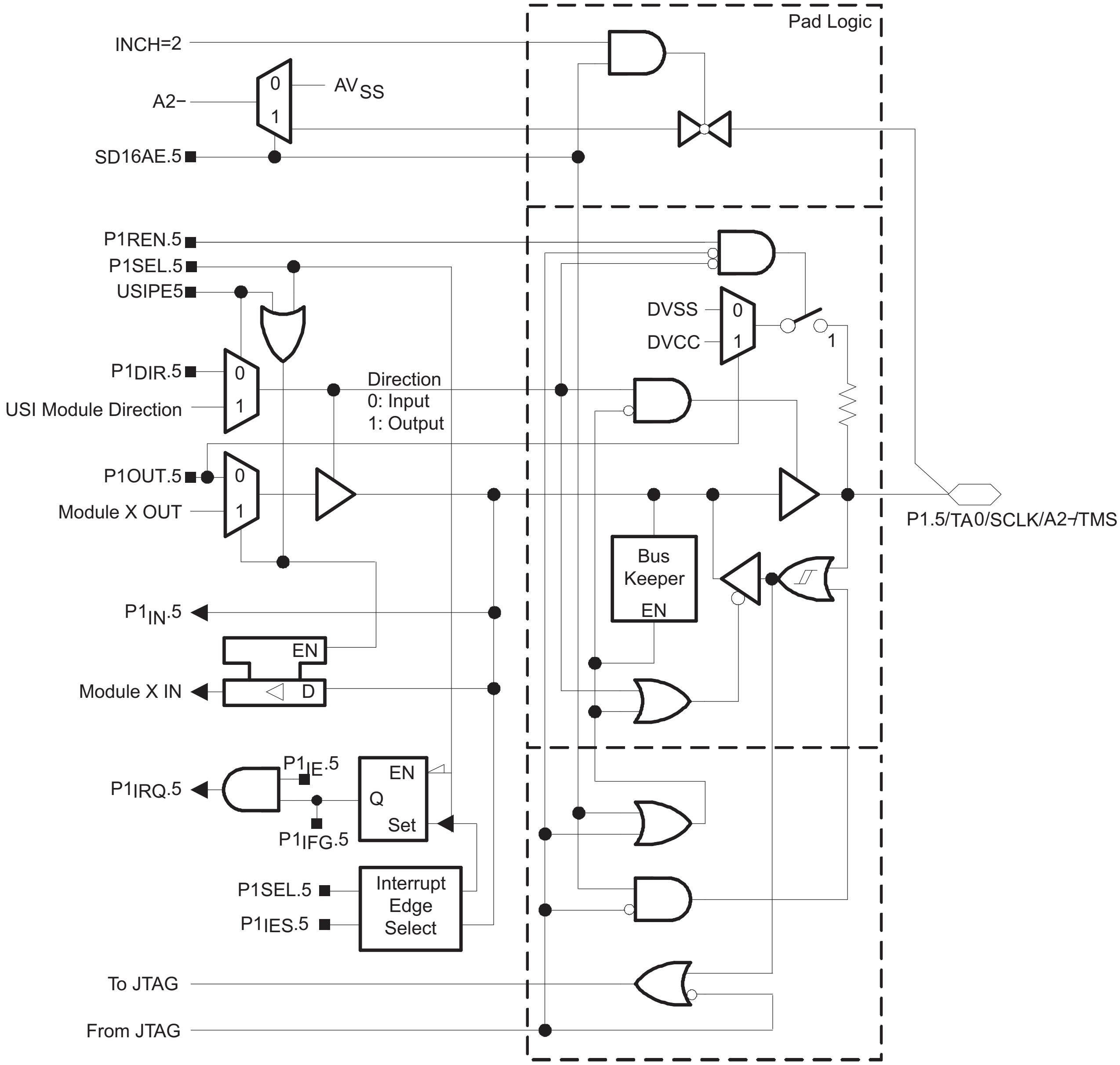
PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)(2)			
			P1DIR.x	P1SEL.x	SD16AE.x	INCHx
P1.0/TACLK/ACLK/A0+	0	P1.0(3) input/output	0/1	0	0	N/A
		Timer_A2.TACLK/INCLK	0	1	0	N/A
		ACLK	1	1	0	N/A
		A0+(4)	X	X	1	0
P1.1/TA0/A0-/A4+	1	P1.1(3) input/output	0/1	0	0	N/A
		Timer_A2.CCI0A	0	1	0	N/A
		Timer_A2.TA0	1	1	0	N/A
		A0-(4)(5)	X	X	1	0
		A4+(4)	X	X	1	4
P1.2/TA1/A1+/A4-	2	P1.2(3) input/output	0/1	0	0	N/A
		Timer_A2.CCI1A	0	1	0	N/A
		Timer_A2.TA1	1	1	0	N/A
		A1+(4)	X	X	1	1
		A4-(4)(5)	X	X	1	4
P1.3/VREF/A1-	3	P1.3(3) input/output	0/1	0	0	N/A
		VREF	X	1	0	N/A
		A1-(4)(5)	X	X	1	1

(1) X = Don't care
(2) N/A = Not available or not applicable
(3) Default after reset (PUC/POR)
(4) Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(5) With SD16AE.x = 0 the negative inputs are connected to VSS if the corresponding input is selected.

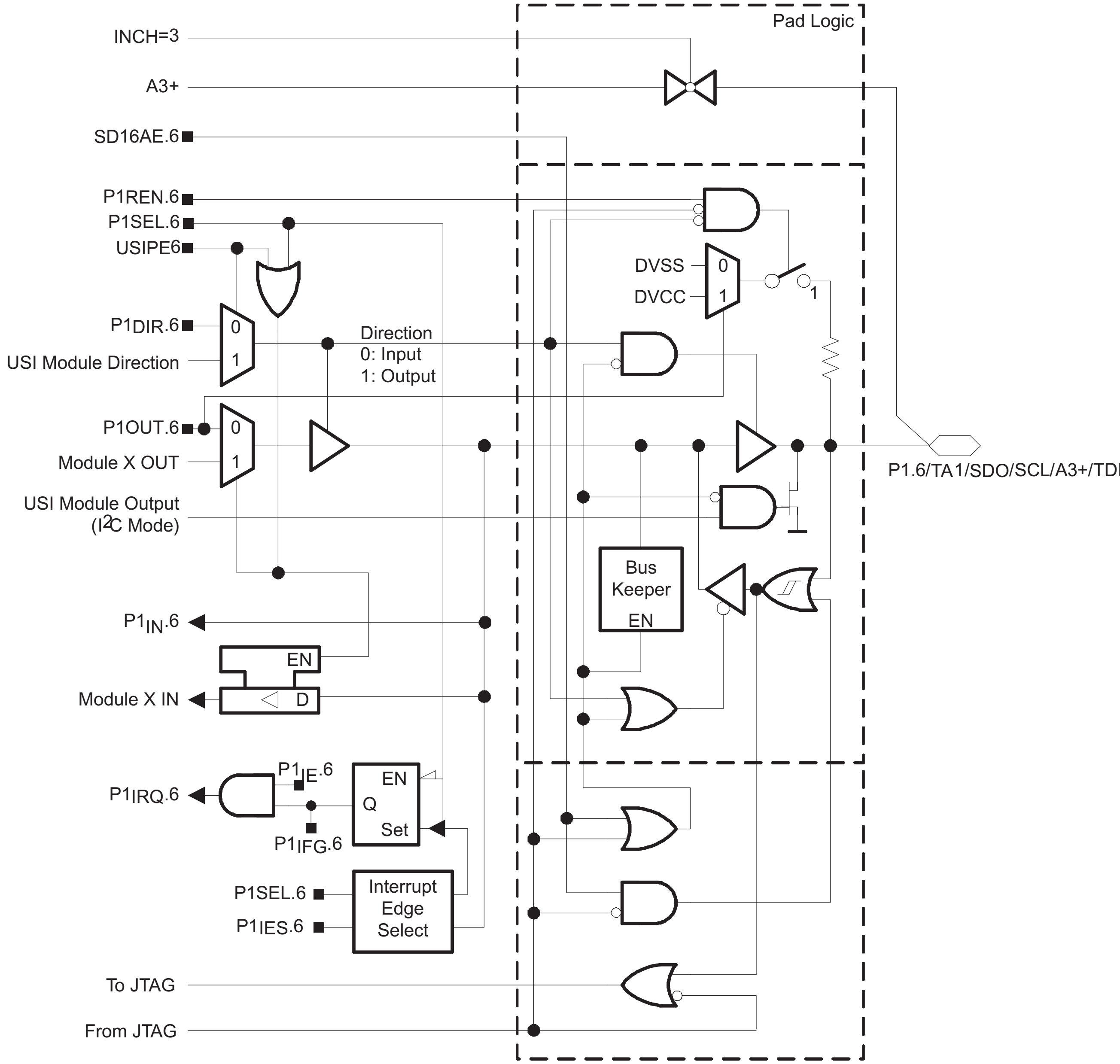
Port P1 (P1.4) Pin Schematics



Port P1 (P1.5) Pin Schematics



Port P1 (P1.6) Pin Schematics



Port P1 (P1.7) Pin Schematics

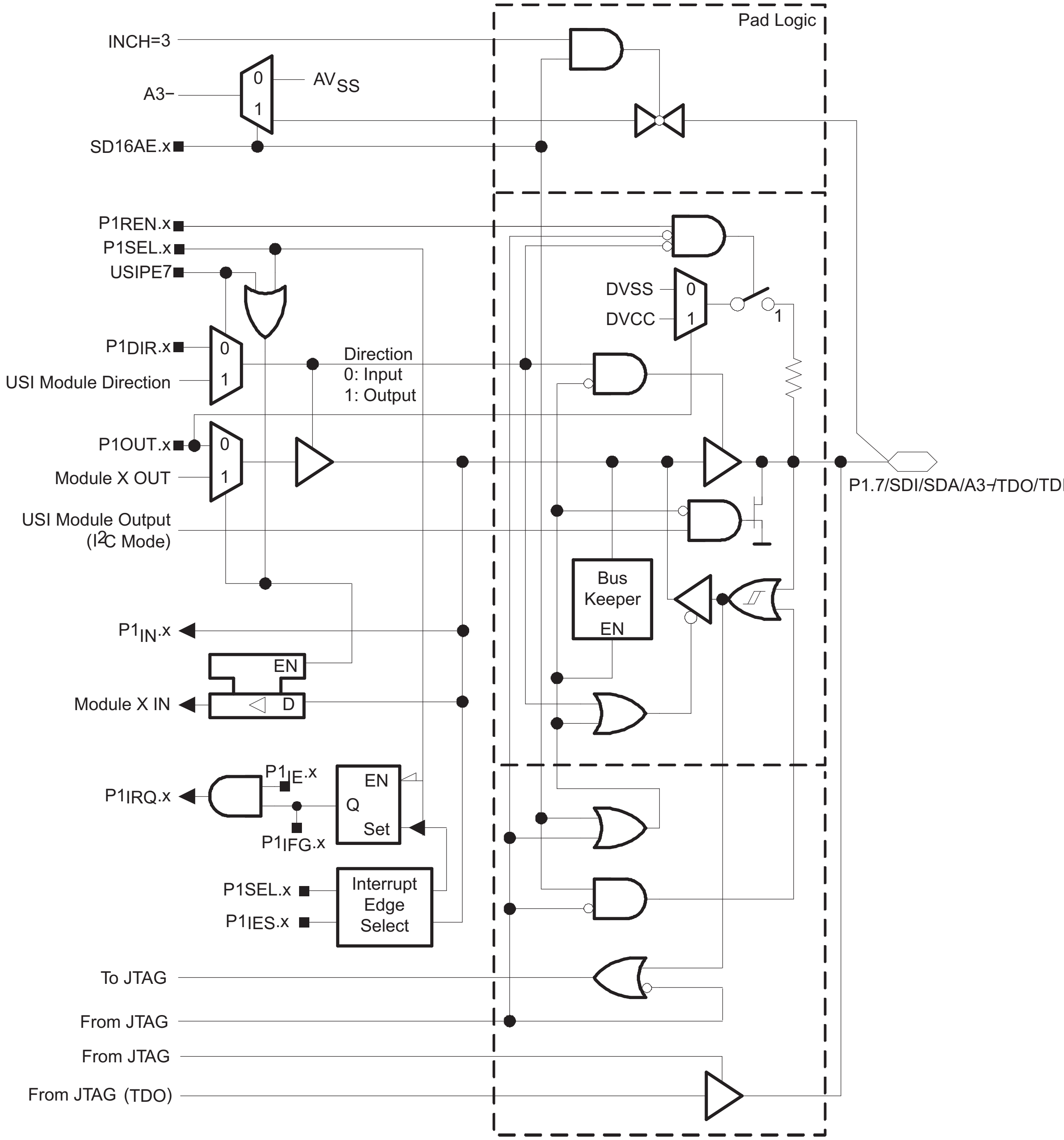


Table 14. Port P1 (P1.4 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[(1)(2)]					
			P1DIR.x	P1SEL.x	USIP.x	SD16AE.x	INCHx	JTAG Mode
P1.4/SMCLK/A2+/TCK	4	P1.4[(3)] input/output	0/1	0	N/A	0	N/A	0
		N/A	0	1	N/A	0	N/A	0
		SMCLK	1	1	N/A	0	N/A	0
		A2+[(4)]	X	X	N/A	1	2	0
		TCK[(5)]	X	X	N/A	X	X	1
P1.5/TA0/SCLK/A2-/TMS	5	P1.5[(3)] input/output	0/1	0	0	0	N/A	0
		N/A	0	1	0	0	N/A	0
		Timer_A2.TA0	1	1	0	0	N/A	0
		SCLK	X	X	1	0	N/A	0
		A2-[(4)(6)]	X	X	X	1	2	0
		TMS[(5)]	X	X	X	X	X	1
P1.6/TA1/SDO/SCL/ A3+/TDI	6	P1.6[(3)] input/output	0/1	0	0	0	N/A	0
		Timer_A2.CCI1B	0	1	0	0	N/A	0
		Timer_A2.TA1	1	1	0	0	N/A	0
		SDO (SPI) / SCL (I2C)	X	X	1	0	N/A	0
		A3+[(4)]	X	X	X	1	3	0
		TDI[(5)]	X	X	X	X	X	1
P1.7/SDI/SDA/A3-/ TDO/TDI	7	P1.7[(3)] input/output	0/1	0	0	0	N/A	0
		N/A	0	1	0	0	N/A	0
		DVSS	1	1	0	0	N/A	0
		SDI (SPI) / SDA (I2C)	X	X	1	0	N/A	0
		A3-[(4)(6)]	X	X	X	1	3	0
		TDO/TDI[(5)(7)]	X	X	X	X	X	1

(1) X = Don't care
(2) N/A = Not available or not applicable
(3) Default after reset (PUC/POR)
(4) Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(5) In JTAG mode the internal pullup/down resistors are disabled.
(6) With SD16AE.x = 0 the negative inputs are connected to VSS if the corresponding input is selected.
(7) Function controlled by JTAG

Port P2 (P2.6) Pin Schematics

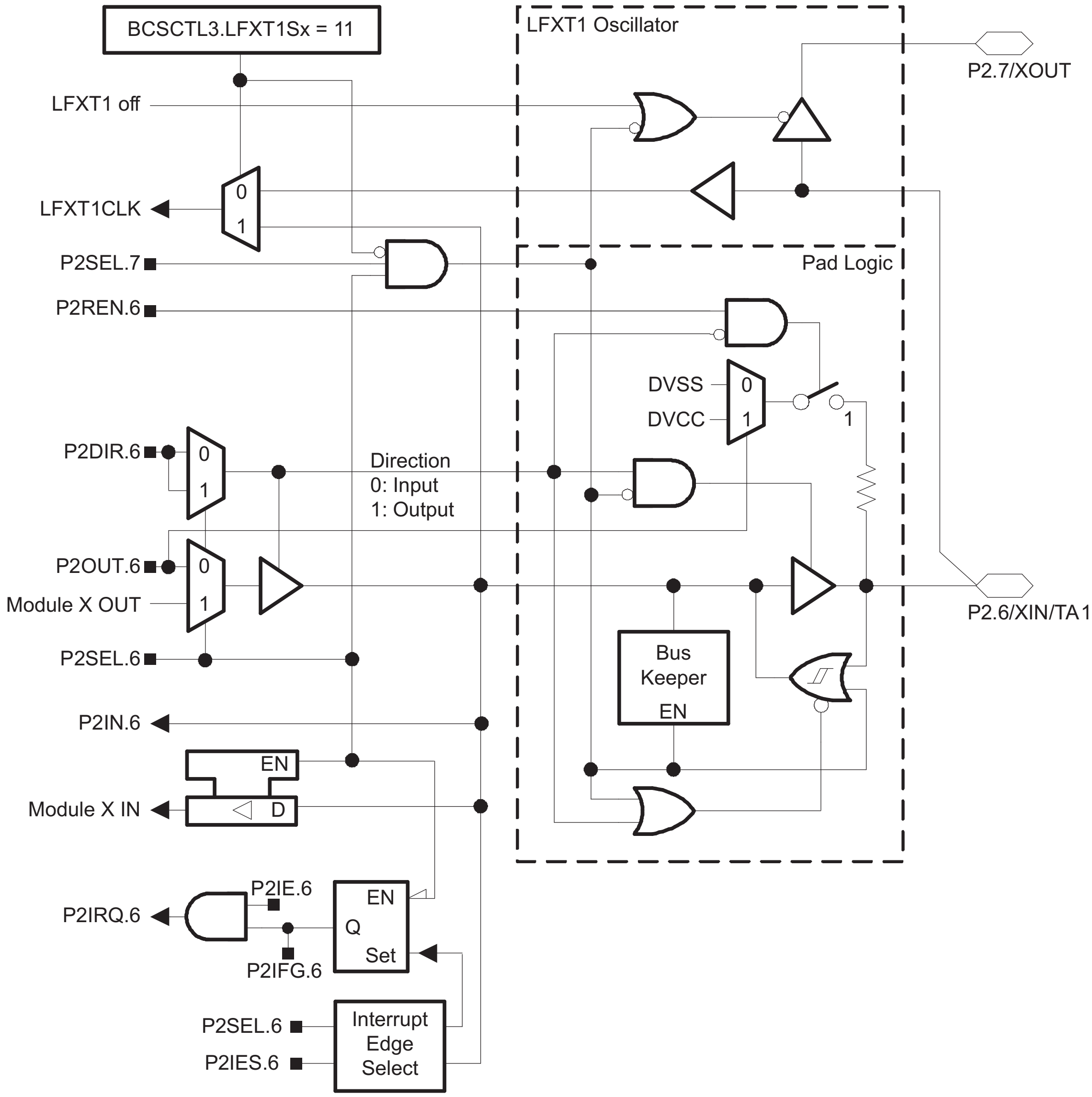


Table 15. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.6/XIN/TA1	6	P2.6 input/output	0/1	0
		XIN (1) (2)	0	1
		Timer_A2.TA1	1	1

(1) Default after reset (PUC/POR)
(2) XIN is used as digital clock input if the bits LFXT1Sx in register BCSCTL3 are set to 11.

Port P2 (P2.7) Pin Schematics

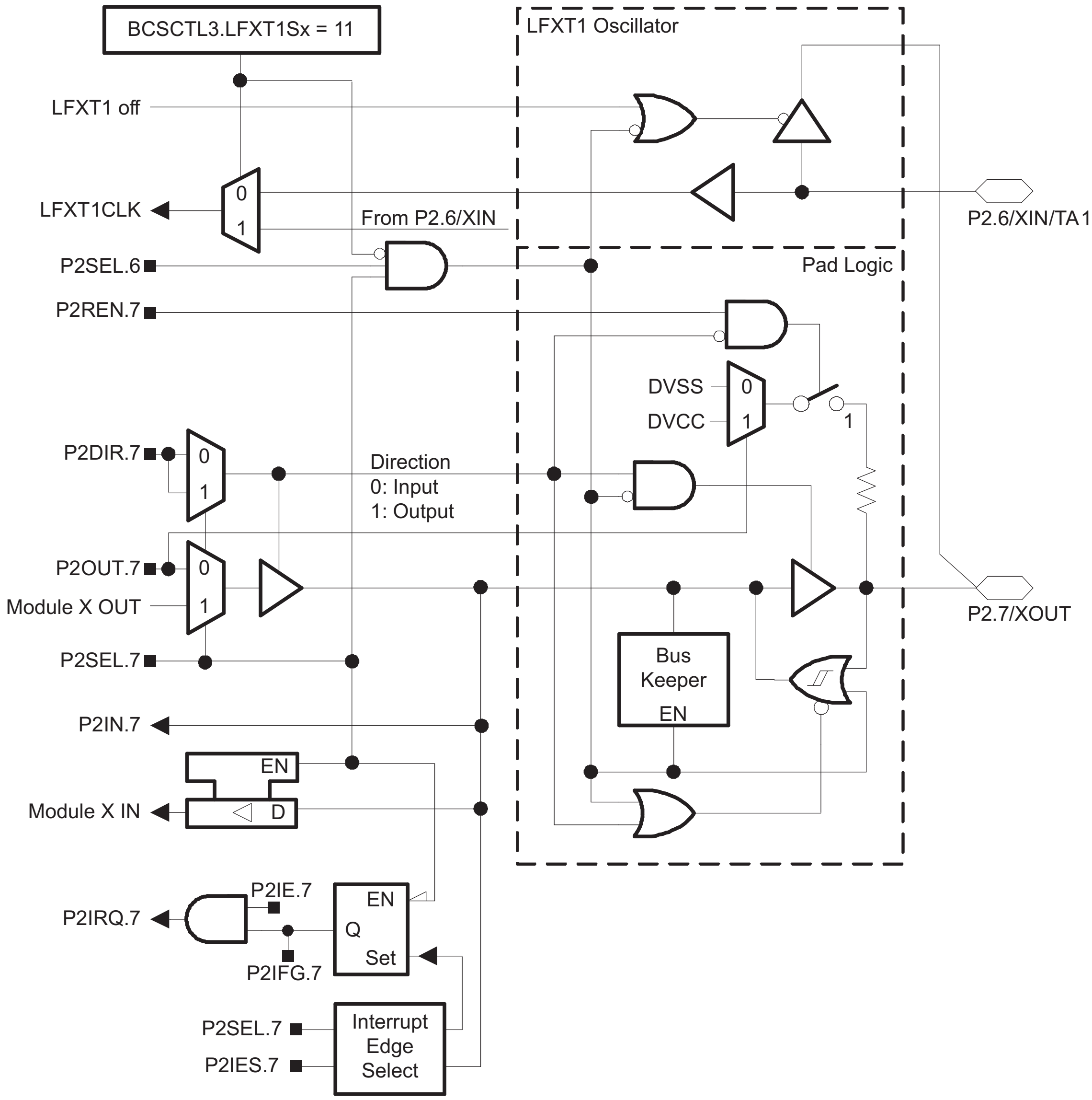


Table 16. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.7/XOUT	7	P2.7 input/output	0/1	0
		DVSS	0	1
		XOUT(1)(2)	1	1

(1) Default after reset (PUC/POR)
(2) If the pin P2.7/XOUT is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2013QRSATEP	ACTIVE	QFN	RSA	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M430F 2013Q	Samples
V62/11613-01XE	ACTIVE	QFN	RSA	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M430F 2013Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF MSP430F2013-EP :

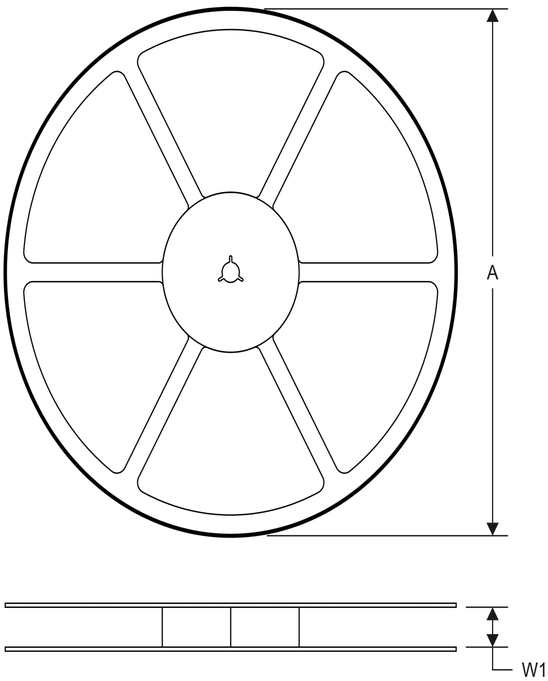
- Catalog: MSP430F2013

NOTE: Qualified Version Definitions:

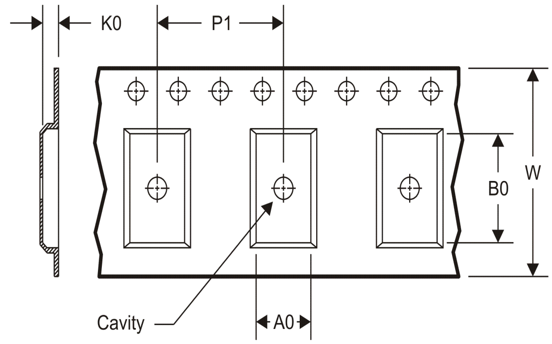
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



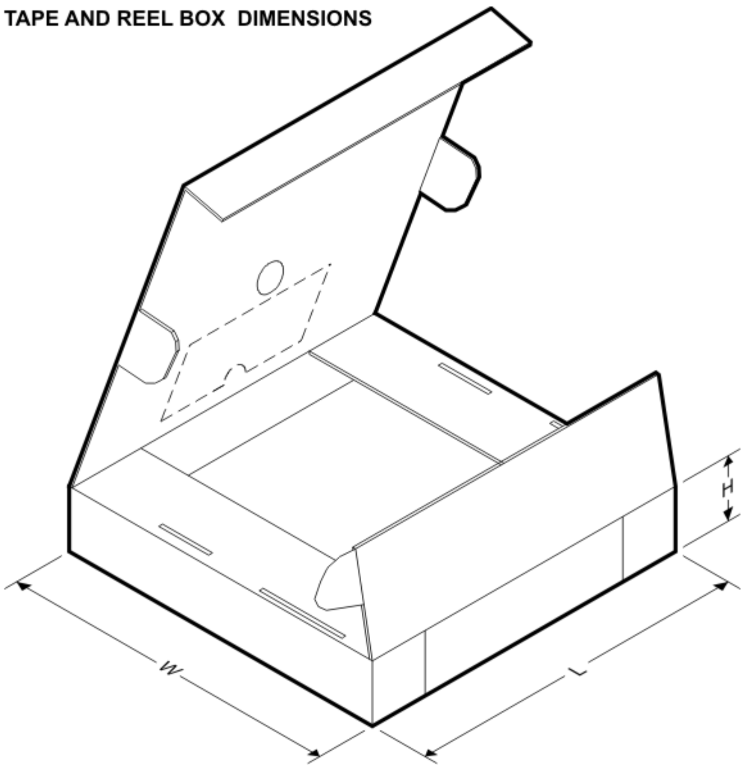
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2013QRSATEP	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

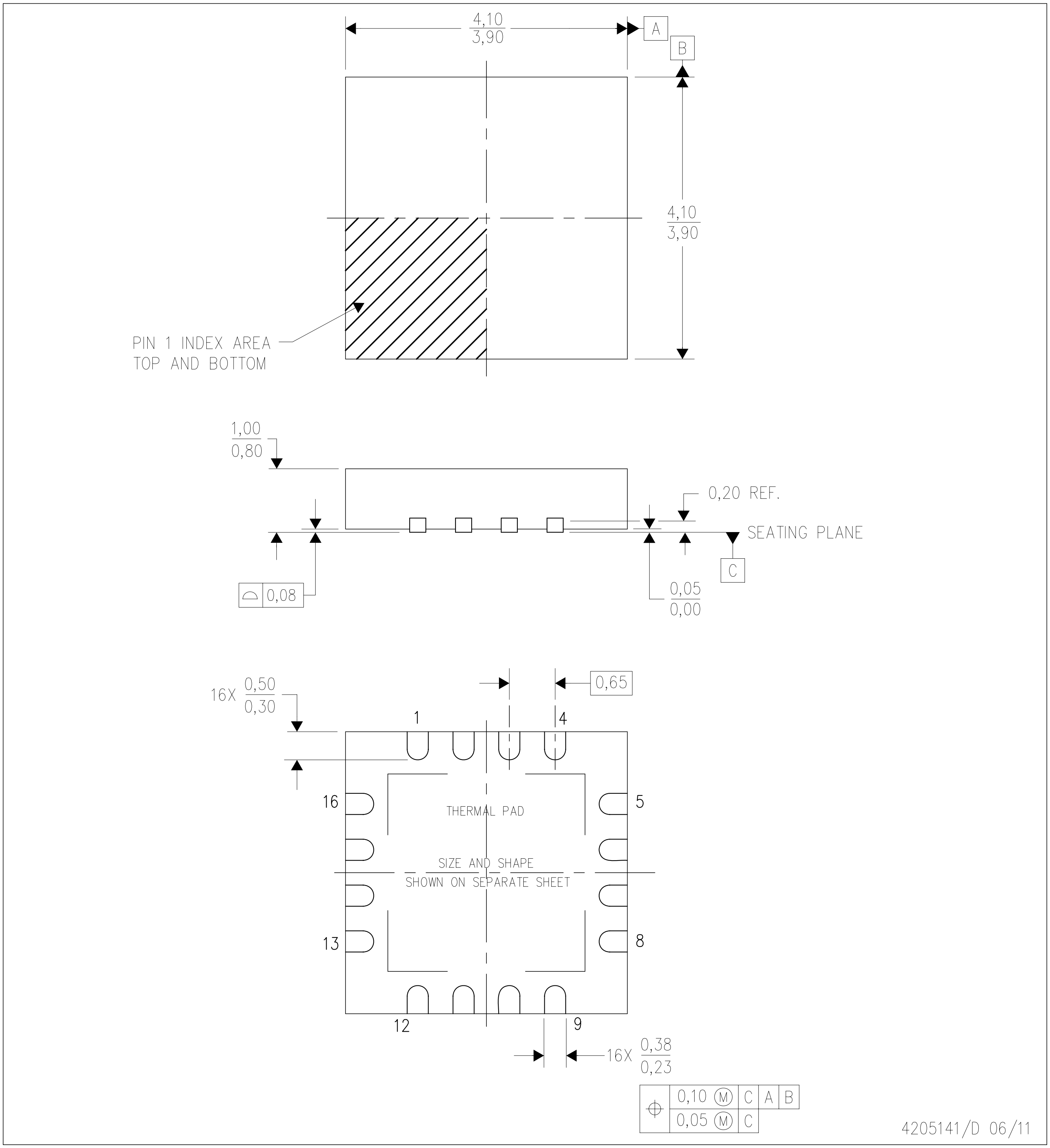
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2013QRSATEP	QFN	RSA	16	250	210.0	185.0	35.0

RSA (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

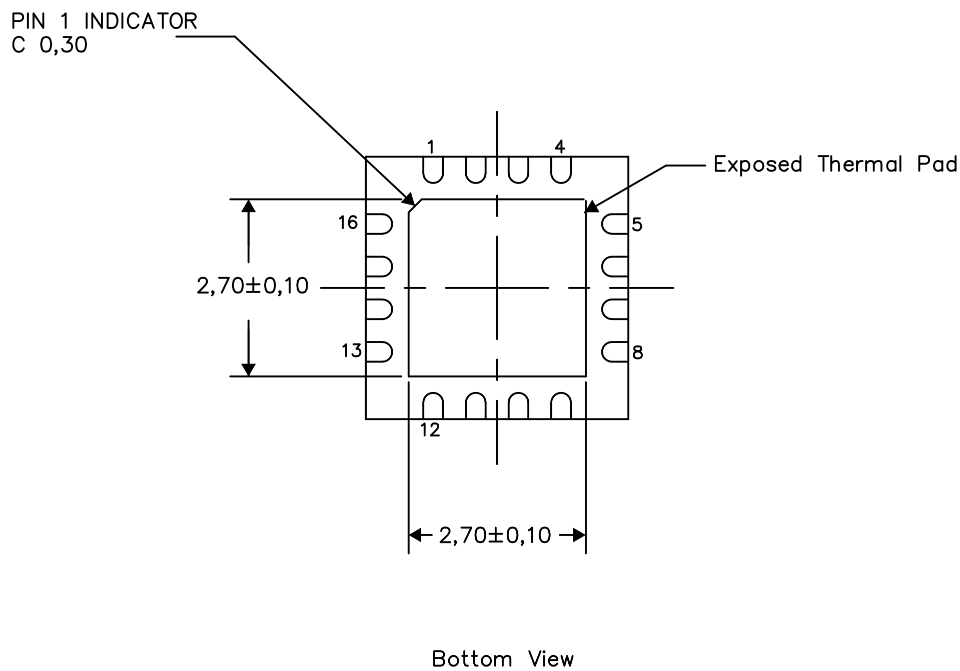
RSA (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

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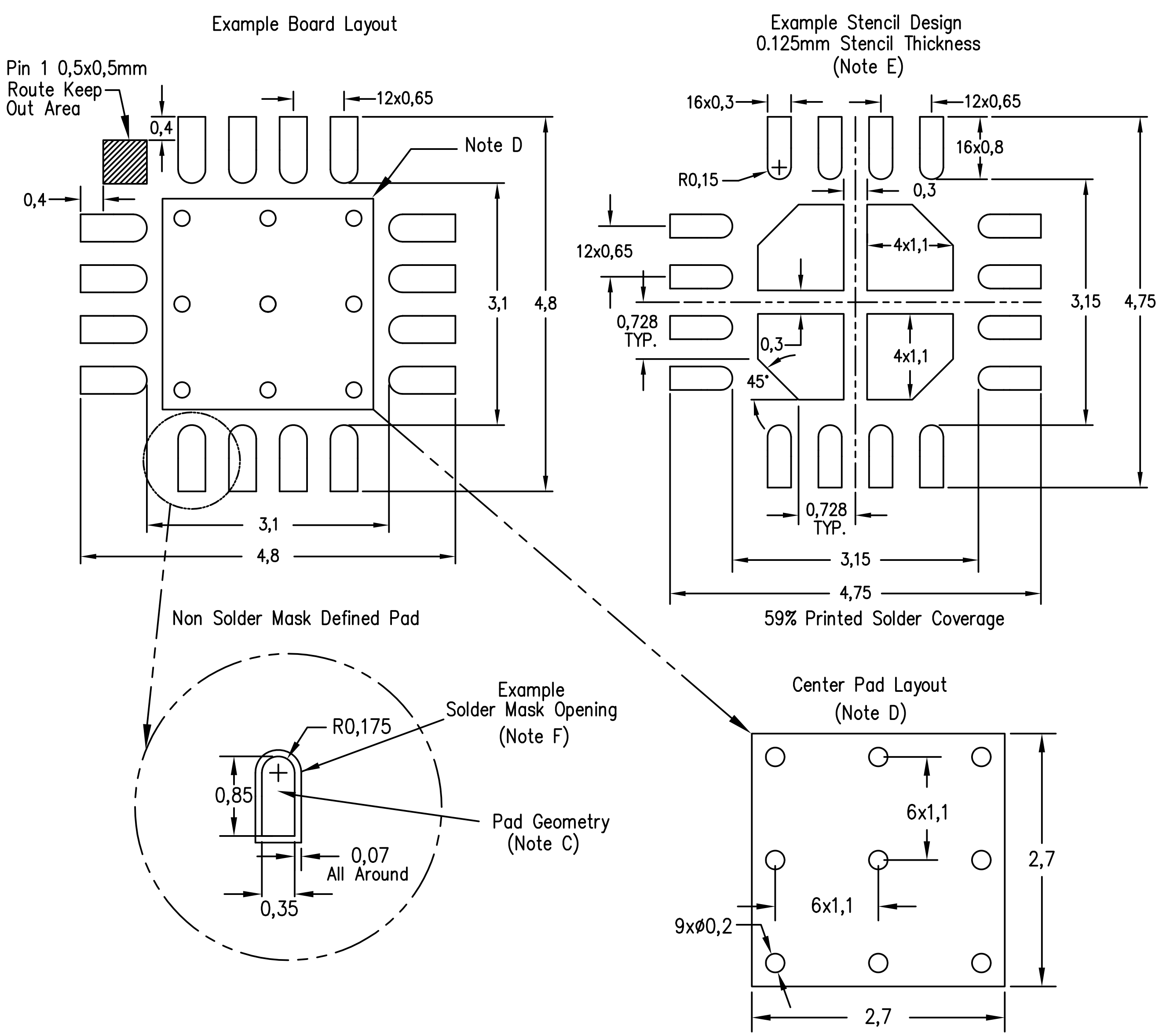
NOTES:
A. All linear dimensions are in millimeters

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.