CHANGE NOTIFICATION

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900

July 22, 2014

Dear Sir/Madam: PCN# 072214

Subject: Notification of Change to LTC2484, LTC2485 Datasheet

Please be advised that Linear Technology Corporation has made a change to the LTC2484, LTC2485 specifications in order to improve device manufacturability. The Maximum External Oscillator Frequency (f_{EOSC}) in the Timing Characteristics is being reduced from 4000kHz to 1000kHz.
In addition, the on-chip PTAT signal (Internal PTAT Signal) performance and summary of Output Data Format (Table 3) have been clarified as shown in the attached datasheet pages. No changes are being made to the circuit or the test methodology. Product shipped after September 22, 2014 will be tested to the new limit.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by email at JASON.HU@LINEAR.COM. If I do not hear from you by September 22, 2014, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 15)	●	10		~~4000~~ 1000	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		60Hz Mode	●	131.0	133.6	136.3	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		External Oscillator	●		41036/f_{EOSC} (in kHz)		ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		External Oscillator	●		20556/f_{EOSC} (in kHz)		ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10)			38.4		kHz
		External Oscillator (Notes 10, 11)			f_{EOSC}/8		kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 10)	●			4000	kHz
t_{LESCK}	External SCK Low Period	(Note 10)	●	125			ns
t_{HESCK}	External SCK High Period	(Note 10)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12)	●	0.81	0.83	0.85	ms
		External Oscillator (Notes 10, 11)	●		256/f_{EOSC} (in kHz)		ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 10)	●		32/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}\downarrow$ to SDO Low		●	0		200	ns
t_2	$\overline{CS}\uparrow$ to SDO Hi-Z		●	0		200	ns
t_3	$\overline{CS}\downarrow$ to SCK$\downarrow$	(Note 10)	●	0		200	ns
t4	$\overline{CS}\downarrow$ to SCK$\uparrow$	(Note 10)	●	50			ns
t_{KQMAX}	SCK$\downarrow$ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK$\downarrow$	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}\downarrow$		●	50			ns
t_6	SCK Hold After $\overline{CS}\downarrow$		●			50	ns
t_7	SDI Setup Before SCK$\uparrow$	(Note 5)	●	100			ns
t_8	SDI Hold After SCK$\uparrow$	(Note 5)	●	100			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REFCM} = V_{REF}/2$, FS = $0.5V_{REF}$

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ + IN^-)/2$

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as digital input and the driving clock is f_{ESCK}. In internal SCK mode, the SCK pin is used as digital output and the output clock signal during the data output is f_{ISCK}.

Note 11: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.

Note 15: Refer to Applications Information section for performance vs data rate graphs.

Note 16: For V_{CC} < 3V, V_{IH} is 2.5V for pin f_O.

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	10		~~4000~~1000	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		60Hz Mode	●	131.0	133.6	136.3	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		External Oscillator (Note 10)	●		41036/f_{EOSC}		ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		External Oscillator (Note 10)	●		20556/f_{EOSC}		ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(SDA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for Both SDA and SCL Signals	(Note 14)	●	20+0.1C_B		300	ns
t_f	Fall Time for Both SDA and SCL Signals	(Note 14)	●	20+0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REF} = REF^+ – REF^–$, $V_{REFCM} = (REF^+ + REF^–)/2$, FS = 0.5$V_{REF}$; $V_{IN} = IN^+ – IN^–$, $V_{INCM} = (IN^+ + IN^–)/2$.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the CA0/f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses the internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF.

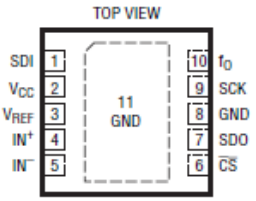
Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 6V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2484C ..... 0°C to 70°C
LTC2484I ..... –40°C to 85°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2484CDD#PBF	LTC2484CDD#TRPBF	LBSS	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2484IDD#PBF	LTC2484IDD#TRPBF	LBSS	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (NORMAL SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

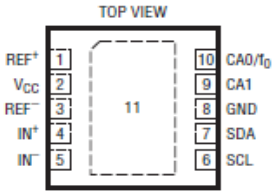
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1 ≤ V_{REF} ≤ V_{CC}, –FS ≤ V_{IN} ≤ +FS (Note 5)	●	24			Bits
Integral Nonlinearity	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)	●		2 1	10	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 14)	●		0.5	2.5	µV
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC}			10		nV/°C
Positive Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}	●			25	ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}	●			25	ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Total Unadjusted Error	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V 5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V			15		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Output Noise	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, GND ≤ IN^- = IN^+ ≤ V_{CC} (Note 13)			0.6		μV_{RMS}
Internal PTAT Signal	T_A = 27°C		390	~~420~~	450	mV
~~Internal PTAT Temperature Coefficient~~				~~1.4~~		~~mV/°C~~

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 6V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2485C ..... 0°C to 70°C
LTC2485I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2485CDD#PBF	LTC2485CDD#TRPBF	LBST	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2485IDD#PBF	LTC2485IDD#TRPBF	LBST	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (NORMAL SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1 ≤ V_{REF} ≤ V_{CC}, –FS ≤ V_{IN} ≤ +FS (Note 5)	●	24			Bits
Integral Nonlinearity	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)	●		2 1	10	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 13)	●		0.5	2.5	µV
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC}			10		nV/°C
Positive Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}	●			25	ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^- = 0.75V_{REF}, IN^+ = 0.25V_{REF}	●			25	ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^- = 0.75V_{REF}, IN^+ = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Total Unadjusted Error	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6) 5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)			15 15 15		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Output Noise	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, GND ≤ IN^- = IN^+ ≤ V_{CC} (Note 12)			0.6		μV_{RMS}
Internal PTAT Signal	T_A = 27°C		390	~~420~~	450	mV
~~Internal PTAT Temperature Coefficient~~				~~1.4~~		~~mV/°C~~

Table 3. LTC2484 Output Data Format

DIFFERENTIAL INPUT VOLTAGE V_{IN}*	BIT 31 EOC	BIT 30 DMY	BIT 29 SIG	BIT 28 MSB	BIT 27	BIT 26	BIT 25	...	BIT 0
V_{IN}* ≥ FS**	0	0	1	1	0	0	0	...	0
FS** – 1LSB	0	0	1	0	1	1	1	...	1
0.5 • FS**	0	0	1	0	1	0	0	...	0
0.5 • FS** – 1LSB	0	0	1	0	0	1	1	...	1
0	0	0	1/0***	0	0	0	0	...	0
–1LSB	0	0	0	1	1	1	1	...	1
–0.5 • FS**	0	0	0	1	1	0	0	...	0
–0.5 • FS** – 1LSB	0	0	0	1	0	1	1	...	1
–FS**	0	0	0	1	0	0	0	...	0
V_{IN}* < –FS**	0	0	0	0	1	1	1	...	****

* The differential input voltage $V_{IN} = IN^+ – IN^–$.
** The full-scale voltage FS = 0.5 • V_{REF}.
*** The sign bit changes state during the 0 output code when the device is operating in the 2× speed mode.
**** When operating in the 2× speed mode, the underrange output code is 0xOFFFFxxx.

Table 3. LTC2485 Output Data Format

DIFFERENTIAL INPUT VOLTAGE V_{IN}*	BIT 31 SIG	BIT 30 MSB	BIT 29	BIT 28	BIT 27	...	BIT 0
V_{IN}* ≥ FS**	1	1	0	0	0	...	0
FS** – 1LSB	1	0	1	1	1	...	1
0.5 • FS**	1	0	1	0	0	...	0
0.5 • FS** – 1LSB	1	0	0	1	1	...	1
0	1/0***	0	0	0	0	...	0
–1LSB	0	1	1	1	1	...	1
–0.5 • FS**	0	1	1	0	0	...	0
–0.5 • FS** – 1LSB	0	1	0	1	1	...	1
–FS**	0	1	0	0	0	...	0
V_{IN}* < –FS**	0	0	1	1	1	...	****

* The differential input voltage $V_{IN} = IN^+ – IN^–$.
** The full-scale voltage FS = 0.5 • V_{ROF}.
*** The sign bit changes state during the 0 output code when the device is operating in the 2x speed mode.
**** When operating in the 2x speed mode, the underrange output is 0x3FFFxxx.