STDP2690
Advanced DisplayPort to DisplayPort (dual mode) converter

Datasheet

Rev A

MegaChips

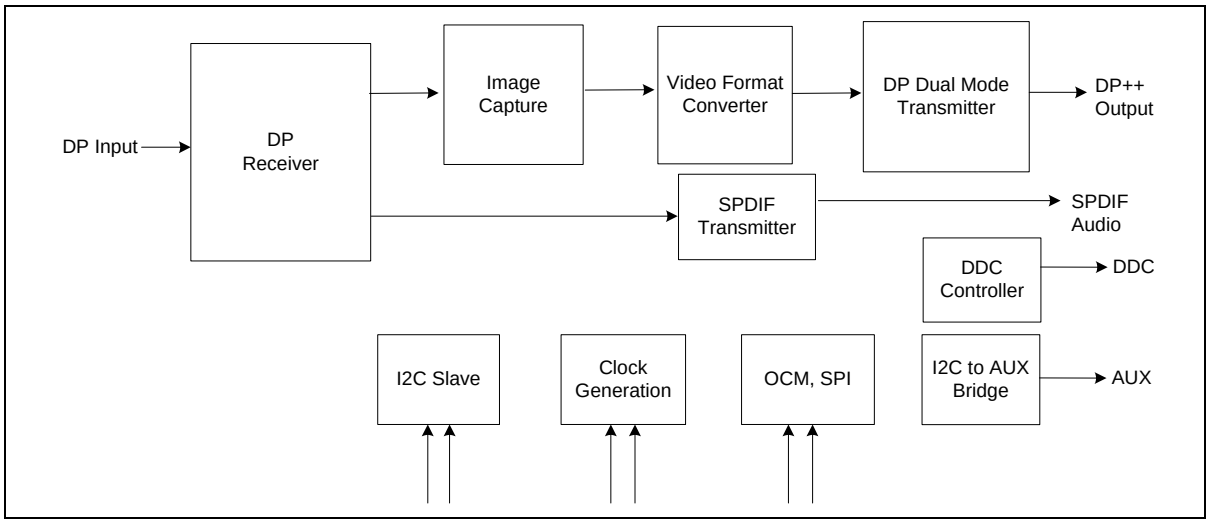
MegaChips' Proprietary Information

Features

- DisplayPort® dual-mode transmitter
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - Supports eDP operation
  - HDMI/DVI operation with level translator
- DisplayPort receiver
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - Supports eDP operation
- SPDIF audio output
  - 192 kHz/24 bits
  - Compressed/LPCM
- HDCP repeater with embedded keys
- ASSR - eDP display authentication option
- AUX to I2C bridge for EDID/MCCS pass through
- Spread spectrum on DisplayPort interface for EMI reduction
- Device configuration options
  - SPI Flash
  - I2C host interface
- Deep color support
  - RGB/YCC (4:4:4) – 16-bit color
  - YCC (4:2:2) – 16-bit color
  - Color space conversion – YUV to RGB and RGB to YUV
- Bandwidth
  - Video resolution up to 4K x 2K @ 30 Hz; 1920 x 1080 @ 120 Hz
  - Audio 7.1 Ch up to 192 kHz sample rate
- Low power operation; active 493 mW, standby 21 mW
- Package
  - 81 BGA (8 x 8 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- Audio-video accessory (dongle) for PC/notebooks and docking stations
- Thunderbolt source and peripheral devices



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1. Description

The STDP2690 is a high-speed DisplayPort to DisplayPort dual mode converter IC targeted for applications such as audio-video accessories, docking stations, Thunderbolt storage devices, etc. This device includes a VESA DP Standard Ver. 1.2a compliant receiver and transmitter, implementing single link DisplayPort input and output ports comprising four Main lanes, AUX CH, and HPD.

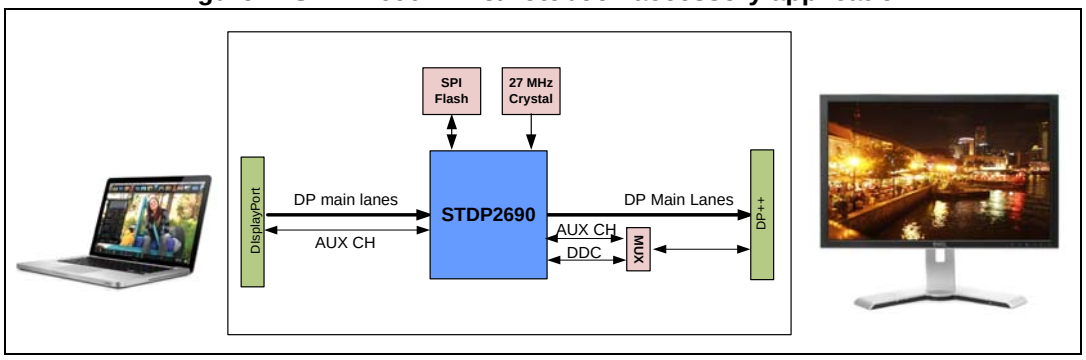
The STDP2690 uses MegaChips' latest generation DisplayPort dual mode transmitter technology that supports both DisplayPort and TMDS signal formats (DP++). DisplayPort receiver and transmitter support HBR2 speed, a data rate of 5.4 Gbps per lane with a total bandwidth of 21.6 Gbps link rate. The transmitter is capable of supporting HDMI or single link DVI output through a passive level translator (dongle). When configured as HDMI output, this device supports link rate up to 2.97 Gbps that corresponds to a pixel rate of 297 MHz, adequate for handling video timings up to FHD 120 Hz 3D formats. This device delivers deep color video up to 16-bits per color at 1080p 60 Hz and lower video resolutions. The STDP2690 allows audio transport from the source to desired audio rendering devices over the DP++ output or through the SPDIF port. The audio signal from the source can be routed simultaneously to DP++ and SPDIF output ports. For example, the STDP2690 allows routing of any two audio channels on the SPDIF port, while transporting up to eight channels on the DP++ port.

The STDP2690 supports RGB and YCbCr colorimetric formats with color depth of 16, 12, 10, and 8 bits. This device features HDCP 1.3 content protection scheme with an embedded key option for secure transmission of digital audio-video content. It also operates as an HDCP repeater for the downstream sink. The eDP authentication option ASSR (Alternative Scrambler Seed Reset) is supported for embedded application.

The AUX-to-I2C translator in the STDP2690 allows the upstream DisplayPort source to access EDID and transfer MCCS commands to a downstream sink over the HDMI interface when used with a level translator. This device has an on-chip microcontroller with SPI and I2C host interface for system configuration purposes. STDP2690 can be configured with an external SPI Flash for custom applications. In addition, it allows register level configuration from an external host controller through I2C interface.

2. Application overview

Figure 1. STDP2690 in PC/notebook accessory application



3. Feature attributes

3.1 Input interface

- DP standard Ver. 1.2a compliant
- Main link configuration (SST format only, no MST format support)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: 1 Mbps Manchester transaction format
- HPD: IRQ_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB or YCC422 or YcC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates

3.2 Output interface

- DP++ transmitter interface featuring
  - AC coupled DisplayPort Ver. 1.2a interface
  - AC coupled HDMI 1.4 interface to external level translators
- DP main link configuration (SST format only, no MST format support)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: Manchester transaction format
- HPD: IRQ_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB or YCC422 or YcC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates
- HDMI link rate: 2.97 Gbps/data pair max

3.3 Deep color support

- RGB/YCC (4:4:4) – 16-bit color
- YCC (4:2:2) – 16-bit color
- Color space conversion – YUV to RGB and RGB to YUV

3.4 Supported video timings

- 4096 x 2160 (4K x 2K) 60 Hz: 24 bits/pixel (DP to DP only)
- 4096 x 2160 (4K x 2K) 24 Hz/30 Hz: 24 bits/pixel (DP to HDMI)
- 1920 x 1080 (FHD) 120 Hz: 24 bits/pixel
- 2560 x 1600 (WQXGA) 60 Hz: 24 bits/pixel
- Up to 1920 x 1080 (FHD) 60 Hz, 48, 36, 30 bits/pixel
- All compatible 3D formats defined in DP 1.2a and HDMI 1.4 specifications
- All standard CEA861 timing formats

3.5 Supported audio timings

- All audio formats as specified in DP 1.2a and HDMI 1.4 specifications
- SPDIF; 2-Ch LPCM, AC3, DTS, bit depth up to 24 bits, sample rate up to 192 kHz

3.6 Control channel interfaces

- AUX CH, I2C host interface, SPI (optional), and UART (UART for test/debug purposes only)

3.7 HDCP 1.3 support

- Key sets for DP RX and DP/HDMI TX integrated in one-time programmable ROM (OTP)
- Standalone HDCP repeater capability
- Supports eDP display authentication option ASSR (Alternate Scrambler Seed Reset)

3.8 Package

- 81 BGA (8 x 8 mm), 0.8 ball pitch

3.9 Power supply voltages

- 3.3 V I/O; 1.2 V core

3.10 ESD

- 2 KV HBM, 500 V CDM

4. BGA footprint and pin lists

4.1 Ball grid array diagram

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

Some signal names in BGA diagrams have been abbreviated. Refer to*Table 2: Pin list on page 14* for full signal names sorted by pin number.

Table 1. Key to BGA diagrams

Function	Type	Key
AVDD12_RX	VCC/VDD	
AVDD33_RX	VCC/VDD	
AVDD33_RCOSC	VCC/VDD	
AVDD12_TX	VCC/VDD	
AVDD33_TX	VCC/VDD	
DVDD12	VCC/VDD	
DVDD33	VCC/VDD	
System ground	VSS/GND	
No connect/Do not connect	NC/DNC	NC

The STDP2690 is available in a 81-pin BGA package.

Figure 2. STDP2690 BGA diagram

	01	02	03	04	05	06	07	08	09	
A	CPHY_RX3_N	CPHY_RX3_P	CPHY_RX2_N	CPHY_RX2_P	CPHY_RX1_N	CPHY_RX1_P	CPHY_RX0_N	CPHY_RX0_P	CPHY_RXAUXP	A
B	SPI_DI	SPI_CSN	AVDD12_RX	AVDD12_RX	AVDD33_RX	CPHY_RX_REXT	AVDD12_PLL	TEST_MISN	CPHY_RXAUXN	B
C	SPI_CLK	SPI_DO	VSS	VSS	AVDD33_RX	AVDD33_RX	AVDD33_RCOSC	TESTMODE0_ CONFIG1	UART_RX	C
D	PWR_CTRL	I2C_SDA	DVDD12	VSS	VSS	VSS	DVDD12	TESTMODE1_ CONFIG2	UART_TX	D
E	CHRG_CTRL	I2C_SCL	DVDD12	VSS	VSS	VSS	DVDD12	VSS	IRQ	E
F	PWR_SENSE	SPDIF	DVDD33	VSS	VSS	VSS	VSS	HPD_OUT_ AUX_HPD	CEC	F
G	HPD_IN	HDMITX_DDC_SDA	DVDD33	VSS	VSS	AVDD33_TX	VSS	RESETn	XTAL	G
H	DPTX_AUXN	HDMITX_DDC_SCL	TX_REXT	AVDD12_TX	AVDD12_TX	AVDD12_TX	AVDD12_OSC	DVDD25_SM	TCLK	H
J	DPTX_AUXP	DPTX_L3N_ HDMI_TXCKN	DPTX_L3P_ HDMI_TXCKP	DPTX_L2N_ HDMI_TX0N	DPTX_L2P_ HDMI_TX0P	DPTX_L1N_ HDMI_TX1N	DPTX_L1P_ HDMI_TX1P	DPTX_L0N_ HDMI_TX2N	DPTX_L0P_ HDMI_TX2P	J
	01	02	03	04	05	06	07	08	09	

4.2 Full pin list sorted by pin number

Table 2. Pin list

Pin number	Net name
A1	CPHY_RX3_N
A2	CPHY_RX3_P
A3	CPHY_RX2_N
A4	CPHY_RX2_P
A5	CPHY_RX1_N
A6	CPHY_RX1_P
A7	CPHY_RX0_N
A8	CPHY_RX0_P
A9	CPHY_RXAUXP
B1	SPI_DI
B2	SPI_CSN
B3, B4	AVDD12_RX
B5	AVDD33_RX
B6	CPHY_RX_REXT
B7	AVDD12_PLL
B8	TEST_MISN
B9	CPHY_RXAUXN
C1	SPI_CLK
C2	SPI_DO
C3, C4	VSS
C5, C6	AVDD33_RX
C7	AVDD33_RCOSC
C8	CONFIG1
C9	UART_RX
D1	PWR_CTRL
D2	I2C_SDA
D3	DVDD12
D4, D5, D6	VSS
D7	DVDD12
D8	CONFIG2
D9	UART_TX
E1	CHRG_CTRL
E2	I2C_SCL

Table 2. Pin list (continued)

Pin number	Net name
E3	DVDD12
E4, E5, E6	VSS
E7	DVDD12
E8	VSS
E9	IRQ
F1	PWR_SENSE
F2	SPDIF
F3	DVDD33
F4, F5, F6, F7	VSS
F8	HPD_OUT_AUX_HPD
F9	CEC
G1	HPD_IN
G2	HDMITX_DDC_SDA
G3	DVDD33
G4, G5	VSS
G6	AVDD33_TX
G7	VSS
G8	RESETn
G9	XTAL
H1	DPTX_AUXN
H2	HDMITX_DDC_SCL
H3	TX_REXT
H4, H5, H6	AVDD12_TX
H7	AVDD12_OSC
H8	DVDD25_SM
H9	TCLK
J1	DPTX_AUXP
J2	DPTX_L3N_HDMI_TXCKN
J3	DPTX_L3P_HDMI_TXCKP
J4	DPTX_L2N_HDMI_TX0N
J5	DPTX_L2P_HDMI_TX0P
J6	DPTX_L1N_HDMI_TX1N
J7	DPTX_L1P_HDMI_TX1P
J8	DPTX_L0N_HDMI_TX2N
J9	DPTX_L0P_HDMI_TX2P

5. Connections

5.1 Pin list

I/O Legend: I = Input; O = Output; P = Power; G = Ground; IO = Bi-direction; AI = Analog input; AO = Analog output; AIO = Analog I/O; TRI = Tristate; TOL = Tolerance; PD = Internal 50K pulldown; PU = Internal 50K pull-up; OPENDR = Open drain output

Note: Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the Description column.

Table 3. DisplayPort receiver pins

Pin	Assignment	I/O	Description	Reset state
B9	CPHY_RXAUXN	AIO, 3V3 tol	AC couple 0.1uF. Use 20 ohm damping resistor in series and 1M ohm pull down to GND before cap.	Tristate
A9	CPHY_RXAUXP	AIO, 3V3 tol	AC couple 0.1uF. Use 20 ohm damping resistor in series and 1M ohm pull up to 3.3 V before cap.	Tristate
B6	CPHY_RX_REXT	AI, 3V3 tol	Combo receiver external 249 ohm resistor to VDD33.	NA
A8	CPHY_RX0_P	AI, 3V3 tol	AC couple 0.1uF. Use 100K ohm pull down to GND between the connector and AC-coupling cap.	Input
A7	CPHY_RX0_N			
A6	CPHY_RX1_P			
A5	CPHY_RX1_N			
A4	CPHY_RX2_P			
A3	CPHY_RX2_N			
A2	CPHY_RX3_P			
A1	CPHY_RX3_N			

Table 4. System function pins

Pin	Assignment	I/O	Description	Reset state
B8	TEST_MISN	I, 3V3 tol, TRI, INT PD	Connect to GND	Input, Low
H9	TCLK	AIO, 1V2 tol	Connect to 27 MHz crystal oscillator with 22 pF to 1.2V	NA
G9	XTAL	AIO, 1V2 tol		
G8	RESETn	AIO, 3V3 tol	3K ohm resistor to 3.3V	NA
B2	SPI_CSN	IO, 3V3 tol, TRI, INT PU	To SPI chip select. Also see bootstraps.	Output, High
C2	SPI_DO	IO, 3V3 tol, TRI INT PD	To SPI data out. Also see bootstraps.	Output, Low

Table 4. System function pins

Pin	Assignment	I/O	Description	Reset state
B1	SPI_DI	IO, 3V3 tol, TRI, INT PD	From SPI data in.	Input, Low
C1	SPI_CLK	IO, 3V3 tol, TRI, INT PD	To SPI clock. Also see bootstraps.	Output, Low

Table 5. General purpose input/output and multi-function pins

Pin	Assignment	I/O	Description	Reset state
F9	CEC	3.3V IO, 5V tol, OPENDR	To CONN PIN14 with 5 M res to GND.	OPENDR
F8	HPD_OUT_AUX_HPD	IO, 3V3 tol, TRI	To the upstream HPD signal pin on the DP connector. 100K res to GND.	Output
E9	IRQ	IO, 3V3 tol, TRI	GPIO/IRQ out for host interface. Also see bootstrap function.	TRI, Low
D9	UART_TX	IO, 3V3 tol, OPENDR	To debug port UART_TX/alt I2C_SDA/GPIO. Needs external 2K res to 3.3V, FS, FT	OPENDR
C9	UART_RX	IO, 3V3 tol, OPENDR	To debug port UART_RX/alt I2C_SCL/GPIO. Needs external 2K res to 3.3V, FS, FT	Input
F2	SPDIF	IO, 3V3 tol, TRI, PU	To external buffer for SPDIF output or use as GPIO. Also see bootstrap function.	Output, High
G1	HPD_IN	IO, 5V tol, OPENDR	From HDMI connector. Needs 100K to GND.	Input
D1	PWR_CTRL	IO, 3V3 tol, TRI	Use as GPIO	Output
E1	CHRG_CTRL	IO, 3V3 tol, TRI	Use as GPIO	Output
D2	I2C_SDA	IO, 3V3 tol, TRI	GPIO/I2C_SDA slave or master, FS, FT	TRI
E2	I2C_SCL	IO, 3V3 tol, TRI	GPIO/I2C_SCL slave or master, FS, FT	TRI
F1	PWR_SENSE	IO/AI, 3V3 tol, OPENDR	GPIO/power sense analog/level sensing input, FS, FT	OPENDR
G2	HDMI_DDC_SDA	IO, 5V tol, OPENDR	GPIO/HDMI DDC SDA, FS, FT	OPENDR
H2	HDMI_DDC_SCL		GPIO/HDMI DDC SCL, FS, FT	OPENDR
D8	CONFIG2	IO, 3V3 tol, TRI	GPIO, 3.3V pad	Input
C8	CONFIG1			Input

Table 6. Transmitter pins

Pin	Assignment	I/O	Description	Reset state
H3	TX_REXT	AI, 1V2 tol	Transmitter, external 249 ohm resistor to VDD12	NA
H1	DPTX_AUXN	AIO, 1V2 tol	Dual mode transmitter DPTX_AUXN. AC couple to TX connector. External 100 K resistor to GND.	Tristate
J1	DPTX_AUXP	AIO, 1V2 tol	Dual mode transmitter DPTX_AUXP. AC couple to TX connector. External 100 K resistor to VDD33.	Tristate

Table 6. Transmitter pins

Pin	Assignment	I/O	Description	Reset state
J2	DPTX_L3N_HDMI_TXCKN	AIO, 1V2 tol	Dual mode transmitter HDMI_TXCKN or DPTX_L3N. AC couple to TX connector.	Output
J3	DPTX_L3P_HDMI_TXCKP	AIO, 1V2 tol	Dual mode transmitter HDMI_TXCKP or DPTX_L3P. AC couple to TX connector.	Output
J4	DPTX_L2N_HDMI_TX0N	AIO, 1V2 tol	Dual mode transmitter HDMI_TX0N or DPTX_L2N. AC couple to TX connector.	Output
J5	DPTX_L2P_HDMI_TX0P	AIO, 1V2 tol	Dual mode transmitter HDMI_TX0P or DPTX_L2P. AC couple to TX connector.	Output
J6	DPTX_L1N_HDMI_TX1N	AIO, 1V2 tol	Dual mode transmitter HDMI_TX1N or DPTX_L1N. AC couple to TX connector.	Output
J7	DPTX_L1P_HDMI_TX1P	AIO, 1V2 tol	Dual mode transmitter HDMI_TX1P or DPTX_L1P. AC couple to TX connector.	Output
J8	DPTX_L0N_HDMI_TX2N	AIO, 1V2 tol	Dual mode transmitter HDMI_TX2N or DPTX_L0N. AC couple to TX connector.	Output
J9	DPTX_L0P_HDMI_TX2P	AIO, 1V2 tol	Dual mode transmitter HDMI_TX2P or DPTX_L0P. AC couple to TX connector.	Output

Note: The default DP and HDMI output signals mapping match the standard DP and HDMI connector pin mapping, However lane swapping and polarity swapping is possible through software configuration.

Table 7. System power and ground

Pin	Assignment	Description
F3, G3	DVDD33	I/O VDD, 3.3V digital supply. De-couple using 100 nF.
D3, D7, E3, E7	DVDD12	Core VDD, 1.2V digital supply. De-couple using 100 nF.
C7	AVDD33_RCOSC	3.3V RC-oscillator analog supply. De-couple using 100 nF.
B7	AVDD12_PLL	1.2V analog PLL supply. De-couple using 10 uF and 100 nF.
B3, B4	AVDD12_RX	1.2V analog receiver supply. EMI filter rail and de-couple using 10 uF and 100 nF.
B5, C5, C6	AVDD33_RX	3.3V analog receiver supply. EMI filter rail and de-couple using 10 uF and 100 nF.
G6	AVDD33_TX	3.3V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
H4, H5, H6	AVDD12_TX	1.2V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
H7	AVDD12_OSC	1.2V analog crystal oscillator supply. De-couple using 100 nF.
H8	DVDD25_SM	Decoupling point for internal 2.5V LDO supply. De-couple using 10 uF and 100 nF.
C3, C4, D4, D5, D6, E4, E5, E6, E8, F4, F5, F6, F7, G4, G5, G7	VSS	Common GND. Connect to GND plane

5.2 Bootstrap configuration

DC Levels on some device pins are specified during de-asserting edge of power-on reset (RESETn goes High). The levels specified below must be adhered to for normal function of the device.

Table 8. Bootstrap configuration

BS signal name	Internal PU/PD	Assignment	Function
IROM_DEBUGn_Bootstrap5	PULL UP	SPI_CSN	Reserved. SPI_CSN *must not* be Pulled Down during Power-On RESET.
XTAL_OSC_SEL_Bootstrap4	PULL UP	SPDIF_OUT	Reserved. SPDIF_OUT *must not* be Pulled Down during Power-On RESETn.
ICD_DEBUG_Bootstrap3	PULL DN	SPI_DO	Reserved. SPI_DO *must not* be Pulled Up during Power-On RESETn.
XROM_EN_Bootstrap2	PULL DN	SPI_CLK	Reserved. SPI_CLK *must not* be Pulled Up during Power-On RESETn.
RESERVED_Bootstrap1	PULL DN	IRQ	Reserved. IRQ pin *must not* be Pulled Up during Power-On RESETn.
ATE_MODE_EN_Bootstrap0	Open drain	UART_TX	Reserved. UART_TX *must* be Pulled Up during Power-On RESETn.

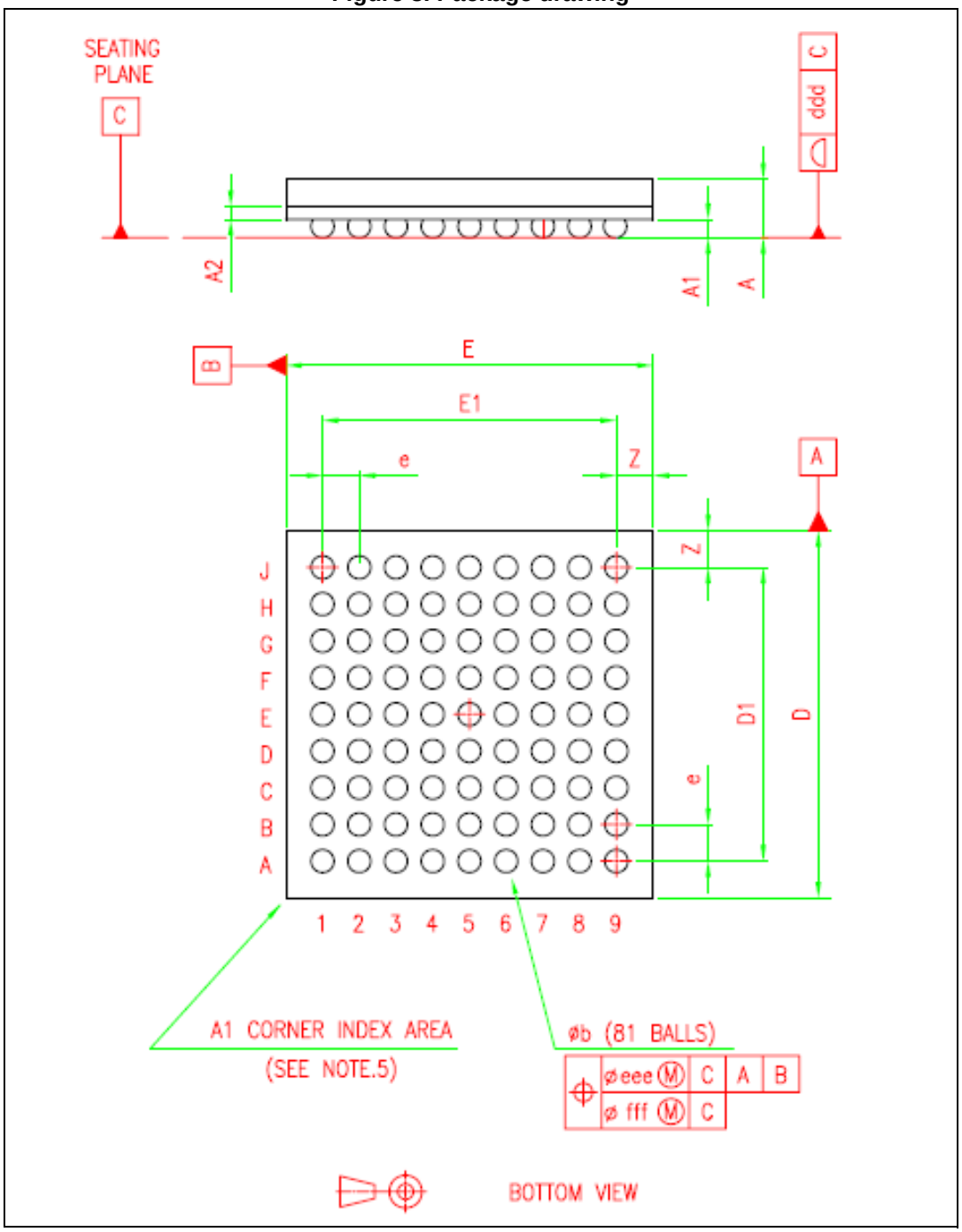
Note: When the pin corresponding to a specific bootstrap is left NC, it will take the value of the assigned by the internal PULLUP (Level 1) or PULLDN (Level0). The internal resistor used is around 50k ohm. To select a non-default value on a bootstrap, an external PULLUP or PULLDN resistor tied to the opposite direction that overcomes the internal PULLUP or PULLDN needs to be used.

6. Package specifications

Package type: 81 BGA (8 x 8 mm / ball pitch 0.8 mm)

6.1 Package drawing

Figure 3. Package drawing



6.2 BGA8X8 dimensions

Figure 4. Package dimensions

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			1.4			1.33	(1)
A1	0.27			0.35	0.40	0.45	
A2		0.28		0.24	0.28	0.32	
A4			0.60	0.57	0.585	0.60	
b	0.45	0.50	0.55	0.45	0.50	0.55	(2)
D	7.85	8.00	8.15	7.90	8.00	8.10	
D1		6.40			6.40		
E	7.85	8.00	8.15	7.90	8.00	8.10	
E1		6.40			6.40		
e		0.80			0.80		
Z		0.80			0.80		
ddd			0.12			0.12	
eee			0.15			0.15	(3)
fff			0.08			0.08	(4)

Note: *(1) – LFBGA stands for Low profile Fine pitch Ball Grid Array.*
– Low profile: 1.20mm < A = 1.70mm / Fine pitch: e < 1.00mm.
– The total profile height (Dim A) is measured from the seating plane "C" to the top of the component.
– The maximum total package height is calculated by the RSS method (Root Sum Square):
A Max = A1 Typ + A2 Typ + A4 Typ + v ($A1^2 + A2^2 + A4^2$ tolerance values).

(2) – The typical ball diameter before mounting is 0.50mm.

(3) – The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

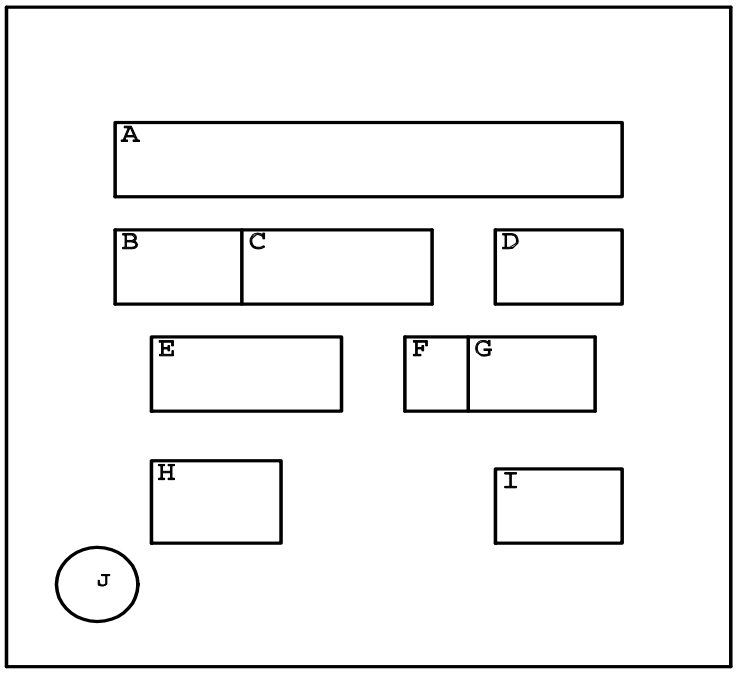
4) – The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

(5) – The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
– A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

6.3 Marking field template and descriptors

The STDP2690 marking template is shown below.

Figure 5. Marking template



Field descriptors are shown below.

Table 9.Field descriptors

Field	Description	Marking
A	Product code	STDP2690
B	2-character assembly plant code	99
C	3-character BE sequence code	“XYZ”
D	2-character diffusion plant code	VQ
E	3-character country of origin code	MYS
F	1-digit assembly year	“Y”
G	2-digit assembly week	“WW”
H	Standard MegaChips logo	M
I	2-character version code	AD
J	Ball A1 identifier	a DOT

6.4 Classification reflow profile

Please refer to the DisplayPort Application Note: Classification reflow profile for SMD devices (C0353-APN-06) for reflow diagram and details.

7. Electrical specifications

7.1 Absolute maximum ratings

Applied conditions greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. The device should never exceed absolute maximum conditions since it may affect device reliability.

Table 10. Absolute maximum ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (1,2)	$V_{VDD\_3.3}$	-0.3	3.3	3.63	V
1.2 V supply voltages (1.2)	$V_{VDD\_1.2}$	-0.3	1.2	1.26	V
Input voltage for tolerance for 5V I/O pin(1,2)	$V_{IN5Vtol}$	-0.3	-	5.5	V
Input voltage tolerance for 3.3V I/O pin(1,2)	$V_{IN3V3tol}$	-0.3	-	3.63	V
ESD - Human Body Model (HBM)	V_{ESD}	-	-	±2	kV
ESD - Charged Device Model (CDM)	V_{ESD}	-	-	±500	V
Latch-up	I_{LA}	-	-	±200	mA
Ambient operating temperature	T_A	0	-	70	°C
Storage temperature	T_{STG}	-40	-	125	°C
Operating junction temperature	T_J	0	70	125	°C
Thermal resistance (Junction to Ambient)	θ_{JA}	-	52.4	-	°C/W
Thermal resistance (Junction to Case)	θ_{JC}	-	24.4	-	°C/W
Peak IR reflow soldering temperature	T_{SOL}	-	-	260	°C

Note (1): All voltages are measured with respect to GND.

Note (2): Absolute maximum voltage ranges are for transient voltage excursions.

7.2 DC characteristics

Table 11. DC characteristics

Parameter	Symbol	Min	Typ	Max(1)	Units
Power					
3.3 V supply voltages (analog and digital)	$V_{VDD\_3.3}$	3.14	3.3	3.47	V
1.2 V supply voltages (analog and digital)	$V_{VDD\_1.2}$	1.14	1.2	1.26	V
Power					
Measurement conditions: 1920 x 1080 / 120 Hz test pattern: ON-OFF dot.			493		mW
Sleep mode			21		mW

Table 11. DC characteristics

Parameter	Symbol	Min	Typ	Max(1)	Units
Supply current					
Measurement conditions: 1920 x 1080 / 120 Hz test pattern: ON-OFF dot Moire VDD (analog and digital power) = 3.3 V VDDA (analog and digital power) = 1.2 V In all configuration, 8 bits input is used.		-	45.3 286	-	mA
Inputs					
High voltage	V_{IH}	2.0	-	-	V
Low voltage	V_{IL}	-	-	0.8	V
Input hysteresis voltage	V_{HYST}	300	-	-	mV
High current (V_{IN} = 3.3V)	I_{IH}	-	-	±10	µA
Low current (V_{IN} = 0 V)	I_{IL}	-	-	±10	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}	-	-	5	pF
Outputs					
High voltage (I_{OH} = 8mA)	V_{OH}	2.4	-	-	V
Low voltage (I_{OL} = -8 mA)	V_{OL}	-	-	0.4	V
Tri-state leakage current	I_{OZ}	-	-	±10	µA

Note: The values in the Max column represent absolute maximum current consumption under high voltage (+5%) and nominal temperature. These values are measured in an environment that includes some discreet components. Other conditions include: a) Power measurement values are to be used for regulator sizing only, and not directly for package thermal calculations. b) IC performance is only guaranteed when operating within the "DC Characteristics". c) All inputs are 3.3V tolerant.

7.3 AC characteristics

Table 12. Maximum speed of operation

Clock domain	Max speed of operation
Reference Input Clock (TCLK)	27 MHz
Reference Internal Clock (RCLK)	324 MHz
On-Chip Microcontroller Clock (OCLK)	100 MHz
SPDIF audio output	192 kHz
2-Wire Serial Slave (SLAVE_SCL)	400 kHz
2-Wire DDC2bi Slave (VGAx_SCL)	400 kHz
2-Wire Serial Master (MSTRx_SCL)	400 kHz

7.3.1 DisplayPort receiver

Table 13. DisplayPort receiver electrical parameters

Parameter	Symbol	Min	Typ	Max	Units	Comments
DisplayPort receiver system parameters						
HBR2 Unit Interval (5.4Gbps)	UI_HBR2	-	185	-	ps	DisplayPort link RX does not require local crystal for link clock generation
Turbo Unit Interval (3.2Gbps)	UI_TURBO	-	312	-	ps	
HBR Unit Interval (2.7Gbps)	UI_HBR	-	370	-	ps	
RBR Unit Interval (1.62Gbps)	UI_RBR	-	617	-	ps	
Link clock down spreading	Down Spread Amplitude	0	-	0.5	%	Modulation frequency range 0f 30kHz to 33kHz
DisplayPort receiver TP3 parameters						
Minimum Receiver Eye Width at Rx-side connector pins	T_{RX-EYE_CONN}	0.25	-	-	UI	For RBR
Lane intra-pair Skew Tolerance	$L_{RX-SKEW\_INTRA\_PAIR\_HBR2}$	-	-	50	ps	For HBR2. Represents the skew contribution from the cable in addition to the stressed EYE at TP3_EQ.
Lane intra-pair Skew Tolerance	$L_{RX-SKEW\_INTRA\_PAIR\_HBR}$	-	-	60	ps	For HBR. Represents the skew contribution from the cable in addition to the stressed EYE at TP3.
Lane intra-pair Skew Tolerance	$L_{RX-SKEW\_INTRA\_PAIR\_RBR}$	-	-	260	ps	For RBR. Represents the skew contribution from the cable in addition to the stressed EYE at TP3.
Jitter Closed Loop Tracking Bandwidth	$F_{RX-TRACKING-BW\_RBR}$	5.4	-	-	MHz	Minimum CDR closed loop tracking bandwidth at the receiver when the input is a PRBS7 pattern
Jitter Closed Loop Tracking Bandwidth	$F_{RX-TRACKING-BW\_HBR}$	10	-	-	MHz	Minimum CDR closed loop tracking bandwidth at the receiver when the input is a PRBS7 pattern

Table 13. DisplayPort receiver electrical parameters

Parameter	Symbol	Min	Typ	Max	Units	Comments
Jitter Closed Loop Tracking Bandwidth	$F_{RX-TRACKING-BW\_HBR2}$	10	-	-	MHz	Minimum CDR closed loop tracking bandwidth at the receiver when the input is a PRBS7 pattern
DisplayPort receiver TP3_EQ parameters						
Minimum Receiver Eye Width	$T_{RX-TJ\_8b10b\_HBR2}$	0.38	-	-	UI	For HBR2. Measured at 1E-9 BER using HBR2 Compliance EYE pattern.
RX Differential Peak-to-Peak EYE Voltage	$T_{RX-DIFFp-p\_HBR2}$	90	-	-	mV	For HBR2. Measured at 1E-9 BER using HBR2 Compliance EYE pattern.

7.3.2 DisplayPort transmitter

Table 14. DisplayPort transmitter electrical parameters

Parameter	Symbol	Min	Typ	Max	Unit	Comments
DisplayPort transmitter system parameters						
HBR2 unit interval (5.4 Gbps)	UI_HBR2	-	185	-	ps	Frequency high limit = +300 ppm Frequency low limit = 5300 ppm
Turbo unit interval (3.2 Gbps)	UI_TURBO	-	312	-	ps	
HBR unit interval (2.7 Gbps)	UI_HBR	-	370	-	ps	
RBR unit interval (1.62 Gbps)	UI_RBR	-	617	-	ps	
Link clock down spreading	Down Spread Amplitude	0	-	0.5	%	Modulation frequency range 0f 30 kHz to 33 kHz
DisplayPort transmitter TP2 parameters						
Ratio of output voltage level 1/ level 0	$V_{TX-OUTPUT-RATION\_RBR\_HBR}$	0.8	-	6.0	dB	Measured on non-transition bits at pre-emphasis level 0 setting
Ratio of output voltage level 2/ level 1		0.1	-	5.1	dB	
Ratio of output voltage level 3/ level 2		0.8	-	6.0	dB	

Table 14. DisplayPort transmitter electrical parameters

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Ratio of output voltage level 1/ level 0	$V_{TX-OUTPUT-RATION\_HBR2}$	5.2	-	6.9	dB	Measured on non-transition bits at pre-emphasis level 0 setting
Ratio of output voltage level l 2/ level 1		1.6	-	3.5	dB	
Ratio of output voltage level 3/ level 2		1	-	4.4	dB	
Maximum pre-emphasis when disabled	VTX-PREEMP-OFF	-	-	0.25	dB	
Max output voltage level	$V_{TX-DIFFp-p-MAX}$	-	-	1.2	V	
Lane-to-lane output skew	$L_{TX-SKEW-INTER\_PAIR\_HBR\_RBR}$	-	-	2	UI	Applied to all pairwise combinations of supported lanes
Lane-to-Lane output skew	$L_{TX-SKEW-INTER\_PAIR\_HBR2}$	-	-	4UI+500ps	ps	Applied to all pairwise combinations of supported lanes
Lane intra-pair output skew	$L_{TX-SKEW-INTRA\_PAIR}$	-	-	30	dB	Applies to all support lanes
Delta of pre-emphasis Level 1 vs. level 0	$V_{TX-PREEMP-DELTA}$	2	-	-	dB	Applied to all valid voltage settings. No Pre-emphasis Post Cursor2 applied
Delta of pre-emphasis level 2 vs. level 1		1.6	-	-	dB	
Delta of pre-emphasis level 3 vs. level 2		1.6	-	-	dB	
Non-transition reduction output Voltage level 2	$V_{TX-DIFF\_REDUCTION}$	-	-	3	dB	V_{Tx_DIFF} at each non-zero nominal pre-emphasis level must not be lower than the specific amount less than V_{Tx_DIFF} at the zero nominal pre-emphasis level. Modulation frequency range 0f 30 kHz to 33 kHz
Non-transition reduction output Voltage level 1		-	-	3	dB	
Non-transition reduction output Voltage level 0		-	-	1.4	dB	
DisplayPort transmitterTP3_EQ parameters						
Maximum TX total jitter	$T_{TX-TJ\_8b10b\_HBR2}$	-	-	0.62	UI	For HBR2. Measured at 1E-9 BER using HBR2 Compliance EYE pattern.
Maximum TX deterministic jitter	$T_{TX-DJ\_8b10b\_HBR2}$	-	-	0.49	UI	

Table 14. DisplayPort transmitter electrical parameters

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Maximum TX total jitter	$T_{TX-TJ\_D10.2\_HBR2}$	-	-	0.4	UI	For HBR2. Measured at 1E-9 BER using D10.2 compliance pattern.
Maximum TX deterministic jitter	$T_{TX-DJ\_D10.2\_HBR2}$	-	-	0.25	UI	
Maximum TX random jitter	$T_{TX-RJ\_D10.2\_HBR2}$	-	-	0.23	UI	
TX differential peak-to-peak EYE voltage	$T_{TX-DIFFp-p\_HBR2}$	110	-	-	mV	For HBR2. Measured at 1E-9 BER using HBR2 Compliance EYE pattern.

7.3.3 HDMI transmitter

Table 15. HDMI transmitter (DP++) DC characteristics

DC characteristics	Min	Typ	Max	Units	Comments
Single-ended output voltage	400	500	-	mV	
Single-ended high level output voltage, V_H	-	AV_{DD}	-	mV	AV_{DD}=1.2volt
Single-ended low level output voltage, V_L	-	AV_{DD}-500	-	mV	AV_{DD}=1.2volt

Table 16. HDMI transmitter AC characteristics

DC characteristics	Min	Typ	Max	Units	Comments
Intra-pair skew at source connector, max	-	-	0.15	T_{bit}	
Intra-pair skew at source connector, max	-	-	0.2	$T_{character}$	
TMDS differential clock jitter, max	-	-	0.25	T_{bit}	
Rise time/fall time	75	-	-	ps	

7.3.4 Crystal specification

Mode: fundamental

Table 17. Crystal specifications

Parameters	Min	Typ	Max	Units	Comments
Nominal frequency	-	27	-	MHz	
Tolerance	-	± 50	-	ppm	
Load capacitance	-	22	-	pF	
ESR (effective series resistance)	-	-	40	Ohm	

Table 17. Crystal specifications

Parameters	Min	Typ	Max	Units	Comments
Drive level	-	-	100	uW	
Shunt capacitance	-	7	-	pF	

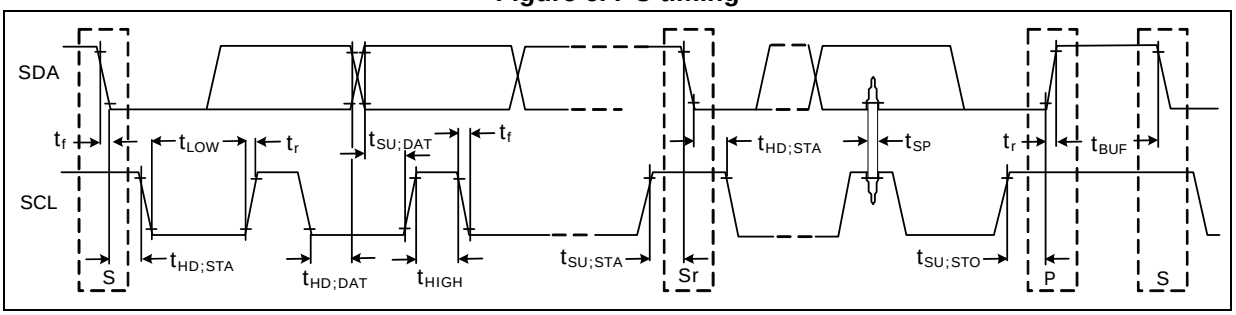
7.3.5 I2C interface timing

Table 18. I2C interface timing

Symbol	Parameter	Conditions	Min	Measured	Max	Unit
f_{SCL}	SCL clock rate	Fast mode	0	393	400	kHz
t_{HD-STA}	Hold time START	After this period, the 1st clock starts	0.6	0.95	-	µs
t_{LOW}	Low period of clock	SCL	1.3	1.1	-	µs
t_{HIGH}	High period of clock	SCL	0.6	0.75	-	µs
$T_{su;STA}$	Setup time for a repeated START		0.6	1.09	-	µs
$t_{HD;DAT}$	Data hold time	For master	0	0.96	0.9(1)	µs
$t_{SU;DAT}$	Data setup time		100	600	-	ns
T_{BUF}	Bus free time between STOP and START		1.3	1.7 ms	-	µs
C_b	Capacitance load for each bus line		-		400	pF
t_r	Rise time		20	220	300	ns
t_f	Fall time		20	25	300	ns
V_{nh}	Noise margin at high level		0.2 VDD	0.3	-	V
V_{nl}	Noise margin at low level		0.1 VDD	0.28	-	

Note: The maximum $t_{HD;DAT}$ only has to be met if the device does not stretch the low period t_{LOW} of the SCL signal. In the diagram below, S = start, P = stop, Sr = Repeated start, and SP= Repeated stop conditions.

Figure 6. I²C timing



7.3.6 SPI interface timing

Table 19. SPI interface timing, VDD = 3.3V

Symbol	Parameter	Min	Max	Units
F_{CLK}	Serial clock frequency	-	50	MHz
T_{SCKH}	Serial clock high time	9	-	ns
T_{SCKL}	Serial clock low time	9	-	ns
T_{SCKR}	Serial clock rise time (slew rate)	0.1	-	V/ns
T_{SCKF}	Serial clock fall time (slew rate)	0.1	-	V/ns
T_{CES}	CE# active setup time	5	-	ns
T_{CEH}	CE# active hold time	5	-	ns
T_{CHS}	CE# not active setup time	5	-	ns
T_{CHH}	CE# not active hold time	5	-	ns
T_{CPH}	CE# high time	50	-	ns
T_{CHZ}	CE# high to high-Z output	-	8	ns
T_{CLZ}	SCK low to low-Z output	0	-	ns
T_{DS}	Data in setup time	5	-	ns
T_{DH}	Data in hold time	5	-	ns
T_{OH}	Output hold from SCK change	0	-	ns
T_{V}	Output valid from SCK	-	8	ns

Figure 7. SPI output or serial interface SPI ROM input timing

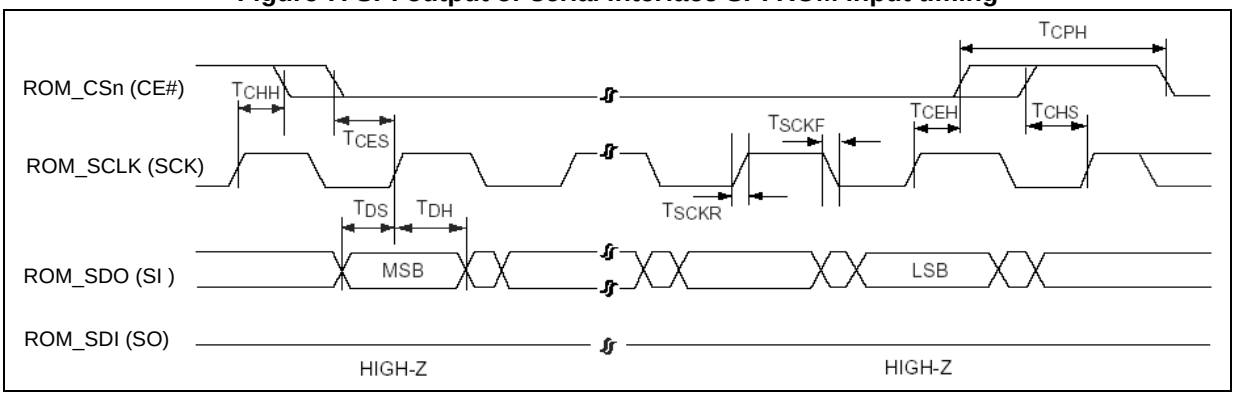
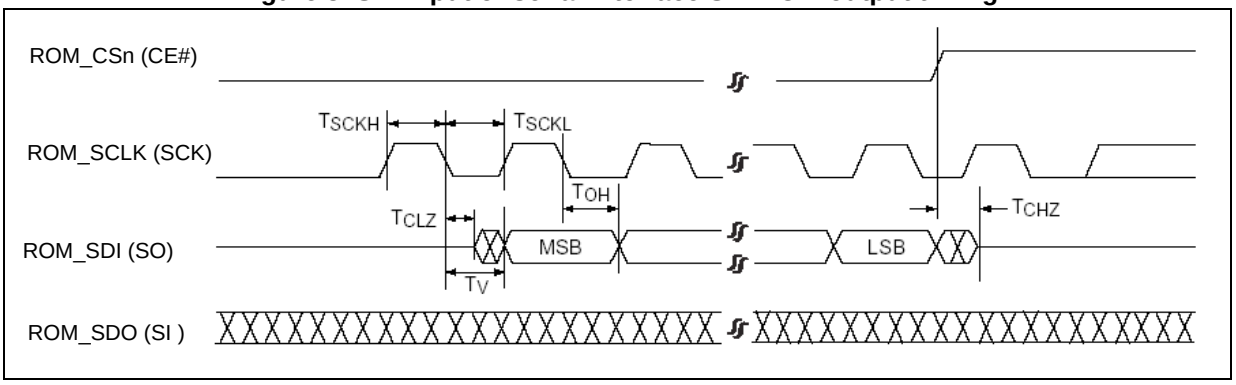


Figure 8. SPI input or serial interface SPI ROM output timing



8. Ordering information

Table 20. Order codes

Part number	Description
STDP2690-AD	81 BGA (8 x 8 mm) delivered in trays
STDP2690-ADT	81 BGA (8 x 8 mm) delivered in tape and reel

9. Revision history

Table 21. Document revision history

Date	Revision	Changes
07-Mar-2016	A	Initial release.

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