AN90006

Circuit design and PCB layout recommendations for GaN FET half bridges

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Document information

Information	Content
Keywords	GaN FET, Half bridges, Circuit design, PCB layout
Abstract	This appplication note explains the Recommendations for circuit design and PCB layout when applying GaN FET half bridges.

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1. Diode-free bridges

Power GaN FETs are nearly ideal switches for many applications. A particular advantage in bridge circuits is that they can carry the freewheeling current without the need of an additional anti-parallel diode. The diagrams in Fig. 1 compare a traditional high-voltage half bridge to a half bridge made with GaN FET devices. In the traditional half bridge each switch (shown here as an IGBT) is paired with a freewheeling diode. Because the HEMT channel exists in pure, undoped GaN, there is no parasitic p-n junction to provide an unwanted current path, and bidirectional flow of majority carriers can be realized in the channel.

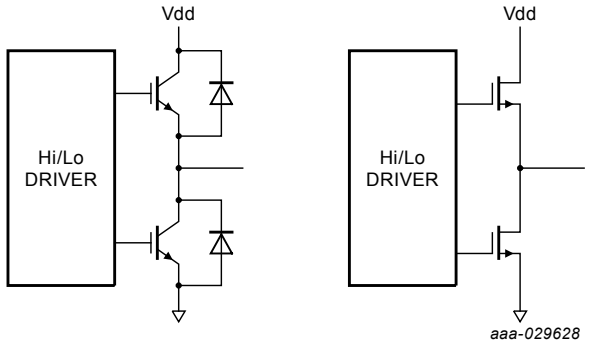
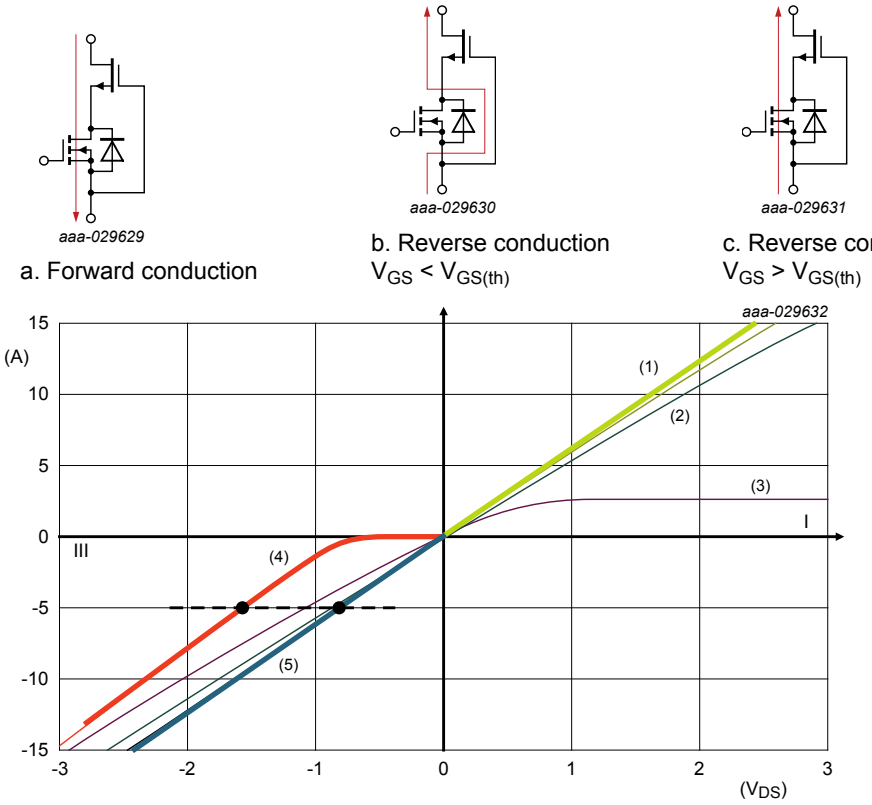


Fig. 1. Comparison of a traditional high-voltage half bridge to a GaN FET half bridge.

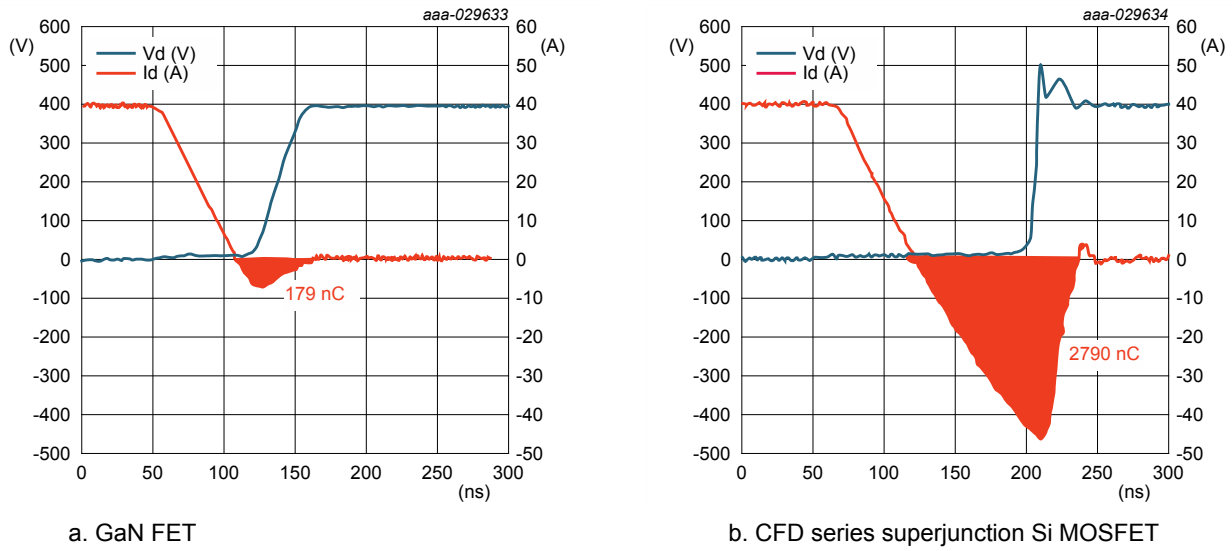
In Nexperia's two-die GaN FET the freewheeling current does indeed flow in the body diode of a silicon MOSFET, but because the silicon MOSFET is a low voltage part, the injected charge is very small. Indicated in Fig. 2 are the current paths for three modes of operation. In the reverse conducting mode the conduction loss may be reduced by enhancing the silicon MOSFET (driving $V_{GS} > V_{GS(th)}$). As indicated in Fig. 2, the voltage drop from source to drain decreases by about 0.8 V with a 5 A reverse current when the gate is enhanced.



(1) V_{GS} = 8 V
(2) V_{GS} = 4 V
(3) V_{GS} = 3 V
(4) V_{GS} = 0 V, 1 V, 2V
(5) V_{DS}

Fig. 2. Current paths in the GaN FET switch for three operating modes, and the corresponding I-V characteristic.

Some transistor technologies include junctions which could, if permitted, serve the function of the freewheeling diode, the body diode of a MOSFET being one example. The reverse recovery charge for these devices will be much larger than for a GaN FET with similar ratings. The graphs shown in Fig. 3 compare the total reverse-recovery charge for a Nexperia GaN FET to a low-Q_{RR} (CFD series) superjunction silicon MOSFET. The Q_{RR} ratio, Si/GaN, varies with exact part numbers.



a. GaN FET

b. CFD series superjunction Si MOSFET

Fig. 3. Reverse recovery charge test result for a GaN FET (left) and a CFD series superjunction Si MOSFET (right).

2. Circuit-design recommendations

The high switching speed of GaN FET devices necessitates observation of a few specific circuit-design guidelines. Before explaining these requirements, however, one simplification may be mentioned: negative gate drive is neither necessary nor recommended. Due to the high threshold voltage (V_{th} = 4 V typical) and extremely low Miller capacitance (Q_{GD} = 6 nC typical), there is adequate turn-off margin with a simple 0 V to 10-12 V drive.

While high-speed switching brings the benefit of reduced power loss, the inherent transients can create stability problems. Specifically, the high $\frac{di}{dt}$ transient during switching, combined with parasitic inductances, leads to transient voltages in the circuit. These voltage transients can interfere with the gate and the driver of the device, and, in the worst case, creates sustained oscillation that must be prevented for safe operation of the circuit. The following section provides guidance on how to eliminate oscillation and how to achieve high switching current with a controlled $\frac{di}{dt}$.

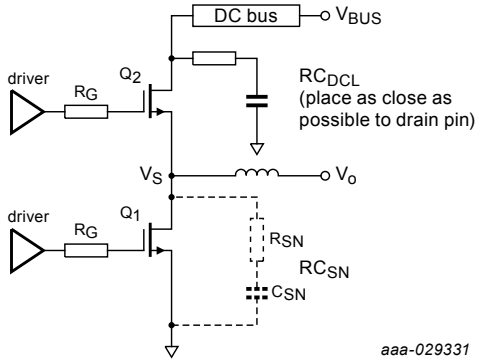


Fig. 4. Half-bridge switching circuit

2.1. Solutions to suppress oscillation

To avoid sustained oscillation, it is important to minimize noise generation, to minimize noise feedback, and to damp the ringing energy resulting from the high current and voltage transients. This can be achieved with the recommendations outlined below using a half-bridge switching circuit in Fig. 4 as an example.

1. Optimize the PCB layout to minimize external parasitic inductances and associated feedback. Details follow in Section 3 of this application note.
2. Use a DC-link RC snubber [RC_{DCL} in Fig. 4]. The DC rail or DC-link, when decoupled with a low-ESR fast capacitor, can be considered a high-Q C-L network at high frequencies (with "L" being the feed inductance of the DC bus). This can interact with the devices during transients and lead to ringing. Adding an RC snubber across the DC-link close to the drain pin of the high-side device can effectively absorb the ringing energy, suppressing potential oscillation. This effect can be seen where the high-frequency ringing at 25 A turn-off is substantially damped with the RC_{DCL}. Since this snubber is not inserted at the switching node, it does not add switching loss to the circuit.

   Note: This is recommended even for single-ended non-half-bridge designs. The practical values of the RC_{DCL} can be two sets of 6 - 10 Ω / 0.5 W SMD resistors in series with a 10 nF / 600 - 1000 V ceramic SMD capacitor, or one 3 - 4 Ω / 1 W resistors in series with a 10 - 20 nF / 600 - 1000 V capacitor if space is limited.
3. Adding a switching-node RC snubber [RC_{SN} in Fig. 4] can further reduce high-frequency ringing and help control $\frac{di}{dt}$ transients at high operating currents. The effect of the RC_{SN} on the switching waveform can be seen at a switching current > I_{SWL}, see Table 1. Unlike the RC_{DCL}, the capacitance of the RC_{SN} does increase switching loss. The degradation in efficiency is minimal however, when using the recommended snubber parameters given in the data sheet, and summarized in Table 1.

2.2. Gate drive and bootstrap supply

Since high slew rates of the order of 50 - 100 V/ns are normal, the high-side gate-driver must have good common-mode transient immunity. Apart from that consideration, there are no special requirements for the Hi/Lo gate driver used with Nexperia's GaN FET switches. As with any insulated-gate power transistor, the gate-drive current should be consistent with the desired turn-on time and total gate charge. As mentioned in the opening paragraph of Section 2, use of a negative gate voltage in the off state is not recommended. Selecting a gate driver with a lower drive current can be appropriate for reducing $\frac{di}{dt}$. Drivers with 0.5 A output current have been used with good results, for example. Nexperia GaN FETs in the TO-247 package include an integrated ferrite bead in series with the gate.

The bootstrap, or floating, supply for the high-side gate drive comprises components R4, D1, C12, and C13 in Fig. 8. The junction capacitance of D1 contributes directly to switching loss, and so a fast, low capacitance diode should be used. Resistor R4 is critical for limiting the inrush charging current; a value of 10 - 15 Ω works well. If an isolated DC-DC converter is used for the high-side supply, the isolation capacitance plays the same role as the junction capacitance of D1 in the bootstrap supply. Inductance in series with this capacitance will create an additional resonance which will be excited with each switching transient, so careful layout applies here. Use of a common-mode choke in the floating supply can be helpful.

2.3. Summary of circuit-design recommendations

- SMD mounting is recommended for all snubber components.
- A gate resistor (RG) is required for all devices.
- The RC_{DCL} snubber reduces voltage ringing due to interaction of the GaN FET with the bypass network.
- The RC_{SN} snubber enables increased output power while slightly reducing light and medium load efficiency.
- The RC_{SN} implementation in a half-bridge has the advantage of allowing a higher peak turn-off switching current due to the reduction of the $\frac{di}{dt}$ seen by the freewheeling device as the main active switch turns off.
- Gate ferrite beads (FB1) may be required for future devices in other package types; TO-247 devices have built-in ferrite beads hence no external FB1 is needed.
- Refer to Nexperia Application Note AN90005 for an explanation of data-sheet limitations and relevant recommendations for when to use a switching-node snubber.

2.4. Required and recommended external components

The recommended components of the half-bridge circuit in Fig. 4 are summarized in Table 1.

They have been tested and verified to prevent oscillation for safe, reliable operation with the recommended gate drive voltage ranges shown. Using a higher “on” voltage is not recommended and may increase the propensity for oscillation and will require a larger gate resistor. Using a lower “on” voltage may increase switching and conduction losses due to increased $R_{DS(on)}$.

Table 1. Recommended components for half-bridge circuit

Parameters \ Part Number	GaN041-650WSA	GaN063-650WSA
Package	TO-247	TO-247
Recommended Gate-Drive Voltage	0 V, 10 - 12 V	0 V, 10 - 12 V
Recommended Gate Resistor (R_g)	30 Ω	30 - 45 Ω
Gate Ferrite Bead (FB1)	Not required	Not required
Recommended RC_{SN}	200 pF + 5 Ω	100 pF + 10 Ω
Recommended RC_{DCL}	(10 nF + 8 Ω) x 2	(10 nF + 8 Ω) x 2
I_{SWL}	17 A	14 A

2.5. To verify GaN FET stable operation

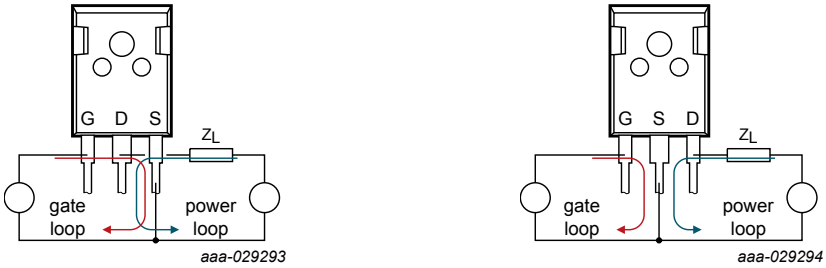
To verify adequate operational margin without oscillation, as a minimum observe the V_{DS} waveforms at the turn-on and turn-off switching edges at the application’s maximum drain current. This may occur during start-up or at the application’s maximum load step. A double-pulse or multi-pulse test is highly recommended utilizing the actual layout, with current levels at or greater than 120 % of the application’s anticipated peak current. Verify that the ringing on the V_{DS} waveform at the transition edges is adequately damped.

3. PCB layout

The parasitic inductances of the input (gate) and output (power) loops contribute significantly to overshoot, ringing, and stability in general.

3.1. Pin assignment

Nexperia GaN FETs in the TO-247 package use a Gate-Source-Drain pin assignment, which differs from that used for older transistors in the same package. The reason for centering the source rather than the drain is that the source is the common node to both gate and power loops. This minimizes coupling of the two loops, as illustrated in Fig. 5.



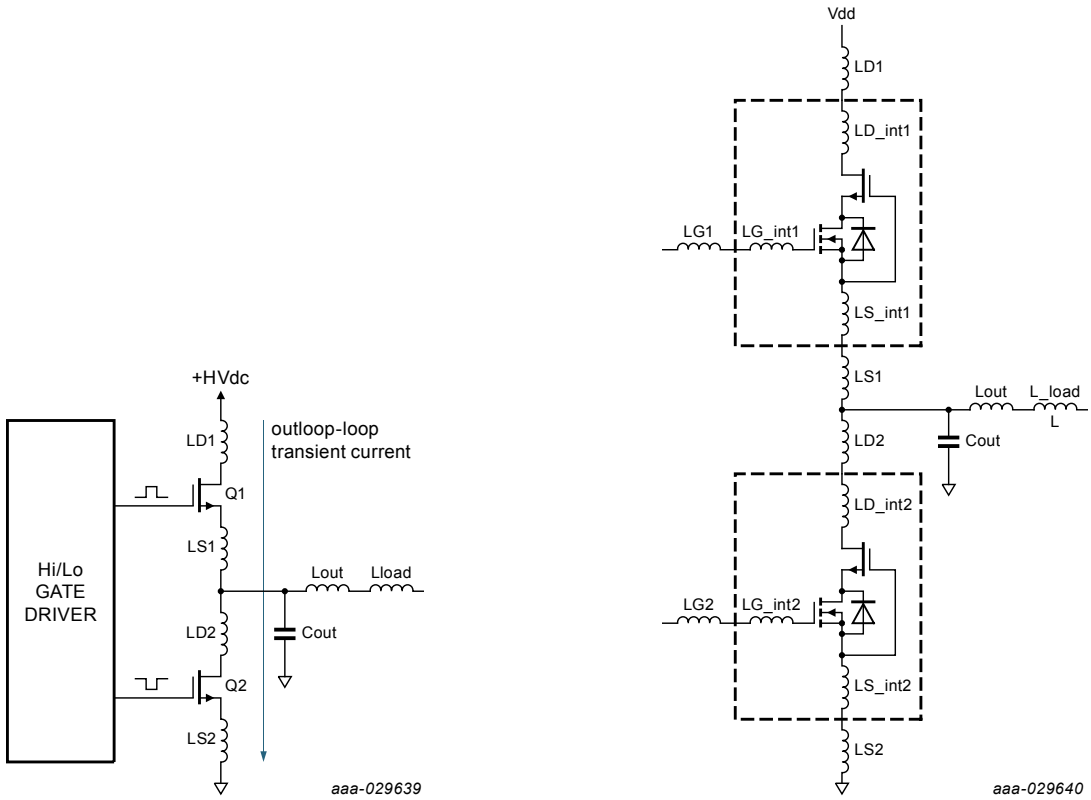
a. Conventional pins assginment

b. Nexperia pin assigment

Fig. 5. Illustration of the de-coupling achieved with a centered-source pin assignment.

3.2. Power loop

Although the various charges are low with GaN FET switches, they are not zero, and there will be a very fast transient current during switching as these charges are redistributed. This current will flow from the positive supply node, through both transistors to the negative supply node. To minimize ringing due to this transient, inductances in this path should be minimized. Referring to Fig. 6, these inductances are indicated as LS1, LD1, LS2, and LD2. To minimize these, low impedance power and ground traces, or planes, should be used and bypass capacitance and DC-link snubber should be placed as close as possible to the transistors. It is not critical to minimize inductance L_{out} since it is in series with the load inductance, and to a first approximation simply adds to it. The connection between the high-side (Q1) source pin and the low-side (Q2) drain pin should also be very short. Placing the two transistors back-to-back on a common heat sink helps accomplish this. Shown in Fig. 7 to Fig. 10, is a portion of the layout of a Nexperia half-bridge evaluation board, indicating the placement of the power transistors.



a. Only elements external to GaN FET packages

b. Both internal and external parasitic elements

Fig. 6. Parasitic elements in the power loop.

Details of the power loop layout are highlighted in Fig. 9. To minimize inductance, the drain of Q1 is connected directly to the power plane; the source of Q2 is connected directly to the ground plane.

The power and ground planes are on internal layers of the PCB, not visible in the figure. The switching node is formed by the wide trace connecting the source of Q1 to the drain of Q2.

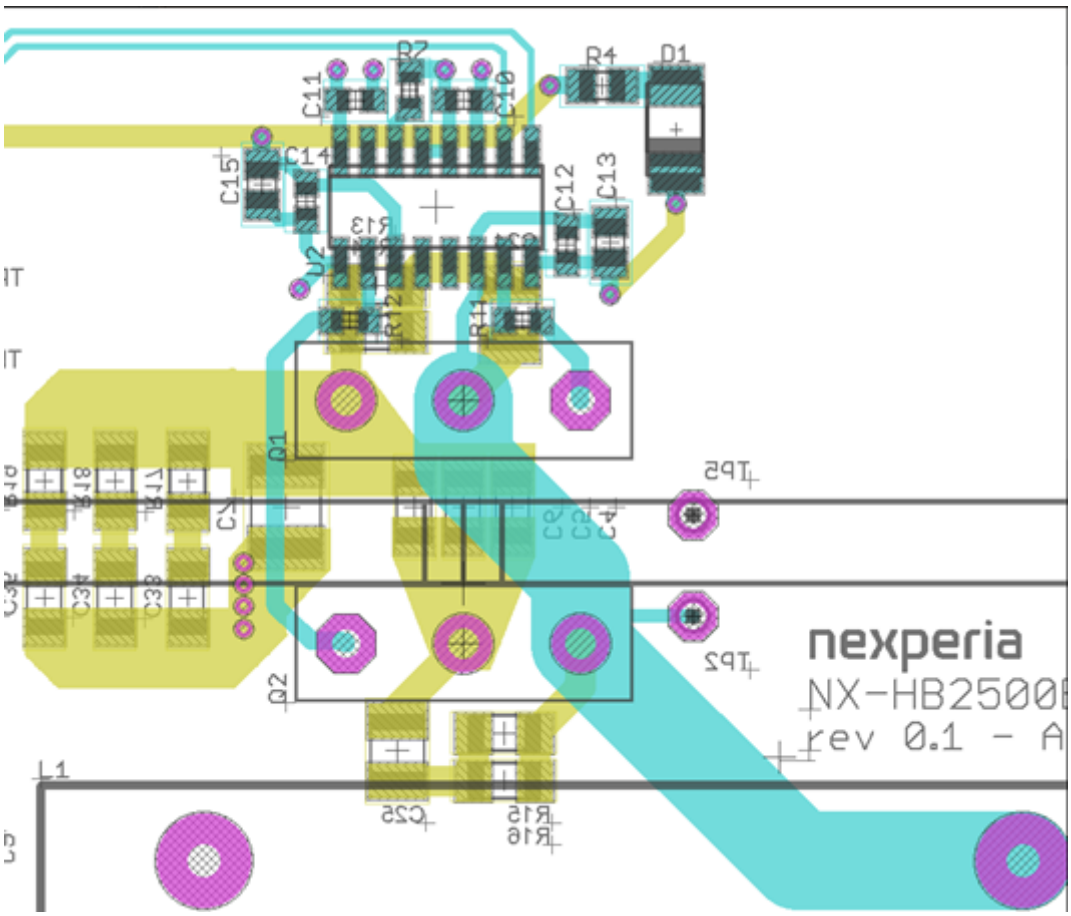


Fig. 7. PCB layout - Power-stage

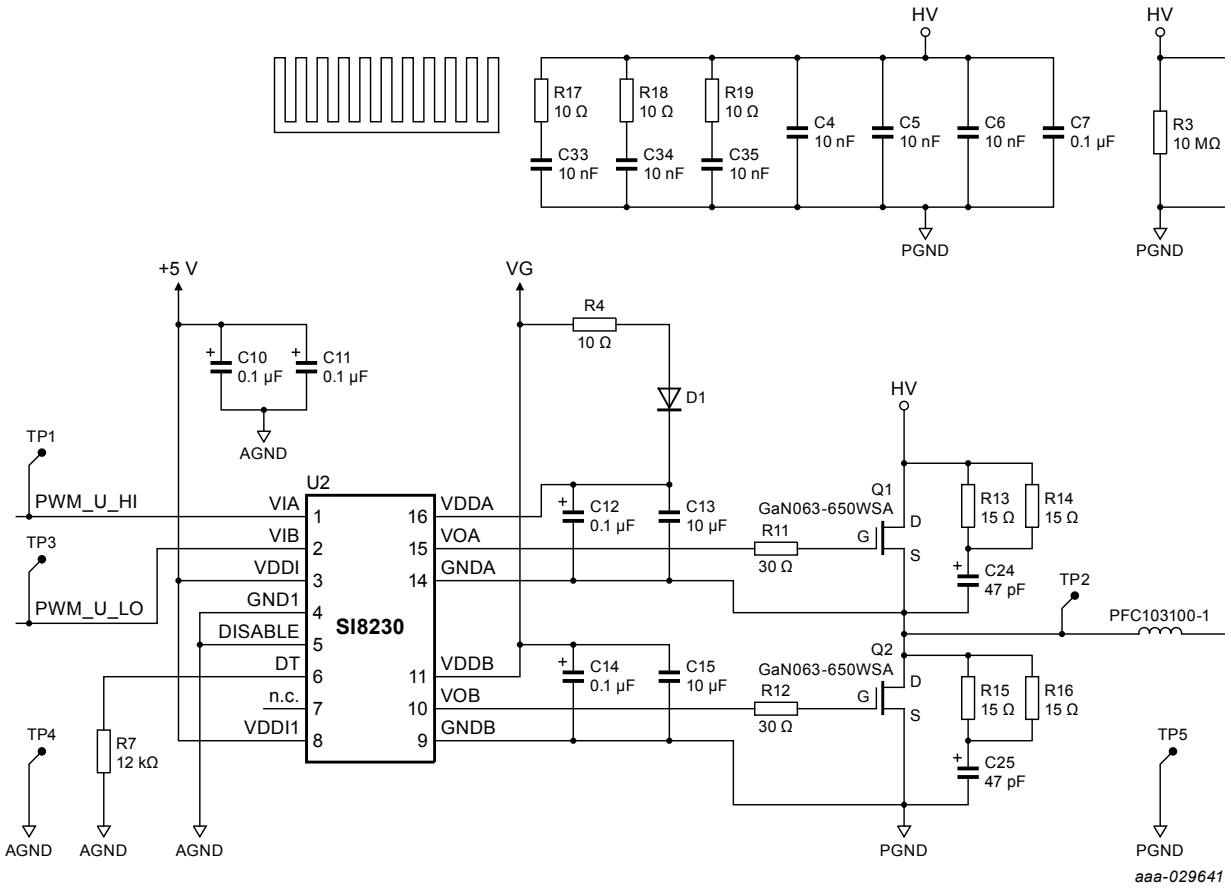


Fig. 8. PCB layout - Corresponding schematic section

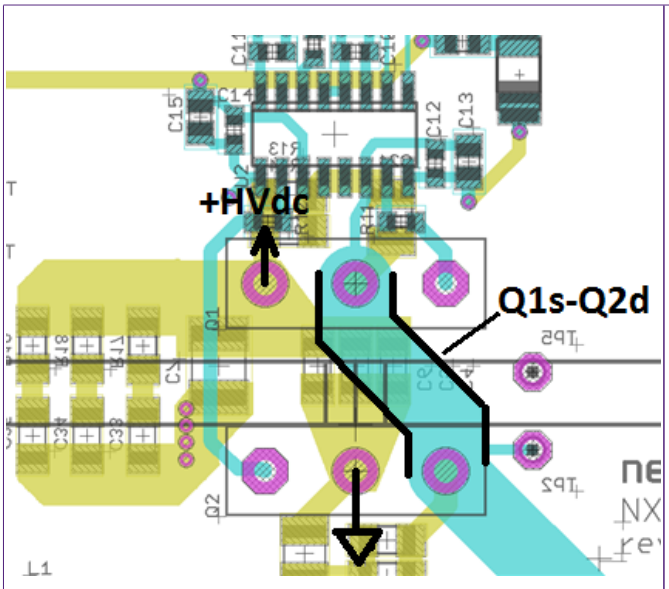


Fig. 9. PCB layout - Detail of power connections

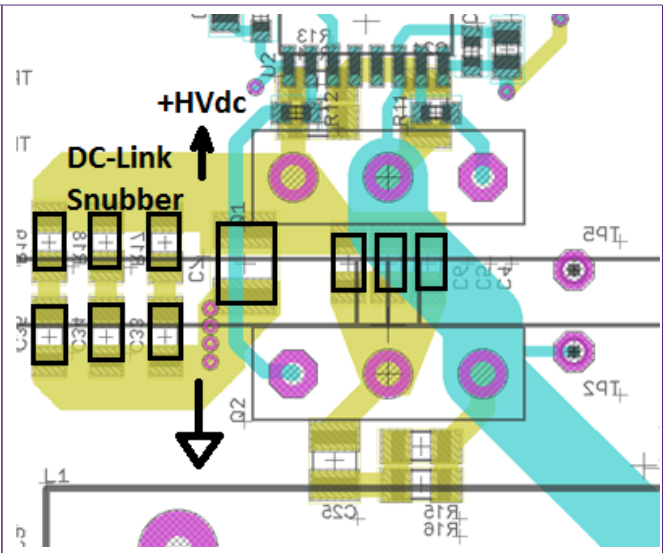
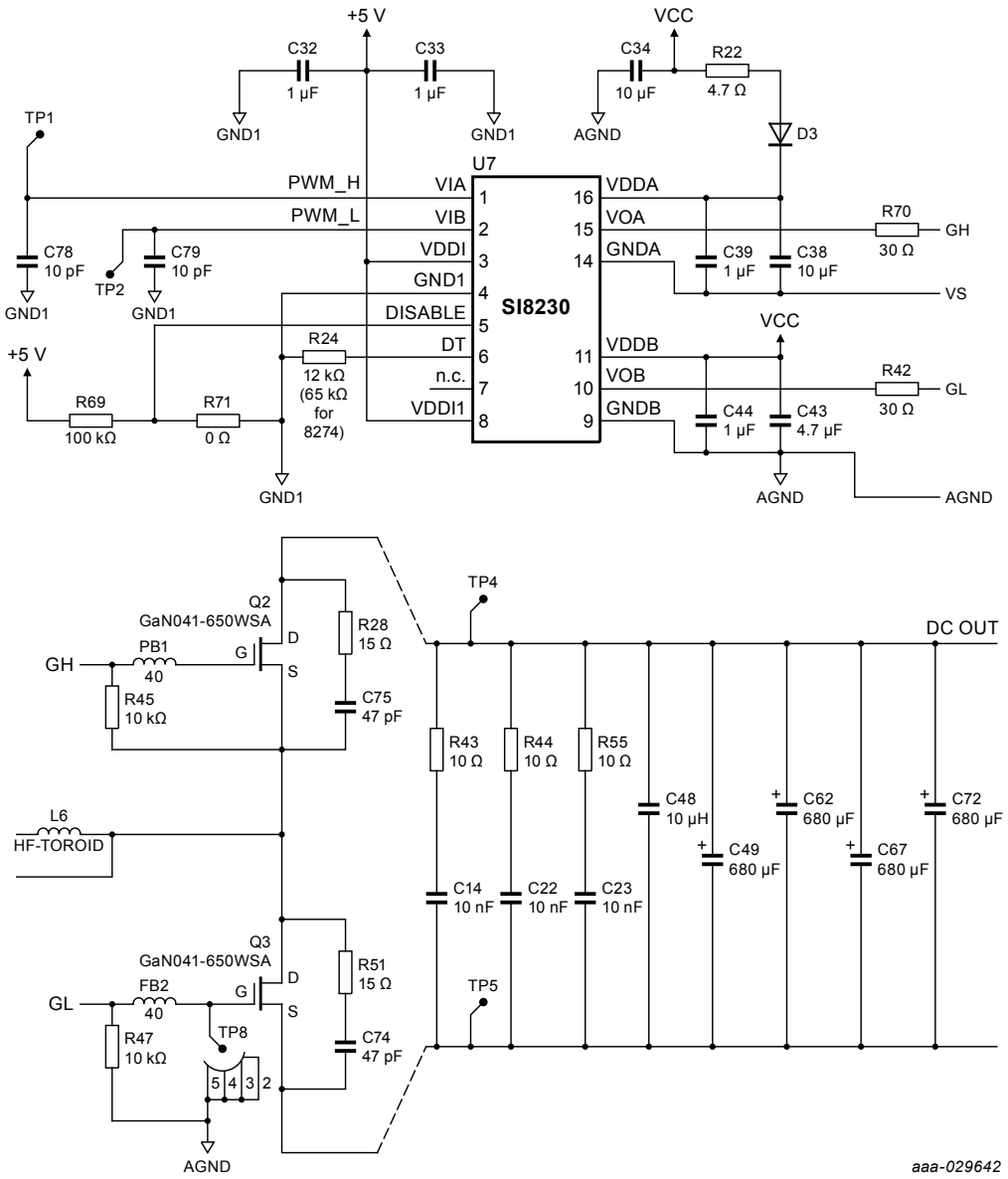
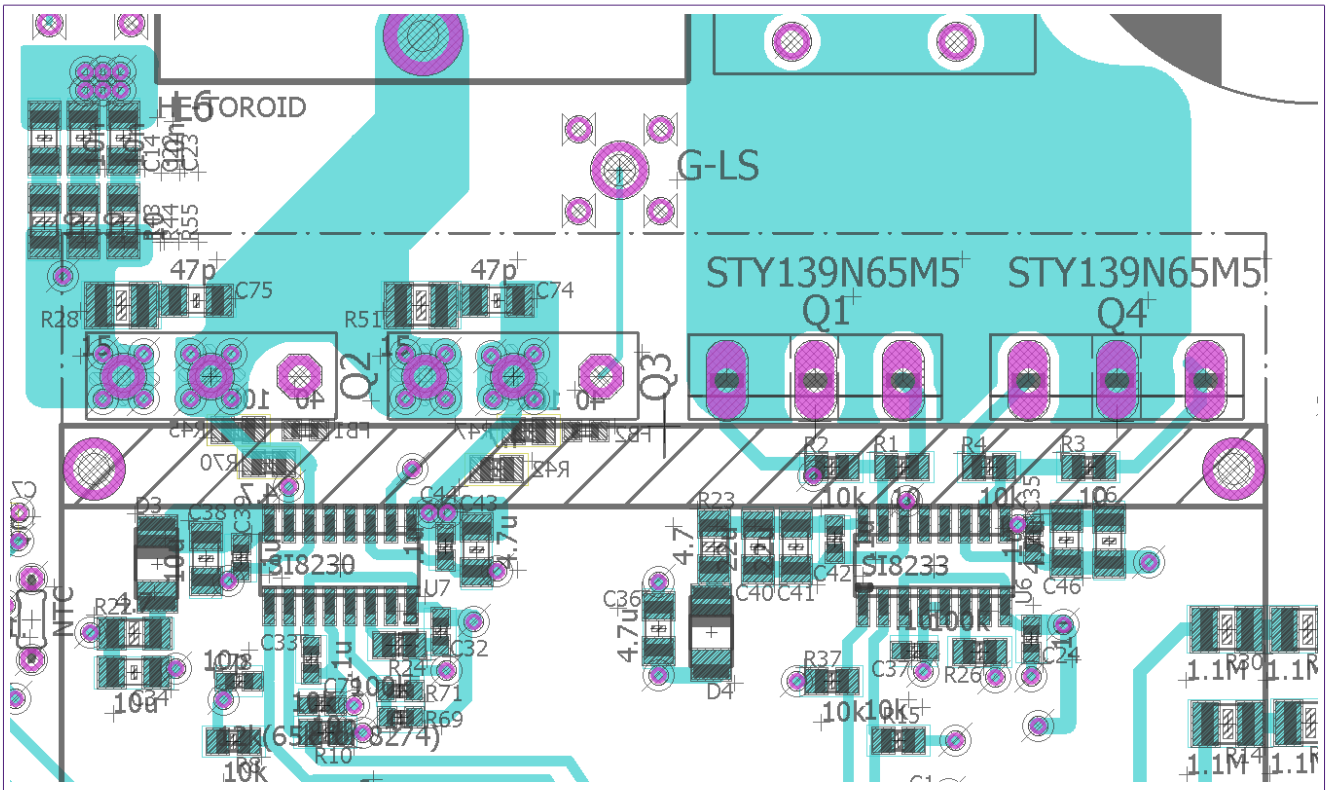


Fig. 10. PCB layout - Detail of bypassing: SMD capacitors on PCB backside

Illustrated in Fig. 11 is an alternative placement where the GaN FETs are side-by-side, rather than back-to-back, as in Fig. 7 to Fig. 10. Inductances are higher with this arrangement, but it is sometimes preferable for manufacturing reasons.



(a) Schematic diagram



(b) PCB layout

Fig. 11. Totem pole PFC PCB.

Capacitance on the switching node, indicated as C_{out} in Fig. 6, adds directly to switching loss, and so the total area of copper which forms the switching node should be kept low, but not so low that inductance becomes significant. A typical 4-layer board with 12 mils (0.3 mm) between outer trace and internal ground plane adds about 15 pF / cm^2. At 100 kHz switching, each 1 cm^2 would add $P = 1/2\ CV^2 f_s$ = 120 mW switching loss, for example.

4. Heat Sink connection

The heat sink should be connected to an AC ground. In the evaluation board of Fig. 7 to Fig. 10 the heat sink is electrically connected to the negative supply, or ground plane. Both low-side and high-side transistors are insulated from the heat sink. For the low-side transistor the capacitance between tab and heat sink is not critical, since the tab of the TO-247 is connected to the source. This transistor could be mounted directly to the heat sink, but the possibility that load current could flow in the heat sink must be allowed for. If a reliable connection between tab and heat sink is either not possible or not desirable, use of an insulator is necessary. For the high-side transistor, capacitance between the TO-247 mounting base and the heat sink will add to switching loss, and so a thick and/or low permittivity insulator should be used.

4.1. Gate-drive loop

As with the output loop, minimizing inductance in the input, or gate-drive loop is critical. Particularly important is the source inductance (LS2 in Fig. 6, for example), which is common to both loops. Any voltage developed across this inductance due to a change in the output current, $\frac{dID}{dt}$, will appear in the input loop. The gate–source loop should be made as compact as possible to minimise the gate loop inductance. The gate-source loop inductance and GaN FET input capacitance form a resonant tank and will have a corresponding resonant frequency. The resonant circuit will be excited into oscillation by the back EMF produced by the $\frac{di}{dt}$ in the source inductance. Fig. 12 Usually the resonant frequency of the gate-source loop will be less than 200 MHz. A ferrite bead fitted in series with the gate can have a beneficial effect by “de-Qing” the gate-source resonant circuit. For this reason, a small ferrite bead is integrated inside the TO-247 package. For future Nexperia GaN FETs where it is not integrated, the ferrite bead should be located as close as possible to the gate pin of the GaN FET so that the damping is applied to the device gate where it is needed. A gate ferrite bead is needed for both single-ended non half-bridges as well as half-bridge designs.

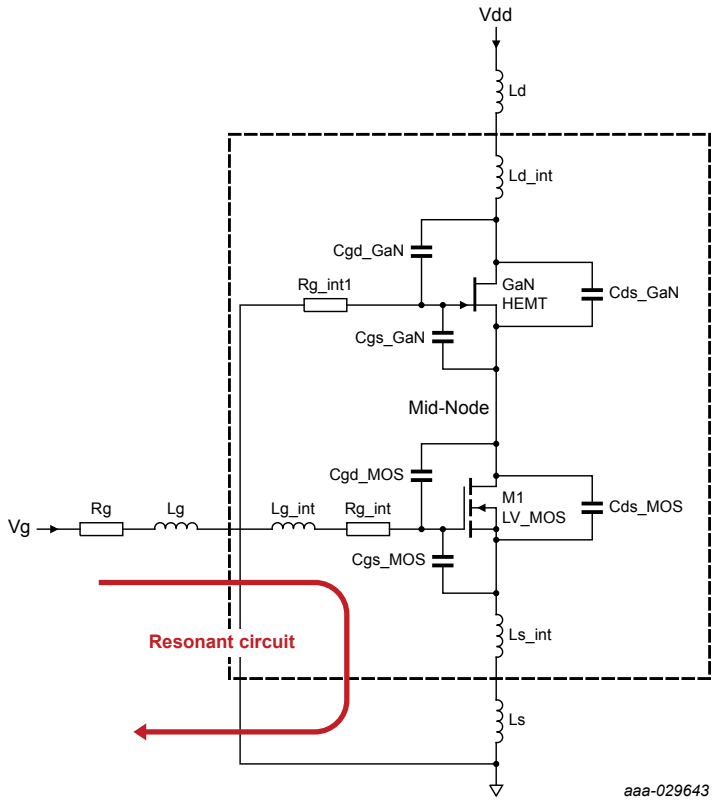


Fig. 12. Input Loop for a cascode GaN FET

4.2. Summary of PCB layout recommendations

- Place the RC_{DCL} as close as possible to the drain pin of the high-side GaN FET and ground it to the large ground plane.
- Use a large area ground plane for an overall low-noise base potential.
- Arrange the gate drive circuit on one side and the output circuit on the other side of the PCB to minimize noise feedback from the output loop to the input loop.
- Place the driver circuit close to the gate of the device.
- Shorten the power loop by arranging the high-side and low-side devices close-by.

5. Revision history

Table 2. Revision history

Revision number	Date	Description
1.1	20190213	AN90006
1.0	20181112	Preliminary AN90006

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