SLG59M1721V

An Ultra-small 1.4 mm^2, 18 mΩ, 2.0 A Integrated Power Switch

General Description

The SLG59M1721V is a high performance 18 mΩ, 2.0 A single-channel nFET integrated power switch which can operate with a 2.5 V to 3.6 V V_{DD} supply to switch power rails from as low as 0.85 V up to the supply voltage. The SLG59M1721V incorporates two-level overload current protection, thermal shutdown protection, and in-rush current control which can easily be adjusted by a small external capacitor.

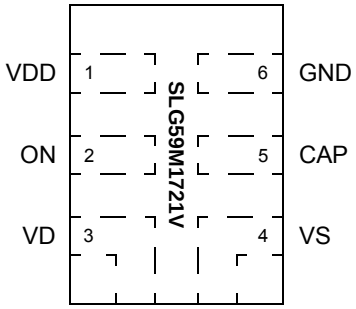
Using a proprietary MOSFET design, the SLG59M1721V achieves a stable 18 mΩ RDSON across a wide input voltage range and over temperature. In addition, the SLG59M1721V's package also exhibits low thermal resistance for high-current operation using Silego's proprietary CuFET technology.

Fully specified over the -40 °C to 85 °C temperature range, the SLG59M1721V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.0 mm x 1.4 mm STDFN package.

Features

- Low RDS_{ON} nFET: 18 mΩ
- Steady-state Operating Current: Up to 2.0 A
- Supply Voltage: 2.5 V ≤ V_{DD} ≤ 3.6 V
- Wide Input Voltage Range: 0.85 V ≤ V_D ≤ V_{DD}
- Capacitor-programmable Start-up and Inrush Current Control
- Two-stage Overcurrent Protection:
  - Fixed 2.6 A Active Current Limit
  - Fixed 0.5 A Short-circuit Current Limit
- Thermal Shutdown Protection
- Operating Temperature: -40 °C to 85 °C
- Low θ_{JA}, 6-pin 1.0 mm x 1.4 mm STDFN Packaging
  - Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

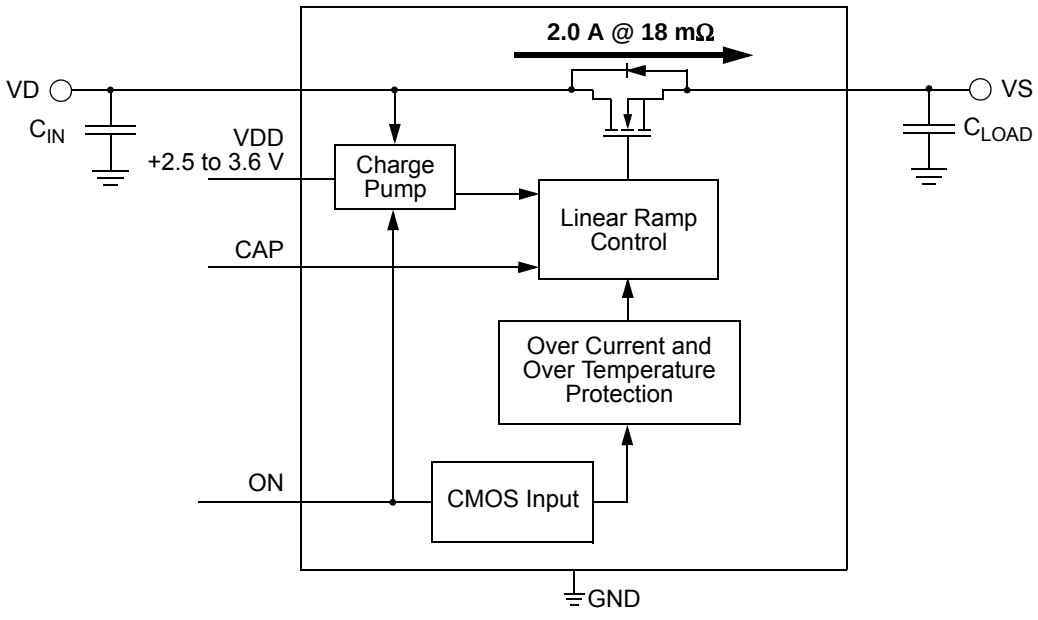


6-pin STDFN
(Top View)

Applications

- GPS Devices
- Notebook & Tablet PCs
- Smartphones
- Portable Consumer Electronics
- Portable Bar-Code Scanners
- Portable POS Terminals

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	With an internal 1.9V UVLO threshold, VDD supplies the power for the operation of the power switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1µF (or larger) capacitor.
2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1721V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with V_{IL} <0.3 V and V_{IH} >0.85V. While there is an internal pull-down circuit to GND (~4MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited.
3	VD	MOSFET	Drain terminal connection of the n-channel FET. Connect a 10-µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VD should be rated at 10 V or higher.
4	VS	MOSFET	Source terminal connection of the n-channel FET. Connect a 10 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VS should be rated at 10 V or higher.
5	CAP	Output	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the VS slew rate and overall turn-on time of the SLG59M1721V. For best performance, the range for CAP values are 1 nF ≤ CAP ≤ 22 nF. Capacitors used at CAP should be rated at 10 V or higher.
6	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1721V	STDFN 6L	Industrial, -40 °C to 85 °C
SLG59M1721VTR	STDFN 6L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	4.5	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Thermal Resistance	1.0 x 1.4 mm 6L STDFN; Determined using 1 in^2, 1 oz. copper pads under VD and VS terminals and FR4 pcb material	--	72	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	0.4	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1ms, 1% duty cycle	--	--	3	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-40 °C to 85 °C	2.5	--	3.6	V
I_{DD}	Power Supply Current (PIN 1)	when OFF	--	--	1	µA
		when ON, No load	--	85	100	µA
RDS_{ON}	Static Drain to Source ON Resistance	T_A 25°C @ 100 mA	--	18	21	mΩ
		T_A 85°C @ 100 mA	--	20	24	mΩ
IDS	Operating Current	V_D = 1.0 V to 3.6 V	--	--	2.0	A
I_{FET_OFF}	MOSFET OFF Leakage Current	V_D = 3.3 V, V_S = 0 V; ON = LOW	--	--	1	µA
V_D	Drain Voltage		0.85	--	V_{DD}	V
T_{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin, R_{LOAD} = 100 Ω, no C_{LOAD}	--	450	650	µs
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S	Configurable [1]			ms
		Example: CAP (PIN 5) = 4 nF, V_{DD} = V_D = 3.3 V, R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	--	1.4	1.7	ms
$T_{SLEWRATE}$	Slew Rate	10% V_S to 90% V_S	Configurable [1]			V/ms
		Example: CAP (PIN 5) = 4 nF, V_{DD} = V_D = 3.3 V, R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	2.5	3.0	3.5	V/ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall, V_{DD} = V_D = 3.3 V, R_{LOAD} = 100 Ω, no C_{LOAD}	--	3.2	--	µs
T_{FALL}	V_S Fall Time	90% V_S to 10% V_S, V_{DD} = V_D = 3.3 V, R_{LOAD} = 100 Ω, no C_{LOAD}	--	0.5	--	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from V_S to GND	10	22	100	µF
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V

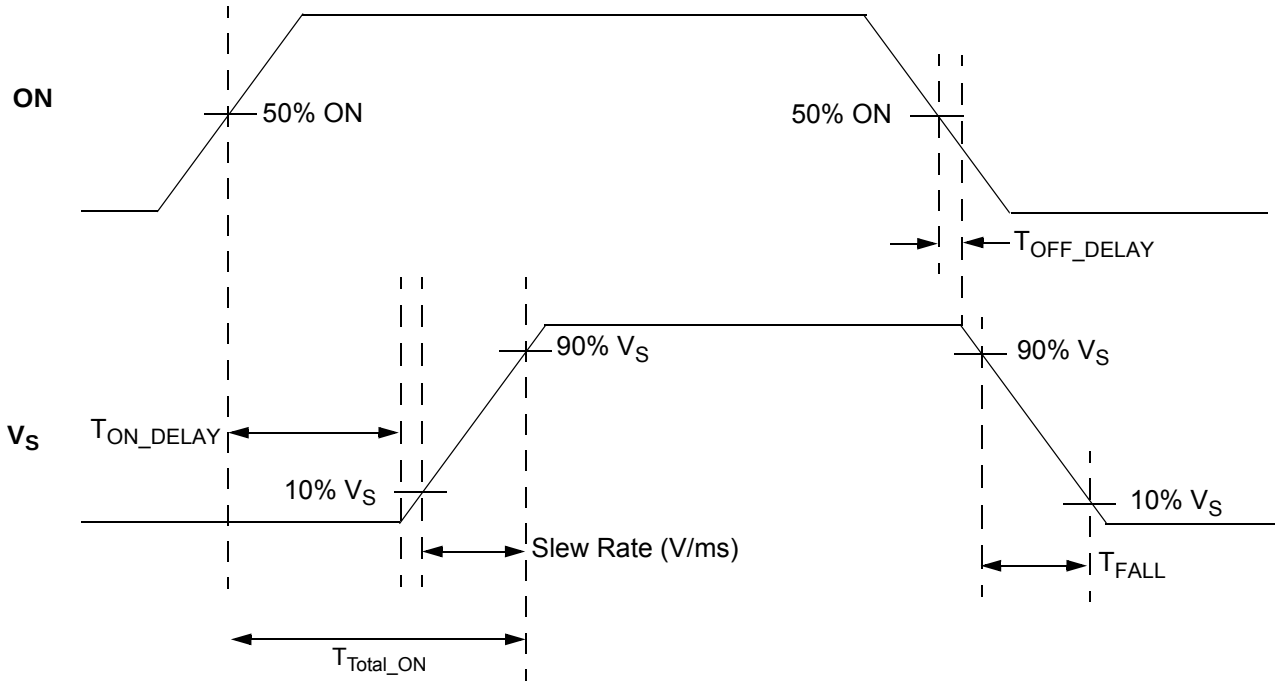
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
I_{LIMIT}	Active Current Limit	MOSFET will automatically limit current when V_S > 250 mV	2.1	2.6	3.1	A
	Short Circuit Current Limit	MOSFET will automatically limit current when V_S < 250 mV	--	0.5	--	A
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	135	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	105	--	°C
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms

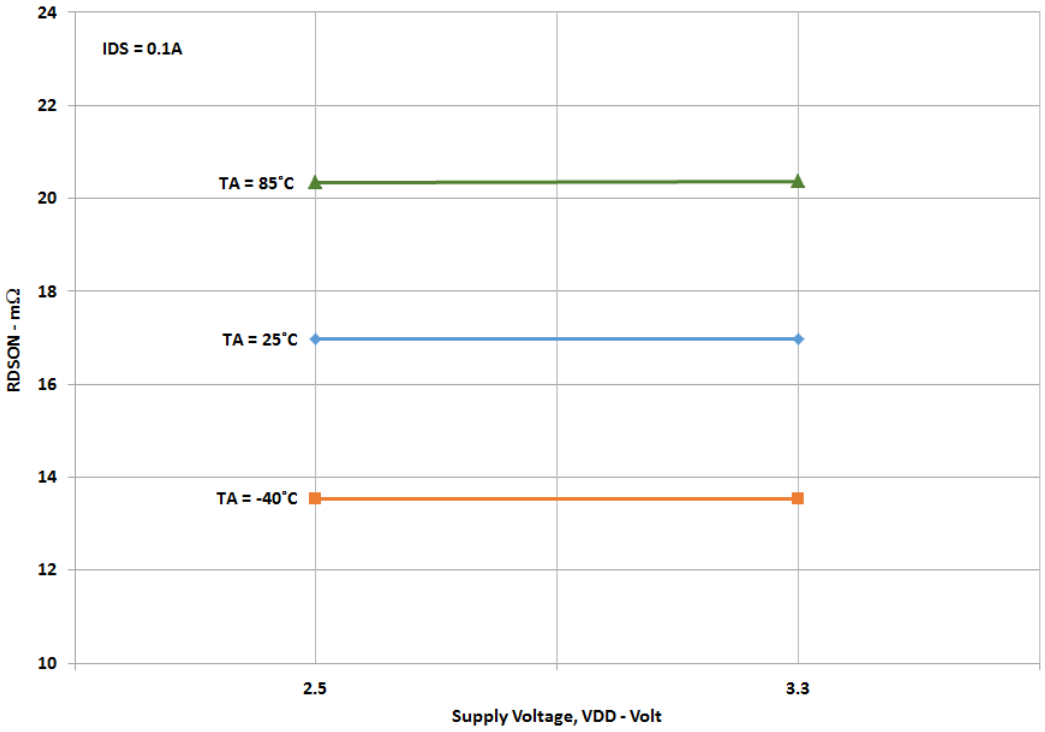
Notes:
1. Refer to table for configuration details.

T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement

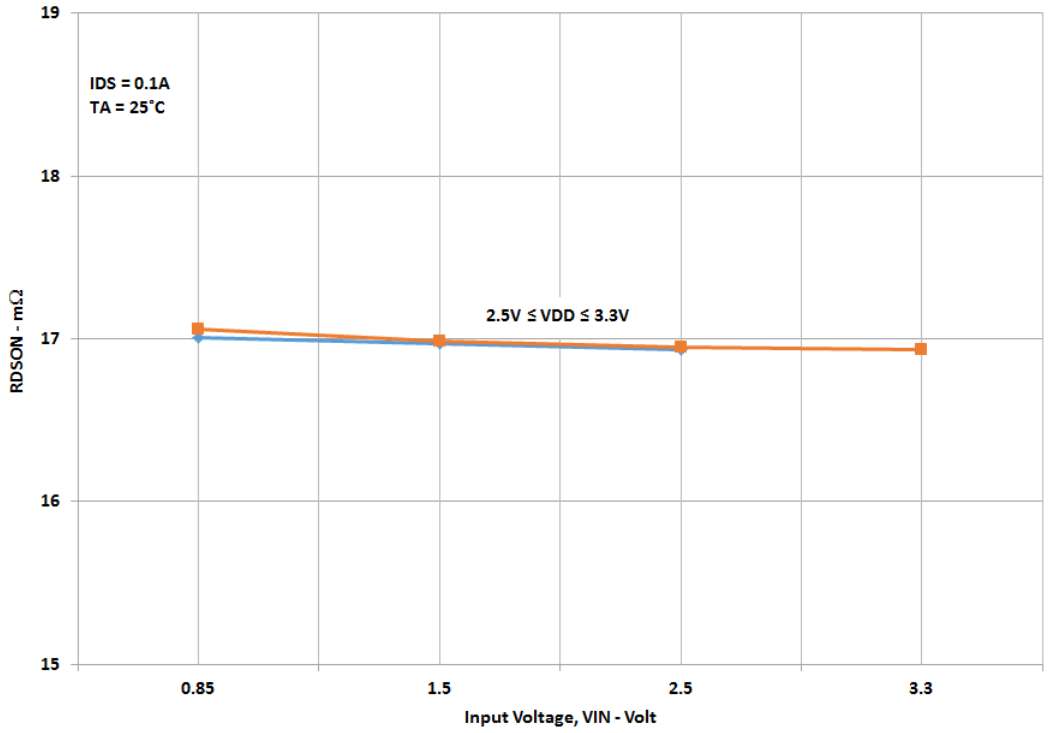


Typical Performance Characteristics

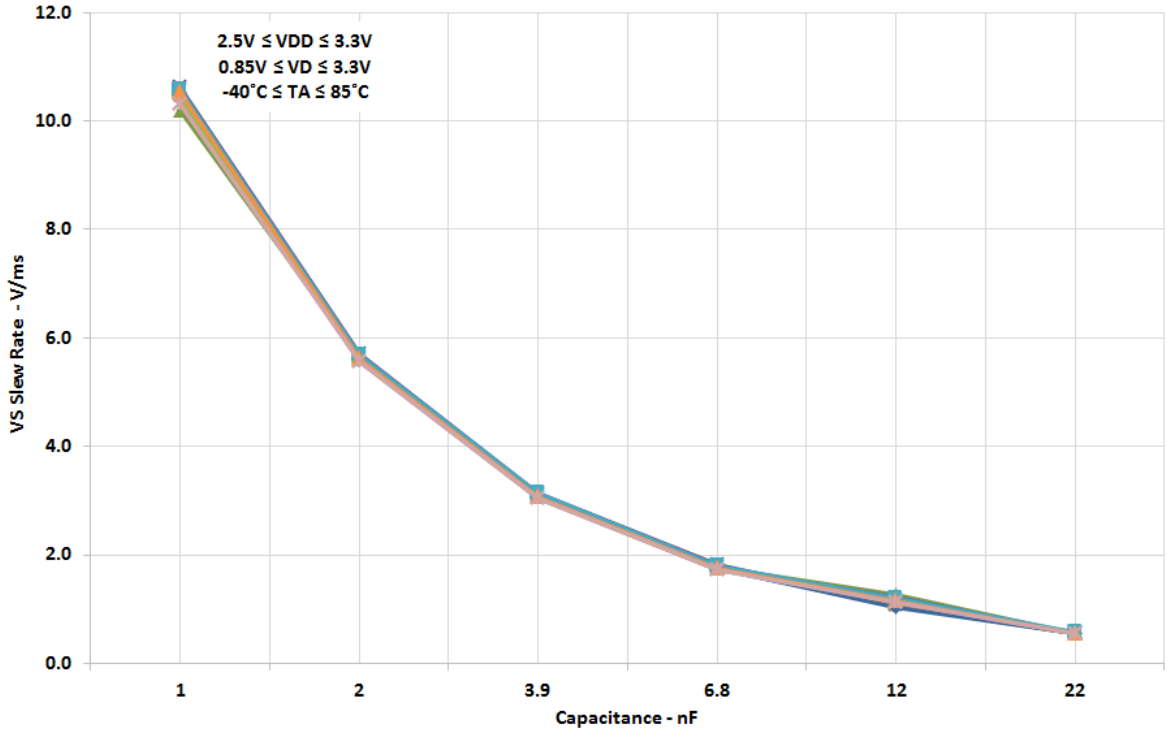
RDS_{ON} vs. V_{DD}, and Temperature



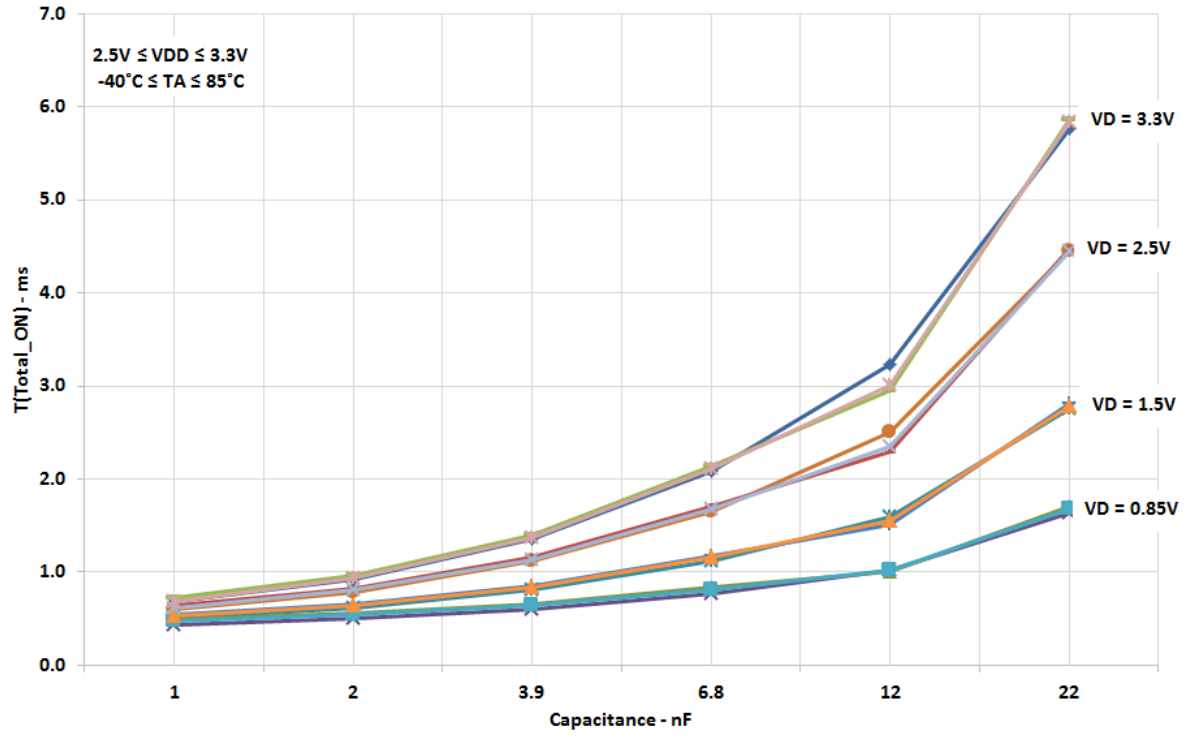
RDS_{ON} vs. V_D and V_{DD}



T_{SLEW} vs. CAP, V_D, V_{DD}, and Temperature



T_{Total_ON} vs. CAP, V_D, V_{DD}, and Temperature



SLG59M1721V Power-Up/Power-Down Sequence Considerations

A nominal power-up sequence is to apply V_{DD} first, followed by V_D only after V_{DD} is > 1.9 V, and finally toggling the ON pin LOW-to-HIGH after V_D is at least 90% of its final value.

A nominal power-down sequence is the power-up sequence in reverse order. It is important that the SLG59M1721V's ON pin is toggled HIGH only after V_{DD} and V_D have reached their steady-state values; otherwise, the power switch will spend an undesirable amount of time in high-resistance mode while powering up, heating up, and possibly reaching its thermal shutdown before ever fully turning on.

If V_{DD} and V_D are applied at the same time, a voltage glitch may appear on the output pin at V_S. To prevent glitches at the output, it is recommended to connect a 10 µF capacitor from the V_S pin to GND and to keep the V_{DD} & V_D ramp times less than 2 ms.

The V_S output follows a linear ramp when the power switch is turned on, provided that the V_S slew time set by CAP is less than the RC time constant formed by the RDS_{ON} of the power switch and load capacitance C_{LOAD}.

SLG59M1721V Current Limiting Operation

The SLG59M1721V has two types of current limiting triggered by the output V_S pin voltage.

1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When the V_S pin voltage > 250 mV, the output current is initially limited to the Active Current Limit (ACL) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's ACL threshold.

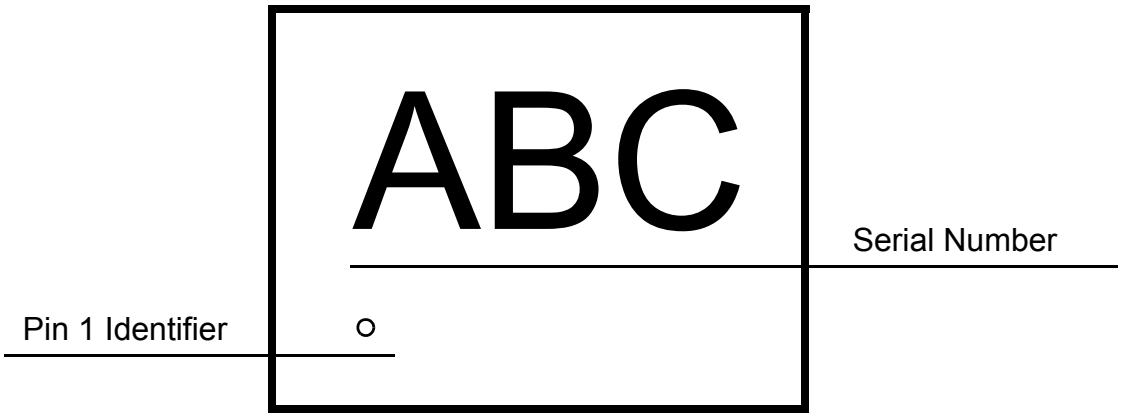
However, if a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the power switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed $THERM_{ON}$ specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

When the V_S pin voltage < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the power switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 500 mA (the SCL threshold). While the internal Thermal Shutdown Protection circuit remains enabled and since the SCL threshold is much lower than the ACL threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

For more information on Silego GreenFET3 integrated power switch features, please visit our Application Notes page at our website and see App Note "AN-1068 GreenFET3 Integrated Power Switch Basics".

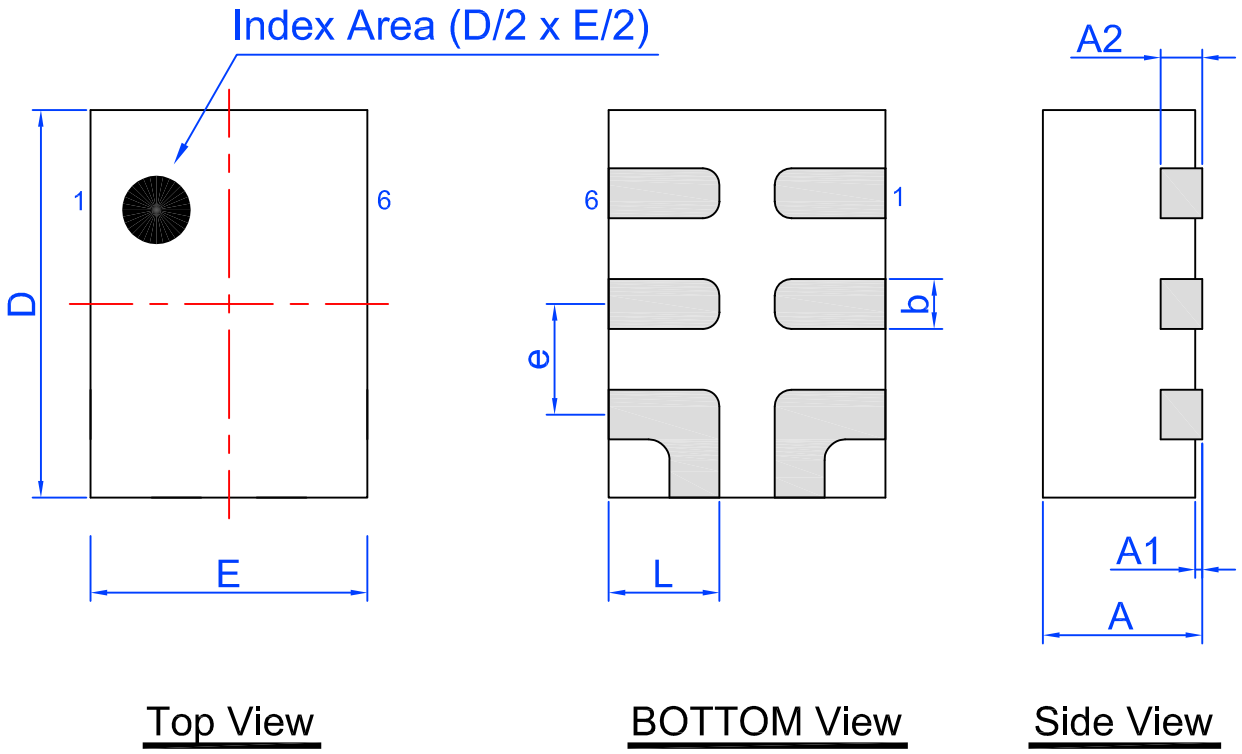
Package Top Marking System Definition



ABC - Part Serial Number Field
each A, B, and C character can be A-Z and 0-9

Package Drawing and Dimensions

6 Lead STDFN Package 1.0 x 1.4 mm

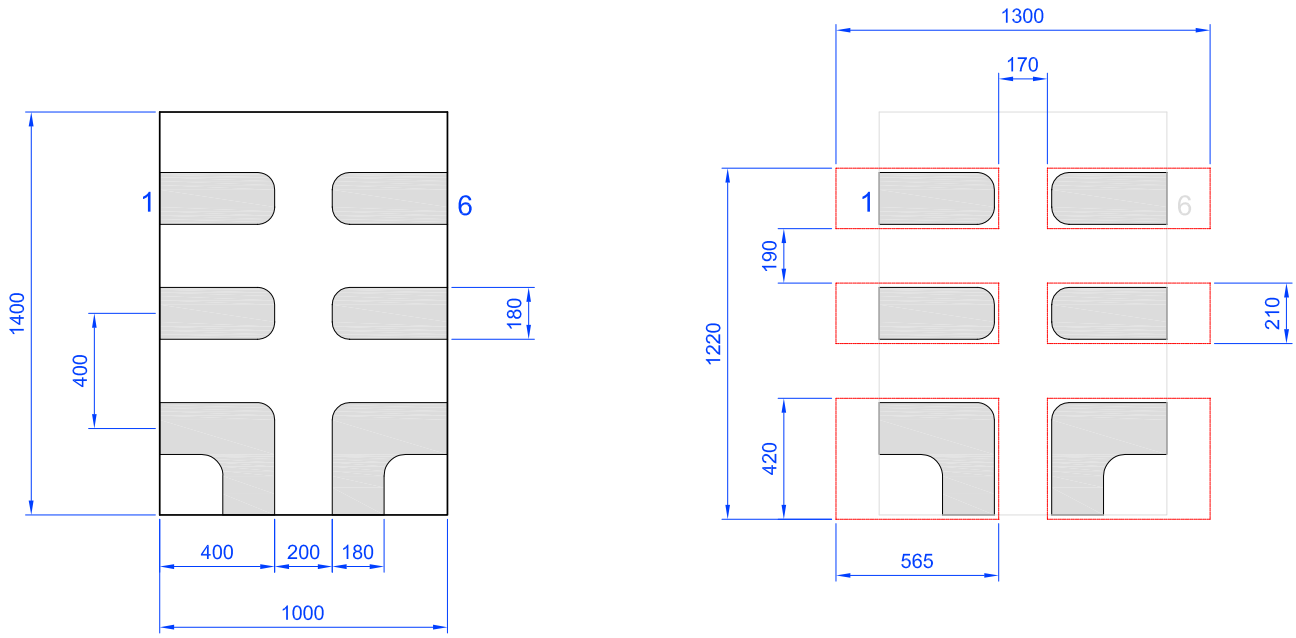


Top View BOTTOM View Side View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.35	1.40	1.45
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	e	0.40 BSC		

Recommended Land Pattern



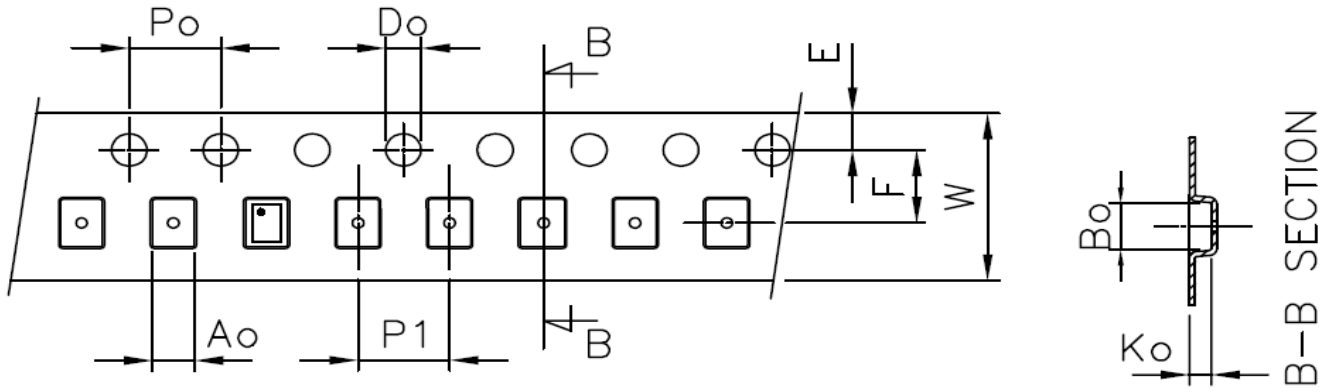
Unit: um

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 6L 1x1.4mm 0.4P FC Green	6	1.0 x 1.4 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 6L 1x1.4mm 0.4P FC Green	1.21	1.62	0.75	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.77 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/23/2017	1.00	Production Release