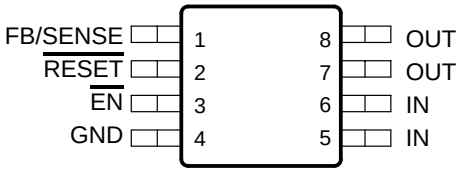
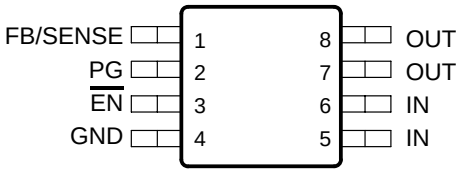
- **Open Drain Power-On Reset With 220-ms Delay (TPS773xx)**
- **Open Drain Power-Good (PG) Status Output (TPS774xx)**
- **250-mA Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.6-V (TPS77316 Only), 1.8-V, 2.7-V, 2.8-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions**
- **Dropout Voltage Typically 200 mV at 250 mA (TPS77333, TPS77433)**
- **Ultralow 92-μA Quiescent Current (Typ)**
- **8-Pin MSOP (DGK) Package**
- **Low Noise (55 $\mu V_{rms}$) Without an External Filter (Bypass) Capacitor (TPS77318, TPS77418)**
- **2% Tolerance Over Specified Conditions For Fixed-Output Versions**
- **Fast Transient Response**
- **Thermal Shutdown Protection**
- **See the TPS779xx Family of Devices for Active High Enable**

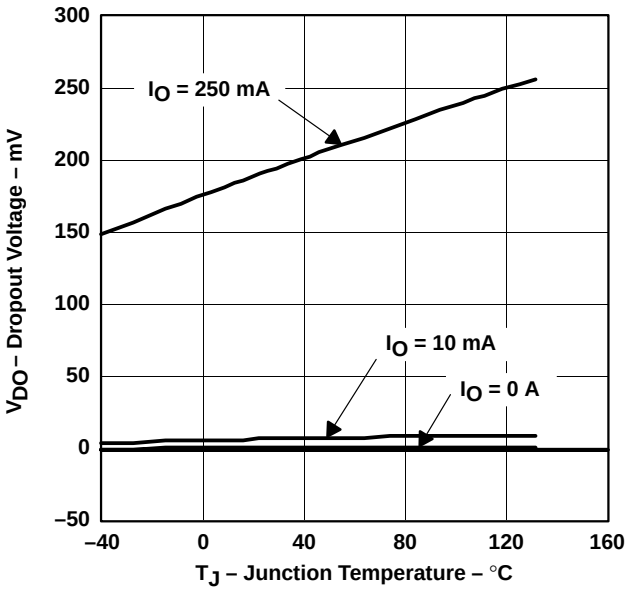
**TPS773xx**
**DGK Package**
**(TOP VIEW)**




**TPS774xx**
**DGK Package**
**(TOP VIEW)**




**TPS77x33**
**DROPOUT VOLTAGE**
**vs**
**JUNCTION TEMPERATURE**




## description

The TPS773xx and TPS774xx are low-dropout regulators with integrated power-on reset and power good (PG) function respectively. These devices are capable of supplying 250 mA of output current with a dropout of 200 mV (TPS77333, TPS77433). Quiescent current is 92 μA at full load dropping down to 1 μA when device is disabled. These devices are optimized to be stable with a wide range of output capacitors including low ESR ceramic (10 μF) or low capacitance (1 μF) tantalum capacitors. These devices have extremely low noise output performance (55 $\mu V_{rms}$) without using any added filter capacitors. TPS773xx and TPS774xx are designed to have fast transient response for larger load current changes.

The TPS773xx or TPS774xx is offered in 1.5-V, 1.6 V (TPS77316 only), 1.8-V, 2.7-V, 2.8-V, 3.3-V, and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is 2% over line, load, and temperature ranges. The TPS773xx and TPS774xx families are available in 8-pin MSOP (DGK) packages.

## description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 200 mV at an output current of 250 mA for 3.3-volt option) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 92 μA over the full range of output current, 0 mA to 250 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The device is enabled when the $\overline{EN}$ pin is connected to a low-level input voltage. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 μA at $T_J$ = 25°C.

The TPS773xx features an integrated power-on reset, commonly used as a supply voltage supervisor (SVS), or reset output voltage. The $\overline{RESET}$ output of the TPS773xx initiates a reset in DSP, microcomputer or microprocessor systems at power up and in the event of an undervoltage condition. An internal comparator in the TPS773xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When OUT reaches 95% of its regulated voltage, $\overline{RESET}$ will go to a high-impedance state after a 220-ms delay. $\overline{RESET}$ will go to low-impedance state when OUT is pulled below 95% (i.e. over load condition) of its regulated voltage.

For the TPS774xx, the power good terminal (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator. An internal comparator in the TPS774xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When OUT falls below 82% of its regulated voltage, PG will go to a low-impedance state. PG will go to a high-impedance state when OUT is above 82% of its regulated voltage.

**AVAILABLE OPTIONS**

| $T_J$ | OUTPUT VOLTAGE (V) | PACKAGED DEVICES MSOP (DGK) | | | |
|---|---|---|---|---|---|
| | TYP | | TPS773xx SYMBOL | | TPS774xx SYMBOL |
| –40°C to 125°C | 5.0 | TPS77350DGK | AGN | TPS77450DGK | AGW |
| | 3.3 | TPS77333DGK | AGM | TPS77433DGK | AGV |
| | 2.8 | TPS77328DGK | AGK | TPS77428DGK | AGT |
| | 2.7 | TPS77327DGK | AGJ | TPS77427DGK | AGS |
| | 1.8 | TPS77318DGK | AGH | TPS77418DGK | AGQ |
| | 1.6 | TPS77316DGK | AWF | — | — |
| | 1.5 | TPS77315DGK | AGG | TPS77415DGK | AGP |
| | Adjustable 1.5 V to 5.5 V | TPS77301DGK | AGF | TPS77401DGK | AGO |

NOTE: The TPS77301 and TPS77401 are programmable using an external resistor divider (see application information). The DGK package is available taped and reeled. Add an R suffix to the device type (e.g., TPS77301DGKR).

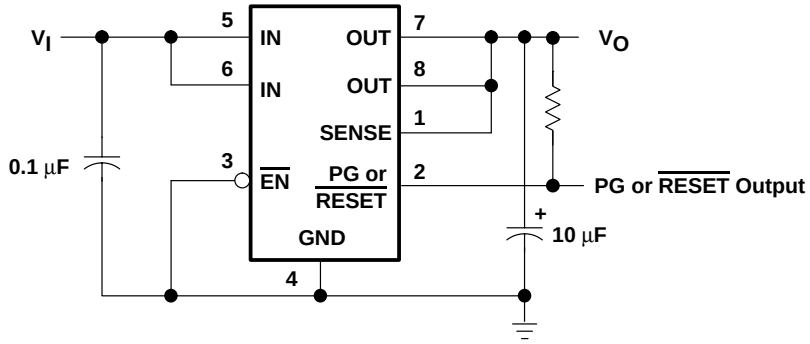
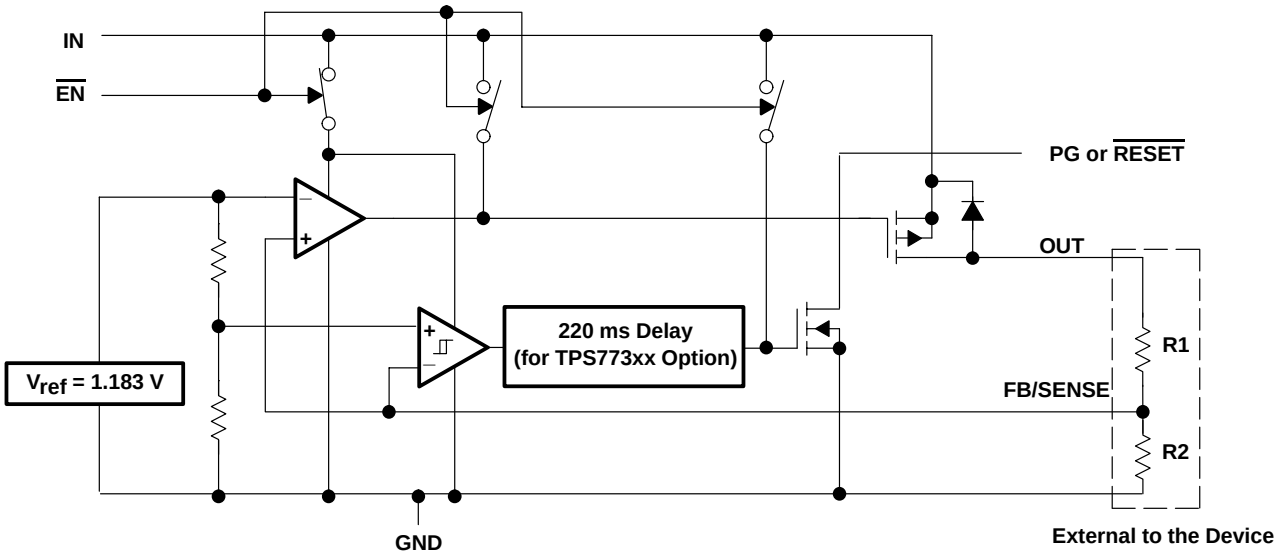


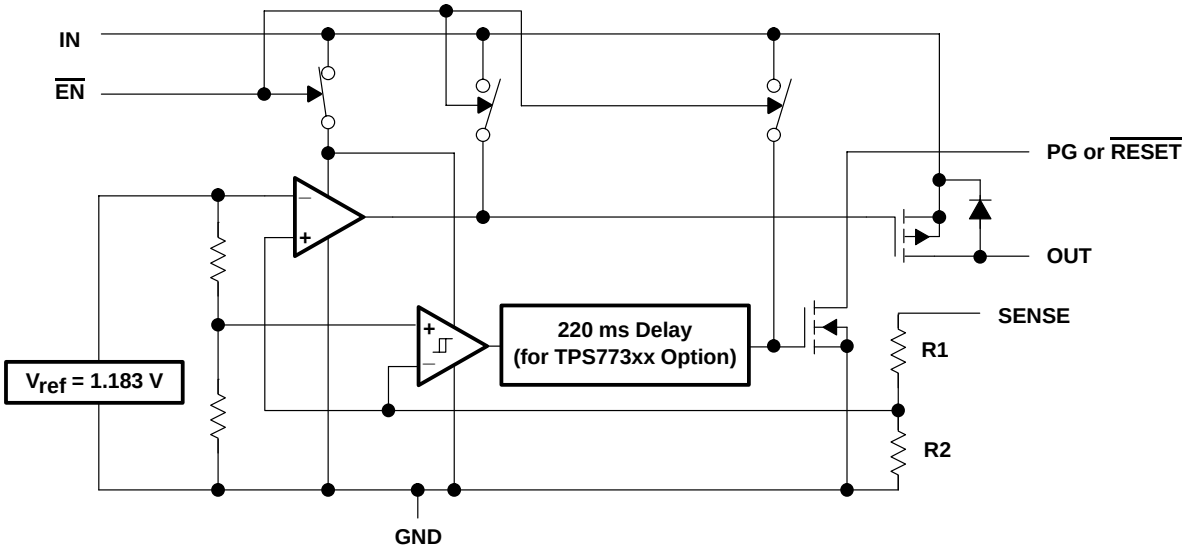

**Figure 1. Typical Application Configuration (For Fixed Output Options)**

## functional block diagrams

### adjustable version



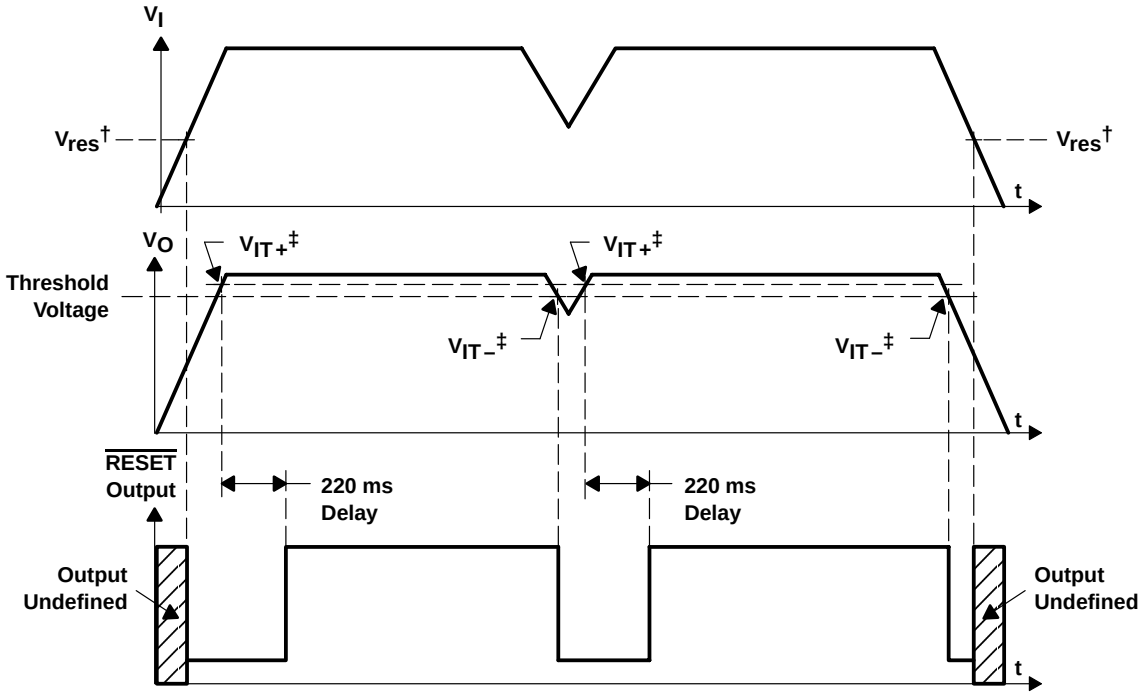

### fixed-voltage version



## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| **TPS773XX** | | | |
| FB/SENSE | 1 | I | Feedback input voltage for adjustable device (sense input for fixed options) |
| $\overline{\text{RESET}}$ | 2 | O | Reset output |
| $\overline{\text{EN}}$ | 3 | I | Enable input |
| GND | 4 | | Regulator ground |
| IN | 5, 6 | I | Input voltage |
| OUT | 7, 8 | O | Regulated output voltage |
| **TPS774XX** | | | |
| FB/SENSE | 1 | I | Feedback input voltage for adjustable device (sense input for fixed options) |
| PG | 2 | O | Power good |
| $\overline{\text{EN}}$ | 3 | I | Enable input |
| GND | 4 | | Regulator ground |
| IN | 5, 6 | I | Input voltage |
| OUT | 7, 8 | O | Regulated output voltage |

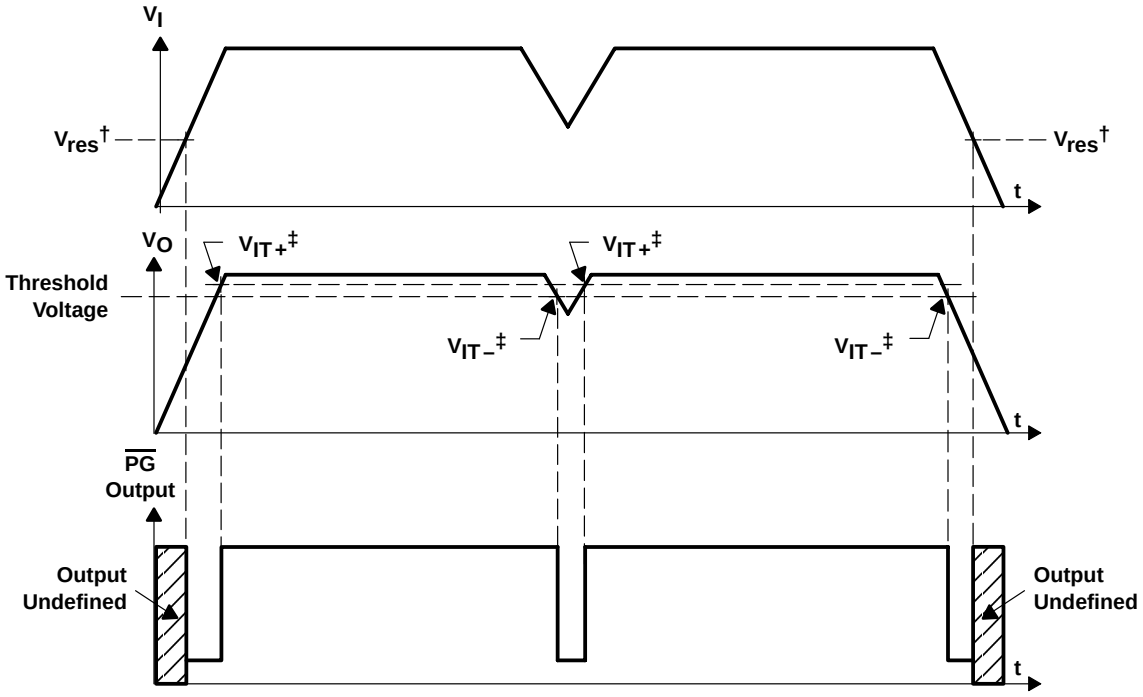
### TPS773xx $\overline{\text{RESET}}$ timing diagram




† $V_{res}$ is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol $V_{res}$ is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ $V_{IT}$ – Trip voltage is typically 5% lower than the output voltage (95%$V_O$) $V_{IT-}$ to $V_{IT+}$ is the hysteresis voltage.

### TPS774xx PG timing diagram




† $V_{res}$ is the minimum input voltage for a valid PG. The symbol $V_{res}$ is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ $V_{IT}$ – Trip voltage is typically 18% lower than the output voltage (82%$V_O$) $V_{IT-}$ to $V_{IT+}$ is the hysteresis voltage.

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range‡, $V_I$ . . . . . –0.3 V to 13.5 V
Voltage range at EN . . . . . –0.3 V to 16.5 V
Maximum RESET voltage (TPS773xx) . . . . . 16.5 V
Maximum PG voltage (TPS774xx) . . . . . 16.5 V
Peak output current . . . . . Internally limited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Output voltage, $V_O$ (OUT, FB) . . . . . 5.5 V
Operating virtual junction temperature range, $T_J$ . . . . . –40°C to 125°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
ESD rating, HBM . . . . . 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

**DISSIPATION RATING TABLE – FREE-AIR TEMPERATURES**

| PACKAGE | AIR FLOW (CFM) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) | $T_A$ < 25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|---|---|---|
| DGK | 0 | 266.2 | 3.84 | 376 mW | 3.76 mW/°C | 207 mW | 150 mW |
| | 150 | 255.2 | 3.92 | 392 mW | 3.92 mW/°C | 216 mW | 157 mW |
| | 250 | 242.8 | 4.21 | 412 mW | 4.12 mW/°C | 227 mW | 165 mW |

### recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Input voltage, $V_I$§ | 2.7 | 10 | V |
| Output voltage range, $V_O$ | 1.5 | 5.5 | V |
| Output current, $I_O$ (see Note 1) | 0 | 250 | mA |
| Operating virtual junction temperature, $T_J$ (see Note 1) | –40 | 125 | °C |

§ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.
NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

**electrical characteristics over recommended operating junction temperature range ($T_J$ = –40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, $I_O$ = 1 mA, $\overline{EN}$ = 0 V, $C_O$ = 10 μF (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output voltage (see Notes 2 and 4) | Adjustable voltage | 1.5 V ≤ $V_O$ ≤ 5.5 V, | $T_J$ = 25°C | | $V_O$ | | V |
| | | 1.5 V ≤ $V_O$ ≤ 5.5 V | | 0.98$V_O$ | | 1.02$V_O$ | |
| | 1.5-V Output | $T_J$ = 25°C, | 2.7 V < $V_{IN}$ < 10 V | | 1.5 | | V |
| | | 2.7 V < $V_{IN}$ < 10 V | | 1.470 | | 1.530 | |
| | 1.6-V Output | $T_J$ = 25°C, | 2.7 V < $V_{IN}$ < 10 V | | 1.6 | | V |
| | | 2.7 V < $V_{IN}$ < 10 V | | 1.568 | | 1.632 | |
| | 1.8-V Output | $T_J$ = 25°C, | 2.8 V < $V_{IN}$ < 10 V | | 1.8 | | V |
| | | 2.8 V < $V_{IN}$ < 10 V | | 1.764 | | 1.836 | |
| | 2.7-V Output | $T_J$ = 25°C, | 3.7 V < $V_{IN}$ < 10 V | | 2.7 | | |
| | | 3.7 V < $V_{IN}$ < 10 V | | 2.646 | | 2.754 | |
| | 2.8-V Output | $T_J$ = 25°C, | 3.8 V < $V_{IN}$ < 10 V | | 2.8 | | |
| | | 3.8 V < $V_{IN}$ < 10 V | | 2.744 | | 2.856 | |
| | 3.3-V Output | $T_J$ = 25°C, | 4.3 V < $V_{IN}$ < 10 V | | 3.3 | | |
| | | 4.3 V < $V_{IN}$ < 10 V | | 3.234 | | 3.366 | |
| | 5.0-V Output | $T_J$ = 25°C, | 6.0 V < $V_{IN}$ < 10 V | | 5.0 | | V |
| | | 6.0 V < $V_{IN}$ < 10 V | | 4.900 | | 5.100 | |
| Quiescent current (GND current) (see Notes 2 and 4) | | $T_J$ = 25°C | | | 92 | | μA |
| | | | | | | 125 | |
| Output voltage line regulation ($\Delta V_O/V_O$) (see Note 3) | | $V_O$ + 1 V < $V_I$ ≤ 10 V, | $T_J$ = 25°C | | 0.005 | | %/V |
| | | $V_O$ + 1 V < $V_I$ ≤ 10 V | | | | 0.05 | %/V |
| Load regulation | | $T_J$ = 25°C | | | 1 | | mV |
| Output noise voltage | | BW = 300 Hz to 100 kHz, $T_J$ = 25°C, TPS77318, TPS77418 | | | 55 | | μVrms |
| Output current limit | | $V_O$ = 0 V | | | 0.9 | 1.3 | A |
| Peak output current | | 2 ms pulse width, | 50% duty cycle | | 400 | | mA |
| Thermal shutdown junction temperature | | | | | 144 | | °C |
| Standby current | | $\overline{EN}$ = $V_I$, | $T_J$ = 25°C | | | 1 | μA |
| | | $\overline{EN}$ = $V_I$ | | | | 3 | μA |
| FB input current | Adjustable voltage | FB = 1.5 V | | | | 1 | μA |
| High level enable input voltage | | | | 2 | | | V |
| Low level enable input voltage | | | | | | 0.7 | V |
| Enable input current | | | | –1 | | 1 | μA |
| Power supply ripple rejection (TPS77318, TPS77418) | | f = 1 kHz, | $T_J$ = 25°C | | 55 | | dB |

NOTES: 2. Minimum input operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum input voltage = 10 V, minimum output current 1 mA.

3. If $V_O$ < 1.8 V then $V_{I(max)}$ = 10 V, $V_{I(min)}$ = 2.7 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{I(max)} - 2.7\ V\right)}{100} \times 1000$$

If $V_O$ > 2.5 V then $V_{I(max)}$ = 10 V, $V_{I(min)} = V_O$ + 1 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{I(max)} - \left(V_O + 1\right)\right)}{100} \times 1000$$

4. $I_O$ = 1 mA to 250 mA

**electrical characteristics over recommended operating junction temperature range ($T_J$ = –40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, $I_O$ = 1 mA, $\overline{EN}$ = 0 V, $C_O$ = 10 μF (unless otherwise noted) (continued)**

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| PG (TPS774xx) | Minimum input voltage for valid PG | | $I_{(PG)}$ = 300 μA, $V_{(PG)} \le$ 0.8 V | | 1.1 | | V |
| | Trip threshold voltage | | $V_O$ decreasing | 79 | | 85 | %$V_O$ |
| | Hysteresis voltage | | Measured at $V_O$ | | 0.5 | | %$V_O$ |
| | Output low voltage | | $V_I$ = 2.7 V, $I_{(PG)}$ = 1 mA | | 0.15 | 0.4 | V |
| | Leakage current | | $V_{(PG)}$ = 5 V | | | 1 | μA |
| Reset (TPS773xx) | Minimum input voltage for valid $\overline{\text{RESET}}$ | | $I_{(RESET)}$ = 300 μA | | 1.1 | | V |
| | Trip threshold voltage | | $V_O$ decreasing | 92 | | 98 | %$V_O$ |
| | Hysteresis voltage | | Measured at $V_O$ | | 0.5 | | %$V_O$ |
| | Output low voltage | | $V_I$ = 2.7 V, $I_{(RESET)}$ = 1 mA | | 0.15 | 0.4 | V |
| | Leakage current | | $V_{(RESET)}$ = 5 V | | | 1 | μA |
| | RESET time-out delay | | | | 220 | | ms |
| $V_{DO}$ | Dropout voltage (see Note 5) | 2.8-V Output | $I_O$ = 250 mA, $T_J$ = 25°C | | 270 | | mV |
| | | | $I_O$ = 250 mA | | | 475 | |
| | | 3.3-V Output | $I_O$ = 250 mA, $T_J$ = 25°C | | 200 | | |
| | | | $I_O$ = 250 mA | | | 330 | |
| $V_{DO}$ | Dropout voltage (see Note 5) | 5.0-V Output | $I_O$ = 250 mA, $T_J$ = 25°C | | 125 | | |
| | | | $I_O$ = 250 mA | | | 190 | |

NOTE 5: IN voltage equals $V_O$(typ) – 100 mV; 1.5 V, 1.6 V, 1.8-V, and 2.7-V dropout voltage limited by input voltage range limitations (i.e., 3.3 V input voltage needs to drop to 3.2 V for purpose of this test).

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_O$ | Output voltage | vs Output current | 2, 3 |
| | | vs Junction temperature | 4, 5 |
| | Ground current | vs Junction temperature | 6 |
| | Power supply rejection ratio | vs Frequency | 7 |
| | Output spectral noise density | vs Frequency | 8 |
| $Z_o$ | Output impedance | vs Frequency | 9 |
| $V_{DO}$ | Dropout voltage | vs Input voltage | 10 |
| | | vs Junction temperature | 11 |
| | Line transient response | | 12, 14 |
| | Load transient response | | 13, 15 |
| | Output voltage and enable pulse | vs Time | 16 |
| | Equivalent series resistance (ESR) | vs Output current | 18 – 21 |

## TYPICAL CHARACTERISTICS

TPS77x33
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

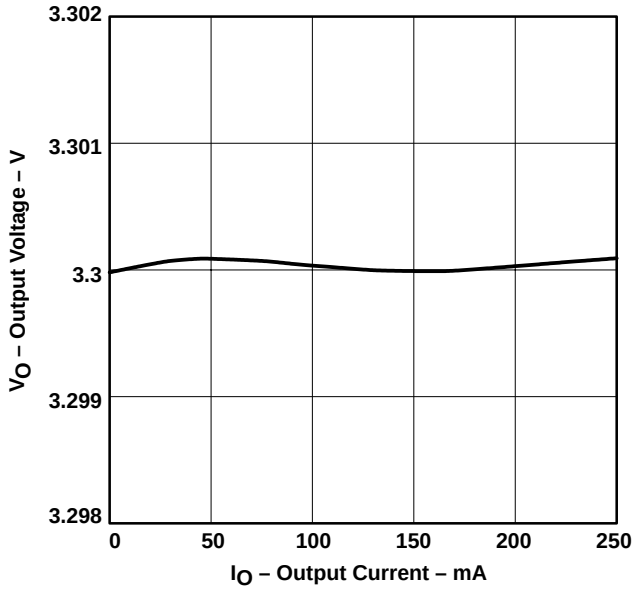



Figure 2

TPS77x18
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

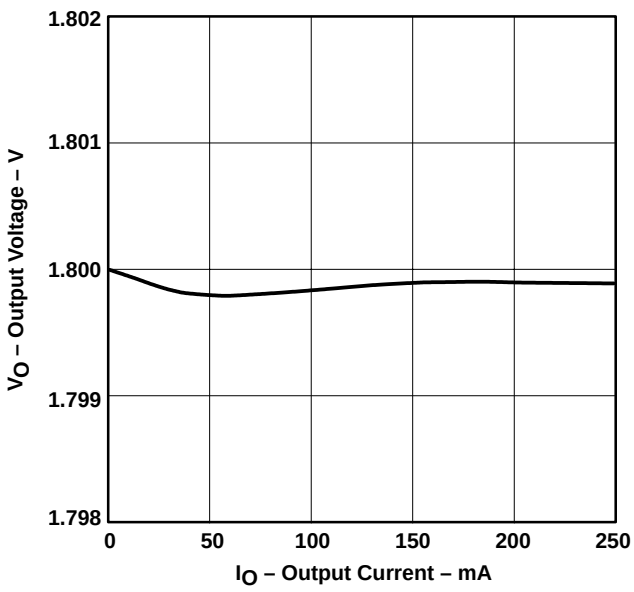



Figure 3

TPS77x33
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

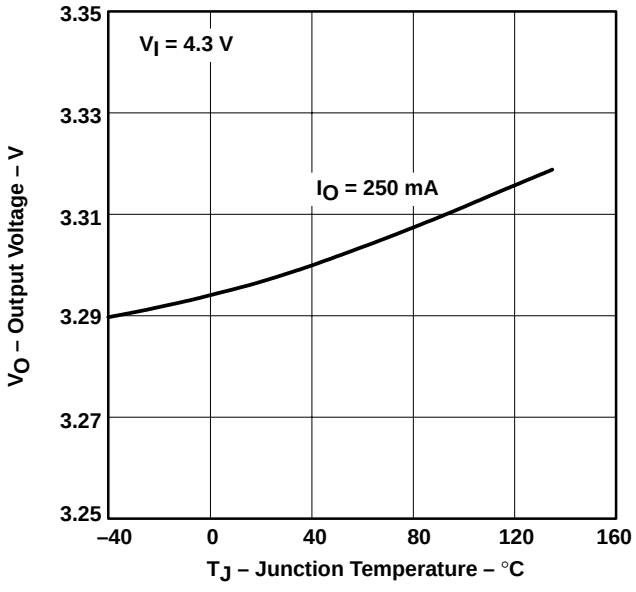



Figure 4

TPS77x18
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

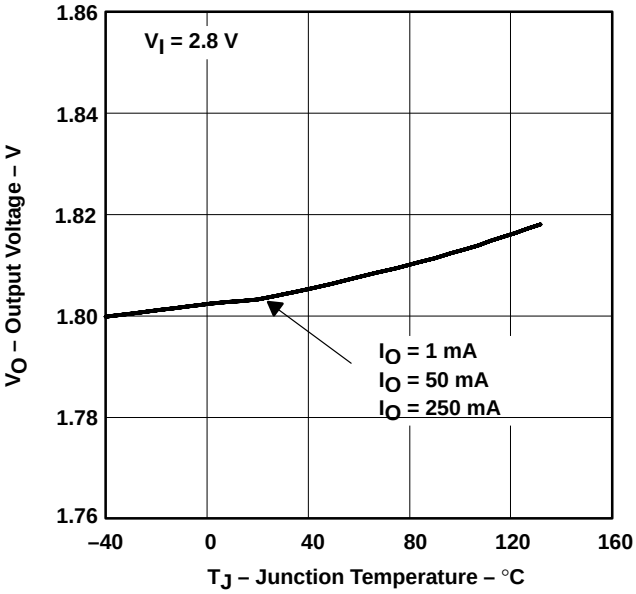



Figure 5

## TYPICAL CHARACTERISTICS

**TPS77xxx**
**GROUND CURRENT**
**vs**
**JUNCTION TEMPERATURE**

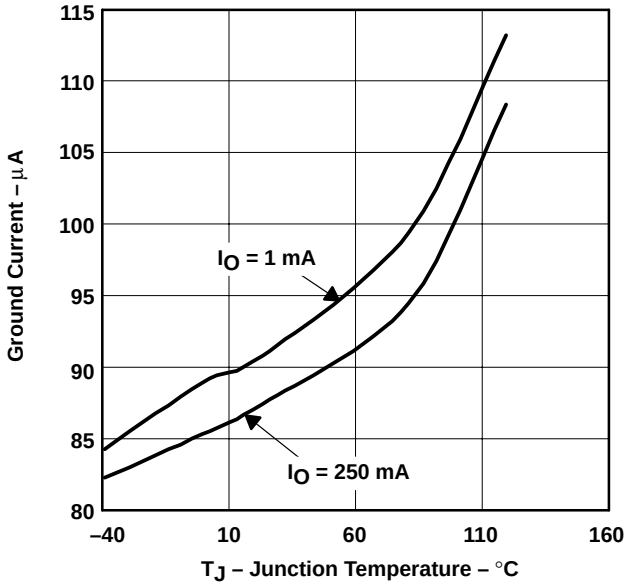



**Figure 6**

**TPS77x33**
**POWER SUPPLY REJECTION RATIO**
**vs**
**FREQUENCY**

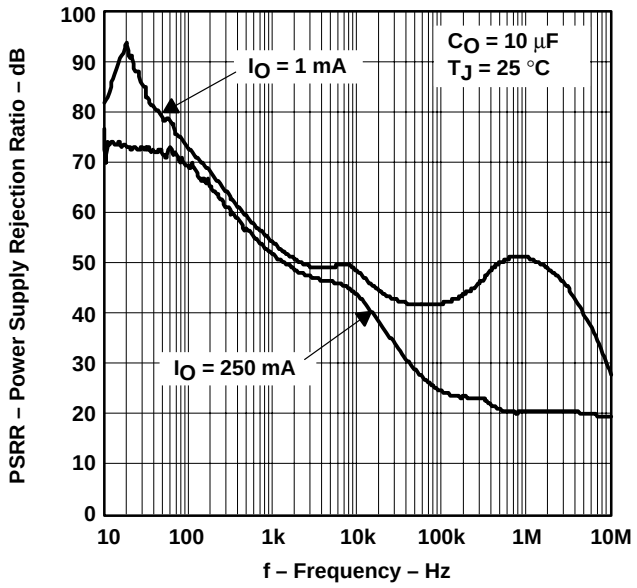



**Figure 7**

**TPS77x33**
**OUTPUT SPECTRAL NOISE DENSITY**
**vs**
**FREQUENCY**

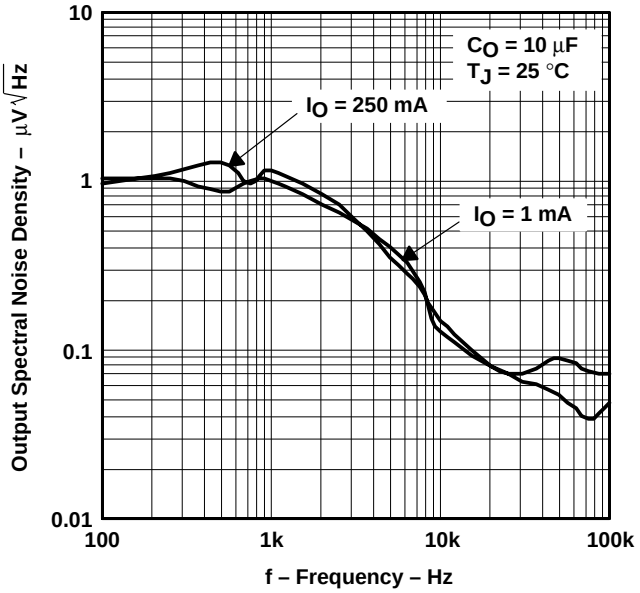



**Figure 8**

## TYPICAL CHARACTERISTICS

**TPS77x33**
**OUTPUT IMPEDANCE**
**vs**
**FREQUENCY**

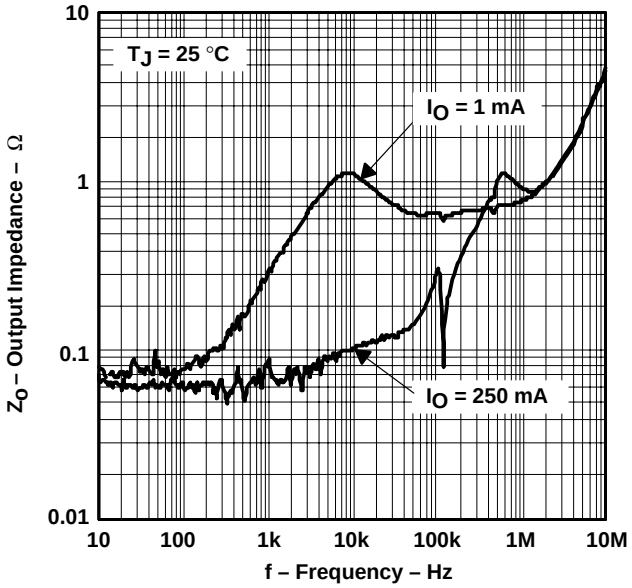



**Figure 9**

**TPS77x01**
**DROPOUT VOLTAGE**
**vs**
**INPUT VOLTAGE**

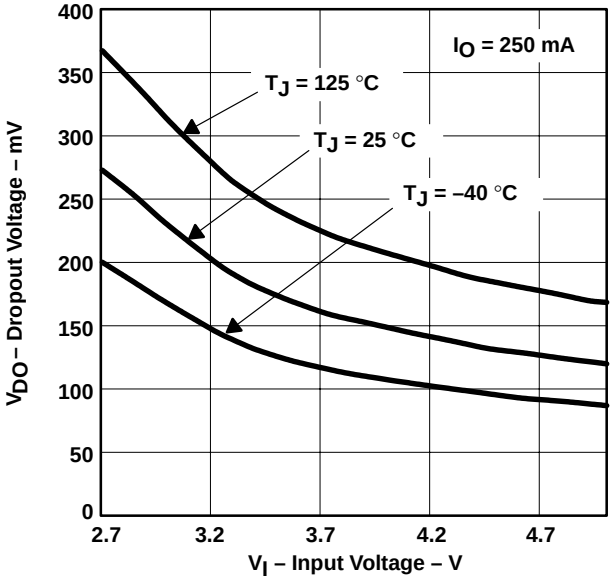



**Figure 10**

**TPS77x33**
**DROPOUT VOLTAGE**
**vs**
**JUNCTION TEMPERATURE**

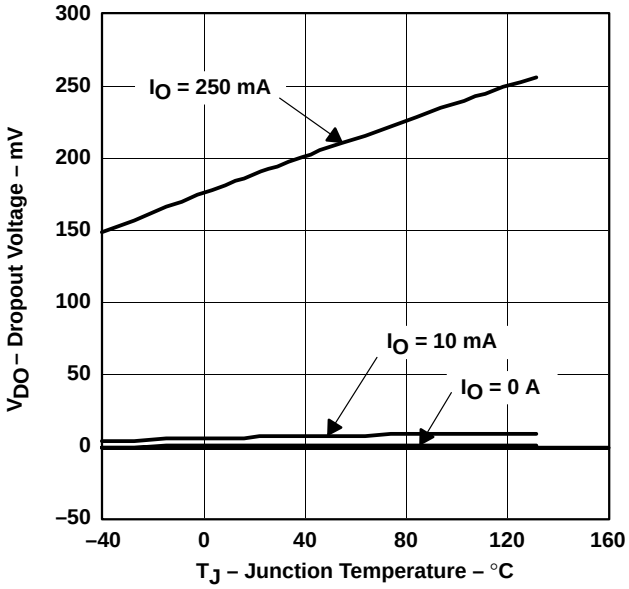



**Figure 11**

## TYPICAL CHARACTERISTICS

TPS77x18
LINE TRANSIENT RESPONSE

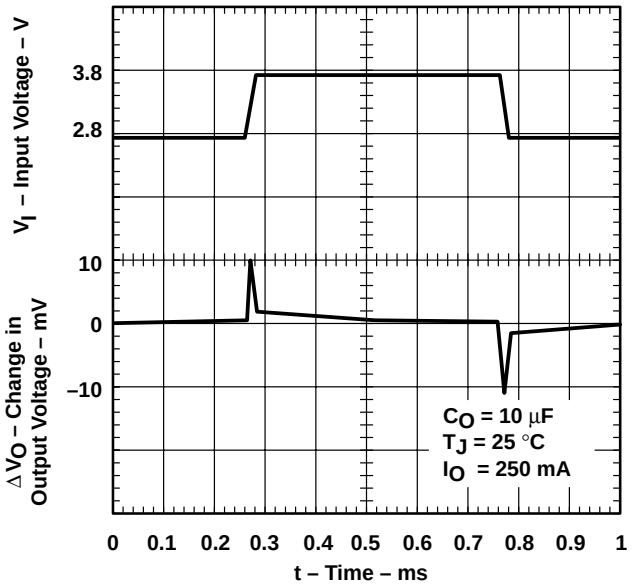



Figure 12

TPS77x18
LOAD TRANSIENT RESPONSE

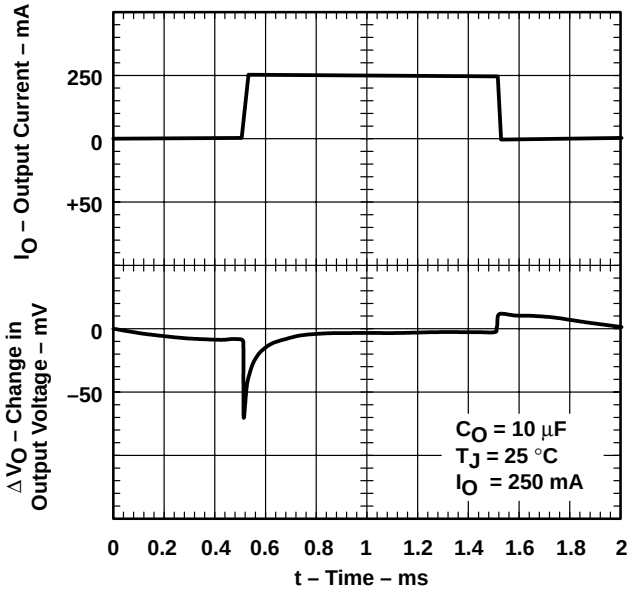



Figure 13

TPS77x33
LINE TRANSIENT RESPONSE

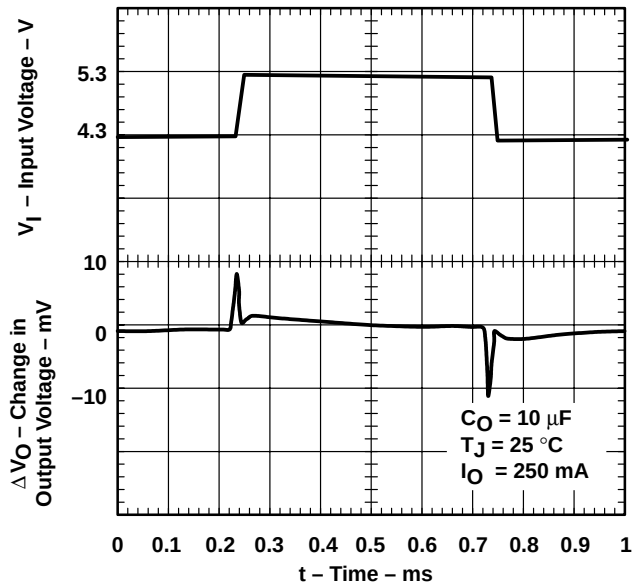



Figure 14

TPS77x33
LOAD TRANSIENT RESPONSE

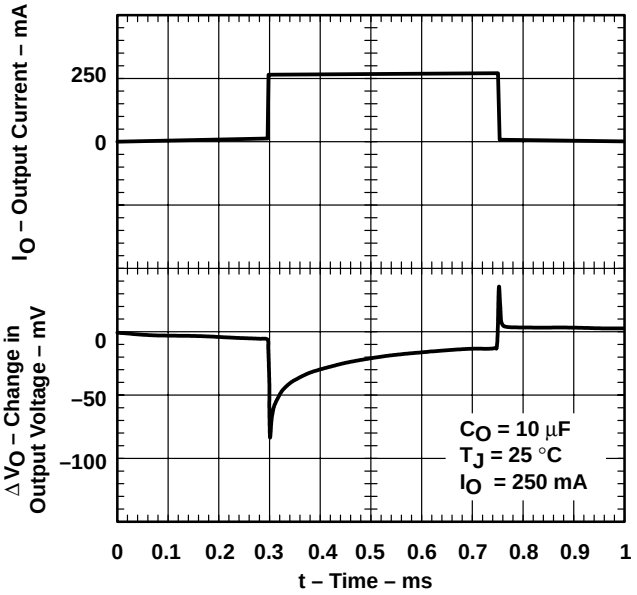



Figure 15

## TYPICAL CHARACTERISTICS

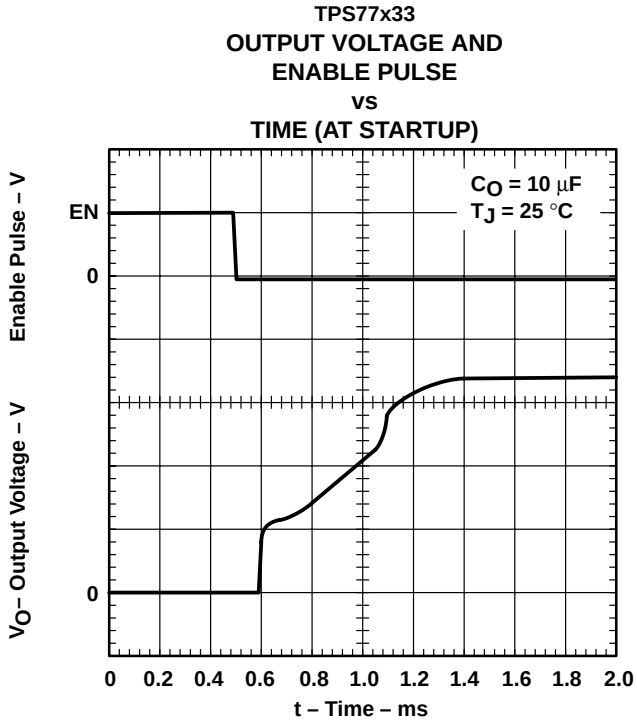



**Figure 16**

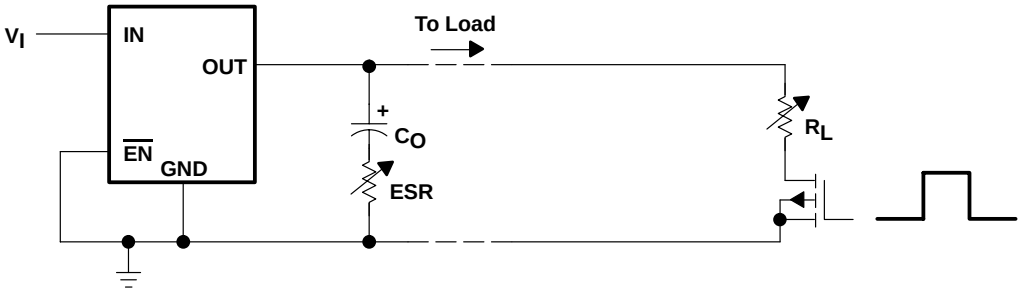



**Figure 17. Test Circuit for Typical Regions of Stability (Figures 18 through 21) (Fixed Output Options)**

## TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

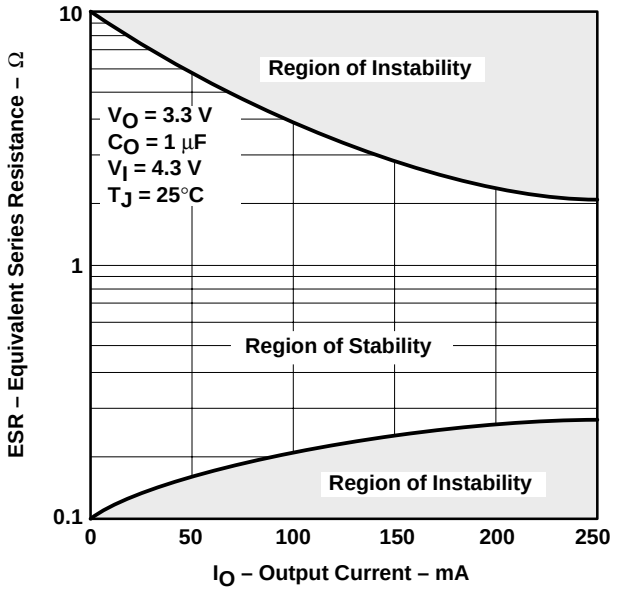



Figure 18

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

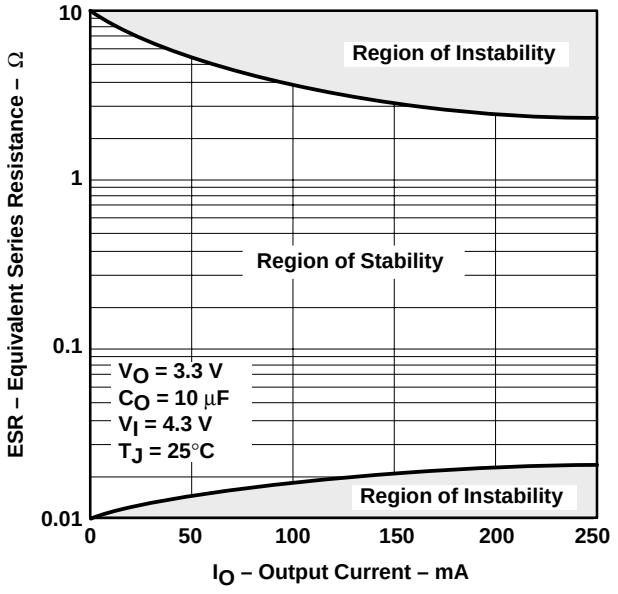



Figure 19

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

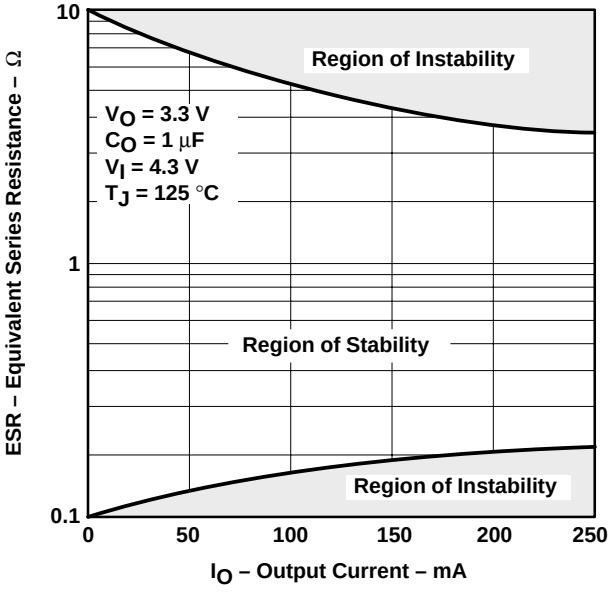



Figure 20

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

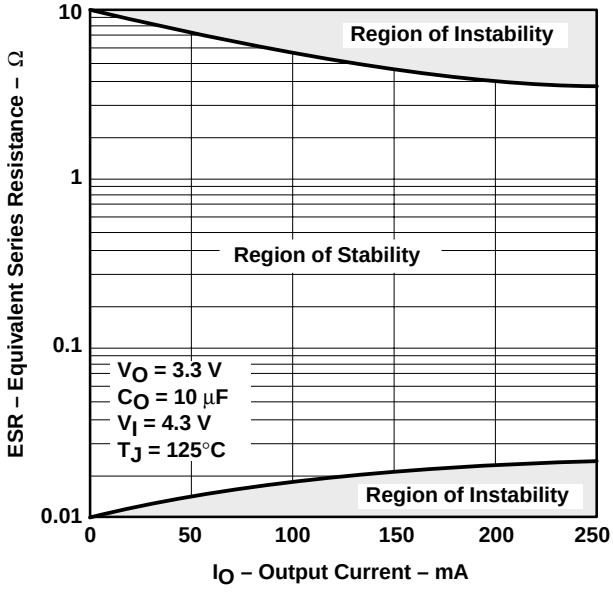



Figure 21

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to $C_O$.

## APPLICATION INFORMATION

### pin functions

#### enable ($\overline{\text{EN}}$)

The $\overline{\text{EN}}$ terminal is an input which enables or shuts down the device. If $\overline{\text{EN}}$ is a logic high, the device will be in shutdown mode. When $\overline{\text{EN}}$ goes to logic low, then the device will be enabled.

#### power good (PG) (TPS774xx)

The PG terminal is an open drain, active high output that indicates the status of $V_{out}$ (output of the LDO). When $V_{out}$ reaches 82% of the regulated voltage, PG will go to a high-impedance state. It will go to a low-impedance state when $V_{out}$ falls below 82% (i.e. over load condition) of the regulated voltage. The open drain output of the PG terminal requires a pullup resistor.

#### sense (SENSE)

The SENSE terminal of the fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way to minimize/avoid noise pickup. Adding RC networks between the SENSE terminal and $V_{out}$ to filter noise is not recommended because it may cause the regulator to oscillate.

#### feedback (FB)

FB is an input terminal used for the adjustable-output options and must be connected to an external feedback resistor divider. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and $V_{out}$ to filter noise is not recommended because it may cause the regulator to oscillate.

#### reset ($\overline{\text{RESET}}$) (TPS773xx)

The $\overline{\text{RESET}}$ terminal is an open drain, active low output that indicates the status of $V_{out}$. When $V_{out}$ reaches 95% of the regulated voltage, $\overline{\text{RESET}}$ will go to a high-impedance state after a 220-ms delay. $\overline{\text{RESET}}$ will go to a low-impedance state when $V_{out}$ is below 95% of the regulated voltage. The open-drain output of the $\overline{\text{RESET}}$ terminal requires a pullup resistor.

### external capacitor requirements

An input capacitor is not usually required; however, a bypass capacitor (0.047 μF or larger) improves load transient response and noise rejection if the TPS773xx or TPS774xx is located more than a few inches from the power supply. A higher-capacitance capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Most low noise LDOs require an external capacitor to further reduce noise. This will impact the cost and board space. The TPS773xx and TPS774xx have very low noise specification requirements without using any external components.

Like all low dropout regulators, the TPS773xx or TPS774xx requires an output capacitor connected between OUT (output of the LDO) and GND (signal ground) to stabilize the internal control loop. The minimum recommended capacitance value is 1 μF provided the ESR meets the requirement in Figures 19 and 21. In addition, a low-ESR capacitor can be used if the capacitance is at least 10 μF and the ESR meets the requirements in Figures 18 and 20. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

## APPLICATION INFORMATION

### external capacitor requirements (continued)

Ceramic capacitors have different types of dielectric material with each exhibiting different temperature and voltage variation. The most common types are X5R, X7R, Y5U, Z5U, and NPO. The NPO type ceramic type capacitors are generally the most stable over temperature. However, the X5R and X7R are also relatively stable over temperature (with the X7R being the more stable of the two) and are therefore acceptable to use. The Y5U and Z5U types provide high capacitance in a small geometry, but exhibit large variations over temperature; therefore, the Y5U and Z5U are not generally recommended for use on this LDO. Independent of which type of capacitor is used, one must make certain that at the worst case condition the capacitance/ESR meets the requirement specified in Figures 18 – 21.

Figure 22 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

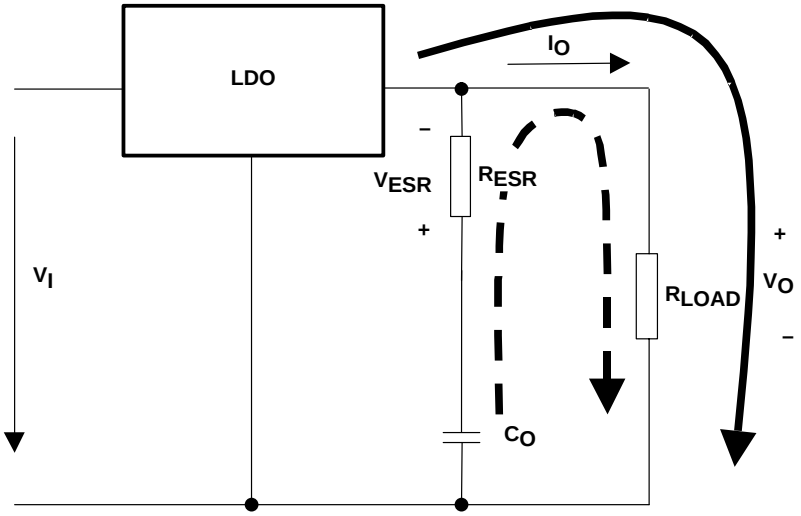



**Figure 22. LDO Output Stage With Parasitic Resistances ESR**

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V_{Cout} = V_{out}$). This means no current is flowing into the $C_{out}$ branch. If $I_{out}$ suddenly increases (transient condition), the following occurs:

- The LDO is not able to supply the sudden current need due to its response time ($t_1$ in Figure 23). Therefore, capacitor $C_{out}$ provides the current for the new load condition (dashed arrow). $C_{out}$ now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop will occur at $R_{ESR}$. This voltage is shown as $V_{ESR}$ in Figure 22.
- When $C_{out}$ is conducting current to the load, initial voltage at the load will be $V_{out} = V_{Cout} – V_{ESR}$. Due to the discharge of $C_{out}$, the output voltage $V_{out}$ will drop continuously until the response time $t_1$ of the LDO is reached and the LDO will resume supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as $t_2$ in Figure 23.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

## APPLICATION INFORMATION

### conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

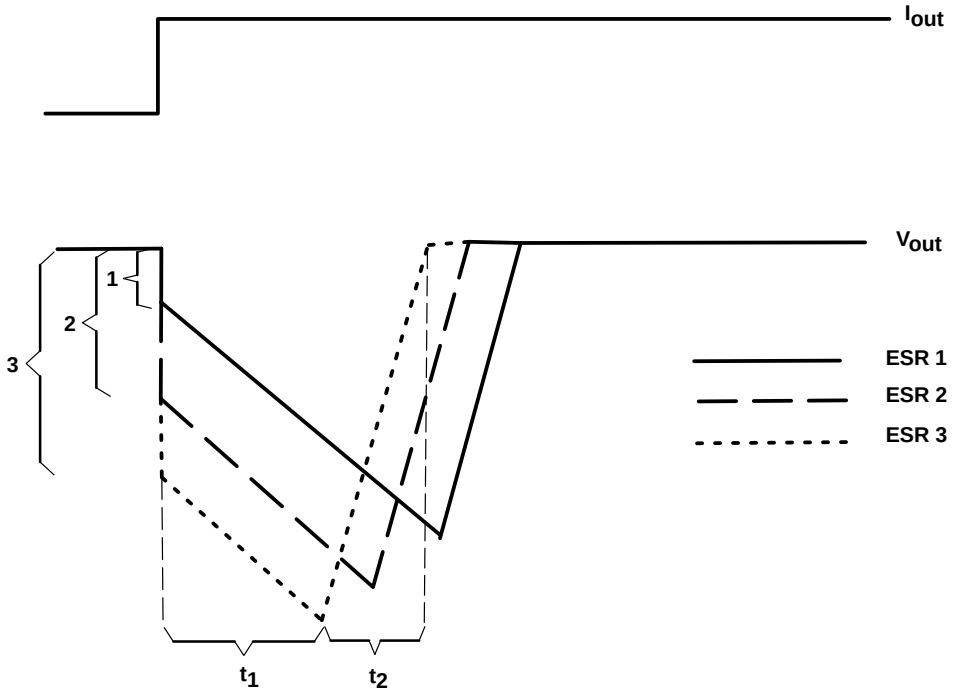



**Figure 23. Correlation of Different ESRs and Their Influence to the Regulation of $V_{out}$ at a Load Step From Low-to-High Output Current**

## APPLICATION INFORMATION

### programming the TPS77x01 adjustable LDO regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 24. The output voltage is calculated using:

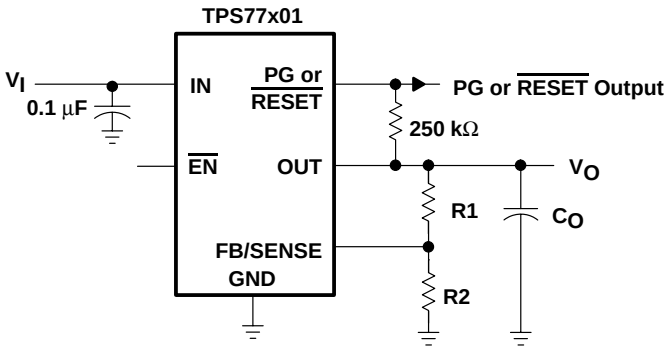
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

$V_{ref}$ = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided, as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$




**OUTPUT VOLTAGE PROGRAMMING GUIDE**

| OUTPUT VOLTAGE | R1 | R2 | UNIT |
|---|---|---|---|
| 2.5 V | 33.5 | 30.1 | kΩ |
| 3.3 V | 53.8 | 30.1 | kΩ |
| 3.6 V | 61.5 | 30.1 | kΩ |

**NOTE: To reduce noise and prevent oscillation, R1 and R2 need to be as close as possible to the FB/SENSE terminal.**

**Figure 24. TPS77x01 Adjustable LDO Regulator Programming**

## APPLICATION INFORMATION

### regulator protection

The TPS773xx or TPS774xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS773xx or TPS774xx also features internal current limiting and thermal protection. During normal operation, the TPS773xx or TPS774xx limits output current to approximately 0.9 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

### power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, $P_D$, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 266.2°C/W for the 8-terminal MSOP with no airflow.

$T_A$ is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS77301DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGF | Samples |
| TPS77301DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGF | Samples |
| TPS77315DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGG | Samples |
| TPS77315DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGG | Samples |
| TPS77316DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AWF | Samples |
| TPS77316DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AWF | Samples |
| TPS77318DGK | LIFEBUY | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGH | |
| TPS77318DGKG4 | LIFEBUY | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGH | |
| TPS77318DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGH | Samples |
| TPS77328DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGK | Samples |
| TPS77333DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGM | Samples |
| TPS77333DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGM | Samples |
| TPS77350DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGN | Samples |
| TPS77350DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGN | Samples |
| TPS77401DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGO | Samples |
| TPS77415DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGP | Samples |
| TPS77418DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGQ | Samples |
| TPS77428DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGT | Samples |
| TPS77433DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGV | Samples |
| TPS77433DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGV | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS77450DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AGW | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

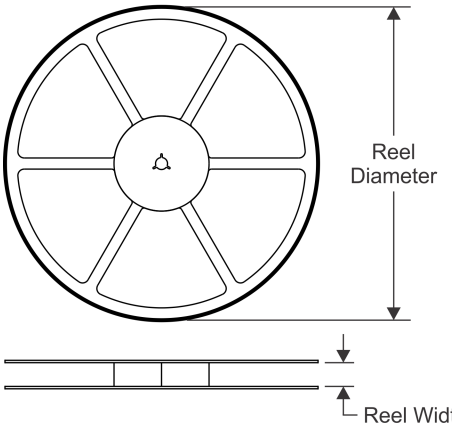
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

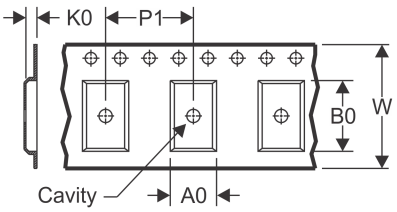
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

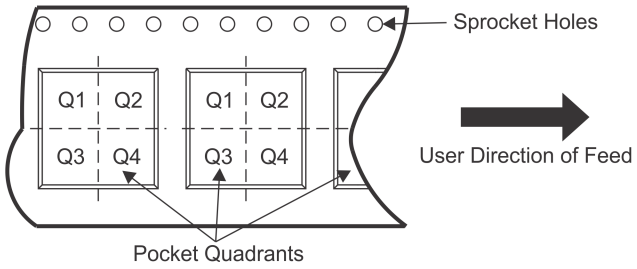



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

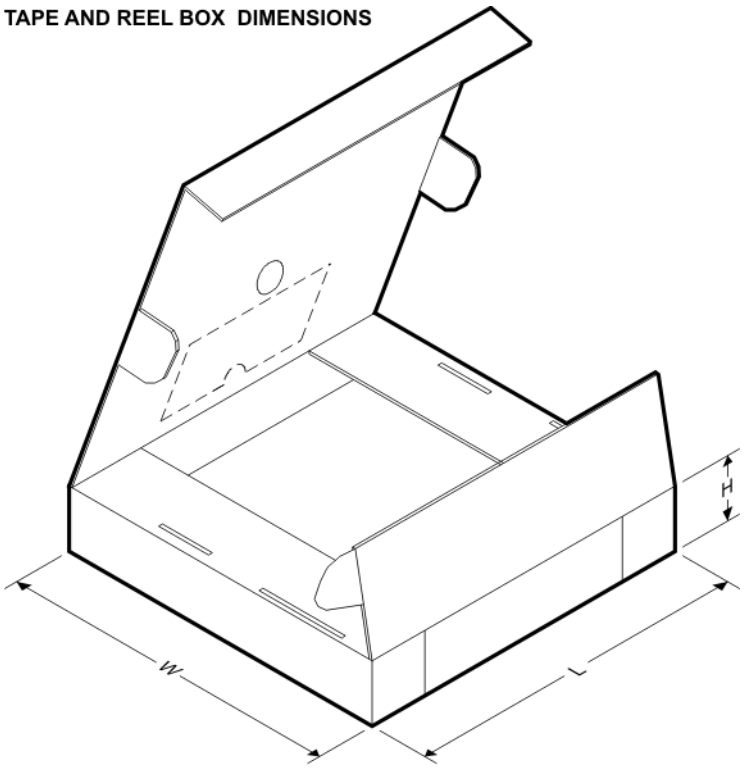
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS77301DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS77315DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS77316DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS77318DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS77333DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS77350DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS77433DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS77301DGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS77315DGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS77316DGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS77318DGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS77333DGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS77350DGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS77433DGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |

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