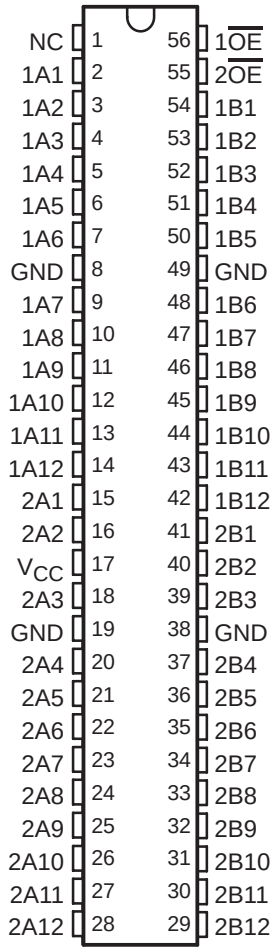
SCDS043I − DECEMBER 1997 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

**DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

The SN74CBTLV16211 provides 24 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable ($\overline{OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

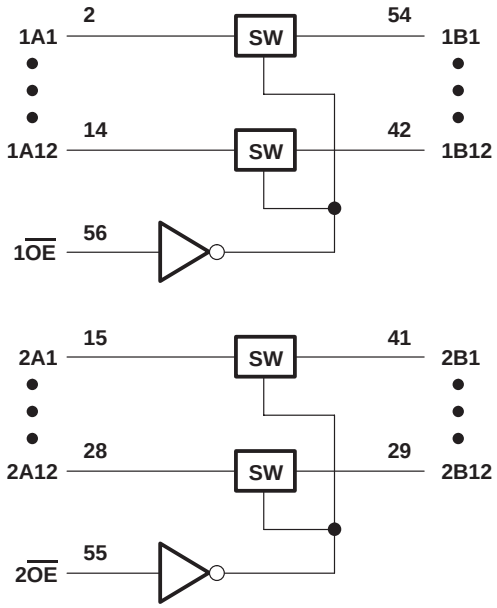
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SSOP − DL | Tube | SN74CBTLV16211DL | CBTLV16211 |
| | | Tape and reel | SN74CBTLV16211DLR | |
| | TSSOP − DGG | Tape and reel | SN74CBTLV16211GR | CBTLV16211 |
| | TVSOP − DGV | Tape and reel | SN74CBTLV16211VR | CN211 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

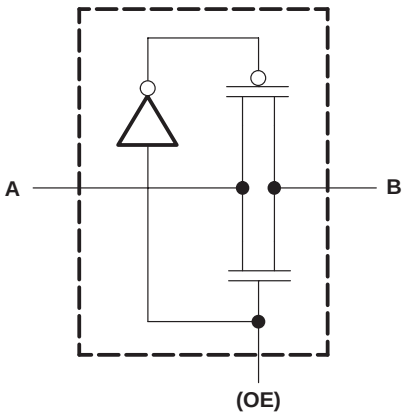
**FUNCTION TABLE**
**(each 12-bit bus switch)**

| INPUT $\overline{OE}$ | FUNCTION |
|---|---|
| L | A port = B port |
| H | Disconnect |

## logic diagram (positive logic)




## simplified schematic, each FET switch



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 4.6 V
Continuous channel current . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 64°C/W
DGV package . . . . . 48°C/W
DL package . . . . . 56°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

NOTE 3: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 3 V, | $I_I$ = −18 mA | | | | −1.2 | V |
| $I_I$ | | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | | ±1 | μA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 3.6 V | | | | 10 | μA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, | $I_O$ = 0, | $V_I$ = $V_{CC}$ or GND | | | 10 | μA |
| $\Delta I_{CC}$‡ | Control inputs | $V_{CC}$ = 3.6 V, | One input at 3 V, | Other inputs at $V_{CC}$ or GND | | | 300 | μA |
| $C_i$ | Control inputs | $V_I$ = 3.3 V or 0 | | | | 4.5 | | pF |
| $C_{io(OFF)}$ | | $V_O$ = 3.3 V or 0, | $\overline{OE}$ = $V_{CC}$ | | | 6.5 | | pF |
| $r_{on}$§ | | $V_{CC}$ = 2.3 V, TYP at $V_{CC}$ = 2.5 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 8 | Ω |
| | | | | $I_I$ = 24 mA | | 5 | 8 | |
| | | | $V_I$ = 1.7 V, | $I_I$ = 15 mA | | 27 | 40 | |
| | | $V_{CC}$ = 3 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 7 | |
| | | | | $I_I$ = 24 mA | | 5 | 7 | |
| | | | $V_I$ = 2.4 V, | $I_I$ = 15 mA | | 10 | 15 | |

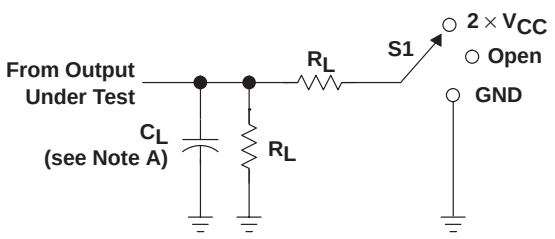
† All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
‡ This is the increase in supply current for each input that is at the specified voltage level, rather than $V_{CC}$ or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$¶ | A or B | B or A | | 0.15 | | 0.25 | ns |
| $t_{en}$ | $\overline{OE}$ | A or B | 1 | 7 | 1 | 6.2 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | 1 | 7.2 | 1 | 7.7 | ns |

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

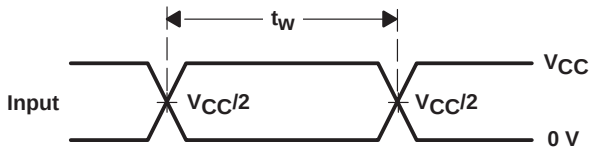
## PARAMETER MEASUREMENT INFORMATION



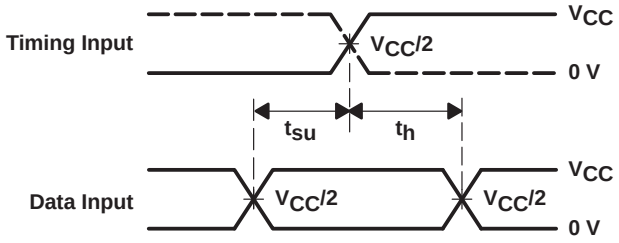

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

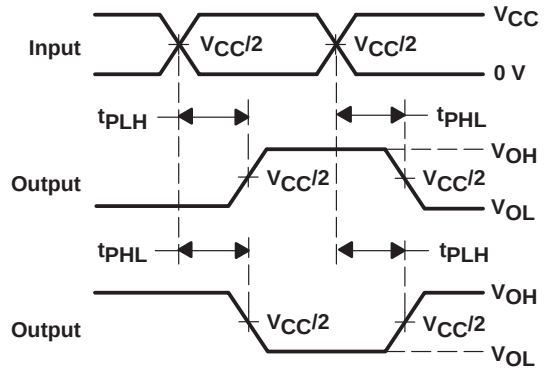
| $V_{CC}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|
| 2.5 V ±0.2 V | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ±0.3 V | 50 pF | 500 Ω | 0.3 V |



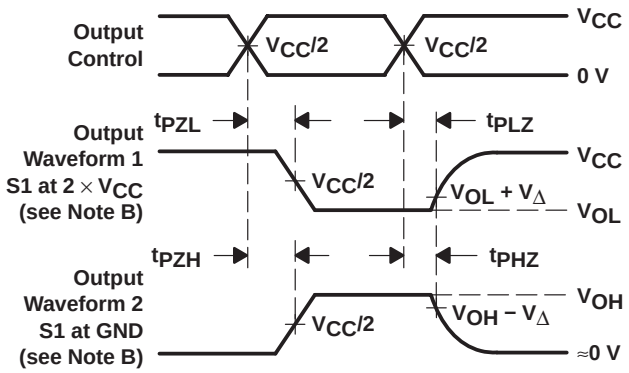

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74CBTLV16211DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16211 | Samples |
| 74CBTLV16211GRG4 | ACTIVE | TSSOP | DGG | 56 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16211 | Samples |
| SN74CBTLV16211DL | ACTIVE | SSOP | DL | 56 | 20 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16211 | Samples |
| SN74CBTLV16211DLR | ACTIVE | SSOP | DL | 56 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16211 | Samples |
| SN74CBTLV16211GR | ACTIVE | TSSOP | DGG | 56 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16211 | Samples |
| SN74CBTLV16211VR | ACTIVE | TVSOP | DGV | 56 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CN211 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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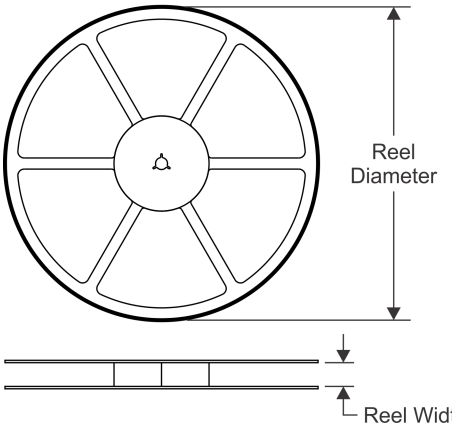
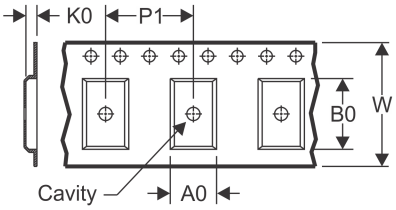
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

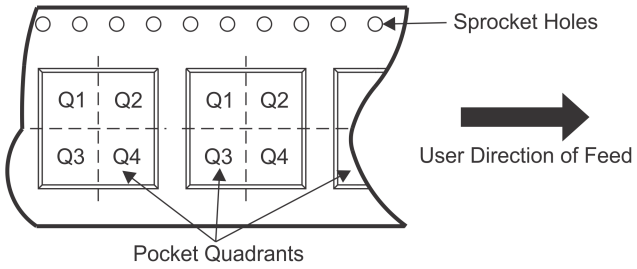



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

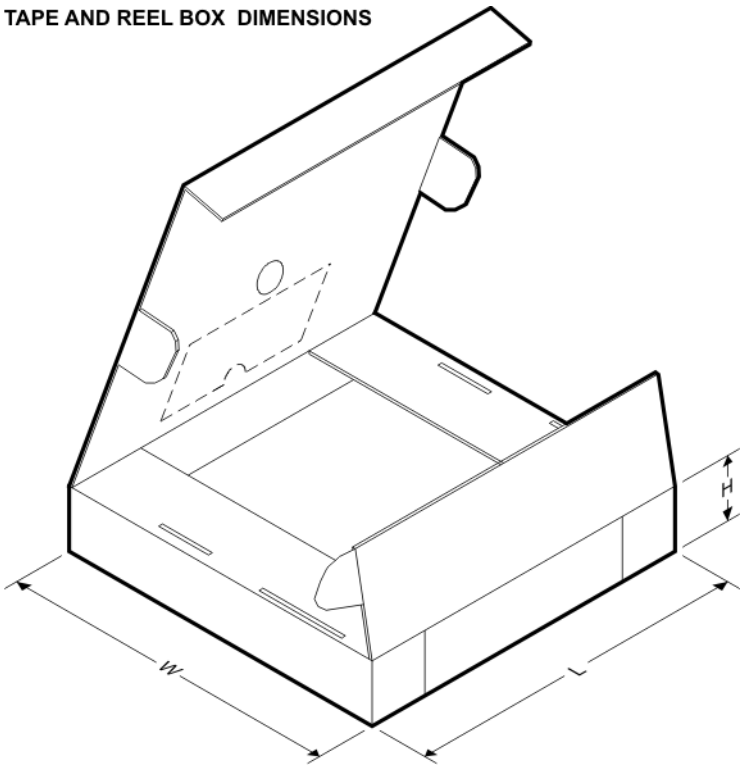
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74CBTLV16211DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74CBTLV16211GR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74CBTLV16211VR | TVSOP | DGV | 56 | 2000 | 330.0 | 24.4 | 6.8 | 11.7 | 1.6 | 12.0 | 24.0 | Q1 |

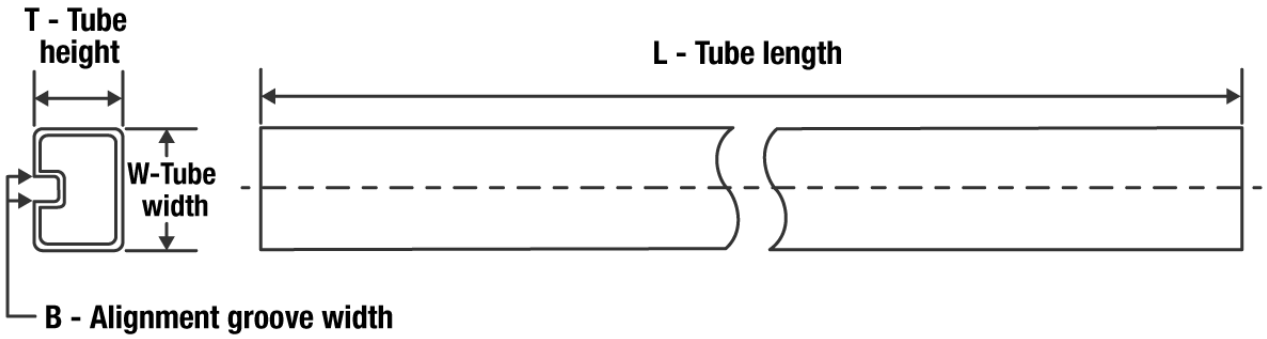
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74CBTLV16211DLR | SSOP | DL | 56 | 1000 | 367.0 | 367.0 | 55.0 |
| SN74CBTLV16211GR | TSSOP | DGG | 56 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74CBTLV16211VR | TVSOP | DGV | 56 | 2000 | 367.0 | 367.0 | 45.0 |

## TUBE

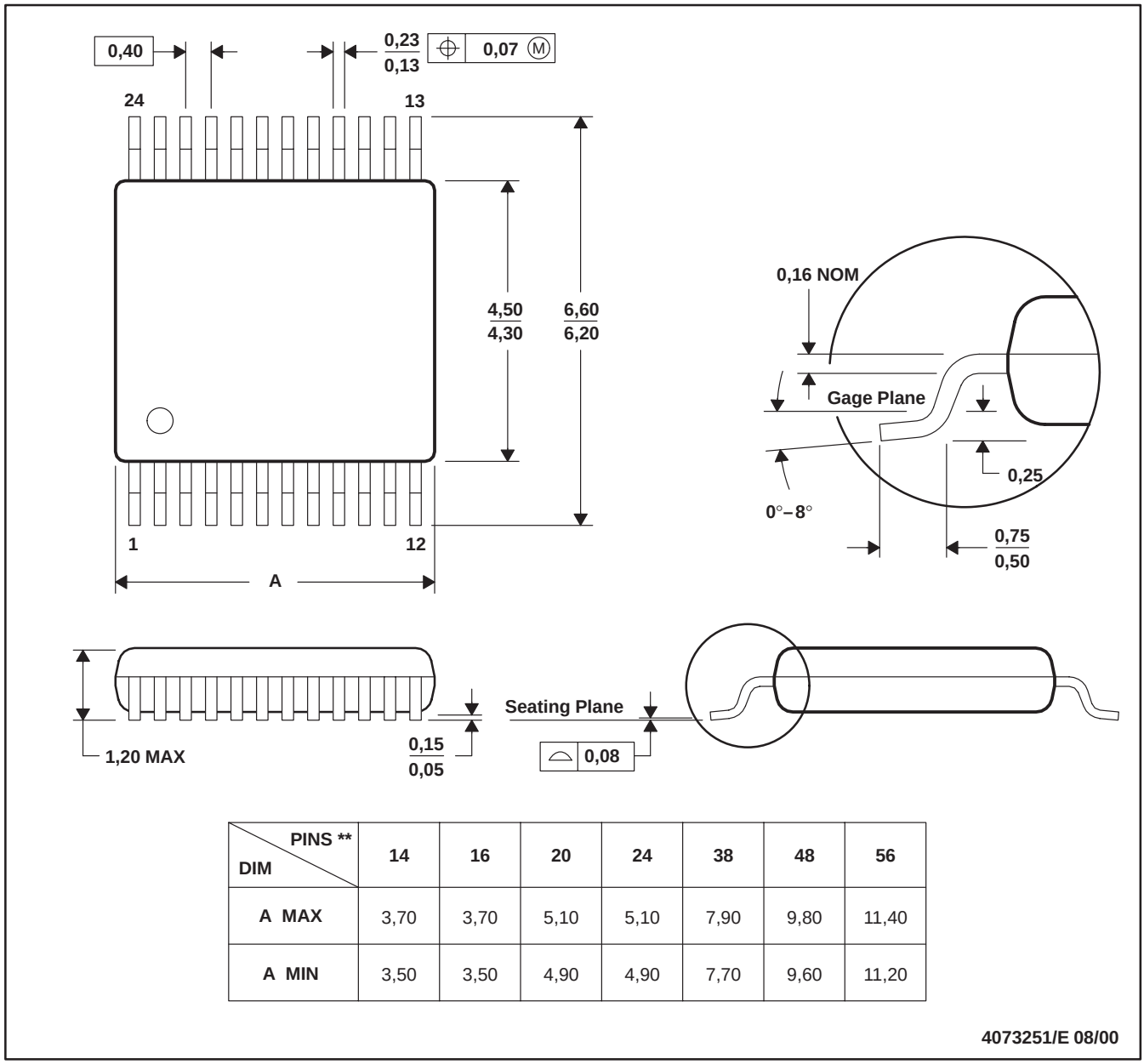



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74CBTLV16211DL | DL | SSOP | 56 | 20 | 473.7 | 14.24 | 5110 | 7.87 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

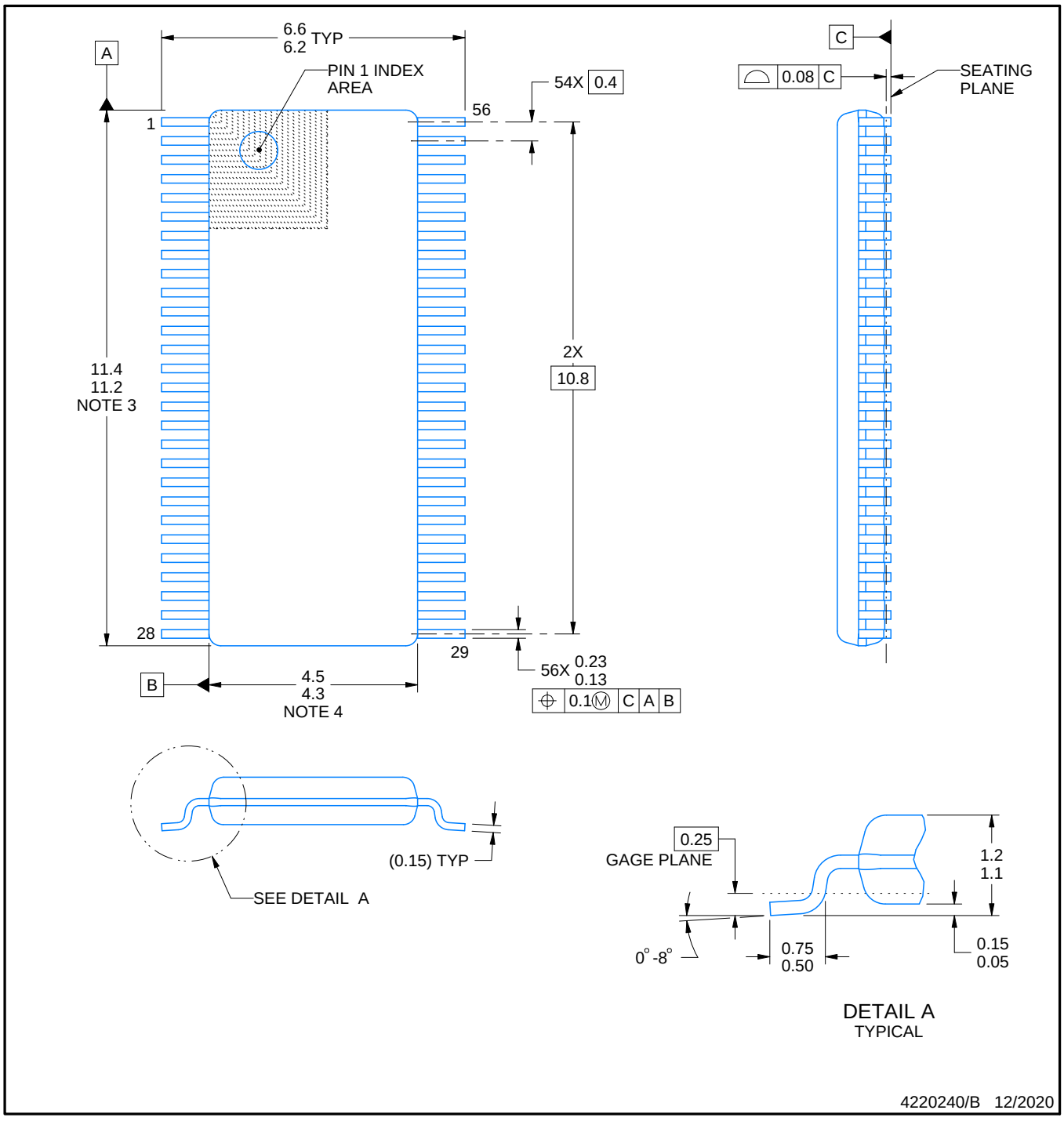
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# PACKAGE OUTLINE

## DGV0056A

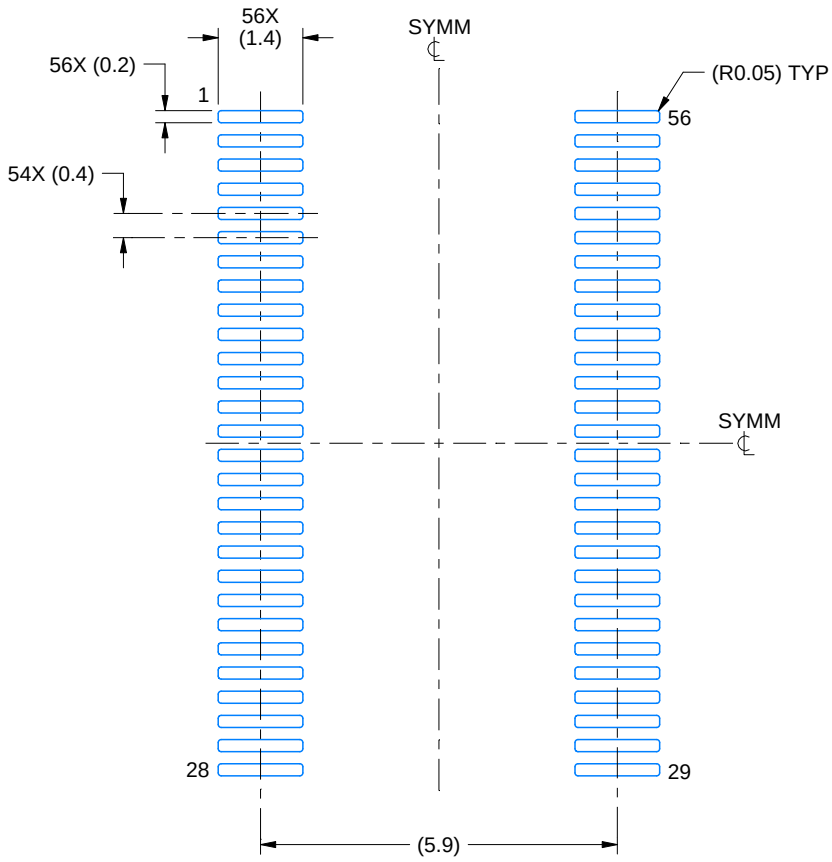
## TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

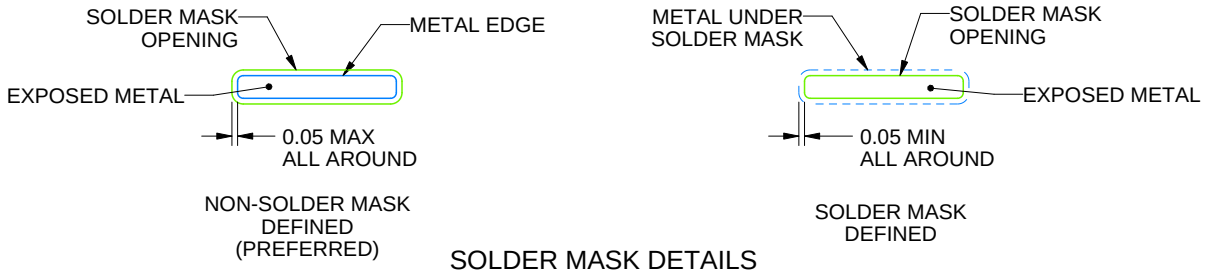



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

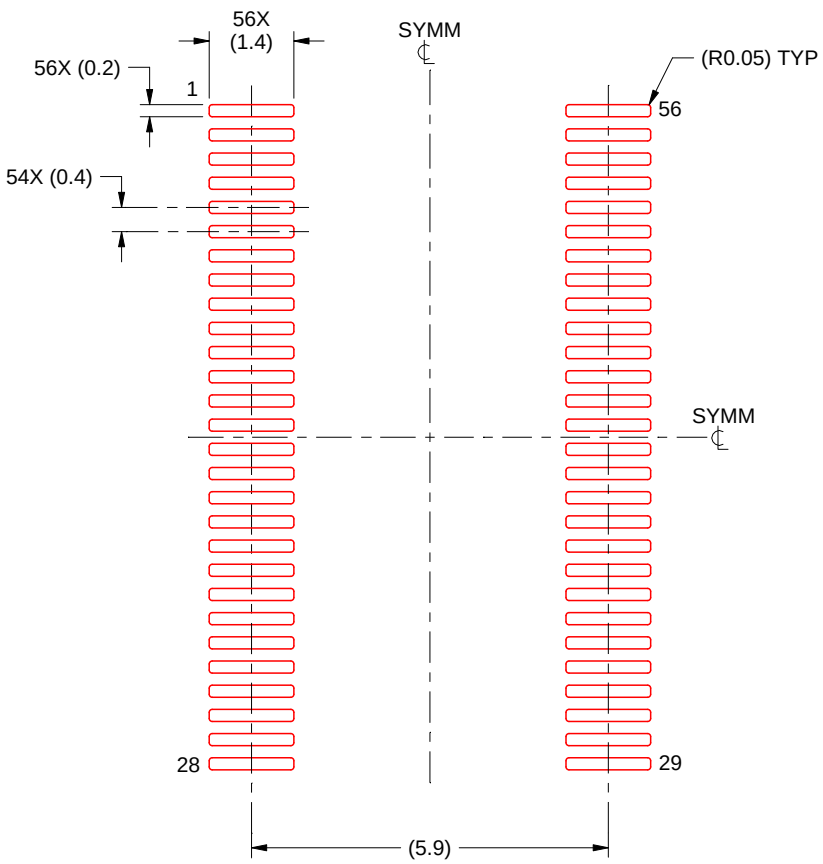



SOLDER MASK DETAILS

4220240/B 12/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



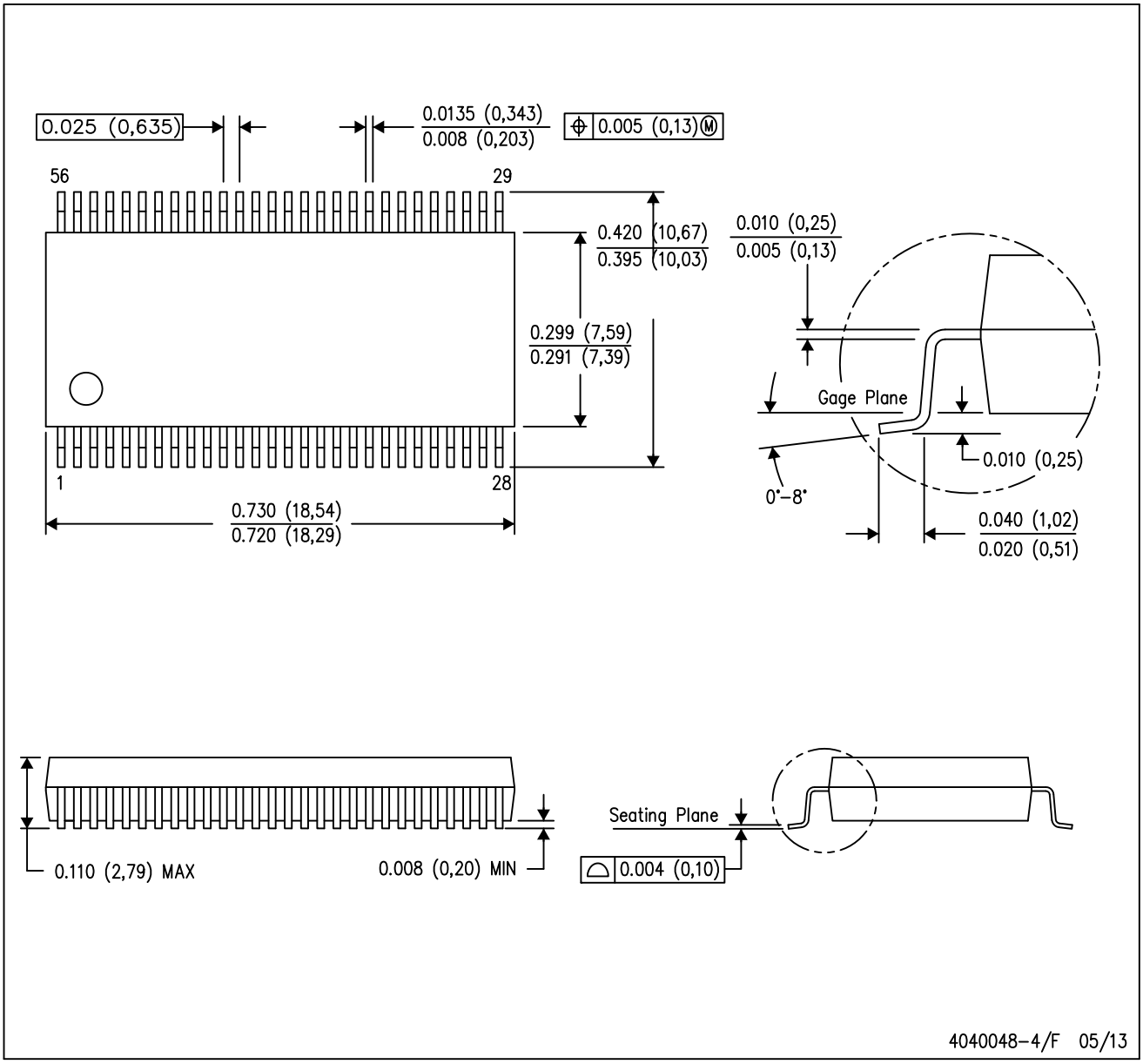

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4220240/B 12/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

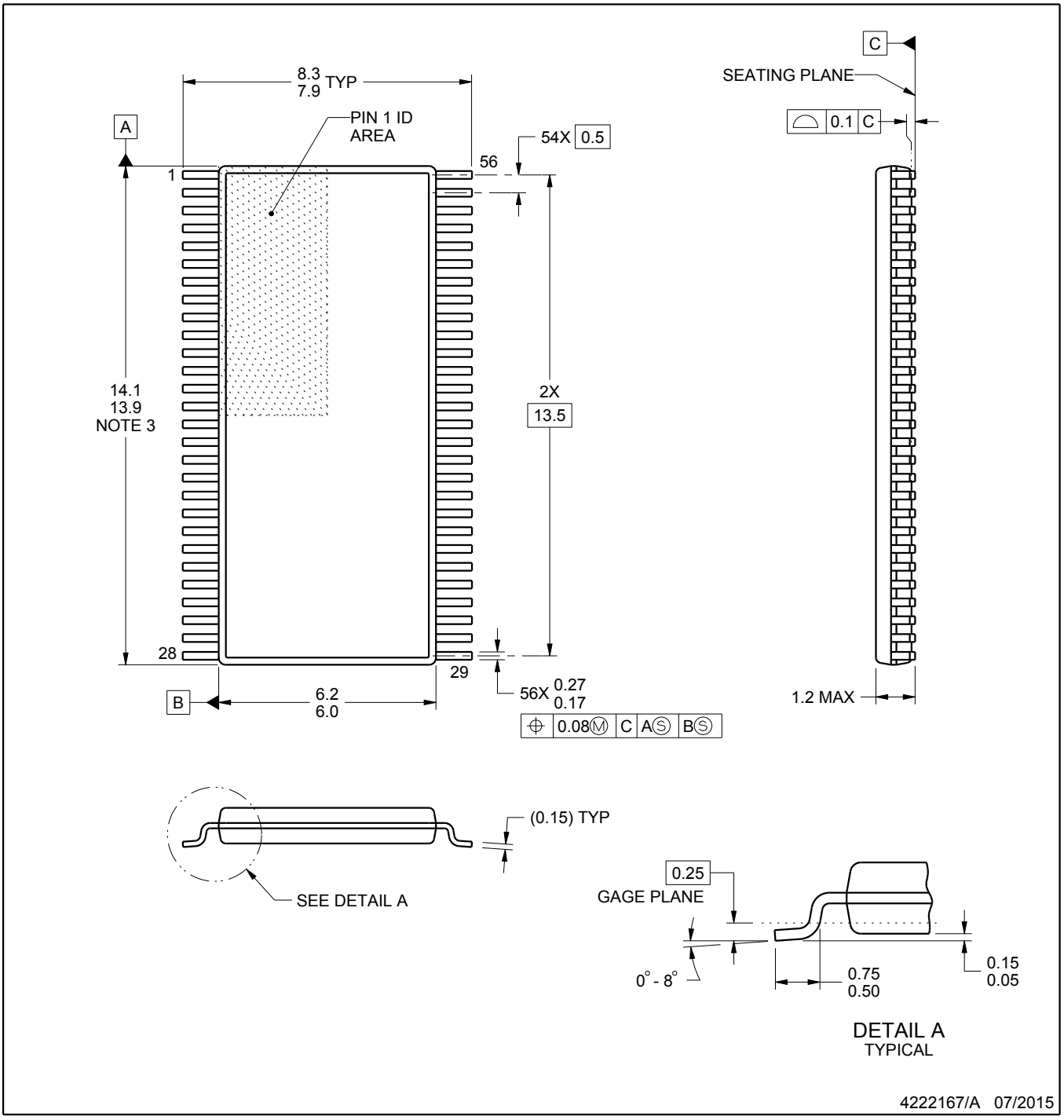
PowerPAD is a trademark of Texas Instruments.

# PACKAGE OUTLINE

## DGG0056A

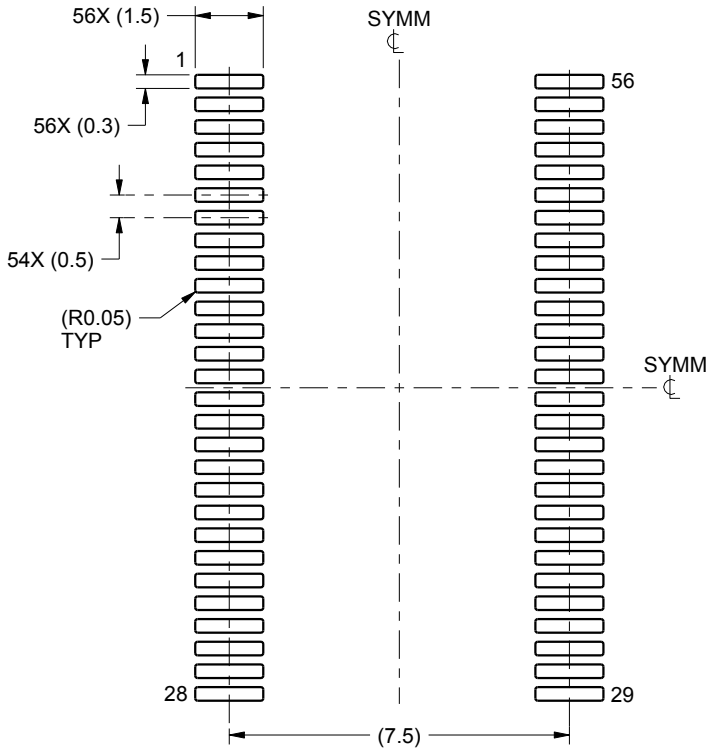
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

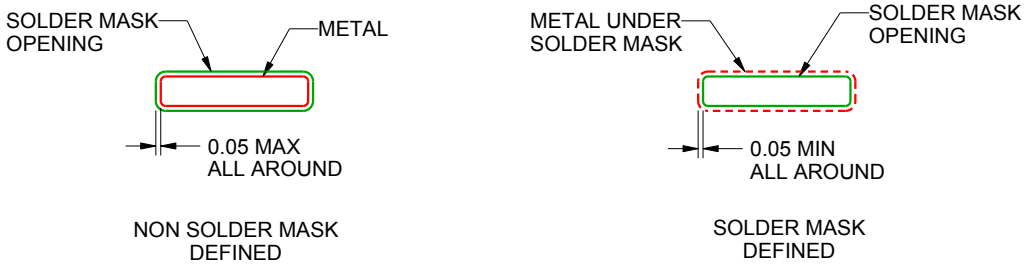



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
SCALE:6X




SOLDER MASK DETAILS

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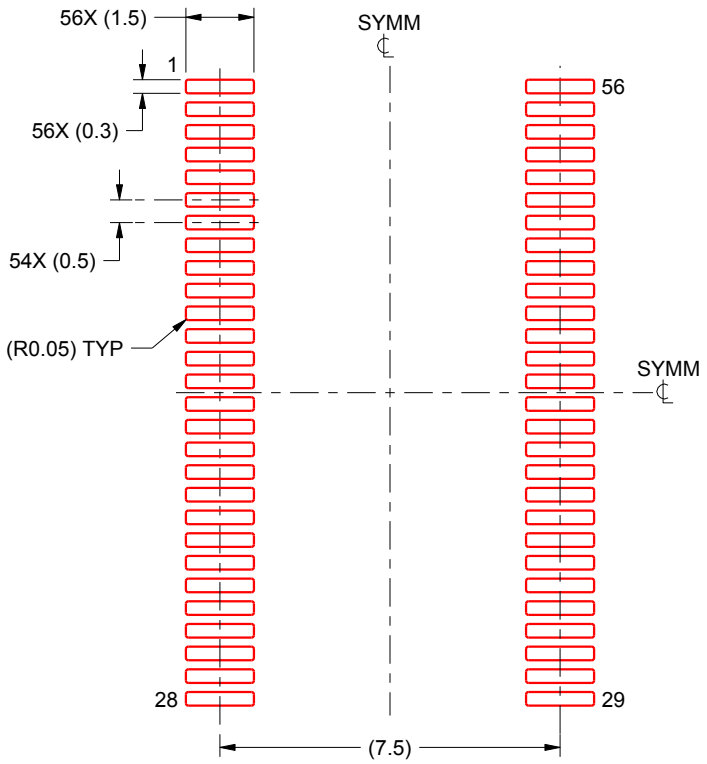
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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