PRODUCT DISCONTINUANCE NOTIFICATION

EOL-000120

Date: March 31, 2016 P1/3

☐ Semtech Corporation, 200 Flynn Road, Camarillo CA 93012
☒ Semtech Canada Corporation, 4281 Harvester Road, Burlington, Ontario L7L 5M4 Canada
☐ Semtech Irvine, 5141 California Ave., Suite 100, Irvine CA 92617
☐ Semtech Neuchatel Sarl, Route des Gouttes d'Or 40, CH-2000 Neuchatel Switzerland
☐ Nanotech Semiconductor, Semtech Corporation, 2 West Point Court, Bristol, United Kingdom, BS32 4PY
☐ Semtech Corpus Christi SA de CV, Carretera Matamorros Edificio 7, Reynosa, Tamaulipas, Mexico 88780
☐

Product Discontinuance Details

Purpose, Description and Effect of Change:

This notification is to inform your company that Semtech is discontinuing the manufacture of the product listed below. In accordance with Semtech's product discontinuation policy, we are hereby giving notice of these product changes in order for your company to make any final lifetime purchases of the discontinued product that are still in supply.

Part Number(s) Affected:	**Customer Part Number(s) Affected:** ☒ N/A
GN1113-INE3 and GN1114-INE3	

Replacement or Alternate Part Number(s) ☐N/A or Not Offered

For existing designs: N/A

New Designs:
GN2040-INE3, GN2042-INE3, GN2044-INE3, GN2044-INTE3D, GN2044SINE3 and GN2044SINTE3D.

Last Time Buy (LTB) Date	**Oct 1, 2016**	**Must Accept Final Delivery by**	**April 1, 2017**
Sample Availability of Alt. Part	Now	**Qualification Report Availability of Alt. Part**	Now

Supporting Documents for Alternate or Replacement parts/Attachments:

Datasheets for GN2040-INE3, GN2042-INE3, GN2044-INE3 and GN2044SINE3.

Last Time Buy Conditions

We request you carefully review this information and notify your purchasing offices and buyers to place your company's final purchases for available discontinued products as soon as possible according to the following last time buy terms and conditions.

1. **Availability:** The ***Last Time Buy Date*** and ***Date to Accept Final Delivery*** are noted above. All orders must have a ***requested ship date before the Date to Accept Final Delivery*** or the order will be rejected. ***The Last Time Buy Date automatically expires when the final available inventory quantity has been scheduled and sold.***

2. **Pricing:** The product unit price will be subject to Semtech's individual price quotation of your company's last time buy requirements.

3. **Order Acceptance/Change Conditions:**
   A. Semtech will accept last time orders from your company for the discontinued products as "Firm and Final". As such, these orders will not be subject to any reschedule, cancellation, or termination by your company without Semtech's prior written authorization and payment of full termination charges.
   B. Semtech reserves its right to make changes in the scheduled delivery dates, or to terminate remaining undelivered quantities of your company's last time buy order, due to changes in Semtech's last time manufacturing capabilities, or for commercially impracticable circumstances which makes delivery not feasible.

4. **Quantities:** The following applies to final buy quantities for the available discontinued product:
   A. **First:** The quantities in any existing unfilled orders and contracts acknowledged by Semtech will be honored, then
   B. **Next:** The unfilled quantities in any volume agreement(s) or quantities in unexpired standalone quote(s) will be accepted, and
   C. **Finally:** Any additional reasonable quantity of product that Semtech quotes based upon your company's identified requirements will be taken.

IN THE EVENT OF CONFLICT FOR THE LIMITED AVAILABILITY PRODUCT, QUANTITIES FOR CUSTOMER'S OR DISTRIBUTOR'S ORDERS WILL BE DETERMINED ON A FIRST-COME FIRST-SERVE BASIS; AND WILL BE SUBJECT TO SEMTECH'S AVAILABLE INVENTORY AND REMAINING MANUFACTURING CAPACITY FOR THE PRODUCT.

Limited Warranty

All discontinued product orders subject to this notice shall carry Semtech's standard limited warranty; or, if applicable, the warranty set forth in a duly executed formal contract between Semtech and your company will apply; except that:

1. Semtech will accept all valid warranty claims for credit only, unless a replacement order is otherwise agreed upon by Semtech and the replacement parts can be manufactured or delivered from remaining inventory.
2. The applicable warranty period for making any return claims for discontinued products will be no later than ninety (90) days following delivery of the discontinued products.
3. Any return claims must be made under Semtech's current Return Material Authorization "RMA" procedures.

Additional Provisions

SEMTECH ACCEPTS NO LIABILITY FOR EXCESS REPROCUREMENT COSTS OR FOR ANY SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES WHATSOEVER ASSOCIATED WITH THIS NOTICE, WITH ITS PRODUCTS, OR WITH THE FINAL MANUFACTURE AND PERFORMANCE AGAINST ANY LAST TIME BUY ORDERS RELATED TO THE DISCONTINUED PRODUCTS COVERED BY THIS NOTICE.

We regret the inconvenience and impact this notice may cause your company. Semtech's sales, marketing, and

distribution personnel stand ready to assist you in placing your company's final orders, or in providing the product information you require.

For product inquiries or purchase order information, please contact your local Semtech sales representative.

Issuing Authority		
Semtech Business Unit:	SIP	
Semtech Contact Info:	Luis Blanco Semtech Corporation Senior Director, Quality Engineering 4281 Harvester Road Burlington, ON L7L 5M4 lblanco@semtech.com Office: (905) 632-7253 Fax: (905) 632-2055	

FOR FURTHER INFORMATION & WORLDWIDE SALES COVERAGE: http://www.semtech.com/contact/index.html#support

Features

- Dual CDR with 9.8Gb/s to 11.3Gb/s reference-free operation and integrated trace drivers
- Integrated limiting amplifier with typical sensitivity of 2.5mV
- Digital control through I^2C or SPI interface
- Programmable Jitter Transfer bandwidth
- Bi-directional loopback
- Low power to enable SFP+ SONET modules:
  - GN2040 power = 245mW
- Integrated Jitter Filter to ensure robust jitter generation performance and compliance to the OC192 standards
- Highly-configurable, including the following programmable features:
  - Limiting Amplifier Equalization
  - Transmit Input Equalization
  - Input Slice Level Adjust
  - LOS with adjustable threshold and hysteresis
  - Polarity invert and mute in both directions
  - Output de-emphasis
- Integrated analog to digital converter, which provides access to digital diagnostic information on supply voltage and die temperature
- 1.8V power supply
- Programmable divide by 16 or 64 clock output from either transmit or receive recovered clocks
- 5x5 32-pin QFN package
- -40°C to 100°C case operation

Applications

- XFP & SFP+ 10Gb/s SONET optical transceivers
- XFP & SFP+ 10G Ethernet optical transceivers
- XFP DWDM optical transceivers
- SFP+ line card repeater
- 40GbE CFP modules

General Description

The GN2040 is an integrated bi-directional CDR and limiting amplifier for XFP SONET and 10GBase-LR Ethernet applications. It can also be used as a low-power SFP+ line card repeater for limiting links. In addition to reducing power versus the GN2010-family, the GN2040 offers a selectable jitter filter to ensure compliance to jitter generation specifications. Based on the Semtech ClearEdge™ technology, the GN2040 delivers best in class eye quality.

In addition to enabling lower power modules, the GN2040 offers a selectable jitter filter to ensure compliance to difficult to meet jitter generation specifications.

The transmit path consists of optional input equalization, a Tx CDR, and a de-emphasis driver. The receive path is comprised of a limiting amplifier with programmable equalization, an Rx CDR and output de-emphasis. Both transmit and receive directions offer the option for polarity invert, loopback, output mute, and programmable output equalization. The GN2040 consumes only 245mW from a 1.7V supply.

The GN2040 is a highly-programmable device, with features supporting DWDM applications. These include a programmable slice level adjust and programmable limiting amplifier peaking.

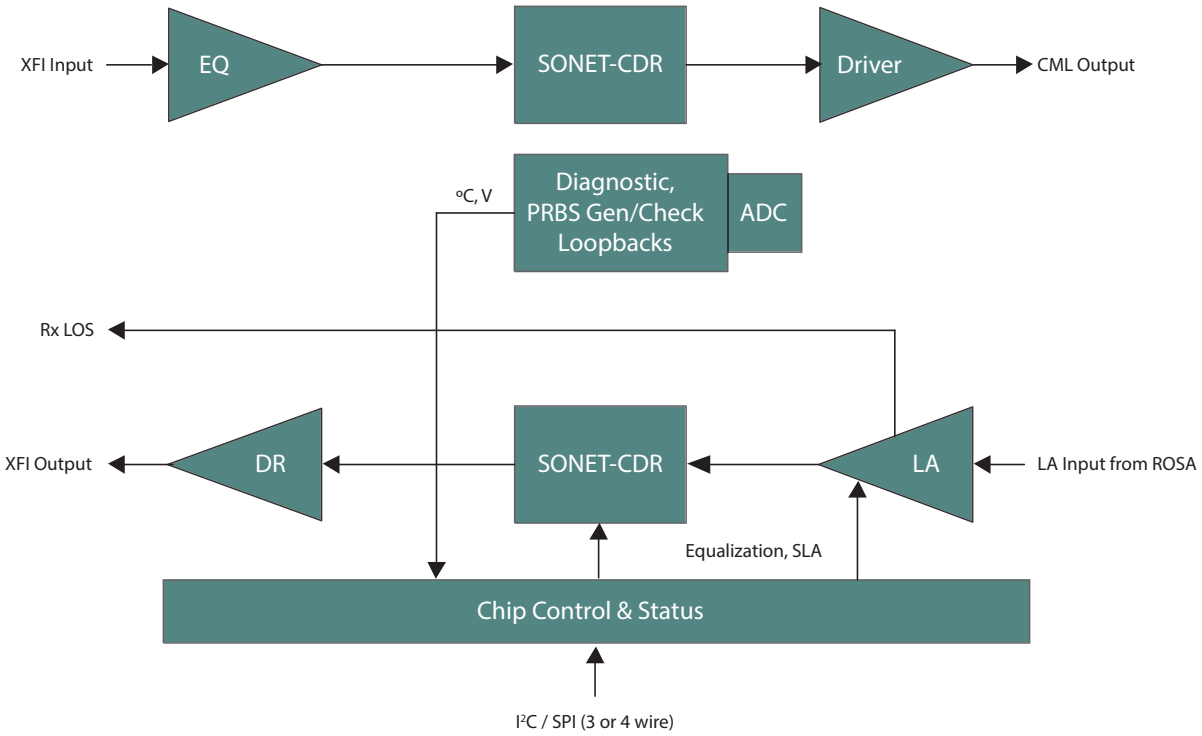


Figure A: GN2040 Functional Block Diagram

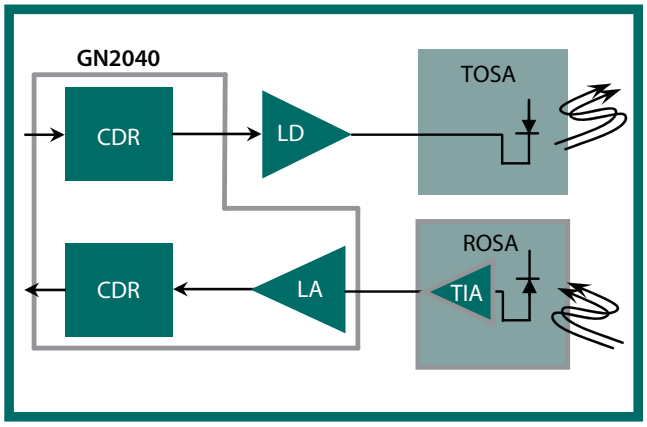


Figure B: Typical Usage - XFP Optical Module

Revision History

Version	ECO	Date	Changes and / or Modifications
4	025762	August 2015	Minor updates.
3	025197	April 2015	Updated Data Rate parameter in Table 2-5: AC Electrical Characteristics.
2	024792	March 2015	Updated Figure 7-1: Package Dimensions and Section 4.8.3.
1	022965	November 2014	Correction to Table 2-2: DC Electrical Characteristics and Table 2-5: AC Electrical Characteristics.
0	021847	November 2014	Updated Loop Bandwidth values in Table 4-1 and Table 4-3.
B	015653	June 2014	Updates: Added content to Detailed Description and Register Descriptions. Reformatted document with new corporate template.
A	158538	October 2012	New document.

Contents

1. Pin Out

1.1 Pin Assignment

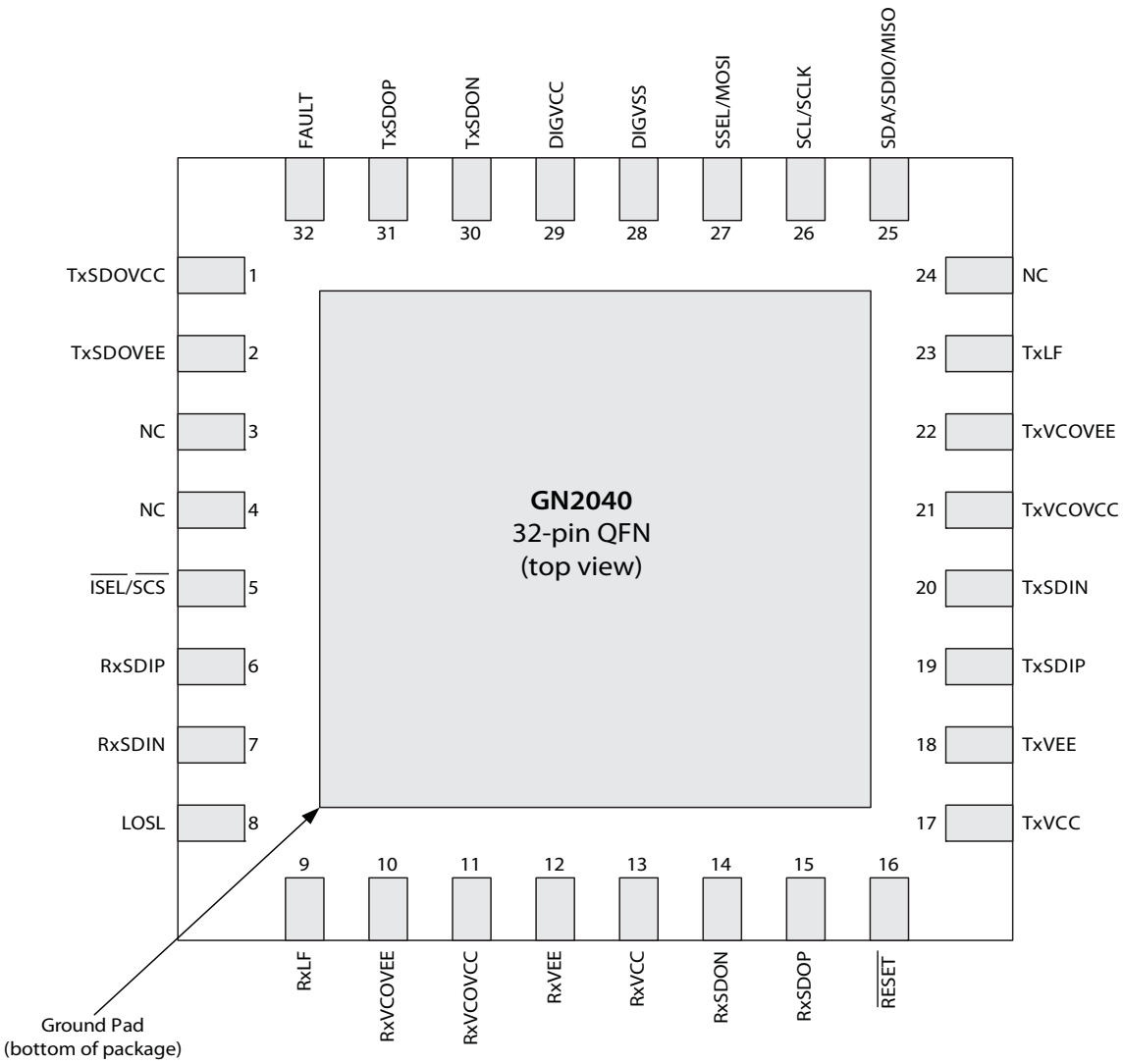


Figure 1-1: Pin Assignment

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin #	Name	Type	Description
1	TxSDOVCC	Power	Power supply for transmit signal path output.
2	TxSDOVEE	Ground	Ground for transmit signal path output.
3, 4	NC	—	No connect (unused).
5	$\overline{\text{ISEL}}$/$\overline{\text{SCS}}$	Digital Input	Digital active-low LVTTL/LVCMOS-compliant input. $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ selects the host interface mode during a device reset. When LOW or left unconnected, this pin selects I^2C host interface mode. When HIGH, this pin selects SPI host interface mode on device power-on or reset. $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ is an SPI-compliant active-LOW chip-select pin in SPI host interface mode. $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ is not used in I^2C host interface mode.
6, 7	RxSDIP, RxSDIN	Input	High-speed input for the receive signal path.
8	LOSL	Digital Output	XFP/SFP+ compliant, active-high. Open-collector Loss-Of-Signal indicator requires an external pull-up resistor. When LOSL is LOW, the transmit and receive signal paths are operating properly. When LOSL is high-impedance, the device has detected a condition that indicates invalid data in the transmit and/or receive signal paths. It consists of a logical OR of the following signals: • Receive signal path CDR Loss of Signal (included by default) • Receive signal path CDR Loss of Lock (masked by default) • Transmit signal path CDR Loss of Signal (masked by default) • Transmit signal path CDR Loss of Lock (masked by default) Loss-of-signal/loss-of-lock inputs from either signal path can be masked or enabled.
9	RxLF	Passive	Loop filter capacitor connection for receive signal path.
10	RxVCOVEE	Ground	Ground for receive signal path VCO.
11	RxVCOVCC	Passive	1.8V power supply for receive signal path VCO.
12	RxVEE	Ground	Ground for receive signal path and output.
13	RxVCC	Power	Power supply for receive signal path and output.
14, 15	RxSDON, RxSDOP	Output	High-speed differential output for receive signal path.
16	$\overline{\text{RESET}}$	Digital Input	Digital active-low 1.8V CMOS-compliant input. Device reset control pin. This is an active pull-down. It is recommended that $\overline{\text{RESET}}$ be pulled down by an external 10kΩ resistor and be driven by the Micro on the module.
17	TxVCC	Power	Power supply for transmit signal path.
18	TxVEE	Ground	Ground for transmit signal path.
19, 20	TxSDIP, TxSDIN	Input	High-speed input for the transmit signal path.

Table 1-1: Pin Descriptions

Pin #	Name	Type	Description
21	TxVCOVCC	Passive	1.8V power supply for transmit signal path VCO.
22	TxVCOVEE	Ground	Ground for transmit signal path VCO.
23	TxLF	Passive	Loop filter capacitor connection for transmit signal path.
24	NC	No Connect	Unused.
25	SDA/SDIO/MISO	Digital Input/ Output	Digital active-high serial data signal for the host interface. Schmitt triggered in input mode. Bi-directional, I^2C-compliant, open-drain driver/receiver in I^2C host-interface mode. Bi-directional, 1.8V CMOS-compliant driver/receiver in 3-wire SPI host-interface mode. 1.8V CMOS-compliant active-high output driver in 4-wire SPI host-interface mode.
26	SCL/SCLK	Digital Input	Digital active-high clock input signal for the serial host interface. Schmitt triggered in input mode. Bi-directional, I^2C-compliant, open-drain driver/receiver in I^2C host-interface mode (SCL). 1.8V CMOS-compliant input in either SPI host-interface mode (SCLK).
27	SSEL/MOSI	Digital Input	Digital active-high 1.8V CMOS-compliant input. SSEL selects the SPI port style when SPI host interface mode is selected: When LOW or left unconnected during device reset, this pin selects 3-wire SPI host interface mode. When HIGH during device reset, this pin selects 4-wire SPI host interface mode on device power on or reset. Following device reset, SSEL MOSI is an active-high SPI-compliant receiver. SSEL/MOSI is not used in I^2C host interface mode.
28	DIGVSS	Ground	Ground for low-speed digital I/O and internal logic.
29	DIGVCC	Power	Power supply (1.8V) for low-speed digital I/O.
30, 31	TxSDON, TxSDOP	Output	High-speed differential output for transmit signal path.
32	FAULT	Digital Output	XFP/SFP+-compliant active-high digital output. Open-collector Fault indicator. Requires an external pull-up resistor. When FAULT is LOW, the transmit and receive signal paths are operating properly. When FAULT is high-impedance, the device has detected a condition that indicates invalid data in the transmit and/or receive signal paths. It consists of a logical OR of the following signals: • Transmit signal path CDR Loss of Lock • Transmit signal path CDR Loss of Signal • Receive signal path CDR Loss of Lock • Receive signal path CDR Loss of Signal

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
1.8V Supply Voltage	-0.5 to +2.1V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_A < 125°C
Input Voltage Range (any input pin)	-0.3 to (V_{CC} + 0.3)V_{DC}
Solder Reflow Temperature (for 3 seconds)	260°C

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

$V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to 100°C. Typical values are V_{CC} = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 10.3Gb/s. PRBS31 data. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Power	Output swing 400mV_{ppd}. Jitter filter mode off.		—	245	311	mW	1
Control Logic Input Specifications							
Input Low Voltage		V_{IL}	0	—	0.8	V	—
Input High Voltage		V_{IH}	2.0	—	V_{CC}	V	—
Input Low Current	V_{IL} = 0V	I_{IL}	—	-100	—	µA	—
Input High Current	V_{IH} = 3.3V, V_{CC} = 1.8V	I_{IH}	—	100	—	µA	—
Schmitt Trigger Thresholds							
DC Low-to-High Threshold	V_{CC} = 1.9V		0.93	1.05	1.16	V	2
DC High-to-Low Threshold			0.51	0.70	0.85	V	2
DC Low-to-High Threshold	V_{CC} = 1.8V		0.88	0.99	1.13	V	3
DC High-to-Low Threshold			0.41	0.67	0.77	V	3

Table 2-2: DC Electrical Characteristics (Continued)

$V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to 100°C. Typical values are V_{CC} = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 10.3Gb/s. PRBS31 data. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
DC Low-to-High Threshold	V_{CC} = 1.7V		0.83	0.94	1.07	V	—
DC High-to-Low Threshold			0.36	0.59	0.73	V	—
AC Low-to-High Threshold	$V_{CC\_1.8}$ = 1.7V		0.76	0.91	1.06	V	4
AC High-to-Low Threshold			0.44	0.57	0.69	V	4
AC Low-to-High Threshold	$V_{CC\_1.8}$ = 1.9V		0.93	1.06	1.19	V	5
AC High-to-Low Threshold			0.70	0.82	0.93	V	5
Status Indicator Output Specifications							
Indicator Output Logic LOW	I_{SINK}(max) = 3mA	V_{OL}	—	0.2	0.4	V	—
Rx Side Specification							
Input Termination (RxSDIP/N)	Differential		80	100	120	Ω	—
Output Termination (RxSDOP/N)	Differential		80	100	120	Ω	—
Tx Side Specification							
Input Termination (TxSDIP/N)	Differential		80	100	120	Ω	—
Output Termination (TxSDOP/N)	Differential		80	100	120	Ω	—

Notes:

1. Typical power is specified at 1.7V.
2. Typical Noise Immunity = 0.34V (see Section 4.9.3).
3. Typical Noise Immunity = 0.43V (see Section 4.9.3).
4. Typical Noise Immunity = 0.72V (see Section 4.9.3).
5. Typical Noise Immunity = 0.76V (see Section 4.9.3).

2.2.1 Power Dissipation

Table 2-3: Power Dissipation

$V_{CC\_1.8}$	Total Current	Total Power
V	mA	mW
1.6	142	227
1.7	144	245
1.8	147	265
1.89	150	284

2.2.2 Power Features

Table 2-4: Power Features

Feature	Description	Typical Baseline Power (mW)	Typical Delta Power (mW)
Base Power		**245**	
Incremental Power Features			
LA Boost at Maximum			0.0
Slice Adjust at Maximum			12.6
PRBS7 Generator	Path for PRBS7 Generator to RxSDO is on		39.7
PRBS7 Checker	PRBS7 Checker is on		55.7
Diag + ADC	Temperature, Supply Sensor, ADC		5.3
Tx Jitter Filter Mode Enabled at Maximum			9.5
High Performance SONET IJT	RX_PLL_SONET_IJT_SETTING set to maximum		7.0
RxSDO and TxSDO De-emphasis at Maximum Setting			53.5
Power Saving Features			
with Rx CDR Bypassed and Powered-down	CDR bypassed AND powered-down		-58.8
with Tx CDR Bypassed and Powered-down	CDR bypassed AND powered-down		-61.7
with Rx path Powered-down			-100.0
RxSDO Muted			-19.7
TxSDO Muted			-19.0
IJT Mode = 1			-18.5
IJT Mode = 2			-15.0

2.3 AC Electrical Characteristics

Table 2-5: AC Electrical Characteristics

$V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to 100°C. Typical values are V_{CC} = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 10.3Gb/s. PRBS31 data. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Data Rate	Default configuration, $V_{CC\_1.8V} \geq 1.71V$		9.8	10.3125	11.35	Gb/s	—
	Default configuration, $V_{CC\_1.8V} < 1.71V$		9.8	10.3125	11.3	Gb/s	—
Rx Side Specification							
Input Sensitivity			—	2.5	8	mV_{ppd}	—
Input Overload			1200	—	—	mV_{ppd}	—
Limiting Amplifier Equalization Range	Maximum EQ setting		14	—	—	dB	1
Input Sinusoidal Jitter Tolerance	f = 100kHz		20	30	—	UI_{pp}	2, 7
	f = 400kHz		2.5	8	—	UI_{pp}	7
	f = 4MHz		0.5	1.4	—	UI_{pp}	7
	f = 80MHz		0.3	0.5	—	UI_{pp}	7
Jitter Transfer Bandwidth Setting Range	Minimum programmable setting		—	2.2	—	MHz	—
	Maximum programmable setting		—	13	—	MHz	—
Jitter Peaking	With 6MHz LBW, loop filter cap = 220nF		—	—	0.03	dB	—
RxSDO Output Total Jitter	PRBS31 data, BER = 10^{-12}, 11.3Gb/s With optimized boost and swing settings	TJ	—	0.08	0.16	UI_{pp}	—
RxSDO Output Deterministic Jitter	PRBS31 data, BER = 10^{-12}, 11.3Gb/s	DJ	—	0.05	0.088	UI_{pp}	—
RxSDO Output Rise/Fall Time	20% to 80%	t_r, t_f	24	—	—	ps	8
RxSDO Output AC Common Mode Voltage	With XFP connector		—	—	15	mV_{rms}	—

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to 100°C. Typical values are V_{CC} = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 10.3Gb/s. PRBS31 data. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
RxLOS De-assert Threshold Level Setting Range	Minimum programmable setting		—	5	—	mV_{ppd}	—
	Maximum programmable setting		—	400	—	mV_{ppd}	—
RxLOS Threshold Level Variation	1 sigma, IC to IC, RXLOSRANGE = 0,1		—	1.0	—	dB	—
	1 sigma, IC to IC, RXLOSRANGE = 2		—	2.0	—	dB	—
	Over V_{CC} Range		—	1.0	—	dB	—
	Over temperature range -40°C to +100°C, threshold level > $20mV_{ppd}$		—	1.5	—	dB	—
RxLOS Threshold Level Hysteresis Setting Range	Electrical		0	—	6	dB	—
RxLOS Response Time			3	5	20	µs	—
Slice Level Adjust Range	Maximum setting		200	—	—	mV	—
Rx CDR Lock Time	Default mode: loop filter cap = TBDnF, minimum LBW = 1.1MHz, SIJT Mode 2, 3		—	—	1	ms	—
Differential Output Voltage Setting Range	Minimum swing setting		90	120	130	mV_{ppd}	—
	Maximum swing setting		630	800	910	mV_{ppd}	—
Output De-emphasis Setting Range	Maximum de-emphasis setting. Output swing = $350mV_{ppd}$		6	—	—	dB	—
RxSDI Differential Return Loss	<5GHz		—	-14	—	dB	—
	5GHz to 10GHz		—	-10	—	dB	—
RxSDO Differential Return Loss	<5GHz		—	-16	—	dB	—
	5GHz to 10GHz		—	-8	—	dB	—

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to 100°C. Typical values are V_{CC} = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 10.3Gb/s. PRBS31 data. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Tx Side Specification							
Input Sensitivity			—	15	30	mV_{ppd}	—
Input Overload			1200	—	—	mV_{ppd}	—
LOS Threshold Level Setting Range	Minimum programmable setting		—	20	—	mV_{ppd}	—
	Maximum programmable setting		—	100	—	mV_{ppd}	—
Equalization Gain	Maximum programmable setting		—	6	—	dB	4
Input Sinusoidal Jitter Tolerance – jitter filter mode off	f = 120kHz, maximum LBW		7	10	—	UI_{pp}	5, 6
	f = 4MHz		0.4	0.6	—	UI_{pp}	6
	f = 80MHz		0.35	0.5	—	UI_{pp}	6
Input Sinusoidal Jitter Tolerance – jitter filter mode on	f = 120kHz, maximum LBW		10	16	—	UI_{pp}	5, 6
	f = 4MHz		0.4	0.6	—	UI_{pp}	6
	f = 80MHz		0.35	0.5	—	UI_{pp}	6
Jitter Transfer Bandwidth Setting Range	Minimum programmable setting		—	1.5	—	MHz	—
	Maximum programmable setting		—	10.3	—	MHz	—
Jitter Peaking	With 6MHz LBW, loop filter capacitor = 220nF		—	—	0.03	dB	—
Jitter Generation	50kHz to 80MHz		—	34	—	mUI_{pp}	—
	4MHz to 80MHz		—	22	—	mUI_{pp}	—
Total Output Jitter	PRBS31 data, BER = 10^{-12}, 11.3Gb/s	TJ	—	0.08	0.16	UI_{pp}	—
TxSDO Output Rise/Fall time	20% to 80%	t_r, t_f	24	—	—	ps	8

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to 100°C. Typical values are V_{CC} = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 10.3Gb/s. PRBS31 data. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Tx CDR Lock Time	Default mode: loop filter cap = TBDnF, minimum LBW = 1.1MHz, TXPDSONETIJT = 0 TXPLLSONETIJTSETTING = 3		—	—	1	ms	—
Differential Output Voltage Setting Range	Minimum swing setting		90	120	130	mV_{ppd}	—
	Maximum swing setting		630	800	910	mV_{ppd}	—
Output De-emphasis Setting Range	Maximum de-emphasis setting. Output swing = $350mV_{ppd}$		6	—	—	dB	—
TxSDI Differential Return Loss	<5GHz		—	-15	—	dB	—
	5GHz to 10GHz		—	-13	—	dB	—
TxSDO Differential Return Loss	<5GHz		—	-16	—	dB	—
	5GHz to 10GHz		—	-8	—	dB	—

Notes:

1. At 5.35GHz.
2. At jitter frequencies <100kHz, the GN2040 jitter tolerance performance exceeds the SONET GR-253 Rx Tolerance specifications.
3. The maximum adjust range is +/-200mV.
4. At 5.35GHz (dielectric loss).
5. At jitter frequencies <120kHz, the GN2040 jitter tolerance performance exceeds the XFI module transmitter input telecom sinusoidal jitter tolerance specifications (XFP MSA Revision 4.0, Figure 16).
6. In addition to XFI input jitter tolerance requirements.
7. Loop bandwidth setting of 8MHz, IJT mode 3 and IJT setting 31.
8. Measured on host side of XFP or SFP+ connector.

3. Input/Output Circuits

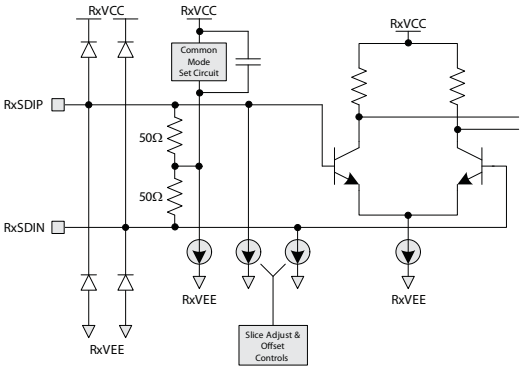


Figure 3-1: RxSDI

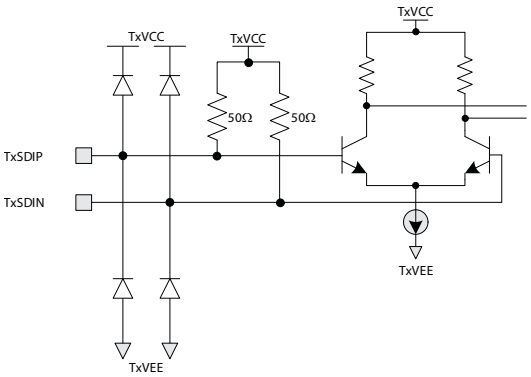


Figure 3-2: TxSDI

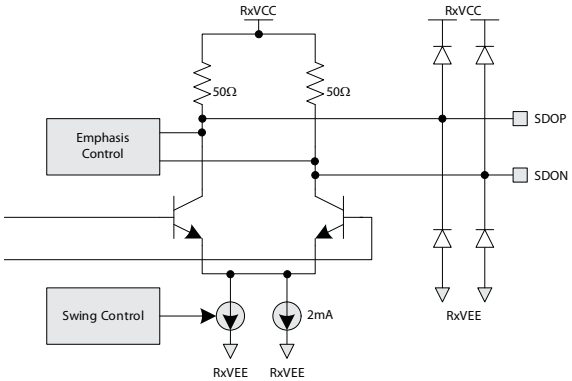


Figure 3-3: RxSDO

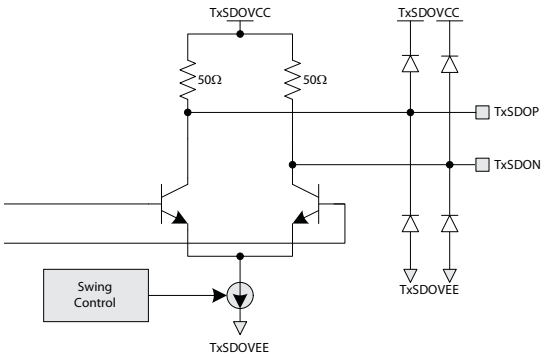
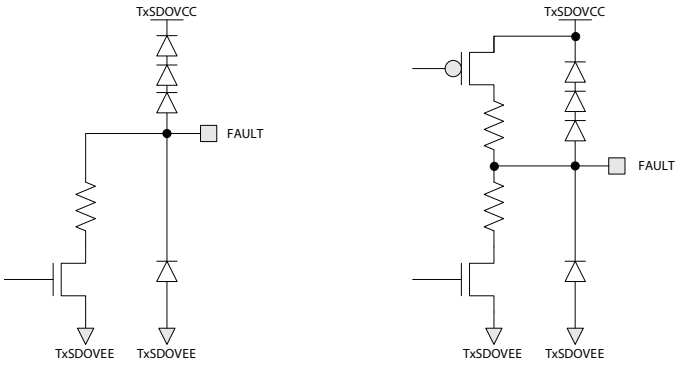
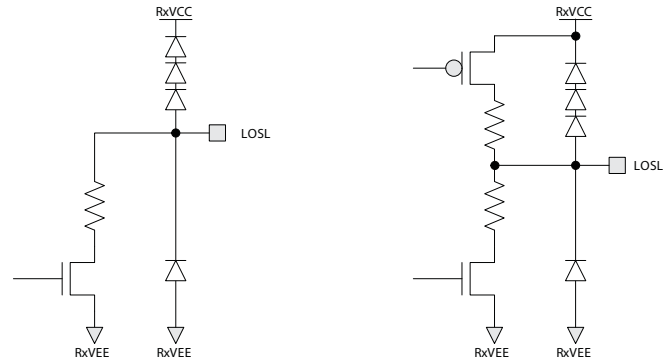


Figure 3-4: TxSDO



Configured as open-drain Configured as LVCMOS

Figure 3-5: FAULT



Configured as open-drain Configured as LVCMOS

Figure 3-6: LOSL

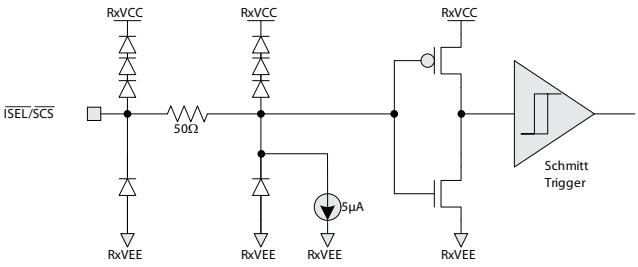


Figure 3-7: $\overline{\text{ISEL}}/\overline{\text{SCS}}$

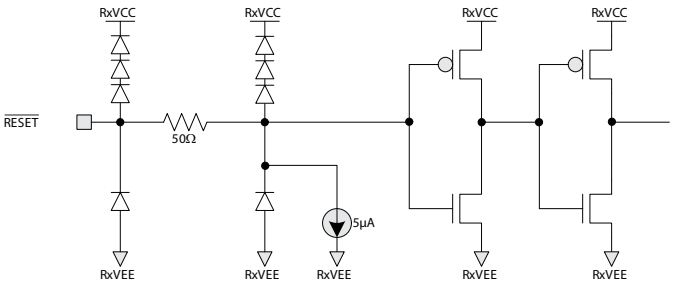


Figure 3-8: $\overline{\text{RESET}}$

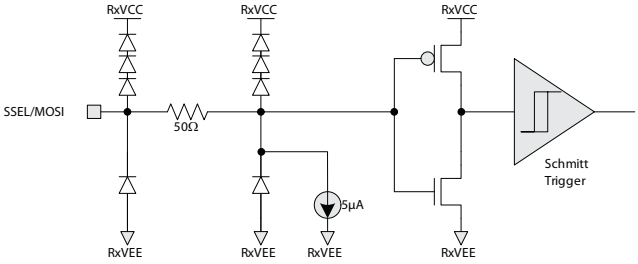


Figure 3-9: SSEL/MOSI

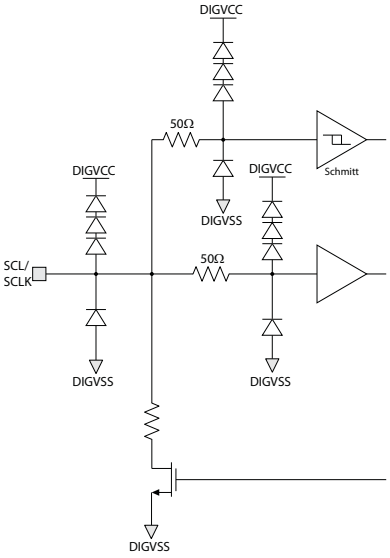


Figure 3-10: SCL/SCLK

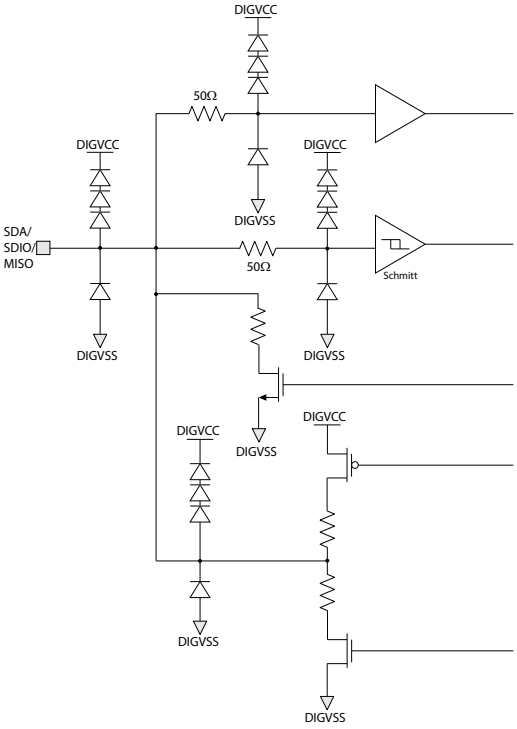


Figure 3-11: SDA/SDIO/MISO

4. Detailed Description

4.1 Multirate CDR Functionality

The GN2040 supports a range of data rates, so that a single part can be used for multiple applications. The GN2040 does not require a reference clock. Some example applications are as follows:

- 10Gb/s Ethernet (10.3Gb/s)
- 10Gb/s Ethernet with FEC (11.1Gb/s)
- 10G Fibre Channel (10.5Gb/s)
- 10G Fibre Channel with FEC (11.3Gb/s)
- SONET OC192 (9.95Gb/s)

4.1.1 Retimer Bypass

The device can be configured to manually bypass each of the Rx and Tx CDRs through the **TX_PLL_BYPASS** and **RX_PLL_BYPASS** controls.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG5	14	TX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Tx CDR into bypass mode.
RXPLL_REG5	24	RX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Rx CDR into bypass mode.

4.2 Receive Path

The GN2040 receive path contains a high-sensitivity limiting amplifier with optional equalization, a multi-rate CDR, and an emphasis driver.

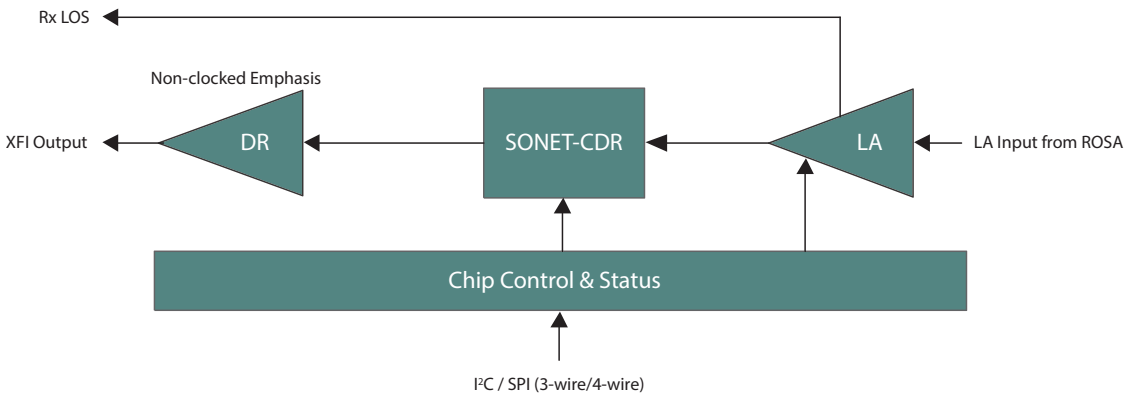


Figure 4-1: Receive Path

4.2.1 Integrated Limiting Amplifier

The GN2040 has an integrated Limiting Amplifier (LA), with better than 10mV sensitivity. Additional features are; slice level adjust and optional equalization on the limiting amplifier input.

4.2.2 Slice Level Adjust

The slicing level of the limiting amplifier can be configured in two modes of operation:

1. Automatic offset correction.
2. Manual slice adjust with a fixed slice level.

By default, the limiting amplifier is configured in automatic offset correction mode, and will slice the incoming signal at the 50% point.

The LA can be configured to allow a user-specified fixed slice level. In this mode, the slice level can be varied by ±200mV from the 50% point in 1mV increments. To enable this mode, **RX_PD_SLICE_ADJ** (shown below) should be set to 0.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPWRDN_REG2	135	RX_PD_SLICE_ADJ	1:1	RW	1	0-1	When HIGH, power-down for LA slice adjust.

To enable the user to adjust the slice level manually, **RX_PD_SLICE_ADJ** must be set to 0 and **RX_MANUAL_SLICE_ADJ_EN** must be set to 1.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG5	52	RXLA_MANUAL_SLICE_ADJ_EN	0:0	RW	0	0-1	When HIGH, enables user to adjust slice level at the Rx input.

The following controls allow the slice adjust polarity and magnitude to be set manually:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG2	49	RXLA_SLICE_ADJ	7:0	RW	00000000	0-255	Slice adjust magnitude control.
RX_REG3	50	RXLA_SLICE_ADJ_POL	0:0	RW	0	0-1	Slice adjust polarity. When HIGH, slice level adjust is positive.

The slice level adjustment can be applied before or after the equalization function (covered in Section 4.2.3). This flexibility allows the device to maintain optimal receive sensitivity performance while optimizing slice adjust. Figure 4-2 shows the two possible insertion points for slice level adjustment:

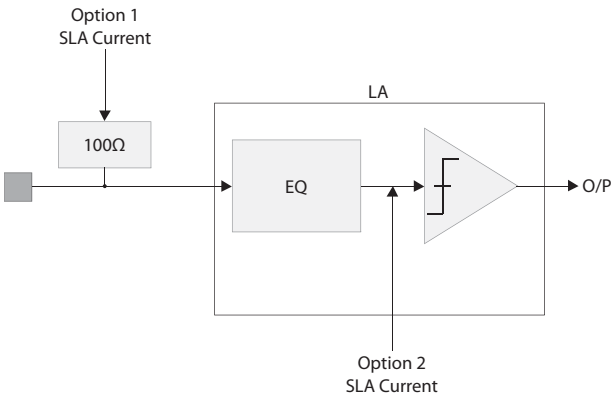


Figure 4-2: Slice Level Adjustment Insertion Points

RXLA_SLICE_ADJ_LO_RANGE should be set to 1 to apply the slice adjust after the equalization function.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG3	50	RXLA_SLICE_ADJ_LO_RANGE	1:1	RW	0	0-1	Selects slice level adjust point. When LOW, slicing point is option 1. When HIGH, slicing point is option 2.

4.2.3 Receive Equalization

The receive input implements an equalizer that provides peaking at 5.35GHz. This feature allows for optimal performance with extended reach connections, and allows for optimization of parameters such as dispersion penalty.

The equalizer implements 0dB to 14dB of high-frequency boost in fifteen steps, while achieving optimal receive sensitivity at any given equalization setting. The equalization setting is set through the **RXLA_BOOST_MSB** control. Additionally, the **RXLA_BOOST_LSB** control provides another 8 steps of fine tune control of the equalization gain at each **RXLA_BOOST_MSB** setting.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG1	48	RXLA_BOOST_MSB	3:0	RW	0000	0-15	RXLA boost control bit MSBs: 0 = 0dB to 15 = 14dB
RX_REG16	63	RXLA_BOOST_LSB	2:0	RW	000	0-7	RXLA boost control bit LSBs for fine tuning gain with smaller step size.

When the equalization setting is 0dB, the equalization function is bypassed and the receive sensitivity performance is the same as that of a limiting amplifier.

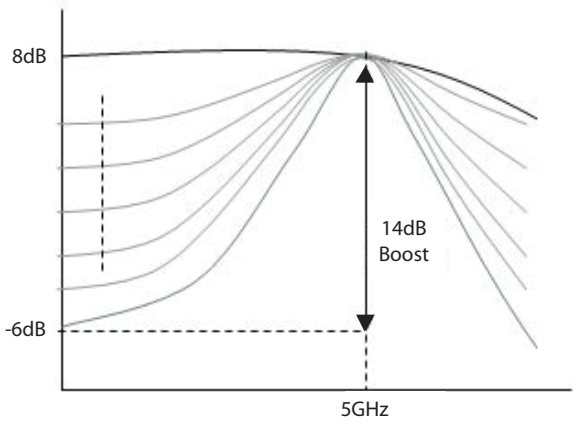


Figure 4-3: Receive Equalization

4.2.4 Rx PLL Variable Loop Bandwidth

The loop bandwidth of the receive Phase Locked Loops (PLLs) can be varied through the digital control interface. The loop bandwidths (LBW) are individually controlled, and can cover a range of less than 2.6MHz to 13MHz through the following 5-bit registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG1	20	RX_PLL_LBW_POS_ADJ	4:0	RW	11101	0-31	Adjusts LBW positive temperature coefficient control.
RXPLL_REG2	21	RX_PLL_LBW_NEG_ADJ	4:0	RW	00111	0-31	Adjusts LBW negative temperature coefficient control.

The temperature coefficient of the loop bandwidth can be adjusted by a weighted summation of **RX_PLL_LBW_POS_ADJ**, which has a positive temperature coefficient, and **RX_PLL_LBW_NEG_ADJ**, which has a negative temperature coefficient.

Table 4-1 shows the recommended settings for a flat loop bandwidth temperature coefficient:

Table 4-1: Rx Loop Bandwidth

RX_PLL_LBW_POS_ADJ	RX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
2	0	2	2.047
4	3	7	3.280
7	5	12	4.513
10	7	17	5.700
13	9	22	6.700
15	11	26	7.500
18	13	31	8.500
21	15	36	9.500
24	17	41	10.250
27	19	46	11.000
29	20	49	11.375

Table 4-1: Rx Loop Bandwidth (Continued)

RX_PLL_LBW_POS_ADJ	RX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
31	22	53	11.875
31	31	62	13.000

4.2.5 Rx CDR Input Jitter Tolerance

The input jitter tolerance of the Rx CDR is configurable to allow power optimization for required performance. Three modes of operation are supported as follows:

- **Mode 1:** Recommended for power-optimized applications. This mode supports the lowest power, but it is not guaranteed to meet the SONET IJT mask
- **Mode 2:** Recommended for most applications, including SONET, Ethernet and Fibre Channel. In this mode, the device is guaranteed to meet the SONET IJT mask.
- **Mode 3:** Recommended for SONET applications that require large margins on SONET IJT mask. This mode consumes extra power.

The RxCDR IJT mode is configured through the following registers. By default, the device is configured in Mode 3.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG9	28	RX_PLL_SELECT_HIGH_IJT	3:3	RW	1	0-1	When HIGH, selects high-margin Sonet IJT mode in conjunction with the RX_PLL_SONET_IJT_SETTING.
RXPLL_REG8	27	RX_PLL_SONET_IJT_SETTING	7:3	RW	00010	0-31	Control for Sonet IJT performance. Used in conjunction with Sonet IJT modes 2 and 3 to set IJT performance. Gradually increase setting for increased margins.
RXPWRDN_REG4	137	RX_PD_SONET_IJT	0:0	RW	0	0-1	When HIGH, powers-down the Rx path Sonet IJT feature to save power.

Table 4-2 shows the recommended settings for above registers for the three IJT modes:

Table 4-2: IJT Mode Settings

IJT Mode	RX_PD_SONET_IJT	RX_PLL_SELECT_HIGH_IJT	RX_PLL_SONET_IJT_SETTING[4:0]
1	1	x	x
2	0	0	2 (or higher, based on user preference)
3	0	1	3 (or higher, based on user preference)

Figure 4-4 shows that Mode 2 and Mode 3 SIJT performance is comparable with maximum LBW settings, with >3UI margin at 400kHz:

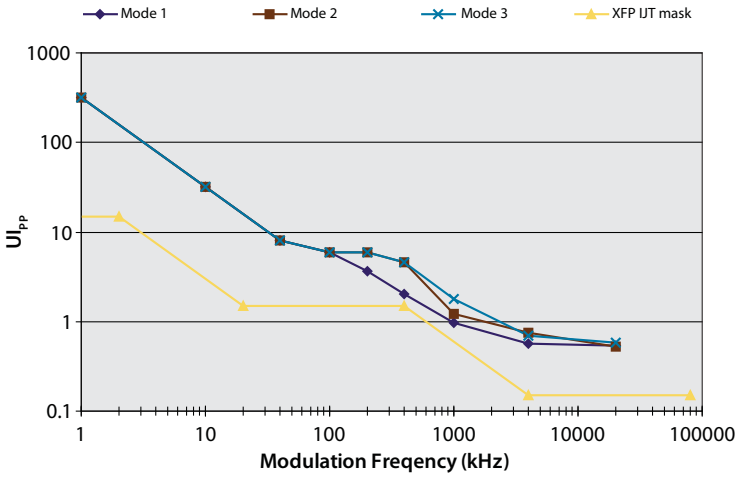


Figure 4-4: S-IJT Mode 1, 2 & 3 (Loop Bandwidth = 6.2MHz)

With higher LBW settings, Mode 2 can be used to meet and exceed S-IJT mask with lower power than Mode 3. Note that in either Mode 2 or Mode 3, the **RX_PLL_SONET_IJT_SETTING** can be adjusted beyond the values provided in Table 4-2 to further optimize SIJT performance margins.

4.2.6 Emphasis Driver with Auto-Mute

The receive path driver is a non-clocked emphasis driver that can be used to compensate for losses in the connector and trace between the module and ASIC. The emphasis operates regardless of the status or state of the Rx CDR. The output swing can be set from 100mV to 800mV in steps of 50mV through the **RX_SDO_SWING[3:0]** register. The emphasis amplitude can be varied from 1dB to 6dB in 16 steps through **RX_SDO_EMPHASIS[3:0]**.

Note: The Rx emphasis in disabled by default. To enable the emphasis, set **RX_PD_RXSDO_EMPHASIS** to 0 to power-on the Rx emphasis block. When emphasis is enabled, the output driver is still limited to approximately 800mV$_{ppd}$ output. Therefore, at some swings settings (i.e. >400mV$_{ppd}$), the full 6dB emphasis may not be realized. See Figure 4-5 for more information.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXSDO_REG1	75	RX_SDO_SWING	3:0	RW	0110	0-15	Driver swing: 100mV$_{ppd}$ to 850mV$_{ppd}$. Default = 6 = 400mV$_{ppd}$.
RXSDO_REG2	76	RX_SDO_EMPHASIS	3:0	RW	0000	0-15	Driver emphasis control.
RXPWRDN_REG1	134	RX_PD_RXSDO_EMPHASIS	3:3	RW	1	0-1	When HIGH, power-down for the trace driver emphasis.

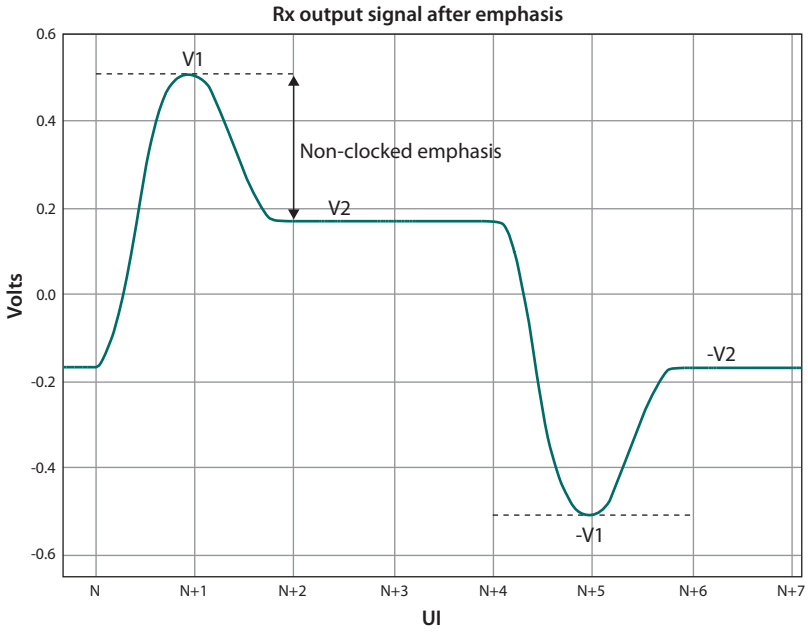


Figure 4-5: Emphasis Waveform Description when Enabled

Figure 4-5 above shows the emphasis waveform. Amplitudes V1, V2 and emphasis in dB are defined as follows:

V1, **V2** and **Emphasis** are defined as follows:

V1 = **RX_SDO_EMPHASIS** setting, which represents the "peak", or superposition of the **RX_SDO_SWING** setting and the **RX_SDO_EMPHASIS** setting.

V2 = **RX_SDO_SWING** setting, which is the DC or Steady State swing, same as when no emphasis is enabled.

Emphasis [dB] = 20 x log(V1/V2). As a guideline, 2V1 should be less than or equal to 800mV.

The output can be configured to automatically mute if Receive LOS is detected through the following registers. When muted, the output driver remains powered-up, and the output common mode is maintained. The output driver can be configured to power-down when muted by setting the **RX_SDO_PWR_DN_ON_MUTE** bit:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXSDO_REG3	77	RX_SDO_FORCE_MUTE	0:0	RW	0	0-1	Mutes driver to CM when not in auto mute mode.
		RX_SDO_AUTO_MUTE_EN	1:1	RW	1	0-1	Enables muting the driver upon LOS.
		RX_SDO_PWR_DN_ON_MUTE	2:2	RW	1	0-1	Enables power-down on mute for output stage.

4.2.7 Output Polarity Invert

Polarity inversion is implemented at the SDO input. Input to the CDR is not affected by polarity inversion. The output polarity can be inverted through the following register:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG5	24	RX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.

4.3 Transmit Path

The transmit path is comprised of a trace equalizer, a multi-rate CDR and a trace driver.

Figure 4-6: Transmit Path

4.3.1 Equalizer

The the transmit path input has an XFI equalizer with up to 6dB gain at 5.35GHz. The equalizer can be controlled through the following register:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TX_REG3	33	TX_EQ_BOOST	1:0	RW	11	0-3	Controls the Tx path input equalization setting: 00 = 0dB 01 = 2dB 10 = 4dB 11 = 6dB

4.3.2 Tx PLL Variable Loop Bandwidth

The loop bandwidth of the transmit Phase Locked Loops (PLLs) can be varied through the digital control interface. The loop bandwidths are individually controlled, and can cover the range of less than 1MHz to 10MHz through following 5-bit registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG1	10	TX_PLL_LBW_POS_ADJ	4:0	RW	01110	0-31	Adjusts LBW positive temperature coefficient control.
TXPLL_REG2	11	TX_PLL_LBW_NEG_ADJ	4:0	RW	00010	0-31	Adjusts LBW negative temperature coefficient control.

The temperature coefficient of the loop bandwidth can be adjusted by weighted summation of **TX_PLL_LBW_POS_ADJ**, which has a positive temperature coefficient and **TX_PLL_LBW_NEG_ADJ**, which has a negative temperature coefficient.

Table 4-3 shows the recommended settings for a flat loop bandwidth temperature coefficient:

Table 4-3: Tx Loop Bandwidth

TX_PLL_LBW_POS_ADJ	TX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
2	0	2	1.413
4	3	7	2.480
7	5	12	3.547
10	7	17	4.555
13	9	22	5.330
15	11	26	5.950
18	13	31	6.725
21	15	36	7.500
24	17	41	8.050
27	19	46	8.600
29	20	49	8.919
31	22	53	9.344
31	31	62	10.300

4.3.3 Tx Jitter Filter Mode

The Tx CDR supports a jitter filter mode to aid in the optimization of jitter generation performance and reduction of jitter present at the Tx CDR input. The jitter filter mode is configured using the following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPWRDN_REG4	133	TX_PD_JIT_FILT	0:0	RW	1	0-1	When HIGH, power-down for the Tx jitter filter.
TXPLL_REG1	10	TX_PLL_LBW_POS_ADJ	4:0	RW	01110	0-31	Adjusts the LBW positive temperature coefficient control.
TXPLL_REG2	11	TX_PLL_LBW_NEG_ADJ	4:0	RW	00010	0-31	Adjusts the LBW negative temperature coefficient control.
TXPLL_REG8	17	TX_JIT_FILT_TRACK_ADJUST	7:3	RW	00010	0-31	Sets the tracking capability when Tx jitter filter mode is enabled.

To enable Tx jitter filter mode, set **TX_PD_JIT_FILT** LOW. Once enabled, **TX_PLL_LBW_POS_ADJ** and **TX_PLL_LBW_NEG_ADJ** are used to set the jitter filter bandwidth, and can be optimized for the desired jitter generation/filtering performance. Lastly, **TX_JIT_FILT_TRACK_ADJUST** is used to set the tracking capability of an internal clock with respect to the Tx input data. This allows for optimization of wander tolerance.

4.3.4 De-emphasis Driver with Auto-Mute

The transmit path driver is a two-tap de-emphasis driver that can be used to compensate for losses in the connector and trace between the module and ASIC. The de-emphasis can compensate for up to 12dB of loss. The output swing can be set from $100mV_{ppd}$ to $860mV_{ppd}$ in steps of approximately $50mV_{ppd}$ through the **TXSDOSWING[3:0]** register. The post-tap amplitude can be varied from 0 to $350mV_{ppd}$ in 32 steps through **TXSDOPOSTTAP[4:0]**.

Note: The Tx de-emphasis in disabled by default. To enable the de-emphasis, set **TXPDTXSDOPE** HIGH to power-on the Tx de-emphasis block.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG27	101	TXSDOSWING	3:0	RW	1010	0-15	Driver swing: 0 to 15 = $100mV_{ppd}$ to $860mV_{ppd}$ in steps of ~$50mV_{ppd}$. Default = 10 = $600mV_{ppd}$.
TXSDO_REG28	102	TXSDOPOSTTAP	4:0	RW	00000	0-31	Driver post tap PE control: 0 = $0mV_{ppd}$, 31= $350mV_{ppd}$ in steps of $11.3mV_{ppd}$.
TXPWRDN_REG1	130	TXPDTXSDOPE	4:4	RW	1	0-1	When HIGH, power-down the Tx path trace driver pre-emphasis.

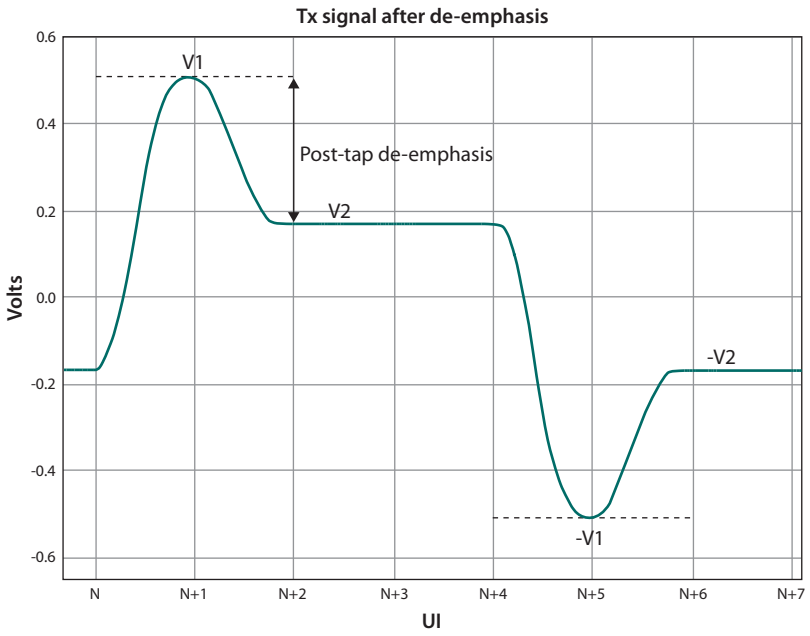


Figure 4-7: Tx De-emphasis Waveform Description with Post-Tap Enabled

Figure 4-7 above shows the de-emphasis waveform. Amplitudes V1, V2 and de-emphasis in dB are defined as follows:

V1, **V2** and **Post Tap De-emphasis** are defined as follows:

V1 = |Vmain tap| + |Vpost tap|, which represents the “peak”.

V2 = |Vmain tap| - |Vpost tap|, which represents DC or Steady State.

Post Tap De-emphasis [dB] = 20 x log(V1/V2)

The output can be configured to automatically mute if transmit LOS is detected through the following registers. When muted, the output driver remains powered-up, and the output common mode is maintained. The output driver can be configured to power-down when muted by setting the **TXSDOPWRDNONMUTE** bit.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG25	99	TXSDOFORCEMUTE	3:3	RW	0	0-15	When HIGH, mutes the driver and maintains common mode when not in auto mute mode.
		TXSDOAUTOMUTEEN	4:4	RW	00000	0-31	When HIGH, enables muting the driver upon LOS.
		TXSDOPWRDNONMUTE	5:5	RW	1	0-1	When HIGH, enables power-down on mute for output stage.

4.3.5 Output Polarity Invert

Polarity inversion is implemented at the SDO input. Input to the CDR is not affected by polarity inversion. The output polarity can be inverted through the following register:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG5	14	TXPOLINV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.

4.4 Status Indicators

The GN2040 supports three status indicators: Loss of Signal (LOS), Loss of Lock (LOL) and Fault. LOS and LOL indicators are available on both the receive and the transmit paths.

4.4.1 Receive Loss of Signal (LOS)

The receive path Loss Of Signal indicator status is available through a register and the LOSL pin. The LOSL pin is by default open-drain, active-high 1.8V LVCMOS compatible. However, the pin can be configured in a 1.8V LVCMOS-compliant compatible mode by setting **OPEN_DRAIN_LOSL** to 0. In addition, LOSL can be configured to be active-low by setting **POLINV_LOSL** HIGH. The status of RxLOS can be read out through **RX_PLL_LOS**. Additionally, the LOSL pin can be configured to provide other status information as per the table below. By default, LOSL only provides status information for RxLOS. If other status indicators are enabled, the LOSL output is the logical OR of all enabled indicators.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TOP_REG2	2	POLINV_LOSL	1:1	RW	0	0-1	When HIGH, inverts polarity of the LOSL output.
		OPEN_DRAIN_LOSL	2:2	RW	1	0-1	When HIGH, makes the LOSL output driver open-drain.
		LOSL_MASK_RXLOS	4:4	RW	0	0-1	When HIGH, masks-out RxLOS from asserting LOSL.
		LOSL_MASK_RXLOL	5:5	RW	1	0-1	When HIGH, masks-out RxLOL from asserting LOSL.
		LOSL_MASK_TXLOS	6:6	RW	1	0-1	When HIGH, masks-out TxLOS from asserting LOSL.
		LOSL_MASK_TXLOL	7:7	RW	1	0-1	When HIGH, masks-out TxLOL from asserting LOSL.
RXPLL_REG10	29	RX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.

The LOS assert threshold can be set from 5mV to 400mV in three distinct ranges. The LOS assert threshold is a function of the **RXLA_BOOST_MSB** setting. Table 4-4 describes the selection of **RXLOS_RANGE** based on the required LOS assert threshold and **RXLA_BOOST_MSB** settings.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG12	59	RXLOS_RANGE	1:0	RW	01	0-3	LOS range: 0 = highest 3 = lowest 2 = (MSB) unused

Table 4-4: LOS Assert Ranges

RXLA_BOOST_MSB [3:0]	LOS Assert Threshold Range		RXLOS_RANGE[1:0]	Resolution (controlled by RXLOS_TH_NEG/POS)	Unit
	Min	Max			
	5	400	LOS Threshold - Total Range	—	mV_{ppd}
0-7	—	—	11 - Unused	—	—
0-7	5	30	10 - Low Range	<0.1mV	mV_{ppd}
0-7	30	100	01 - Mid Range	<1.0mV	mV_{ppd}
0-7	100	400	00 - High Range	<2.0mV	mV_{ppd}
8-15	5	30	11 - Low Range	<0.1mV	mV_{ppd}
8-15	30	100	10 - Mid Range	<1.0mV	mV_{ppd}
8-15	—	—	01 - Unused	—	—
8-15	100	400	00 - High Range	<2.0mV	mV_{ppd}

4.4.1.1 Rx LOS Threshold

The LOS assert threshold is set using the following registers:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
RX_REG9	56	RXLOS_TH_NEG	7:0	RW	01001001	0-255	Negative tempco LOS threshold setting.
RX_REG10	57	RXLOS_TH_POS	7:0	RW	00000000	0-255	Positive tempco LOS threshold setting.

Figure 4-8 to Figure 4-12 shows the typical recommended range of Rx LOS Assert thresholds and corresponding **RX_LOS_TH_NEG[7:0]** setting to achieve these thresholds. It is recommended to keep **RX_LOS_POS[7:0]** = 0. The Rx LOS De-assert thresholds are the same as the Rx LOS Assert thresholds for a hysteresis setting of 0.

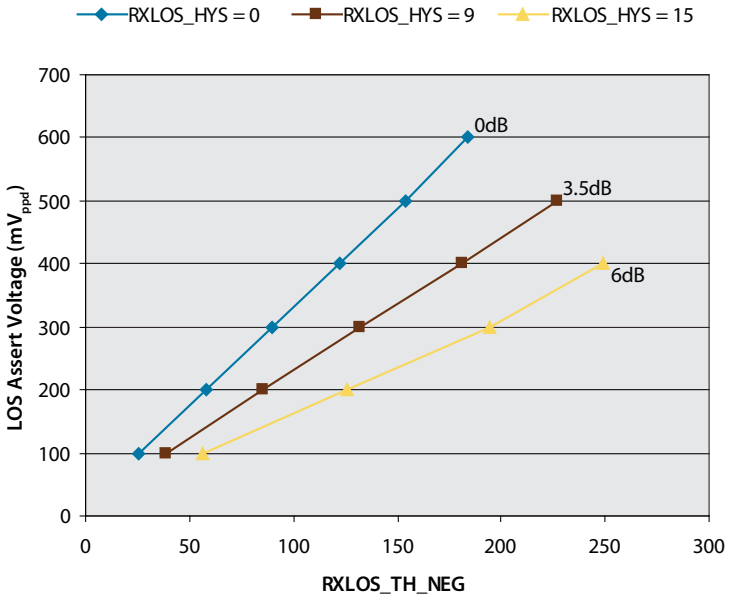


Figure 4-8: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = 0)

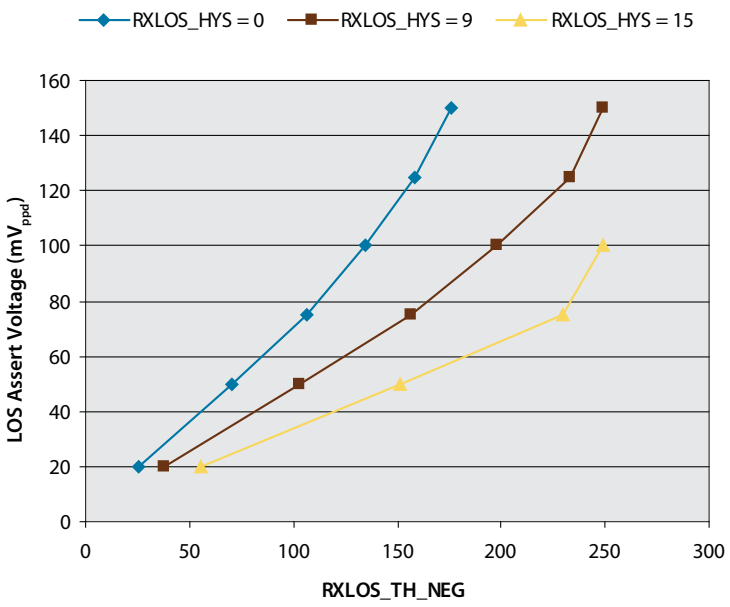


Figure 4-9: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = 1)

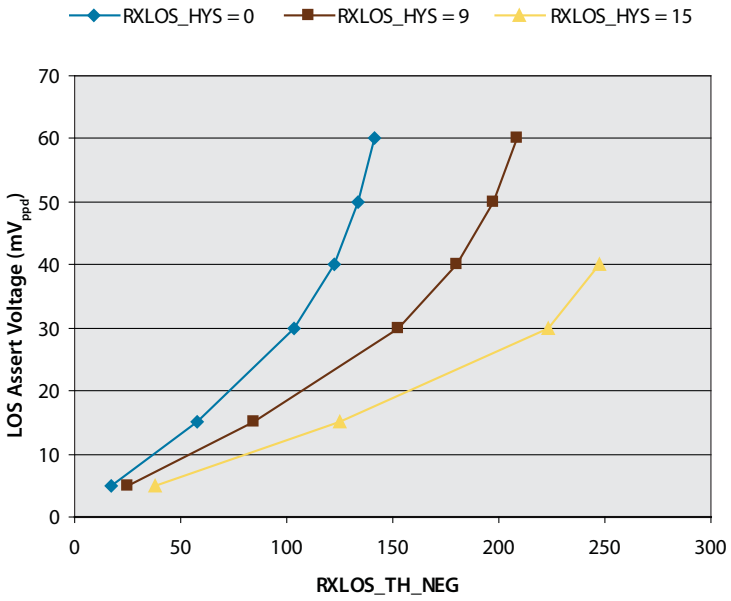


Figure 4-10: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = 2)

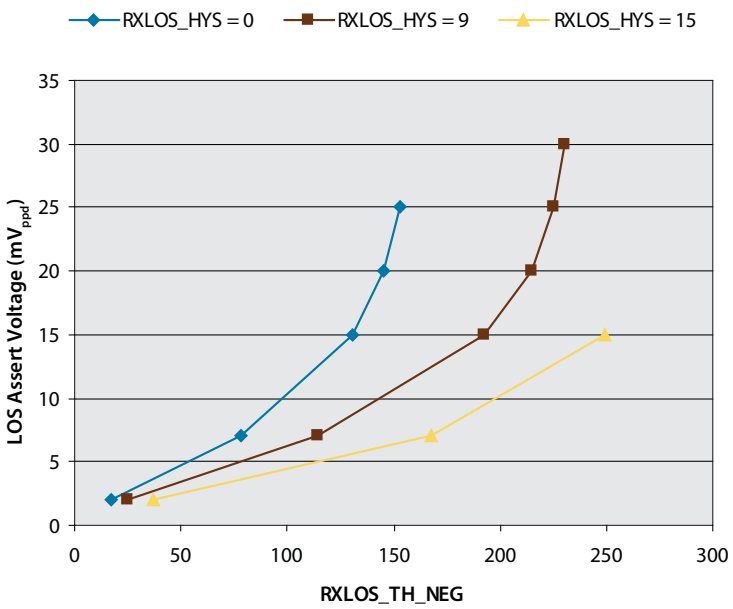


Figure 4-11: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = 3)

The LOS threshold has a slight dependence on the input data rate. Figure 4-12 below gives an indication of the typical variation of data rate, between 9.95Gb/s to 11.3Gb/s.

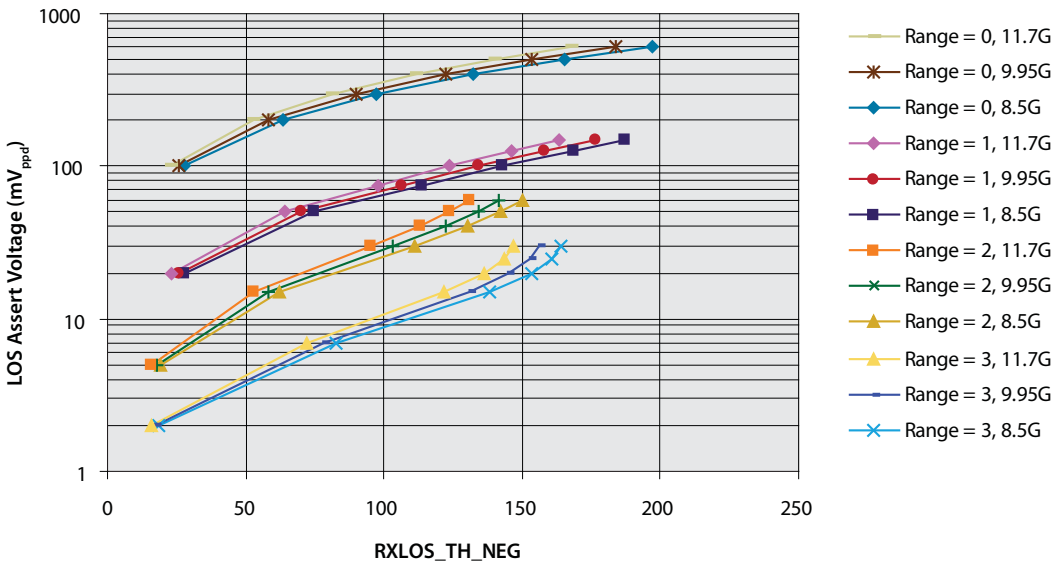


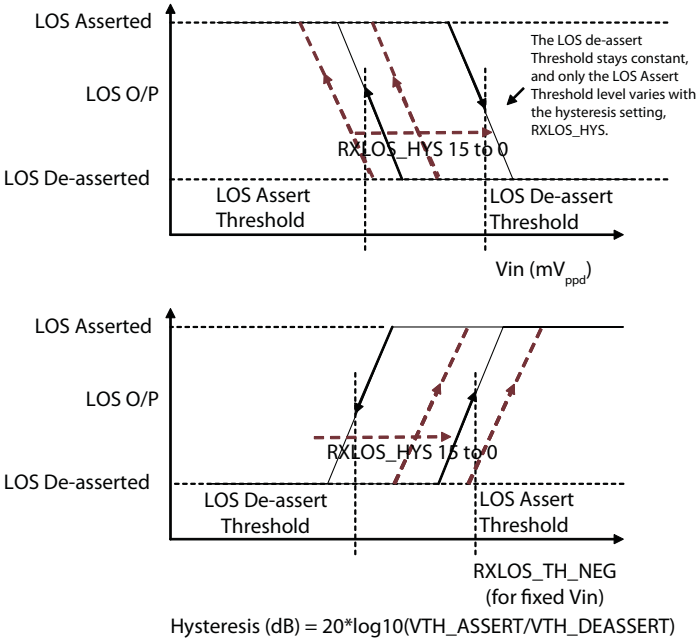
Figure 4-12: Rx LOS Assert Threshold Variation Over Data Rates

4.4.1.2 Rx LOS Hysteresis

The LOS detector supports programmable hysteresis ranging from 0dB to 6dB, adjustable in steps of less than 0.5dB. The following register can be used to program the hysteresis. Note that the effective hysteresis is somewhat dependent on the threshold value:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG11	58	RXLOS_HYS	3:0	RW	1001	0-15	Hysteresis control 0-15 -> 0-6dB. Default = 9 = 3dB.

Hysteresis control only affects the assert threshold. The LOS de-assert threshold is set by **RXLOS_TH_NEG** and **RXLOS_TH_POS** controls only. Figure 4-13 shows the hysteresis characteristics and the impact of **RXLOS_HYS[3:0]**:



RXLOS_HYS	Hysteresis (dB)
0	0.1
1	0.3
2	0.7
3	1.1
4	1.4
5	1.8
6	2.1
7	2.5
8	3.0
9	3.4
10	3.9
11	4.4
12	4.8
13	5.4
15	6.7

Figure 4-13: Rx LOS Hysteresis

To support system diagnostics, a manual LOS assert feature is available through the following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG12	59	RXLOS_FORCE_ASSERT	2:2	RW	0	0-1	Directly sets the state of RXLOS accordingly if RXLOS_FORCE_ASSERT_EN is HIGH.
		RXLOS_FORCE_ASSERT_EN	3:3	RW	0	0-1	When HIGH, LOS is controlled by RXLOS_FORCE_ASSERT.

4.4.2 Transmit Loss of Signal

The transmit path LOS indicator status is available through a register. If desired, its status can be included in the generation of the FAULT or LOSL output pins. The LOS assert threshold can be set from 20mV to 100mV in <1mV steps. In addition the temperature coefficient of the LOS threshold can be adjusted to ensure consistent LOS operation over temperature. The LOS also has hysteresis that is programmable from 0dB to 6dB in steps of less than 0.5dB. A manual LOS assert feature is supported for system diagnostics.

The following registers are used to control the transmit LOS feature:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TX_REG9	39	TXLOS_TH_NEG	7:0	RW	00011011	0-255	Negative temperature coefficient LOS threshold setting.
TX_REG10	40	TXLOS_TH_POS	7:0	RW	00000000	0-255	Positive temperature coefficient LOS threshold setting.
TX_REG11	41	TXLOS_HYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB.
TX_REG12	42	TXLOS_FORCE_ASSERT	3:3	RW	0	0-1	Directly sets the state of TXLOS accordingly if TXLOS_FORCE_ASSERT_EN is HIGH.
		TXLOS_FORCE_ASSERT_EN	4:4	RW	0	0-1	When HIGH, LOS is controlled by TXLOS_FORCE_ASSERT.

4.4.2.1 Tx LOS Threshold

Figure 4-14 and Figure 4-15 show the typical recommended range of Tx LOS assert thresholds and corresponding **TXLOS_TH_NEG[7:0]** setting to achieve these thresholds. It is recommended to keep **TXLOS_TH_POS[7:0]** = 0 to achieve a flat temperature coefficient for LOS threshold. The Tx LOS de-assert thresholds are the same as the Tx LOS assert thresholds for a hysteresis setting of 0.

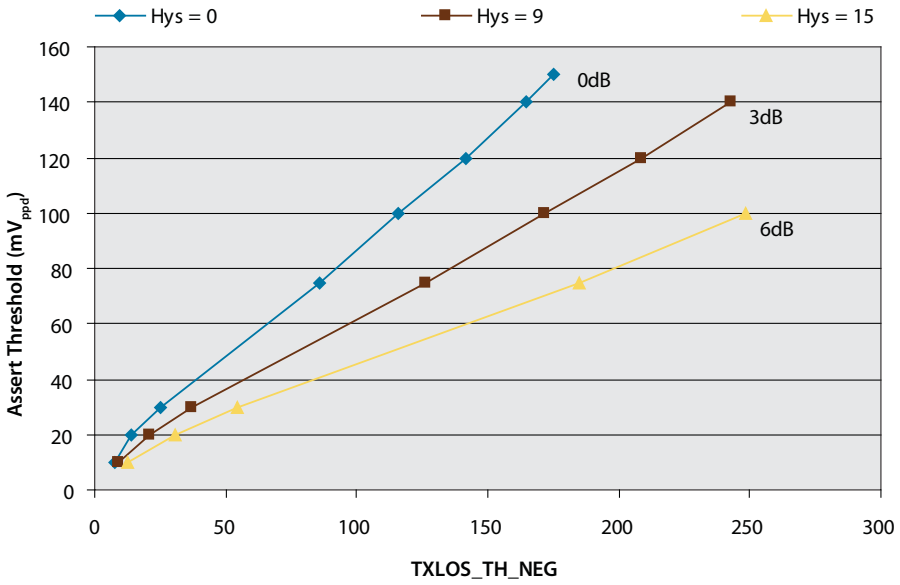


Figure 4-14: Tx LOS Assert Threshold – Typical @ 9.95Gb/s

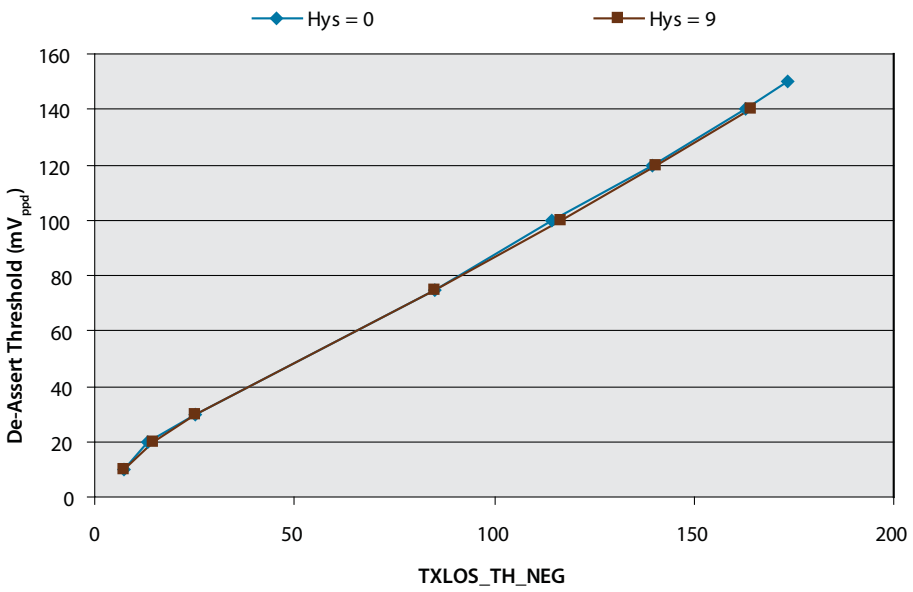


Figure 4-15: Tx LOS De-Assert Threshold – Typical @ 9.95Gb/s

The LOS threshold will have a slight dependence on data rate.

4.4.3 Loss of Lock

The receive path and transmit path LOSS of LOCK (LOL) status indicators are both available in registers as indicated below. These bits can also be included in the FAULT or LOSL outputs:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TXPLL_REG10	19	TX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
RXPLL_REG10	29	RX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.

4.4.4 FAULT

Various status indicator pins are combined to generate a single FAULT indicator output. The FAULT output is, by default, an open-drain 1.8V LVCMOS-compatible output. It can be configured in a 1.8V LVCMOS-compliant mode through Register **2**, bit **3**—**OPEN_DRAIN_FAULT**.

The FAULT output is active-high by default. Its polarity can be changed to make it active-low through Register **2**, bit **0**—**POLINV_FAULT**. When set HIGH, FAULT is configured as an active-low output.

The following status indicator controls can be combined to generate the FAULT output. Each of the indicators can be independently masked through the register controls shown in Table 4-5 below. By default, the FAULT output combines (OR's) the status of all indicators.

The following registers control the masking of the various indicators for FAULT and the configuration of FAULT pin.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG1	1	FAULT_MASK_RXLOS	0:0	RW	0	0-1	When HIGH, masks-out RxLOS from asserting FAULT.
		FAULT_MASK_RXLOL	1:1	RW	0	0-1	When HIGH, masks-out RxLOL from asserting FAULT.
		FAULT_MASK_TXLOS	2:2	RW	0	0-1	When HIGH, masks-out TxLOS from asserting FAULT.
		FAULT_MASK_TXLOL	3:3	RW	0	0-1	When HIGH, masks-out TxLOL from asserting FAULT.
TOP_REG2	2	POLINV_FAULT	0:0	RW	0	0-1	When HIGH, inverts polarity of FAULT output.
		OPEN_DRAIN_FAULT	3:3	RW	1	0-1	When HIGH, makes the FAULT output driver open-drain.

4.5 Test Features

The GN2040 contains built-in test features that can be used during module bring-up or for debug purposes. The test features are not guaranteed and are only meant as functional tests under typical conditions. It is not advised to use these features during mission mode operation.

4.5.1 PRBS Generator and Checker

The GN2040 has a built-in PRBS7 generator and checker. The generator and checker are disabled by default to save power, and can be enabled through the digital control interface. There are multiple ways to use the PRBS generator/checker.

The PRBS Generator frequency is controlled by the **PRBS_GENERATOR_DATA_RATE_CONTROL[5:0]** register. The PRBS generator and checker are meant to be used only as functional debug tests. The register setting of **PRBS_GENERATOR_DATA_RATE_CONTROL[5:0]** = 20 corresponds to a data rate of typically 10.3Gb/s. The PRBS checker uses the recovered clock from the Tx CDR. Refer to Table 4-5 for more details.

Note: PRBS7 input to the PRBS checker must be non-inverted for the checker to operate correctly. As such, care must be taken when using the polarity invert feature in conjunction with external loop back to PRBS checker to ensure that the data polarity to the checker is correct. Internal loop-back paths are not affected by the polarity invert feature.

The following registers enable and configure the PRBS generator and checker:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG3	3	PRBS_GEN_START	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts off the PRBS Generator.
		PRBS_CHK_CLEAR_ERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from the Checker.
TOP_REG6	6	PRBS_CHK_STATUS	0:0	RO	0	0-1	When HIGH, checker detected an error.
LOOPBK_REG1	7	LB_RX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Rx Driver.
		LB_RX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects PRBS generator output into Rx Driver.
LOOPBK_REG2	8	PRBS_CHK_CLK_SEL	1:1	RW	0	0-1	When HIGH, selects the Tx recovered clock. When LOW, selects the Rx recovered clock.
		LB_TX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Tx Driver.
		LB_TX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects PRBS generator output into the Tx Driver.
LOOPBK_REG3	9	PRBS_GENERATOR_DATA_ RATE_CONTROL	5:0	RW	0	0-63	PRBS Generator Frequency Tuning Control. The tuning range is 9.9GHz to 10.4GHz from minimum to maximum setting.
PWRDN_REG2	139	PD_PRBS_GEN	1:1	RW	1	0-1	When HIGH, power-down the PRBS generator and associated buffers.
		PD_PRBS_CHK	2:2	RW	1	0-1	When HIGH, power-down the PRBS checker and associated buffers.

To ensure proper operation of the PRBS7 generator, **PRBS_GEN_START** needs to be set HIGH and then LOW once after the generator is powered-up through **PD_PRBS_GEN**.

To ensure proper operation of the PRBS7 checker, **PRBS_CHK_CLEAR_ERR** needs to be set HIGH and then LOW after application of valid PRBS7 pattern to clear any spurious errors. **PRBS_CHK_STATUS**, may be polled to check for errors flagged by the checker.

The PRBS generator can be configured to apply a PRBS7 pattern to RxSDO or TxSDO.

Table 4-5: PRBS Generator/Checker Configuration

Loopback Mode	Description	PD_PRBS_GEN	PD_PRBS_CHK	PRBS_CHK_CLK_SEL	LB_TX_OUT_PRBS_GEN	LB_RX_OUT_PRBS_GEN	LB_TX_OUT_EN	LB_RX_OUT_EN
PRBS Disabled	Default Mission mode	1	1	X	0	0	0	0
PRBS Generator → Rx Driver → Tx Equalizer → Tx CDR → PRBS Checker	External Rx Loopback (tests TX CDR)	0	0	1	0	1	0	1

4.5.2 Loopback

The GN2040 allows four different loopback paths, and supports loopback on both the electrical side and the optical side. The loopback paths are shown in Table 4-6. The blocks referenced in the different loopback paths are shown in Figure 4-16.

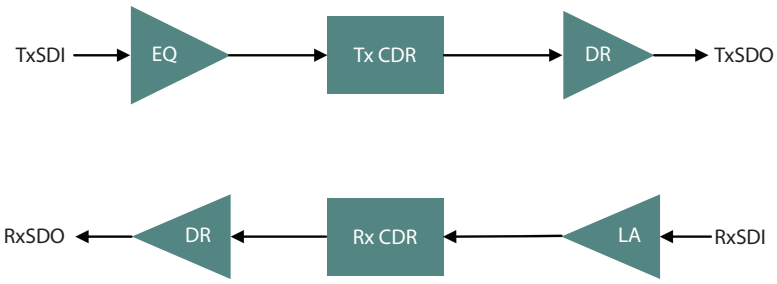


Figure 4-16: Simultaneous Loopback

Table 4-6: Loopback Paths

Mode #	Loopback Path
1	RxSDI → LA → Tx DR → TxSDO
2	RxSDI → LA → RxCDR → Tx DR → TxSDO
3	TxSDI → EQ → Rx DR → RxSDO
4	TxSDI → EQ → TxCDR → Rx DR → RxSDO

When loopback is enabled, the standard data path is not interrupted. For example: in Mode 1, the input to RxSDI will also be accessible at RxSDO. When using loopback modes, the automute feature for RxSDO or TxSDO may have to be disabled if the corresponding RxSDI or TxSDI inputs are unused.

The relevant parameters and their values required to enable each of the loopback options indicated above, are shown in Table 4-7.

The selection of a loopback path impacts the following features:

- Polarity inversion
- Phase adjust for jitter optimization for TxSDO (DR)

Table 4-7 also captures the impact on these features in each loopback mode.

Table 4-7: Loopback Options

Loop Back Mode (see Table 4-6)	LB_RX_OUT_EN	LB_RX_OUT_TX_DATA	LB_RX_OUT_PRBS_GEN	LB_RX_OUT_RX_CLK	RX_PLL_BYPASS	LB_TX_OUT_EN	LB_TX_OUT_RX_DATA	LB_TX_OUT_PRBS_GEN	LB_TX_OUT_TX_CLK	TX_PLL_BYPASS	TX_PLL_POLINV Effective	TX_SDO_PHADJ Available	RX_PLL_POLINV Effective
1	0	0	0	0	1	1	1	0	0	0	Y	N	N
2	0	0	0	0	0	1	1	0	0	0	Y	N	N
3	1	1	0	0	0	0	0	0	0	1	N	—	Y
4	1	1	0	0	0	0	0	0	0	0	N	—	Y
Control Register Address	7	7	7	7	24	8	8	8	8	14	—	—	—
Associated Bit Slice	4	5	6	7	2	4	5	6	7	2	—	—	—

4.6 Digital Diagnostics

The GN2040 has an on-chip ADC to provide diagnostic information through the digital interface. Refer to the GN204x Family ADC Application Note (PDS-060373) for more details.

4.7 Power-Down Options

The GN2040 provides a high-degree of flexibility in configuring the device for optimal power through power-down registers. Typical usage scenarios are shown. For further description on each of the individual control bits, see Table 5-1, registers **134** to **137**. This section describes the power-down controls for the following sub-systems:

1. Rx LA Power-Down
2. Rx CDR & SDO Power-Down
3. Tx CDR Power-Down
4. Tx SDO Power-Down

Table 4-8: Rx LA Power-Down

RX_PD_PATH	RX_PD_LA	RX_PD_LOS	RX_PD_SLICE_ADJ	Description
1	x	1	1	Completely powers-down the Rx LA.
x	1	1	1	Completely powers-down the Rx LA.
0	0	0	0	All features on. This is diagnostic mode.
0	0	0	1	Powers-down the slice adjust mode.
0	0	1	1	Powers down the SLA and LOS feature for lowest power mode.

Table 4-9: Rx CDR & SDO Power-Down

RX_PLL_BYPASS	RX_PD_PATH	RX_PD_RXCDR	RX_PD_SONET_IJT	RX_PD_RXSDO	RX_PD_RXSDO_EMPHASIS	Description
0	1	x	x	1	1	Completely powers-down the Rx CDR and Rx SDO.
0	x	1	x	1	1	Completely powers-down the Rx CDR and Rx SDO
1	0	x	x	0	1	Main data path through Rx CDR and RxSDO is powered-up for bypass mode. (RxLA has to be powered-up).
0	0	0	1	0	1	Standard operating mode, Rx CDR & SDO enabled in low-power mode. High IJT mode and emphasis are disabled.
0	0	0	0	0	0	Standard operating mode, Rx CDR & SDO enabled. High IJT mode and emphasis are enabled. IJT performance is set by RX_PLL_SELECT_HIGH_IJT registers.
0	0	0	1	0	0	Rx CDR & SDO are enabled. High IJT mode is powered-down. Emphasis is enabled.

Table 4-10: Tx CDR Power-Down

TX_PLL_BYPASS	TX_PD_TXPATH	TX_PD_TXCDR	TX_PD_JIT_FILT	TX_PD_TXSDO	Description
0	1	1	x	1	Completely powers-down the Tx CDR and Tx path.
1	0	1	x	0	Main data path through Tx CDR is powered-up for bypass mode. (TxEq has to be powered-up).
0	0	0	1	0	Standard operating mode, Tx CDR is enabled in standard mode.
0	0	0	0	0	Standard operating mode, Tx CDR is enabled in jitter filter mode. (Requires appropriate configuration of jitter filter controls. See Section 4.3.3).

Table 4-11: Tx SDO Power-Down

TX_PD_TXPATH	TX_PD_TXSDO	TX_PD_TXCDR	Description
1	x	x	Completely powers-down the Tx SDO.
x	1	x	Completely powers-down the Tx SDO.
0	0	0	Tx SDO with all features enabled.

4.8 Device Reset

$\overline{\text{RESET}}$ is an active-low signal with LVTTL/LVCMOS-compatible signalling levels. Due to the timing requirements of $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ to $\overline{\text{RESET}}$, it is recommended that $\overline{\text{RESET}}$ be driven by the Micro on the module. An external 10kΩ pull-down resistor is also recommended on the $\overline{\text{RESET}}$ line. $\overline{\text{RESET}}$ does not have a Schmitt trigger since reset negation is internally synchronized. See Figure 3-8.

4.8.1 Reset State During Power-up

The device requires $\overline{\text{RESET}}$ to be continuously pulled to GND during power ramp-up. $\overline{\text{RESET}}$ must continue to remain in that state for the minimum specified time after all of the power supplies have reached 90% of their final settling value. Following a $\overline{\text{RESET}}$ assertion at power-up, the device may be reset again at any time with the minimum specified pulse width on $\overline{\text{RESET}}$. Refer to Figure 4-17.

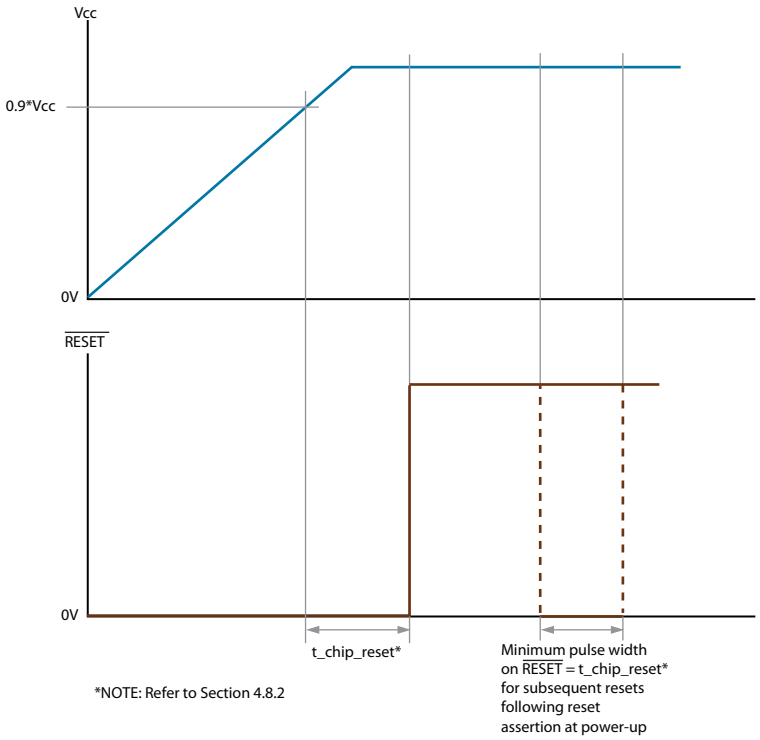


Figure 4-17: Reset State During Power-up

4.8.2 $\overline{\text{RESET}}$ Timing

The following $\overline{\text{RESET}}$ timing specifications apply:

- **t_chip_reset: 10µs**
  Defined as the minimum duration that $\overline{\text{RESET}}$ must be asserted after the supply has reached 90% of final settling value
- **t_ISELb_setup: 500ns**
  Defined as the minimum duration that the $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ pin must be asserted HIGH to select the SPI mode before $\overline{\text{RESET}}$ is negated
- **t_SPI_ready: 500ns**

  Defined as the minimum duration before an SPI/I^2C operation may be initiated, after $\overline{\text{RESET}}$ negation

When I^2C mode is desired, the $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ pin is recommended to be pulled to ground throughout operation of the device.

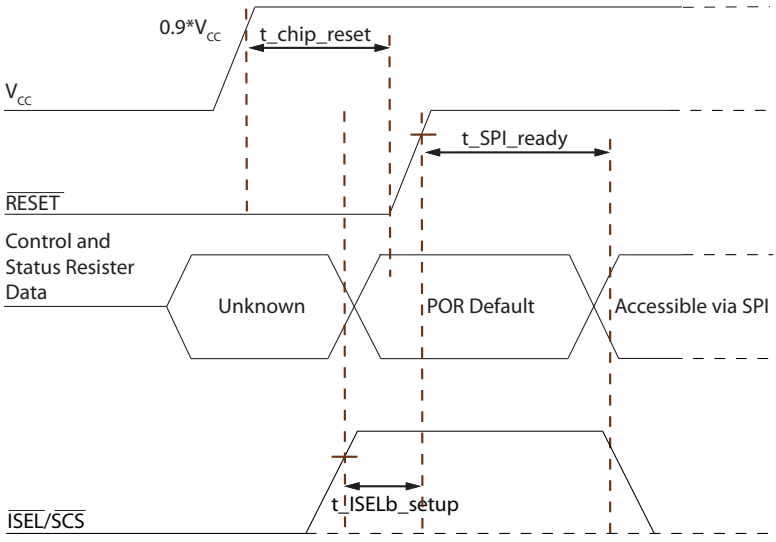


Figure 4-18: GN2040 Device Reset Timing Diagram

4.8.3 I/O and Register States During and After Reset

All configuration registers are set to their post-reset defaults state immediately following $\overline{\text{RESET}}$ assertion.

The following I/O states are applicable upon $\overline{\text{RESET}}$ assertion:

Table 4-12: I/O and Register States During and After Reset

Pin Name	I/O State upon $\overline{\text{RESET}}$ Assertion
SDA/SDIO/MISO	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance with a weak pull-down of 5µA.
SCL/SCLK and SSEL/MOSI	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted, and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance with a weak pull-down of 5µA.
FAULT	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. The loss of lock indicators will assert FAULT HIGH. This output will be high-impedance, and it's state will depend on the external pull-up.
LOSL	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. If a signal is present, the output will be pulled LOW. Otherwise, this output will be high-impedance and it's state will depend on the external pull-up.

Note: While the device is in reset, the SDA/SDI/MISO pin will output the state of the SSEL/MOSI pin. This can inhibit the ability for the master to communicate with other slave devices on the bus.

4.9 Digital Control Interface

The GN2040 has a tri-mode serial control interface to communicate with the part. Either an I^2C or SPI 3-wire, or SPI 4-wire protocol can be used. The protocol is selected using the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ and SSEL pins at the time of reset de-assertion.

When pin $\overline{\text{ISEL}}/\overline{\text{SCS}}$ is held LOW, or left unconnected, and the $\overline{\text{RESET}}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in I^2C mode. After reset de-assertion, the state of the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin is a 'don't care'. However, it is recommended that if the pin is not left unconnected, then it be driven LOW.

When the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin is held HIGH, and the SSEL pin is held LOW or left unconnected, and the $\overline{\text{RESET}}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in a three-wire SPI mode. After reset de-assertion, the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin functions as the $\overline{\text{SCS}}$ pin of a three-wire SPI interface.

When the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin is held HIGH, and the SSEL pin is held HIGH, and the $\overline{\text{RESET}}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in a four-wire SPI mode. After reset de-assertion, the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin functions as the $\overline{\text{SCS}}$ pin, and the SSEL/MOSI functions as the slave data input pin, and the SDA/SDIO/MISO functions as the slave data output of a four-wire SPI interface.

4.9.1 I²C Host Interface Mode

The I²C mode supports standard-mode (100kHz) and fast-mode (400kHz) signalling. The device only supports slave mode. The pins SDA/SDIO and SCL/SCLK are used for bi-directional serial data and clock respectively. Signalling rates lower than the standard-mode and fast-mode rates are also supported by the device.

The GN2040 device slave address is 24_h.

The I²C protocol is implemented as per the following description:

Each access begins with a 7-bit I²C slave address word, an 8-bit register address word, followed by one 8-bit data word in a write command, or the device slave address with the read/write bit plus one 8-bit data word in the read command.

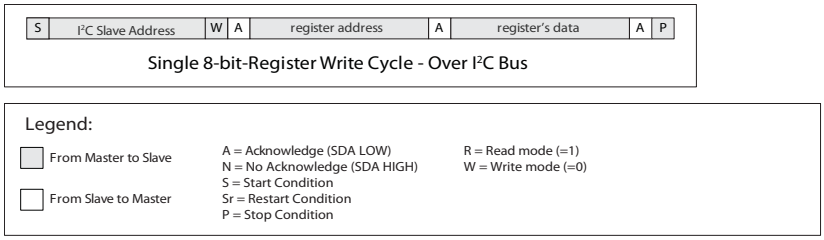


Figure 4-19: Single Register Write Cycle over I²C Bus

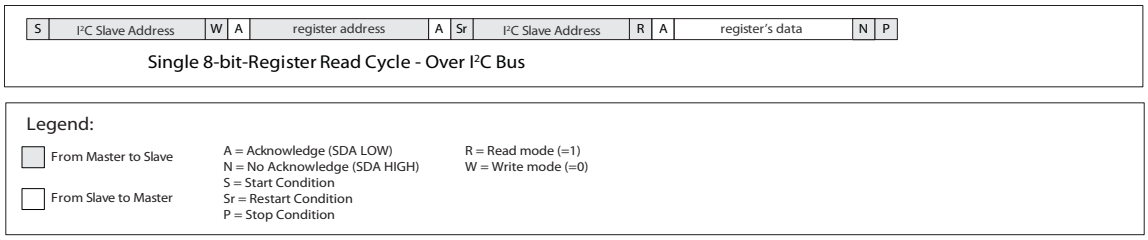


Figure 4-20: Single Register Read Cycle over I²C Bus

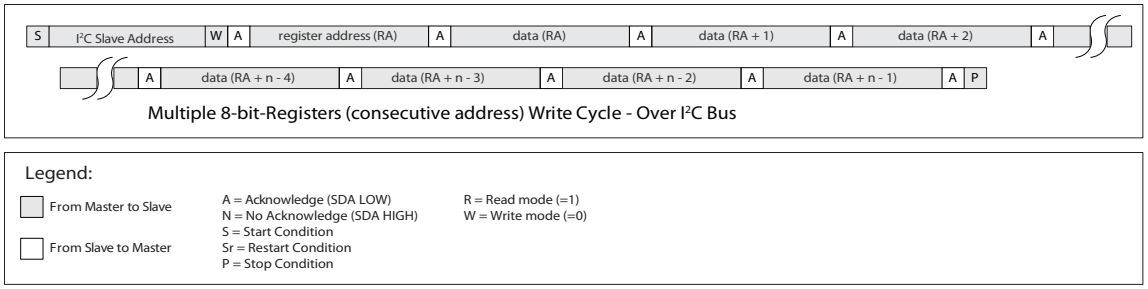


Figure 4-21: Bulk Register Write Cycle over I²C Bus

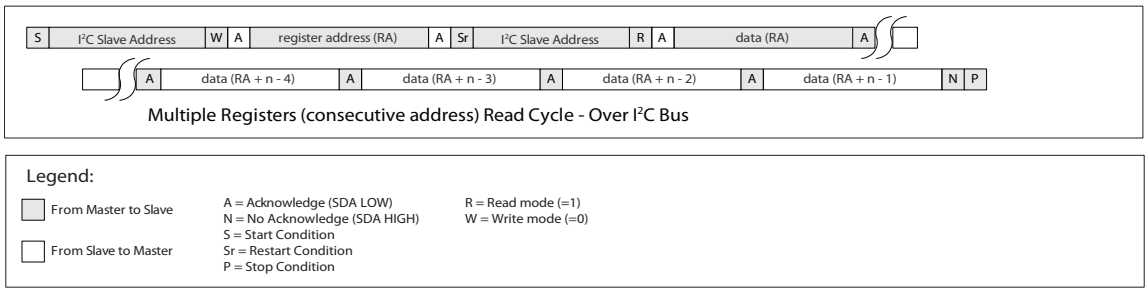


Figure 4-22: Bulk Register Read Cycle over I²C Bus

4.9.2 SPI Host Interface Mode

The GN2040 uses either a 3-wire or a 4-wire SPI protocol. The 3-wire SPI protocol's serial communication takes place via the bi-directional serial data signal (SDA/SDIO). The 4-wire SPI protocol's serial communication uses SSEL/MOSI as its data input and SDA/SDIO as its data output. In both modes, SCL/SCLK is the clock input and $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ is the chip select.

The signalling rate can be up to 10Mb/s. The interface uses 8-bit data and 16-bit address + control.

The 16-bit address + control is made up of an 8-bit address, 1-bit command, 1-bit for auto-increment and 6 unused bits. The 3-wire SPI protocol is implemented as per Figure 4-23 and Figure 4-24. The signal sdo_oen_o is an internal signal indicating the direction of the SDIN_SDOUT pin. When '1', the SDIN_SDOUT pin is configured as an input, when '0', its configured as an output. The 4-wire SPI protocol is implemented as per Figure 4-25.

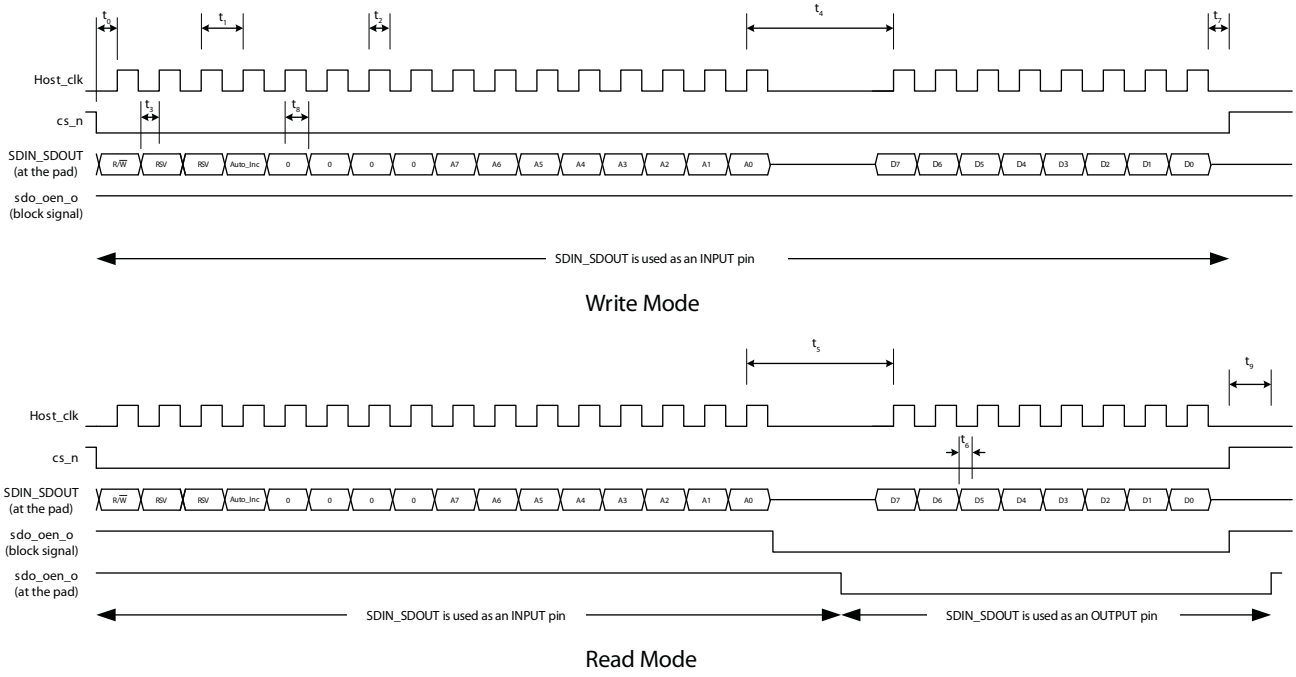


Figure 4-23: SPI Write and Read Timing Diagrams (Single Transaction)

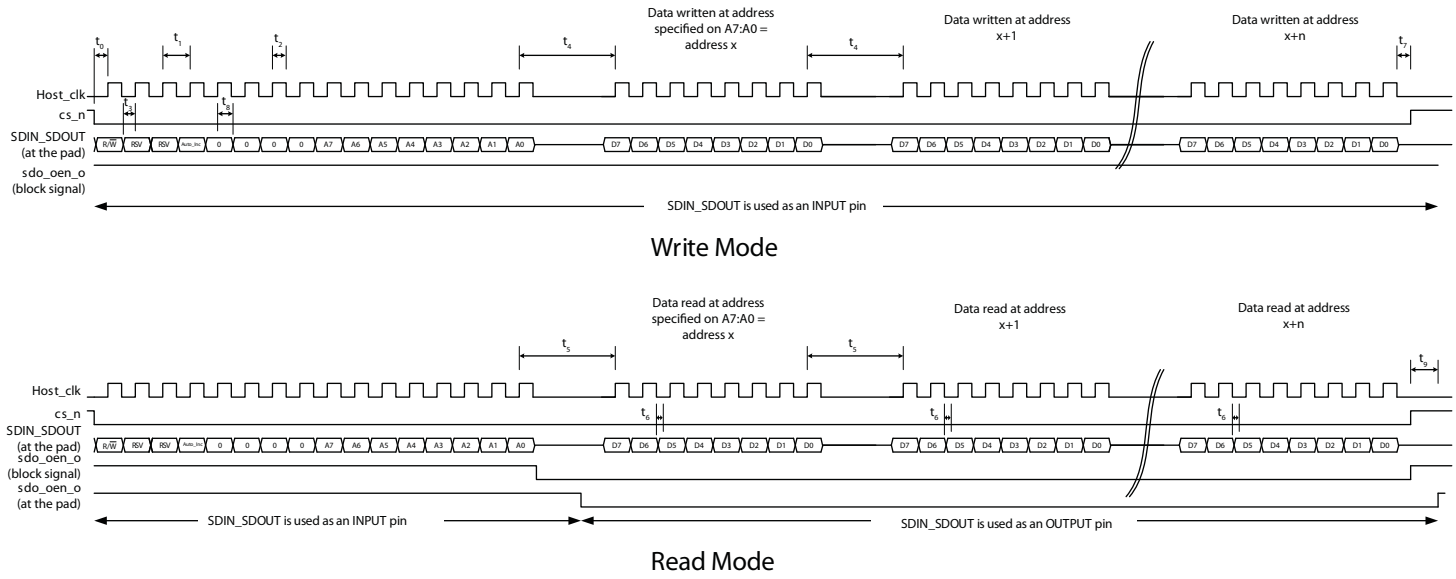


Figure 4-24: SPI Write and Read Timing Diagrams (Auto-Increment Transaction)

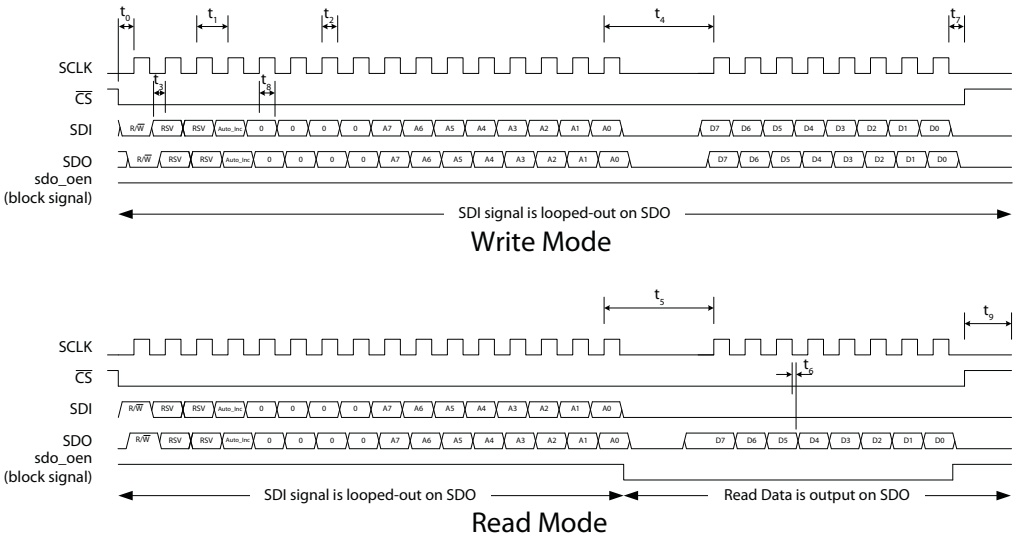


Figure 4-25: SPI Write and Read Timing Diagrams (4-wire)

Table 4-13: SPI Host Interface Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CS_N low before HOST_CLK rising edge	t_0	50% levels; 1.8V operation	1.5	—	—	ns
HOST_CLK period	t_1		100	—	—	ns
HOST_CLK duty cycle	t_2		40	50	60	%
Input data setup time	t_3		1.5	—	—	ns
Time between end of command word (or data in Auto Increment mode) and the first host_clk of the following data word write cycle	t_4		93.5	—	—	ns
Time between end of command word (or data in Auto Increment mode) and the first host_clk of the following data wordread cycle	t_5		420	—	—	ns
Output hold time (15pF load)	t_6		1.5	—	—	ns
CS_N high after last host_clk rising edge	t_7		93.5	—	—	ns
Input data hold time	t_8		1.5	—	—	ns
CS_N high time	t_9		233.6	—	—	ns
CS_N input rise/fall time*	—	20% to 80%	10	—	—	ns

In Figure 4-23, Figure 4-24, and Figure 4-25, CS_N = $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$, HOST_CLK = SCL/SCLK, SDIN_SDOUT = SDA/SDIO, SDI = SSEL/MOSI, and SDO = SDA/SDIO.

There is an auto-increment bit in the command (bit 12) allowing for write burst and read burst transactions.

*The specified minimum rise/fall time must be met to avoid degrading receive sensitivity.

4.9.3 Digital I/O (Schmitt Trigger)

A Schmitt trigger is available on the following signals:

- $\overline{ISEL}/\overline{SCS}$
- SDA/SDIO in input mode
- SCL/SCK in input mode SSEL/MOSI
- SSEL/MOSI

The transfer characteristics of the Schmitt Trigger buffer are shown in Figure 4-26 below:

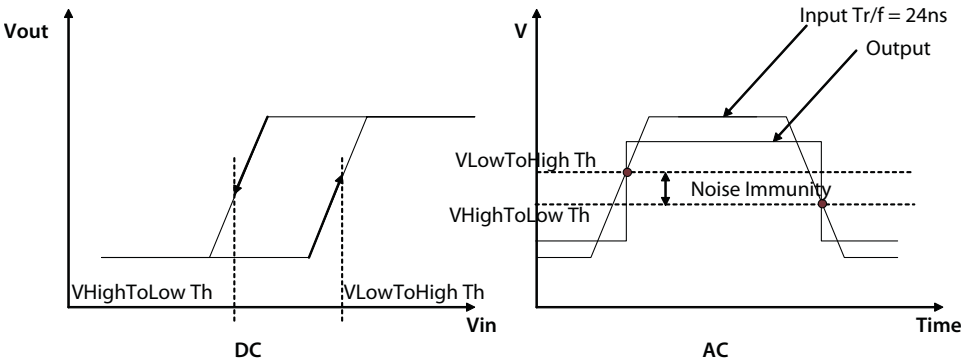


Figure 4-26: Schmitt Trigger Transfer Characteristics

The DC and AC thresholds are shown in Table 2-2: DC Electrical Characteristics.

5. Register Descriptions

Table 5-1: Register Descriptions

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
0	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
1	TOP_REG1	RSVD	7:6	—	0	0-3	Reserved – do not change.
		SPIOUT_OPEN_DRAIN	5:5	RW	0	0-1	0 = Normal SPI operation 1 = Enables SPI output driver open-drain configuration
		RSVD	4:4	—	0	0-1	Reserved – do not change.
		FAULT_MASK_TXLOL	3:3	RW	1	0-1	When HIGH, masks-out TxLOL from asserting FAULT.
		FAULT_MASK_TXLOS	2:2	RW	0	0-1	When HIGH, masks-out TxLOS from asserting FAULT.
		FAULT_MASK_RXLOL	1:1	RW	1	0-1	When HIGH, masks-out RxLOL from asserting FAULT.
		FAULT_MASK_RXLOS	0:0	RW	0	0-1	When HIGH, masks-out RxLOS from asserting FAULT.
2	TOP_REG2	LOSL_MASK_TXLOL	7:7	RW	1	0-1	When HIGH, masks-out TxLOL from asserting LOSL.
		LOSL_MASK_TXLOS	6:6	RW	1	0-1	When HIGH, masks-out TxLOS from asserting LOSL.
		LOSL_MASK_RXLOL	5:5	RW	1	0-1	When HIGH, masks-out RxLOL from asserting LOSL.
		LOSL_MASK_RXLOS	4:4	RW	0	0-1	When HIGH, masks-out RxLOS from asserting LOSL.
		OPEN_DRAIN_FAULT	3:3	RW	1	0-1	When HIGH, makes the FAULT output driver open-drain.
		OPEN_DRAIN_LOSL	2:2	RW	1	0-1	When HIGH, makes the LOSL output driver open-drain.
		POLINV_LOSL	1:1	RW	0	0-1	When HIGH, inverts the polarity of the LOSL output.
		POLINV_FAULT	0:0	RW	0	0-1	When HIGH, inverts the polarity of the FAULT output.
3	TOP_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		PRBS_CHK_CLEAR_ERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from the PRBS Checker.
		PRBS_GEN_START	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts the PRBS Generator.
4	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.
5	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.
6	TOP_REG6	RSVD	7:1	—	0	0-127	Reserved – do not change.
		PRBS_CHK_STATUS	0:0	RO	0	0-1	When HIGH, the PRBS Checker has detected an error.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
7	LOOPBK_REG1	LB_RX_OUT_RX_CLK	7:7	RW	0	0-1	Selects the Rx Clk into the Rx Driver.
		LB_RX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects the PRBS Generator O/P into the Rx Driver.
		LB_RX_OUT_TX_DATA	5:5	RW	0	0-1	Selects the Tx data into the Rx Driver.
		LB_RX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Rx Driver.
		RSVD	3:0	—	0	0-15	Reserved – do not change.
8	LOOPBK_REG2	LB_TX_OUT_TX_CLK	7:7	RW	0	0-1	Selects the Tx Clock into the Tx Driver.
		LB_TX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects the PRBS Generator O/P into the Tx Driver.
		LB_TX_OUT_RX_DATA	5:5	RW	0	0-1	Selects the Rx data into the Tx Driver.
		LB_TX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into Tx Driver.
		RSVD	3:2	—	0	0-3	Reserved – do not change.
		PRBS_CHK_CLK_SEL	1:1	RW	0	0-1	When HIGH, selects the Tx recovered clock. When LOW, selects the Rx recovered clock.
		RSVD	0:0	—	0	0-1	Reserved – do not change.
9	LOOPBK_REG3	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PRBS_GENERATOR_DATA_RATE_CONTROL	5:0	RW	0	0-63	PRBS Generator frequency tuning control. See Section 4.5.1.
10	TXPLL_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TX_PLL_LBW_POS_ADJ	4:0	RW	1110	0-31	Adjusts LBW positive temperature coefficient control. See Section 4.3.2.
11	TXPLL_REG2	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TX_PLL_LBW_NEG_ADJ	4:0	RW	10	0-31	Adjusts LBW negative temperature coefficient control. See Section 4.3.2.
12	RSVD_REG	RSVD	7:0	—	00010010	0-255	Reserved – do not change.
13	RSVD_REG	RSVD	7:0	—	00000101	0-255	Reserved – do not change.
14	TXPLL_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		TX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Tx CDR into bypass mode.
		RSVD	1:1	—	0	0-1	Reserved – do not change.
		TX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.
16	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
17	TXPLL_REG8	TX_JIT_FILT_TRACK_ADJUST	7:3	RW	00010	0-31	Sets the tracking capability when Tx jitter filter mode is enabled. See Section 4.3.3.
		RSVD	2:0	—	101	0-7	Reserved – do not change.
18	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
19	TXPLL_REG10	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		TX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.
20	RXPLL_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		RX_PLL_LBW_POS_ADJ	4:0	RW	11101	0-31	Adjusts LBW positive temperature coefficient control. See Section 4.2.4.
21	RXPLL_REG2	RSVD	7:5	—	0	0-7	Reserved – do not change.
		RX_PLL_LBW_NEG_ADJ	4:0	RW	111	0-31	Adjusts LBW negative temperature coefficient control. See Section 4.2.4.
22	RSVD_REG	RSVD	7:0	—	00010010	0-255	Reserved – do not change.
23	RSVD_REG	RSVD	7:0	—	00000101	0-255	Reserved – do not change.
24	RXPLL_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the CDR into bypass mode.
		RSVD	1:1	—	0	0-1	Reserved – do not change.
		RX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.
26	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
27	RXPLL_REG8	RX_PLL_SONET_IJT_SETTING	7:3	RW	10	0-31	Control for Sonet IJT performance. Used in conjunction with Sonet IJT modes 2 and 3 to set IJT performance. Gradually increase setting for increased margins. See Section 4.2.5.
		RX_PLL_LOCK_DCD_TOL_DIS	2:2	RW	1	0-1	When LOW, enables tolerance of data duty cycle distortion for locking.
		RSVD	1:0	—	1	0-3	Reserved – do not change.
28	RXPLL_REG9	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_PLL_SELECT_HIGH_IJT	3:3	RW	1	0-1	When HIGH, selects high-margin Sonet IJT mode in conjunction with RX_PLL_SONET_IJT_SETTING. See Section 4.2.5.
		RSVD	2:0	—	0	0-7	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
29	RXPLL_REG10	RSVD	7:2	—	0	0-63	Reserved – do not change.
		RX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		RX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.
30	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
31	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
32	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
33	TX_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TX_EQ_BOOST	1:0	RW	11	0-3	Controls the Tx path input equalization setting: 00 = 0dB 01 = 2dB 10 = 4dB 11 = 6dB
34	RSVD_REG	RSVD	7:0	—	111111	0-255	Reserved – do not change.
35	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
36	RSVD_REG	RSVD	7:0	—	101	0-255	Reserved – do not change.
37	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
38	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
39	TX_REG9	TXLOS_TH_NEG	7:0	RW	11011	0-255	Negative temperature coefficient LOS threshold setting. Refer to Section 4.4.2.
40	TX_REG10	TXLOS_TH_POS	7:0	RW	0	0-255	Positive temperature coefficient LOS threshold setting. Refer to Section 4.4.2.
41	TX_REG11	RSVD	7:4	—	0	0-15	Reserved – do not change.
		TXLOS_HYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB.
42	TX_REG12	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TXLOS_FORCE_ASSERT_EN	4:4	RW	0	0-1	When HIGH, LOS is controlled by TXLOS_FORCE_ASSERT.
		TXLOS_FORCE_ASSERT	3:3	RW	0	0-1	Directly sets the state of TXLOS accordingly if TXLOS_FORCE_ASSERT_EN is HIGH.
		RSVD	2:0	—	0	0-7	Reserved – do not change.
45	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
46	RSVD_REG	RSVD	7:0	—	1111	0-255	Reserved – do not change.
47	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
48	RX_REG1	RSVD	7:4	—	111	0-15	Reserved – do not change.
		RXLA_BOOST_MSB	3:0	RW	0	0-15	RXLA boost control bit MSBs. 0 = 0dB to 15 = 14dB

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
49	RX_REG2	RXLA_SLICE_ADJ	7:0	RW	0	0-255	Slice adjust magnitude control.
50	RX_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		RXLA_SLICE_ADJ_LO_RANGE	1:1	RW	0	0-1	Selects slice level adjust point. When LOW, slicing point is option 1. When HIGH, slicing point is option 2. See Section 4.2.2.
		RXLA_SLICE_ADJ_POL	0:0	RW	0	0-1	Slice adjust polarity. When HIGH, slice adjust is positive.
51	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
52	RX_REG5	RSVD	7:1	—	1000	0-127	Reserved – do not change.
		RXLA_MANUAL_SLICE_ADJ_EN	0:0	R/W	0	0-1	When HIGH, enables user to adjust slice level at Rx input. See Section 4.2.2.
53	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
54	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
56	RX_REG9	RXLOS_TH_NEG	7:0	RW	1001001	0-255	Negative tempco LOS threshold setting.
57	RX_REG10	RXLOS_TH_POS	7:0	RW	0	0-255	Positive tempco LOS threshold setting.
58	RX_REG11	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RXLOS_HYS	3:0	RW	1001	0-15	Hysteresis control 0-15 -> 0-6dB. Default 9 = 3dB.
59	RX_REG12	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RXLOS_FORCE_ASSERT_EN	3:3	RW	0	0-1	When HIGH, LOS is controlled by RXLOS_FORCE_ASSERT.
		RXLOS_FORCE_ASSERT	2:2	RW	0	0-1	Directly sets the state of RXLOS accordingly if RXLOS_FORCE_ASSERT_EN is HIGH.
		RXLOS_RANGE	1:0	RW	1	0-3	LOS range: 0 = highest 3 = lowest 2 = (MSB) unused
62	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
63	RX_REG16	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RXLA_BOOST_LSB	2:0	RW	0	0-7	RXLA boost control bit LSBs for fine tuning gain with smaller step size. See Section 4.2.3.
64	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
75	RXSDO_REG1	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_SDO_SWING	3:0	RW	110	0-15	Driver swing: 100mV$_{ppd}$ to 850mV$_{ppd}$, Default = 6 = 400mV$_{ppd}$

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
76	RXSDO_REG2	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_SDO_EMPHASIS	3:0	RW	0	0-15	Driver emphasis control.
77	RXSDO_REG3	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_SDO_PWR_DN_ON_MUTE	2:2	RW	1	0-1	Enables power-down on mute for output stage.
		RX_SDO_AUTO_MUTE_EN	1:1	RW	1	0-1	Enables muting the driver upon LOS.
		RX_SDO_FORCE_MUTE	0:0	RW	0	0-1	Mutes driver to CM when not in auto mute mode.
78	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
79	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
80	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
81	RSVD_REG	RSVD	7:0	—	11110001	0-255	Reserved – do not change.
82	RSVD_REG	RSVD	7:0	—	00000010	0-255	Reserved – do not change.
83	RSVD_REG	RSVD	7:0	—	110	0-255	Reserved – do not change.
84	RSVD_REG	RSVD	7:0	—	110110	0-255	Reserved – do not change.
85	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
86	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
87	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
88	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
89	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
90	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
91	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
92	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
93	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
94	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
95	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
98	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
99	TXSDO_REG25	RSVD	7:6	—	0	0-3	Reserved – do not change.
		TXSDO_PWR_DN_ON_MUTE	5:5	RW	1	0-1	When HIGH, enables power-down on mute for output stage.
		TXSDO_AUTO_MUTE_EN	4:4	RW	1	0-1	When HIGH, enables muting the driver upon LOS.
		TXSDO_FORCE_MUTE	3:3	RW	0	0-1	When HIGH, mutes driver to CM when not in auto mute mode.
		RSVD	2:0	—	0	0-7	Reserved – do not change.
100	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
101	TXSDO_REG27	RSVD	7:4	—	0000	0-15	Reserved – do not change.
		TXSDOSWING	3:0	RW	0110	0-15	Driver swing. 0 to 15 = 100 to 860mV$_{ppd}$. Default = 6 = 400mV$_{ppd}$.
102	TXSDO_REG28	RSVD	7:4	—	0000	0-15	Reserved – do not change.
		TXSDOPOSTTAP	3:0	RW	0000	0-15	Driver post-tap PE control. Default = 0 =1dB. 15 = 6dB.
103	RSVD_REG	RSVD	7:0	—	11000010	0-255	Reserved – do not change.
104	RSVD_REG	RSVD	7:0	—	00000001	0-255	Reserved – do not change.
105	RSVD_REG	RSVD	7:0	—	01010000	0-255	Reserved – do not change.
106	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
107	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
108	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
109	RSVD_REG	RSVD	7:0	—	01000110	0-255	Reserved – do not change.
110	RSVD_REG	RSVD	7:0	—	00110110	0-255	Reserved – do not change.
111	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
112	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
113	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
114	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
115	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
116	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
117	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
118	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
119	RSVD_REG	RSVD	7:0	—	00000000	0-255	Reserved – do not change.
120	RSVD_REG	RSVD	7:0	—	00000000	0-255	Reserved – do not change.
121	ADC_REG0	RSVD	7:4	—	0	0-15	Reserved – do not change.
		ADC_AUTO_CALIBRATION_EN	3:3	RW	1	0-1	1 = Enables Auto ADC Calibration mode 0 = Disables Auto ADC Calibration mode
		ADC_JUST_LSB	2:2	RW	1	0-1	When HIGH, justify towards LSB. When LOW justify towards MSB.
		ADC_AUTO_CONV_EN	1:1	RW	1	0-1	When HIGH, enables auto conversion, set LOW for manual.
		ADC_RESET	0:0	RW	1	0-1	Reset for the ADC.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
122	ADC_REG1	RSVD	7:4	—	0	0-15	Reserved – do not change.
		ADC_SRC_SEL	3:0	RW	0	0-15	Selects ADC source used for measurement: 0000 = ADC reference voltage 0100 = Temperature sensor (vbe@255uA) 0101 = Temperature sensor (vbe@2.55uA) 0111 = V1p8 supply (0.5*v1p8)
123	ADC_REG2	RSVD	7:7	—	0	0-1	Reserved – do not change.
		ADC_CLK_RATE	6:3	RW	11	0-15	ADC clock divide ratio.
		ADC_RESOLUTION	2:0	RWC	11	0-7	ADC resolution control: 0-6 -> 4,6,8,10,12,14,16 bits.
124	ADC_REG3	RSVD	7:1	—	0	0-127	Reserved – do not change.
		ADC_START_CONV	0:0	RWC	0	0-1	ADC start conversion.
125	ADC_REG4	RSVD	7:1	—	0	0-127	Reserved – do not change.
		ADC_DONE_CONV	0:0	RO	0	0-1	ADC conversion done flag.
126	ADC_REG5	ADC_OUT_LO	7:0	RO	0	0-255	ADC output low MSB.
127	ADC_REG6	ADC_OUT_HI	7:0	RO	0	0-255	ADC output high MSB.
128	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
129	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
130	TXPWRDN_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TX_PD_TRDRV_EMPHASIS	4:4	RW	1	0-1	When HIGH, power-down for the Tx trace driver emphasis.
		TX_PD_TRDRV	3:3	RW	0	0-1	When HIGH, power-down for the Tx trace driver.
		RSVD	2:2	—	0	0-1	Reserved – do not change.
		TX_PD_TXCDR	1:1	RW	0	0-1	When HIGH, power-down for the entire Tx CDR.
		TX_PD_TXPATH	0:0	RW	0	0-1	When HIGH, Power-down for the entire Tx path.
131	TXPWRDN_REG2	RSVD	7:2	—	100000	0-63	Reserved – do not change.
		TX_PD_LOS	1:1	RW	0	0-1	When HIGH, power-down for the Tx LOS.
		TX_PD_EQ	0:0	RW	0	0-1	When HIGH, power-down for the Tx input Equalizer.
132	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
133	TXPWRDN_REG4	RSVD	7:1	—	0000111	0-127	Reserved – do not change.
		TX_PD_JIT_FILT	0:0	RW	1	0-1	When HIGH, power-down for the Tx jitter filter.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
134	RXPWRDN_REG1	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_PD_RXSDO_EMPHASIS	3:3	RW	1	0-1	When HIGH, power-down for the trace driver pre-emphasis.
		RX_PD_RXSDO	2:2	RW	0	0-1	When HIGH, power-down for the Rx path trace driver.
		RX_PD_RXCDR	1:1	RW	0	0-1	When HIGH, power-down for the entire Rx CDR.
		RX_PD_PATH	0:0	RW	0	0-1	When HIGH, power-down for the entire Rx path.
135	RXPWRDN_REG2	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_PD_LOS	2:2	RW	0	0-1	When HIGH, power-down for the Rx path LOS.
		RX_PD_SLICE_ADJ	1:1	RW	1	0-1	When HIGH, power-down for the LA slice adjust.
		RX_PD_LA	0:0	RW	0	0-1	When HIGH, power-down for the Rx path LA.
136	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
137	RXPWRDN_REG4	RSVD	7:1	—	111	0-127	Reserved – do not change.
		RX_PD_SONET_IJT	0:0	RW	0	0-1	When HIGH, powers-down the Rx path Sonet IJT feature to save power.
138	RSVD_REG	RSVD	7:0	—	00011111	0-255	Reserved – do not change.
139	PWRDN_REG2	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PD_ADC	5:5	RW	1	0-1	When HIGH, power-down for the ADC.
		PD_SUPPLY_SENSOR	4:4	RW	1	0-1	When HIGH, power-down for the supply sensor.
		PD_TEMP_SENSOR	3:3	RW	1	0-1	When HIGH, power-down for the temperature sensor(s).
		PD_PRBS_CHK	2:2	RW	1	0-1	When HIGH, power-down for the PRBS Checker and associated buffers.
		PD_PRBS_GEN	1:1	RW	1	0-1	When HIGH, power-down for the PRBS Generator and associated buffers.
		RSVD	0:0	—	1	0-1	Reserved – do not change.
140 to 153	RSVD_REG	RSVD	All	—	0	0-255	Reserved – do not change.
154	TXLBW_REG1	RSVD	7:1	—	0	0-127	Reserved – do not change.
		TX_DYN_LBW_ENABLE	0:0	RW	1	0-1	Tx dynamic loop bandwidth block enable: 0 = disabled 1 = enabled
155	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.
156	RSVD_REG	RSVD	7:0	—	00000011	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
157	RSVD_REG	RSVD	7:0	—	00011111	0-255	Reserved – do not change.
158	RSVD_REG	RSVD	7:0	—	00000100	0-255	Reserved – do not change.
159	RXLBW_REG1	RSVD	7:1	—	0	0-127	Reserved – do not change.
		RX_DYN_LBW_ENABLE	0:0	RW	1	0-1	Rx dynamic loop bandwidth block enable: 0 = Disabled 1 = Enabled
160 to 221	RSVD_REG	RSVD	All	—	0	0-255	Reserved – do not change.

6. Applications Information

6.1 Typical Application Circuit

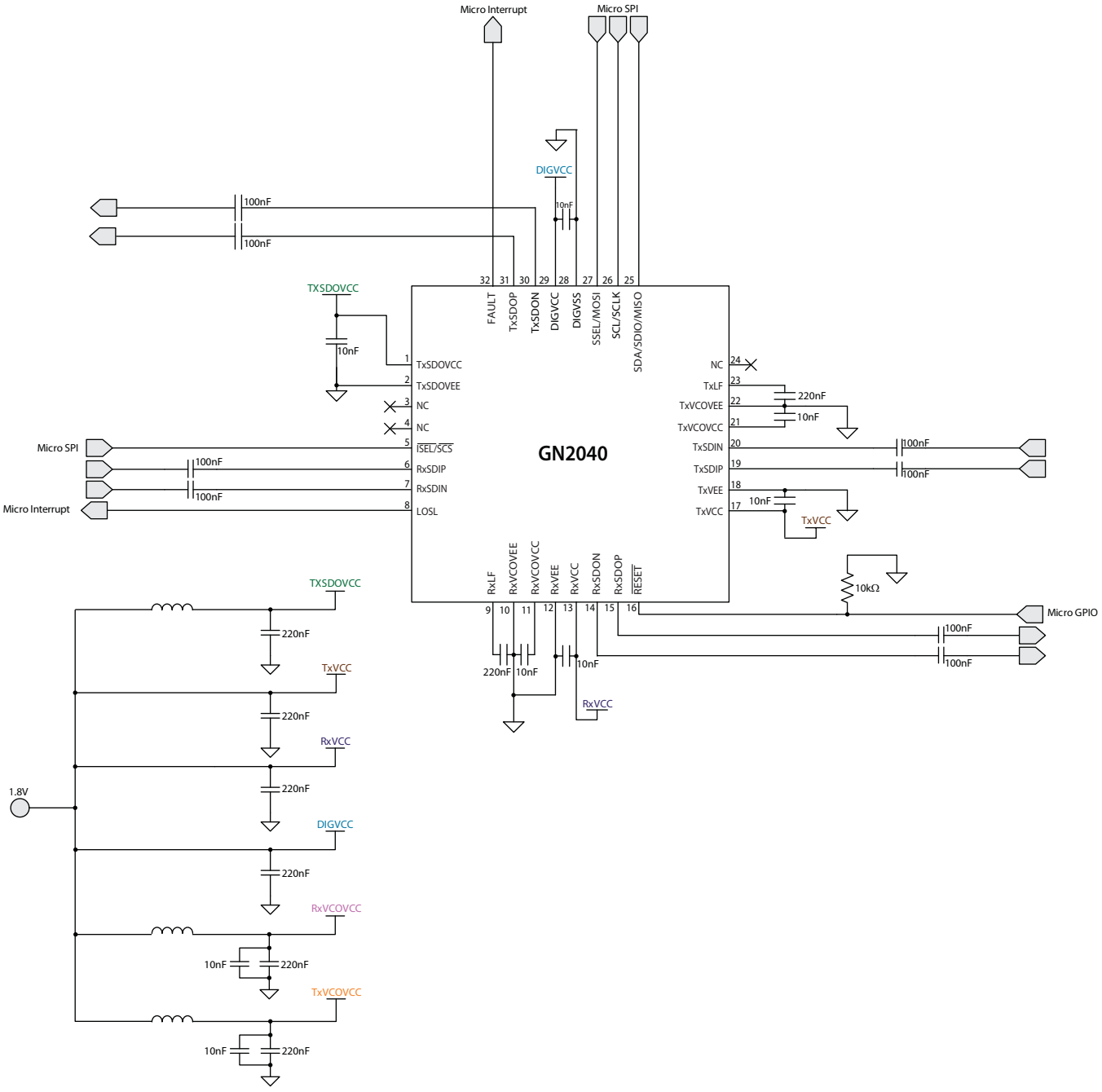


Figure 6-1: Typical Application Circuit

- Use high-quality, temperature-stable LF capacitors. For example, silicon, tantalum or C0G dielectric ceramic capacitors. Lower quality capacitors such as X7R are more sensitive to environmental conditions and may not perform adequately across conditions for this node. Silicone conformal coating can be used with such capacitors as an effective way to mitigate environmental sensitivity

  Note: Please refer to the document "Preventing Loop Filter Capacitor Leakage Current" (PDS-060519) for more information.

- Place lowest value decoupling capacitor closest to the device
- Component values for the TOSA interface must be optimized for the TOSA type
- Status indicator connections are shown for a LVCMOS/LVTTL compatible mode. These I/Os can be configured as open-drain with pull-up
- Host interface is shown configured for SPI mode. I^2C mode is also supported

6.2 Power Supply Filter Recommendations

RC filters for isolating supplies are not recommended due to the large currents drawn from each supply.

- The Tx and Rx VCOs do not have independent supplies; additional filtering for the VCOs is not required

For improved isolation between the Tx and Rx paths, and to achieve the best Rx sensitivity and Tx jitter generation, a supply filter such as the one shown in Figure 6-2 is recommended.

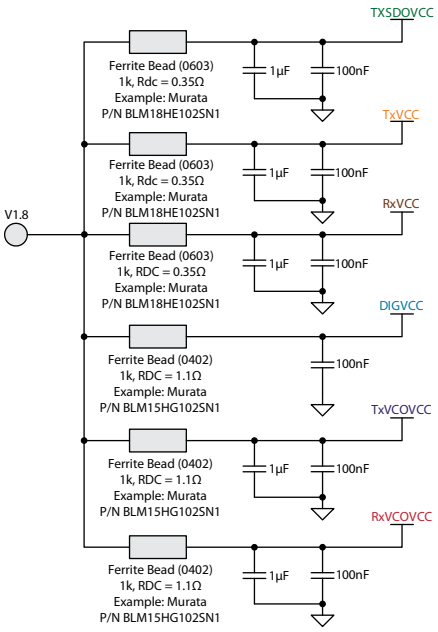


Figure 6-2: Power Supply Filter Recommendations

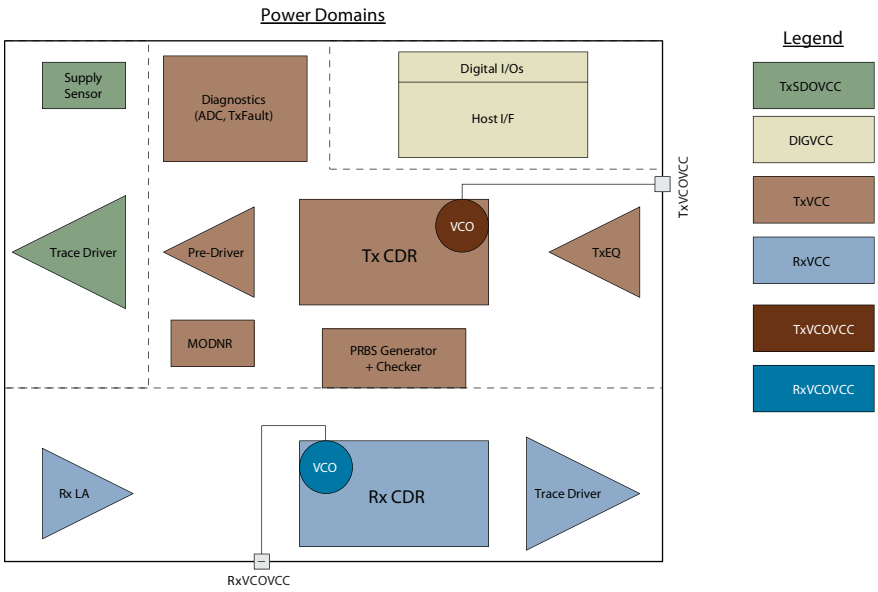


Figure 6-3: Power Supply Domains

6.3 Layout Considerations

The following high-frequency design rules should be considered to achieve optimum performance of the GN2040:

- Use carefully designed controlled-impedance transmission lines with minimal local discontinuities for all high-speed data signals
- Place decoupling capacitors as close as possible to the supply pins
- For optimal electrical and thermal performance, the QFN's exposed pad should be soldered to the module ground plane
- It is recommended to have LF cap ground and VCO caps ground to be common with multiple stitching of vias to ground. Capacitors should be placed from smallest value to largest value away from chip. In addition, the connection from the LF pin to the capacitor should be as small as possible with no vias. Figure 6-4 below demonstrates this technique:

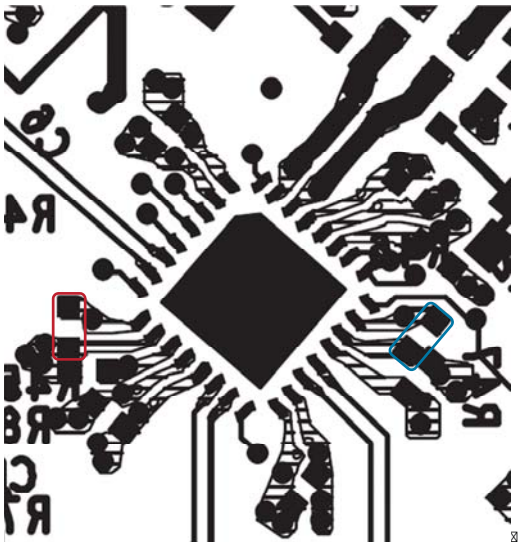


Figure 6-4: Loop Filter Capacitor PCB Layout

- All supply decoupling capacitors should have multiple vias to ground/power planes, and placed as close to chip as possible
- All supplies/grounds should be routed to corresponding decoupling capacitors pads, and never to the centre pad
- The recommended PCB layout for the GN2040 device is shown in Figure 7-2
- Use high-quality, temperature-stable LF capacitors (i.e. capacitors connected to pins 9 and 23). For example: X7R or C0G dielectrics for ceramic capacitors. Lower-quality capacitors with smaller package sizes (e.g. 0201) are more sensitive to environmental conditions and may not perform adequately across conditions for this node. Silicone conformal coating is also an effective way to mitigate environmental sensitivity

7. Package and Ordering Information

7.1 Package Dimensions

The GN2040 is a 5mm x 5mm, 32-pin QFN.

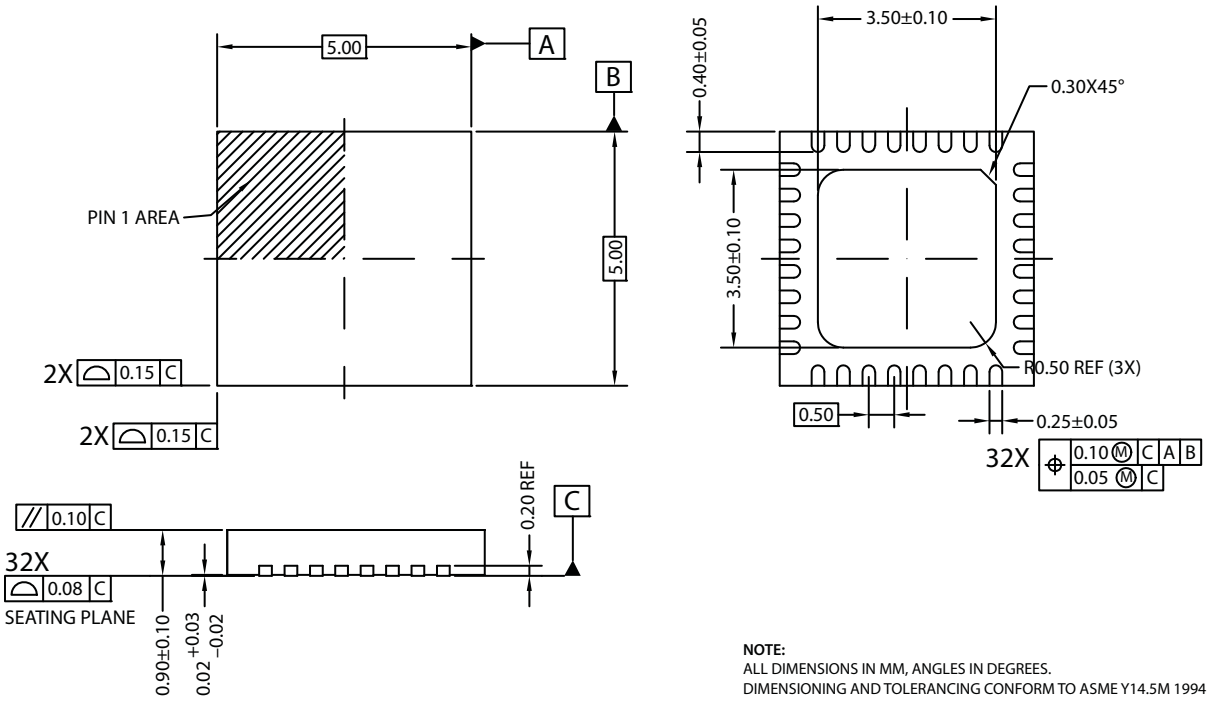
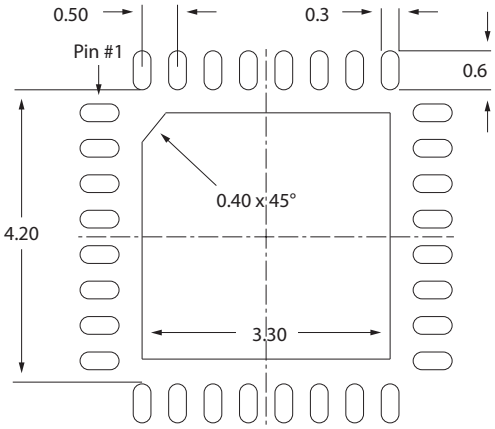


Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint



Notes:
1. All dimensions in mm.
2. Drawing not to scale.
3. 16 thermal relief pins, evenly spaced on centre paddle, connected to ground plane.
4. Drill size: 0.254mm.

Figure 7-2: Recommended PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	32-pin QFN / 5mm x 5mm / 0.5mm pad pitch
Moisture Sensitivity Level	1
Junction to Case Thermal Resistance, θ_{j-c}	17.8°C/W
Junction to Air Thermal Resistance (at zero airflow), θ_{j-a}	26.4°C/W
Psi = Junction-to-Top (of Package) Characterization Parameter, Ψ	0.4°C/W
Pb-free and RoHS compliant	Yes

7.4 Solder Reflow Profile

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 7-3.

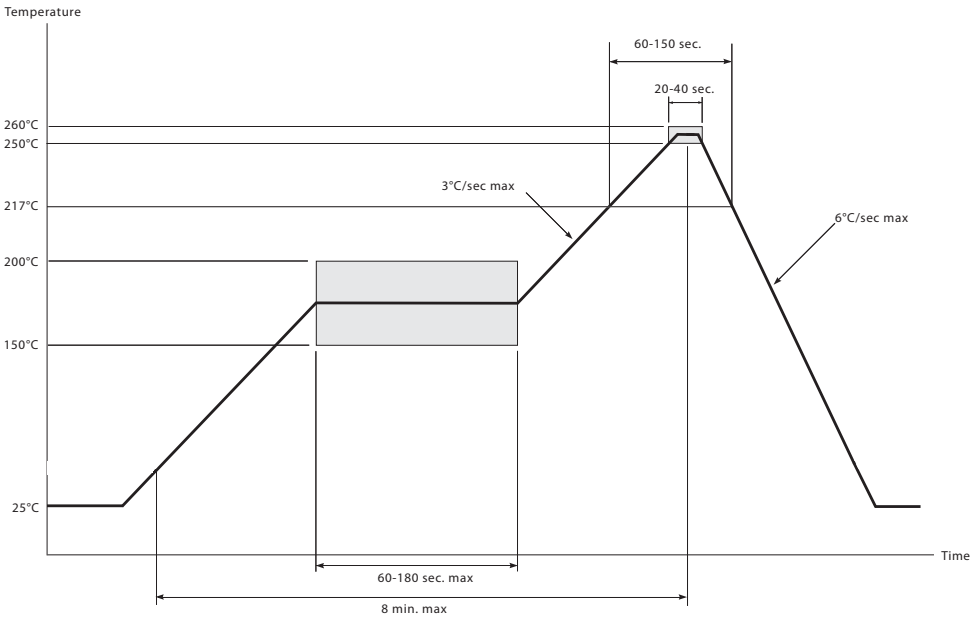


Figure 7-3: Maximum Pb-free Solder Reflow Profile

7.5 Marking Diagram

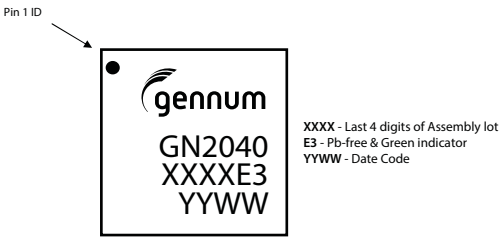


Figure 7-4: Marking Diagram

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Package	Case Temperature Range
GN2040-INE3	32-pin QFN	-40°C to +100°C
GN2040-INTE3D	32-pin QFN (500pc tape and reel)	-40°C to +100°C

DOCUMENT IDENTIFICATION
FINAL DATA SHEET
The product is in production. Semtech reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

GN2042

Dual-CDR Multi-Rate Transceiver with DML Driver

Features

- Dual CDR with 9.8 to 11.3Gb/s reference-free operation and integrated DFB/FP laser driver
- Low power to enable SFP+ <1W 10km SONET modules:
  - GN2042 + TOSA power = 552mW typical at 35mA bias and 35mA modulation
- Integrated Jitter Filter to ensure robust jitter generation performance and compliance to the OC192 standards
- APC loop improvements, including:
  - High dynamic range photo diode current detector
- Integrated limiting amplifier with typical sensitivity of 2.5mV
- Digital control through I^2C or SPI interface
- Programmable Jitter Transfer bandwidth
- Bi-directional loopback
- Highly configurable, including the following programmable features:
  - Limiting Amplifier Equalization
  - Transmit Input Equalization (adjustable)
  - Input Slice Level Adjust
  - LOS with adjustable threshold and hysteresis
  - Tx Fault signalling
  - Polarity invert and mute in both directions
  - Output emphasis
- Integrated analog to digital converter, which provides access to digital diagnostic information on supply voltage, die temperature, laser bias current, transmit optical power, modulation current, biasing current, etc.
- Dual 1.8V / 3.3V supplies (+5%/-15% for 3.3V, +5%/-11% for 1.8V)
  1.8V to be provided by fixed regulator output
- Integrated laser safety features
- 5mm x 5mm 32-pin QFN package
- -40°C to 100°C case operation

Applications

- XFP & SFP+ 10Gb/s SONET optical transceivers
- XFP & SFP+ 10GBase-LR optical transceivers

General Description

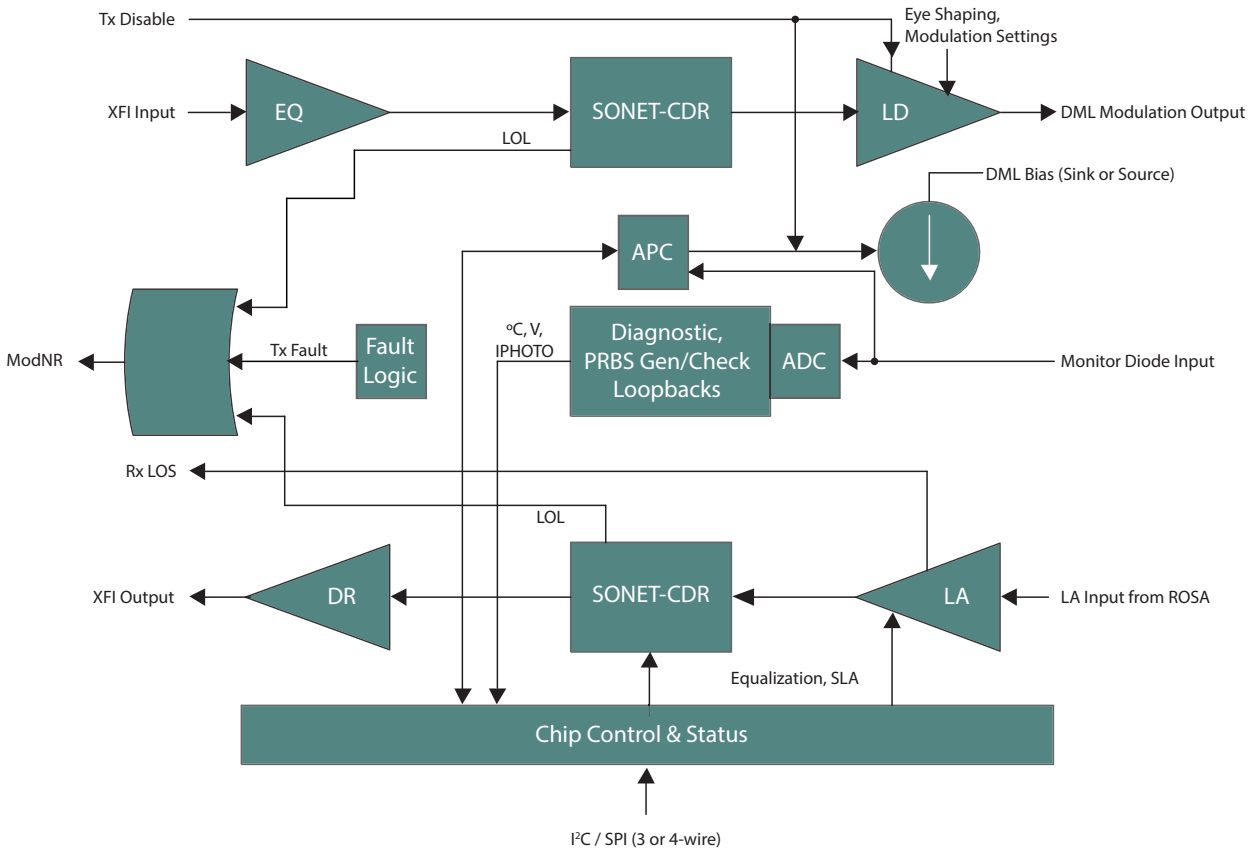
The GN2042 is an integrated bi-directional CDR, DFB/FP laser driver and limiting amplifier designed specifically to enable low power SFP+ re-timed modules for SONET. Based on the Semtech ClearEdge™ technology, the GN2042 delivers best in class eye quality.

In addition to enabling lower power modules, the GN2042 offers a selectable jitter filter to ensure compliance to difficult to meet jitter generation specifications. The GN2042 also features an improved APC loop with extended dynamic range and increased resolution to support a wide variety of TOSAs.

The transmit path consists of optional input equalization, a multi-rate Tx CDR, and a DFB laser driver. The receive path is comprised of a limiting amplifier with programmable equalization, a multi-rate Rx CDR, and output emphasis. Both transmit and receive directions offer highly configurable eye shaping features, which allow for optimal electrical and optical outputs. Both directions also offer the option for polarity-invert, loopback and output mute.

The GN2042 has an integrated analog to digital converter, which through the serial interface, provides digital diagnostic information on supply voltage, die temperature, laser bias current, and transmit optical power. The GN2042 also offers integrated laser safety features.

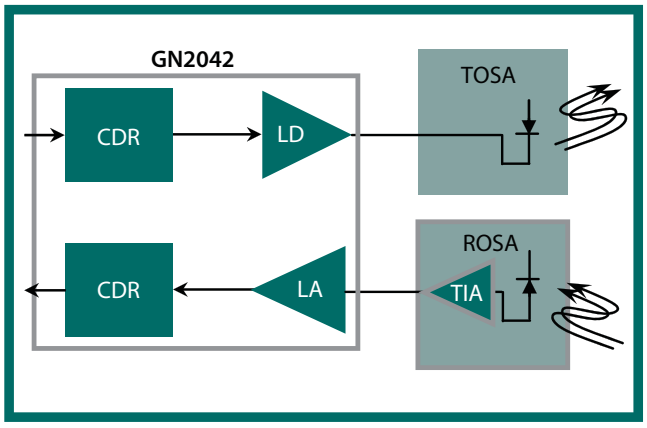
By integrating the laser driver, the GN2042 offers an extremely low-power solution for DML based optical modules. It consumes only 552mW typical from a 3.3V supply and a 1.7V supply, with the laser driver biased at 35mA bias current and 35mA modulation current.



GN2042 Functional Block Diagram

DFB Laser Driver Features

- Low power DML driver
- Laser bias current up to 120mA
- Option for source or sink bias current
- Modulation current into differentially-driven 25Ω TOSA up to 80mA peak-to-peak
- 2x 25Ω single-ended terminations
- Transmitter disable pin
- Crossing point adjustment
- Jitter Optimization with Phase Adjust feature
- Optional on-chip APC loop
- Programmable Tx Fault signalling



Typical Usage - XFP or SFP+ 1310nm Optical Module

Revision History

Version	ECO	Date	Changes and / or Modifications
2	025196	April 2015	Updated Data Rate parameter in Table 2-5: AC Electrical Characteristics.
1	021595	November 2014	Converted document to Final Data Sheet. Updates to Electrical Characteristics. Added Power Dissipation and Power Features sections.
0	018871	May 2014	Converted document to Preliminary Data Sheet. Reformatted document template. Updates to Table 2-2: DC Electrical Characteristics and Table 2-5: AC Electrical Characteristics.
B	014450	July 2013	Updates: Added content to Detailed Description and Register Descriptions.
A	158538	October 2012	New document.

Contents

1. Pin Out

1.1 Pin Assignment

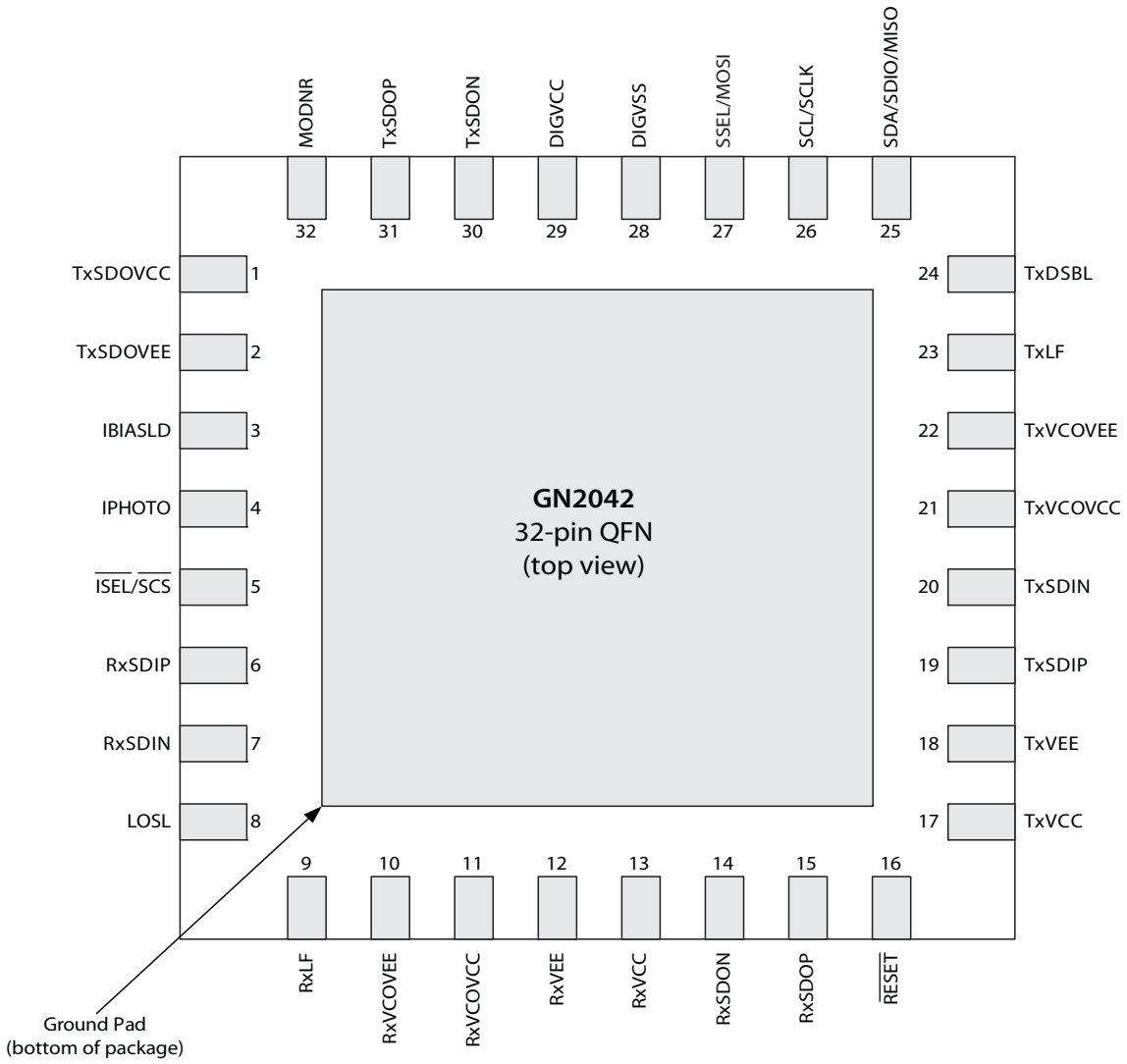


Figure 1-1: Pin Assignment

1.2 Pin Description

Table 1-1: Pin Description

Pin #	Name	Type	Description
1	TxSDOVCC	Power	3.3V power supply for the transmit signal path output.
2	TxSDOVEE	Ground	Ground for the transmit signal path output.
3	IBIASLD	Analog Output	Current sink/source output for the external laser DC bias.
4	IPHOTO	Analog Input	Photodiode monitor current input. Photodiode current is sensed at the IPHOTO pin. IPHOTO can be configured to sink or source photodiode current, when the photodiode is referenced from a positive supply.
5	$\overline{\text{ISEL}}/\overline{\text{SCS}}$	Digital Input	Digital active-low 1.8V – 3.3V LVCMOS-compatible, Schmitt-triggered input. $\overline{\text{ISEL}}/\overline{\text{SCS}}$ selects the host interface mode during a device reset: • When LOW or left unconnected, this pin selects I^2C host interface mode • When HIGH, this pin selects SPI host interface mode After device reset, $\overline{\text{ISEL}}/\overline{\text{SCS}}$ becomes an active-low chip-select pin in SPI host interface mode. $\overline{\text{ISEL}}/\overline{\text{SCS}}$ is not used in I^2C host interface mode after device reset.
6, 7	RxSDIP, RxSDIN	Input	High-speed input for the receive signal path.
8	LOSL	Digital Output	1.8V – 3.3V LVCMOS-compatible active-high open-collector digital output requires an external pull-up resistor. Reconfigurable as a 1.8V-compliant LVCMOS output without external pull-up resistor. Loss-of-Signal/Loss-of-Lock Indicator. When LOSL is LOW, the transmit and receive signal paths are operating properly. When LOSL is high-impedance, the device has detected a condition that indicates invalid data in the transmit and/or receive signal paths. It consists of a logical OR of the following signals: • Receive signal path CDR Loss of Signal (included by default) • Receive signal path CDR Loss of Lock (masked by default) • Transmit signal path CDR Loss of Signal (masked by default) • Transmit signal path CDR Loss of Lock (masked by default) Loss-of-signal/loss-of-lock inputs from either signal path can be masked or enabled.
9	RxLF	Passive	Loop filter capacitor connection for the receive signal path.
10	RxVCOVEE	Ground	Ground for the receive signal path VCO.
11	RxVCOVCC	Power	1.8V power supply for the receive signal path VCO.
12	RxVEE	Ground	Ground for the receive signal path and output.
13	RxVCC	Power	1.8V power supply for the receive signal path and output.
14, 15	RxSDON, RxSDOP	Output	High-speed differential output for the receive signal path.

Table 1-1: Pin Description (Continued)

Pin #	Name	Type	Description
16	$\overline{\text{RESET}}$	Digital Input	Digital active-low 1.8V – 3.3V LVCMOS-compatible input. Device reset control pin. This is an active pull-down. It is recommended that $\overline{\text{RESET}}$ be pulled down by an external 10kΩ resistor and be driven by the Micro on the module.
17	TxVCC	Power	1.8V power supply for the transmit signal path.
18	TxVEE	Ground	Ground for the transmit signal path.
19, 20	TxSDIP, TxSDIN	Input	High-speed input for the transmit signal path.
21	TxVCOVCC	Passive	1.8V power supply for the transmit signal path VCO.
22	TxVCOVEE	Ground	Ground for the transmit signal path VCO.
23	TxLF	Passive	Loop filter capacitor connection for the transmit signal path.
24	TxDSBL	Digital Input	Digital active-high 1.8V – 3.3V LVCMOS-compatible input. When left unconnected or held HIGH, this pin disables the transmit signal path high-speed differential output and the laser DC bias current. When held LOW, the transmit signal path and laser DC bias outputs behave normally. Includes a weak internal pull-up current to disable the laser DC bias current, should this pin be externally disconnected.
25	SDA/SDIO/MISO	Digital Input/ Output	Digital active-high serial data signal for the host interface. Schmitt triggered in input mode. Bi-directional, I^2C-compliant, open-drain driver/receiver in I^2C host-interface mode. Bi-directional, 1.8V LVCMOS-compliant driver/receiver in 3-wire SPI host-interface mode. 1.8V LVCMOS-compliant active-high output driver in 4-wire SPI host-interface mode.
26	SCL/SCLK	Digital Input/ Output	Digital active-high clock input signal for the serial host interface. Schmitt triggered in input mode. Bi-directional, I^2C-compliant, open-drain driver/receiver in I^2C host-interface mode (SCL). 1.8V LVCMOS-compliant input in either SPI host-interface mode (SCLK).
27	SSEL/MOSI	Digital Input	Digital active-high 1.8V – 3.3V LVCMOS-compliant Schmitt-triggered input. SSEL selects the SPI port style when SPI host interface mode is selected: • When LOW or left unconnected during device reset, this pin selects 3-wire SPI host interface mode • When HIGH during device reset, this pin selects 4-wire SPI host interface mode on device power on or reset Following device reset, SSEL/MOSI is an active-high SPI-compliant receiver. SSEL/MOSI is not used in I^2C host interface mode.
28	DIGVSS	Ground	Ground for the low-speed digital I/O and internal logic.
29	DIGVCC	Power	1.8V power supply for the low-speed digital I/O.

Table 1-1: Pin Description (Continued)

Pin #	Name	Type	Description
30, 31	TxSDON, TxSDOP	Output	High-speed differential output for the transmit signal path. Use TxSDOP to drive the EML TOSA.
32	MODNR	Digital Output	1.8V – 3.3V LVCMOS-compliant active-high open-collector digital output requires an external pull-up resistor. Reconfigurable as a 1.8V-compliant LVCMOS output without external pull-up resistor. Module Not Ready Indicator. When MODNR is LOW, the transmit and receive signal paths are operating properly. When MODNR is high-impedance, the device has detected a condition that indicates invalid data in the transmit and/or receive signal paths. It consists of a logical OR of the following signals: • Transmit signal path CDR Loss of Lock • Transmit signal path CDR Loss of Signal • Transmitter Laser Fault • Receive signal path CDR Loss of Lock • Receive signal path CDR Loss of Signal

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
3.3V Supply Voltage	-0.5 to +3.6V_{DC}
1.8V Supply Voltage	-0.5 to +2.1V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_A < 125°C
Input Voltage Range (any input pin except Tx and Rx SDI pins)	-0.3 to ($V_{CC\_3.3V}$ + 0.3)V_{DC}
Input Voltage Range (Tx and Rx SDI pins)	-0.3 to ($V_{CC\_1.8V}$ + 0.3)V_{DC}
Solder Reflow Temperature (3 seconds)	260°C

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

$V_{CC\_3.3}$ = +2.8V to +3.47V, $V_{CC\_1.8}$ = 1.6V to 1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31 data. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Power	Bias/Mod Current = 0mA/0mA. Jitter filter mode off		—	262	306	mW	
	Bias/Mod Current = 35mA/35mA. Jitter filter mode off		—	552	595	mW	1
	Bias/Mod Current = 60mA/60mA. Jitter filter mode off		—	757	801	mW	
$\overline{\text{RESET}}$ Input Specifications							
Input Low Voltage		V_{IL}	0	—	0.8	V	—
Input High Voltage		V_{IH}	1.2	—	$V_{CC\_3.3}$	V	—
Input Low Current	V_{IL} = 0V	I_{IL}	—	-100	—	µA	—
Input High Current	V_{IH} = 3.3V	I_{IH}	—	100	—	µA	—

Table 2-2: DC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.8V to +3.47V, $V_{CC\_1.8}$ = 1.6V to 1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31 data. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Schmitt Trigger Thresholds ($\overline{ISEL}$/$\overline{SCS}$, SDA/SDIO/MOSI, SCL/SCLK, SSEL/MOSI)							
DC Low-to-High Threshold	V_{CC} = 1.9V		0.93	1.05	1.16	V	2
DC High-to-Low Threshold			0.51	0.70	0.85	V	2
DC Low-to-High Threshold	V_{CC} = 1.8V		0.88	0.99	1.13	V	3
DC High-to-Low Threshold			0.41	0.67	0.77	V	3
DC Low-to-High Threshold	V_{CC} = 1.7V		0.83	0.94	1.07	V	—
DC High-to-Low Threshold			0.36	0.59	0.73	V	—
AC Low-to-High Threshold	$V_{CC\_1.8}$ = 1.7V or $V_{CC\_3.3}$ = 2.8V		0.76	0.91	1.06	V	—
AC High-to-Low Threshold			0.44	0.57	0.69	V	—
AC Low-to-High Threshold	$V_{CC\_1.8}$ = 1.9V or $V_{CC\_3.3}$ = 3.46V		0.93	1.06	1.19	V	—
AC High-to-Low Threshold			0.70	0.82	0.93	V	—
Status Indicator Output Specifications (LOSL, MODNR)							
Indicator Output Logic LOW	I_{SINK}(max) = 3mA	V_{OL}	—	0.2	0.4	V	—
Rx Side Specification							
Input Termination (RxSDIP/N)	Differential		80	100	120	Ω	—
Output Termination (RxSDOP/N)	Differential		80	100	120	Ω	—
Tx Side Specification							
Input Termination (TxSDIP/N)	Differential		80	100	120	Ω	—
Output Termination (TxSDOP/N)	Single-ended		—	25	—	Ω	—
Maximum Laser Modulation Current	AC-coupled, differentially-driven load, VCC_1.8 > 1.7V		75	90	—	mA_{pp}	—
	AC-coupled, differentially-driven load, VCC_1.8 ≤ 1.7V		50	60	—	mA_{pp}	—
Maximum Laser Bias Current			120	—	—	mA	—

Table 2-2: DC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.8V to +3.47V, $V_{CC\_1.8}$ = 1.6V to 1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31 data. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
IPHOTO Range	Minimum setting		—	0.025	—	mA	4
	Maximum setting		—	2	—	mA	
TxDSBL, Input HIGH		V_{IH}	1.2	—	V_{CC} + 0.3	V	—
TxDSBL, Input LOW		V_{IL}	-0.3	—	0.7	V	—

Notes:

1. Each output terminated. Includes chip and TOSA power. Typical power is specified at $V_{CC\_1.8}$ = 1.7V and $V_{CC\_3.3}$ = 3.3V. Maximum power is specified at $V_{CC\_1.8}$ = 1.8V and $V_{CC\_3.3}$ = 3.3V.
2. Typical Noise Immunity = 0.34V.
3. Typical Noise Immunity = 0.43V.
4. Can be configured to sink or source photodiode current at the IPHOTO pin when the photodiode is referenced from a positive supply.

2.2.1 Power Dissipation

Table 2-3: Power Dissipation

$V_{CC\_1.8}$	$V_{CC\_3.3}$	Bias Current	Modulation Current	$V_{CC\_1.8}$ Current	$V_{CC\_3.3}$ Current	Total Current	Total Power
V	V	mA	mA	mA	mA	mA	mW
1.6	2.8	0	0	150	0	150	239
1.6	2.8	35	35	150	88	238	484
1.6	2.8	60	60	150	150	300	659
1.7	3.3	0	0	154	0	154	262
1.7	3.3	35	35	154	88	242	552
1.7	3.3	60	60	154	150	304	757
1.8	3.3	0	0	158	0	158	286
1.8	3.3	35	35	158	88	246	575
1.8	3.3	60	60	158	150	308	781

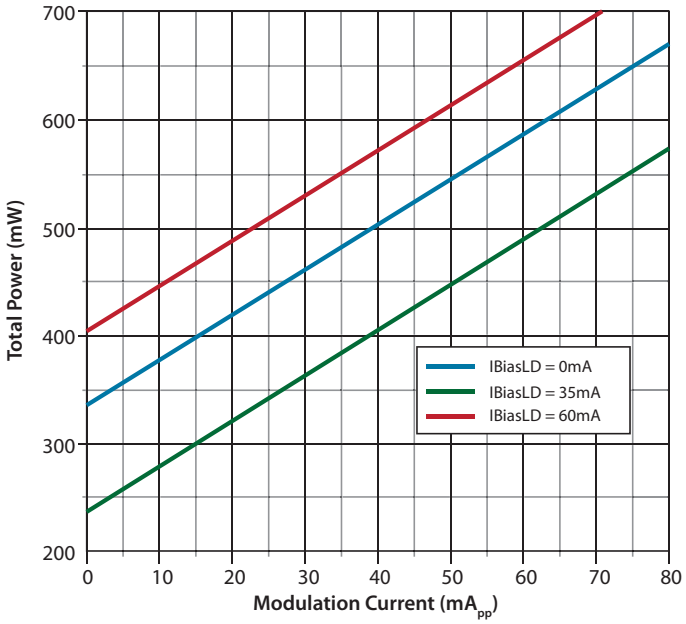


Figure 2-1: Typical Total Power vs. Modulation and Bias Current for 1.6V/2.8V Setting

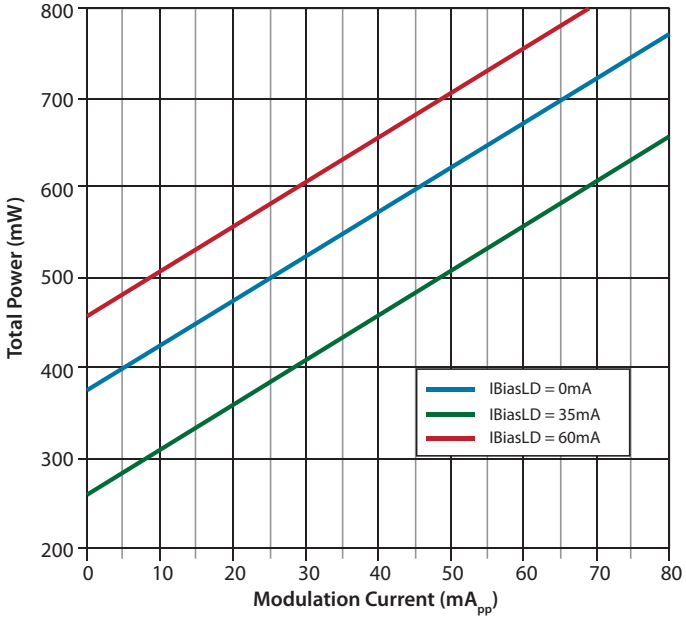


Figure 2-2: Typical Total Power vs. Modulation and Bias Current for 1.7V/3.3V Setting

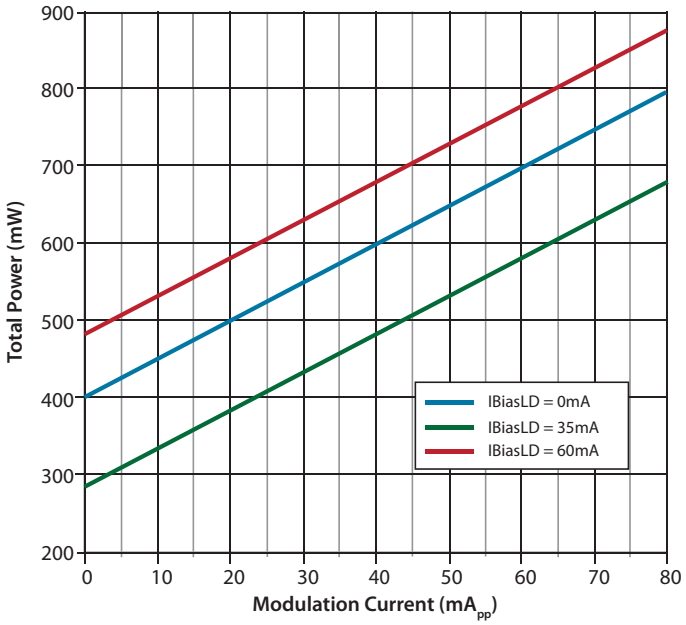


Figure 2-3: Typical Total Power vs. Modulation and Bias Current for 1.8V/3.3V Setting

2.2.2 Power Features

Table 2-4: Power Features

Feature	Description	Typical Baseline Power (mW)	Typical Delta Power (mW)
Base Power	**Mod = 60mA, Bias = 60mA**	**757**	
Incremental Power Features			
LA Boost at Maximum			0
Slice Adjust at Maximum			12.3
PRBS7 Generator	Path for PRBS7 Generator to RxSDO is on		40
PRBS7 Checker	PRBS7 Checker is on		56
Diag + ADC	Temperature, Supply Sensor, ADC		7.6
LD CPA at Maximum	Laser Driver Crossing Point Adjust is at maximum		10.3
LD Jitter Optimization with Phase Adjust at Maximum	Jitter optimization through phase adjust is enabled for laser driver		18.8
LD Rise Pre-emphasis at Maximum Setting			27.4
Tx Jitter Filter Mode Enabled	Tx jitter filter tracking capability set to maximum		9.5
Rx Swing at Maximum			122.7
Power Saving Features			
with Rx CDR Bypassed and Powered-down			-64.1
with Rx and Tx CDR Bypassed and Powered-down			-124.7
with Rx Path Powered-down			-103.6
RxSDO Muted			-25.1
TxSDO Muted			-344.4
Rx IJT Mode 1			-18.5
Rx IJT Mode 2			-15

2.3 AC Electrical Characteristics

Table 2-5: AC Electrical Characteristics

$V_{CC\_3.3}$ = +2.8V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Data Rate	Default configuration, $V_{CC\_1.8V} \geq 1.71V$		9.8	10.3125	11.35	Gb/s	—
	Default configuration, $V_{CC\_1.8V} < 1.71V$		9.8	10.3125	11.3	Gb/s	—
Rx Side Specification							
Input Sensitivity			—	2.5	8	mV_{ppd}	—
Input Overload			1200	—	—	mV_{ppd}	—
Limiting Amplifier Equalization	Maximum EQ setting		14	—	—	dB	1
Input Sinusoidal Jitter Tolerance	f = 100kHz		20	30	—	UI_{pp}	2, 3
	f = 400kHz		2.5	8	—	UI_{pp}	3
	f = 4MHz		0.5	1.4	—	UI_{pp}	3
	f = 80MHz		0.3	0.5	—	UI_{pp}	3
Jitter Transfer Bandwidth Setting Range	Minimum programmable setting		—	2.2	—	MHz	—
	Maximum programmable setting		—	13	—	MHz	—
Jitter Peaking	With default LBW, loop filter capacitor = 220nF		—	—	0.03	dB	—
RxSDO Output Total Jitter	PRBS31 data, BER = 10^{-12}, 11.3Gb/s with optimized boost and swing settings	TJ	—	0.08	0.16	UI_{pp}	—
RxSDO Output Deterministic Jitter	PRBS31 data, BER = 10^{-12}, 11.3Gb/s	DJ	—	0.05	0.088	UI_{pp}	—
RxSDO Output Rise/Fall time	20% to 80%	t_r, t_f	—	—	24	ps	4

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.8V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
RxLOS Assert Threshold Level Setting Range	Minimum programmable setting		—	5	—	mV_{ppd}	—
	Maximum programmable setting		—	400	—	mV_{ppd}	—
RxLOS Threshold Level Variation	1 sigma IC to IC, RXLOSRANGE = 0,1		—	1.0	—	dB	—
	1 sigma IC to IC, RXLOSRANGE = 2		—	2.0	—	dB	—
	Over V_{CC} range		—	1.0	—	dB	—
	Over temperature range -40°C to +100°C, threshold level > $20mV_{ppd}$		—	1.5	—	dB	—
RxLOS Threshold Level Hysteresis Setting Range	Electrical		0	—	6	dB	—
RxLOS Response Time			3	5	20	µs	—
Slice Level Adjust Range	Maximum setting		200	—	—	mV	—
Rx CDR Lock Time	Default mode: loop filter cap = 220nF, minimum LBW setting		—	—	1	ms	—
Differential Output Voltage Setting Range	Minimum swing setting		90	120	130	mV_{ppd}	—
	Maximum swing setting		630	800	910	mV_{ppd}	—
Output Pre-emphasis Setting Range	Maximum pre-emphasis setting. Output swing = $350mV_{ppd}$.		6	—	—	dB	—
RxSDI Differential Return Loss	<5GHz		—	-14	—	dB	—
	5GHz to 10GHz		—	-10	—	dB	—
RxSDO Differential Return Loss	<5GHz		—	-16	—	dB	—
	5GHz to 10GHz		—	-8	—	dB	—

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.8V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Tx Side Specification							
Input Sensitivity			—	15	30	mV_{ppd}	—
Input Overload			1200	—	—	mV_{ppd}	—
LOS Threshold Level Setting Range	Minimum programmable setting		—	20	—	mV_{ppd}	—
	Maximum programmable setting		—	100	—	mV_{ppd}	—
Equalization Gain	Maximum programmable setting		—	6	—	dB	5
Input Sinusoidal Jitter Tolerance – jitter filter mode off	f = 120kHz, maximum LBW		7	10	—	UI_{pp}	6, 7
	f = 4MHz		0.4	0.6	—	UI_{pp}	7
	f = 80MHz		0.35	0.5	—	UI_{pp}	7
Input Sinusoidal Jitter Tolerance – jitter filter mode on	f = 120kHz, maximum LBW		10	16	—	UI_{pp}	6, 7
	f = 4MHz		0.4	0.6	—	UI_{pp}	7
	f = 80MHz		0.35	0.5	—	UI_{pp}	7
Jitter Transfer Bandwidth Setting Range	Minimum programmable setting		—	1.5	—	MHz	—
	Maximum programmable setting		—	10.3	—	MHz	—
Jitter Peaking	With 6MHz LBW, loop filter capacitor = 220nF		—	—	0.03	dB	—
Jitter Generation	50kHz to 80MHz		—	34	—	mUI_{pp}	—
	4MHz to 80MHz		—	22	—	mUI_{pp}	—
Total Output Jitter	TXSDOIMOD = $60mA_{pp}$, PRBS31 data, BER = 10^{-12}, 11.3G		—	0.1	0.18	UI_{pp}	—
Tx CDR Lock Time			—	—	1	ms	8

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.8V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
TxSDO Output Rise/Fall Time	20% to 80%	t_r, t_f	—	26	35	ps	—
TxSDI Differential Return Loss	<5GHz		—	-15	—	dB	—
	5GHz to 10GHz		—	-13	—	dB	—
TxSDO Differential Return Loss	<5GHz		—	-16	—	dB	—
	5GHz to 10GHz		—	-8	—	dB	—
Output Crossing Point Adjust Setting Range	Minimum setting		—	20	—	%	—
	Maximum setting		—	80	—	%	—
Maximum Phase Adjust for Jitter Optimization			—	30	—	ps	—

Notes:

1. At 5.35GHz.
2. At jitter frequencies <100kHz, the GN2042 jitter tolerance performance exceeds the SONET GR-253 RX Tolerance specifications.
3. With default loop bandwidth setting, IJT mode 3 and IJT setting 31.
4. Measured at host-side of XFP or SFP+ connector.
5. At 5.35GHz (dielectric loss)
6. At jitter frequencies <120kHz, the GN2042 jitter tolerance performance exceeds the XFI module transmitter input telecom sinusoidal jitter tolerance specifications (XFP MSA Revision 4.0, Figure 16).
7. In addition to XFI input jitter tolerance requirements.
8. No signal-to-signal (PRBS31 pattern).

3. Input/Output Circuits

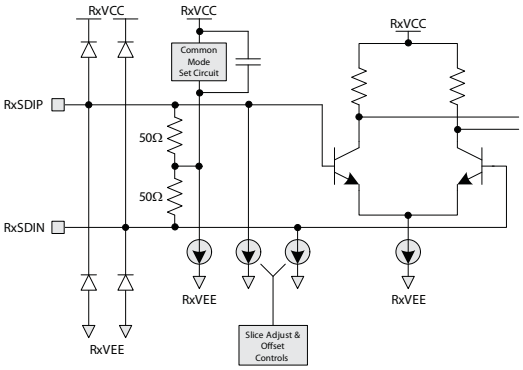


Figure 3-1: RxSDI

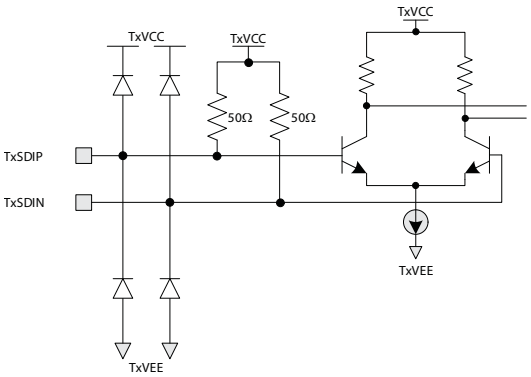


Figure 3-2: TxSDI

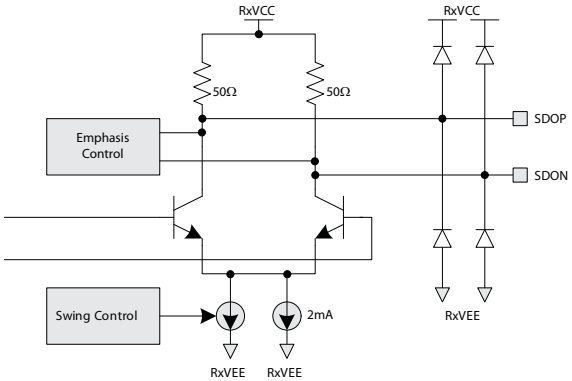


Figure 3-3: RxSDO

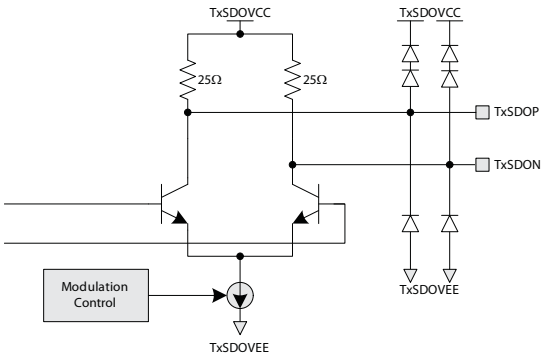


Figure 3-4: TxSDO

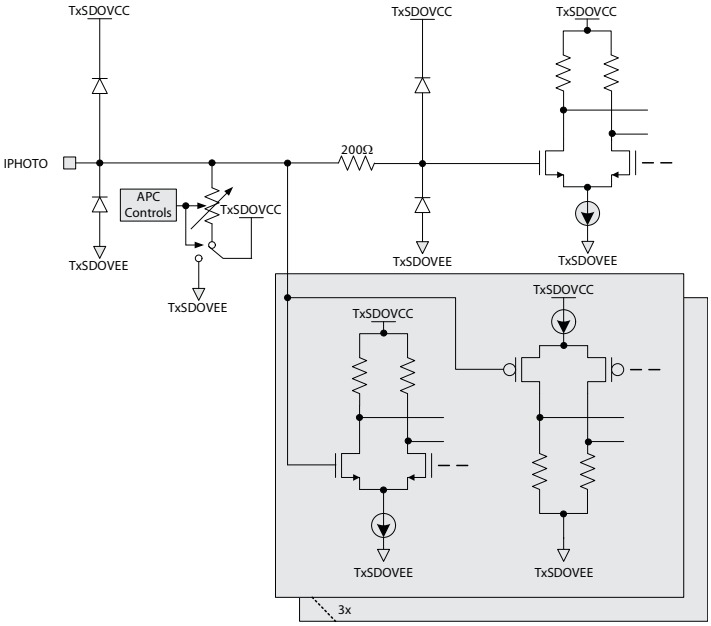


Figure 3-5: IPHOTO

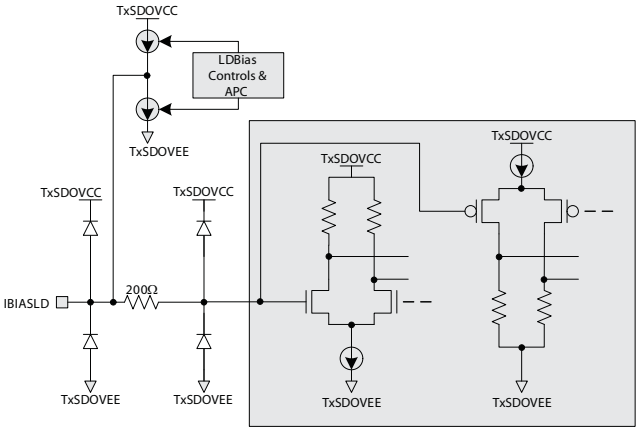
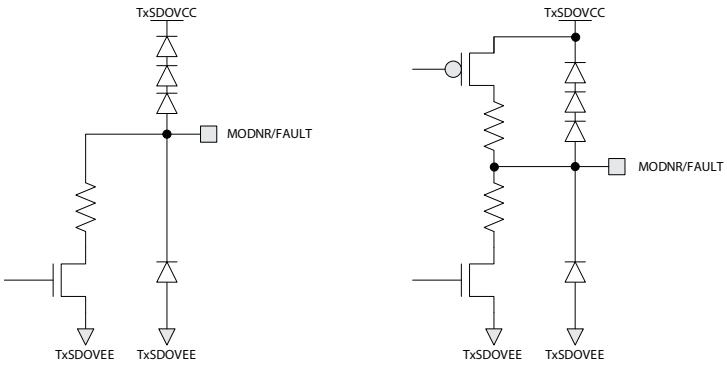


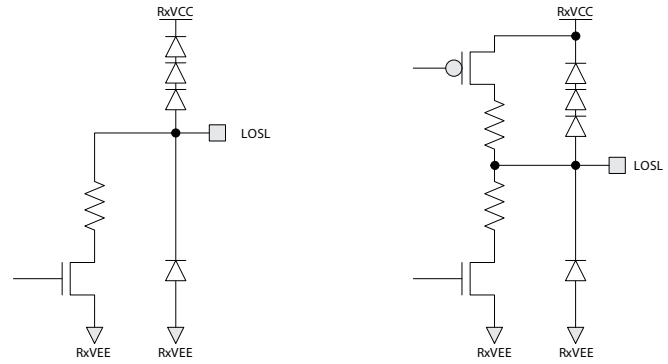
Figure 3-6: IBIASLD



Configured as open-drain

Configured as LVCMOS

Figure 3-7: MODNR/FAULT



Configured as open-drain

Configured as LVCMOS

Figure 3-8: LOSL

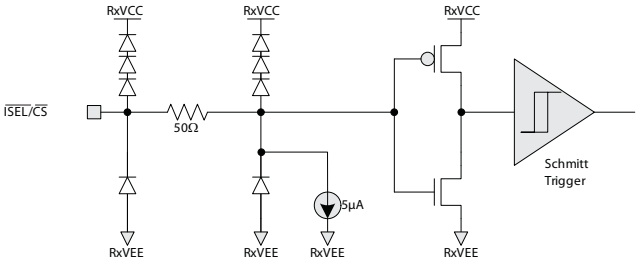


Figure 3-9: $\overline{\text{ISEL}}/\overline{\text{SCS}}$

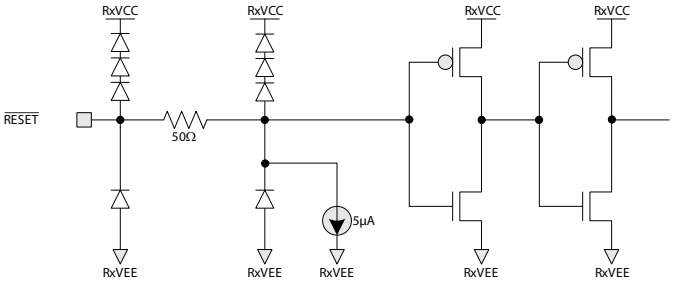


Figure 3-10: $\overline{\text{RESET}}$

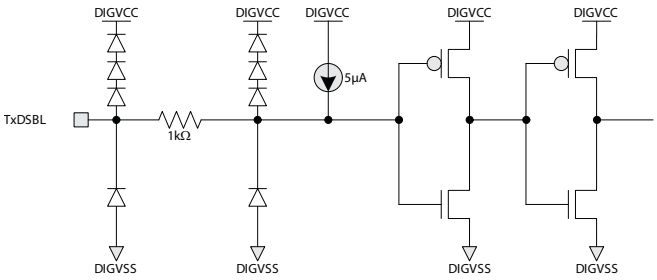


Figure 3-11: TxDSBL

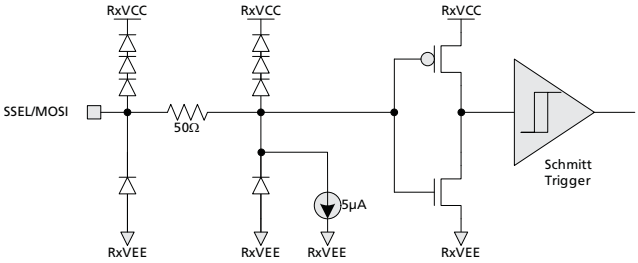


Figure 3-12: SSEL/MOSI

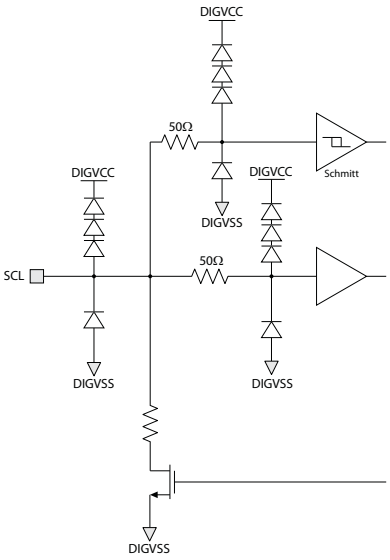


Figure 3-13: SCL

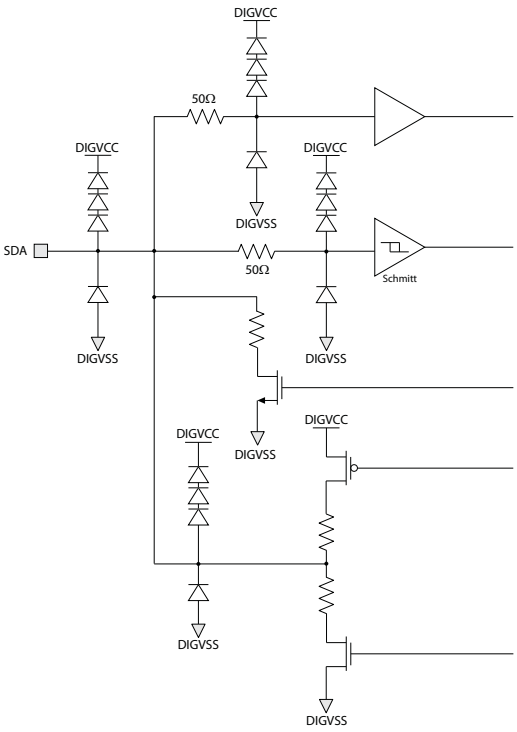


Figure 3-14: SDA

4. Detailed Description

4.1 Multirate CDR Functionality

The GN2042 supports a range of data rates, so that a single part can be used for multiple applications. The GN2042 does not require a reference clock. Some example applications are as follows:

- 10Gb/s Ethernet (10.3Gb/s)
- 10Gb/s Ethernet with FEC (11.1Gb/s)
- 10G Fibre Channel (10.5Gb/s)
- 10G Fibre Channel with FEC (11.3Gb/s)
- SONET OC192 (9.95Gb/s)
- 9.8Gb/s CPRI

4.1.1 Retimer Bypass

The device can be configured to manually bypass each of the Rx and Tx CDRs through the **TX_PLL_BYPASS** and **RX_PLL_BYPASS** controls.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG5	14	TX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Tx CDR into bypass mode.
RXPLL_REG5	24	RX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Rx CDR into bypass mode.

4.2 Receive Path

The GN2042 receive path contains a high-sensitivity limiting amplifier with optional equalization, a multi-rate CDR, and an emphasis driver.

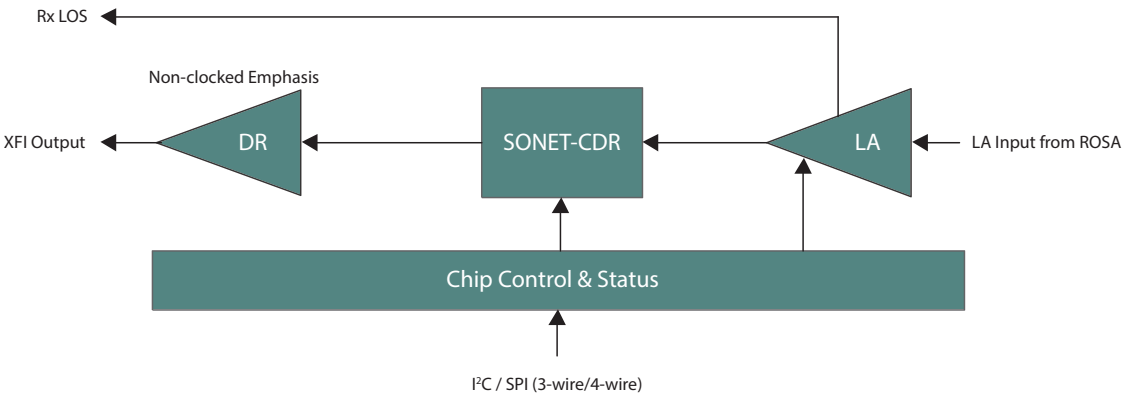


Figure 4-1: Receive Path

4.2.1 Integrated Limiting Amplifier

The GN2042 has an integrated Limiting Amplifier (LA), with better than 10mV sensitivity. Additional features are; slice level adjust and optional equalization on the limiting amplifier input.

4.2.2 Slice Level Adjust

The slicing level of the limiting amplifier can be configured in two modes of operation:

1. Automatic offset correction.
2. Manual slice adjust with a fixed slice level.

By default, the limiting amplifier is configured in automatic offset correction mode, and will slice the incoming signal at the 50% point.

The LA can be configured to allow a user-specified fixed slice level. In this mode, the slice level can be varied by ±200mV from the 50% point in 1mV increments. To enable this mode, **RX_PD_SLICE_ADJ** (shown below) should be set to 0.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPWRDN_REG2	135	RX_PD_SLICE_ADJ	1:1	RW	1	0-1	When HIGH, power-down for LA slice adjust.

To enable the user to adjust the slice level manually, **RX_PD_SLICE_ADJ** must be set to 0 and **RX_MANUAL_SLICE_ADJ_EN** must be set to 1.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG5	52	RXLA_MANUAL_SLICE_ADJ_EN	0:0	RW	0	0-1	When HIGH, enables user to adjust slice level at the Rx input.

The following controls allow the slice adjust polarity and magnitude to be set manually:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG2	49	RXLA_SLICE_ADJ	7:0	RW	00000000	0-255	Slice adjust magnitude control.
RX_REG3	50	RXLA_SLICE_ADJ_POL	0:0	RW	0	0-1	Slice adjust polarity. When HIGH, slice level adjust is positive.

The slice level adjustment can be applied before or after the equalization function (covered in Section 4.2.3). This flexibility allows the device to maintain optimal receive sensitivity performance while optimizing slice adjust. Figure 4-2 shows the two possible insertion points for slice level adjustment:

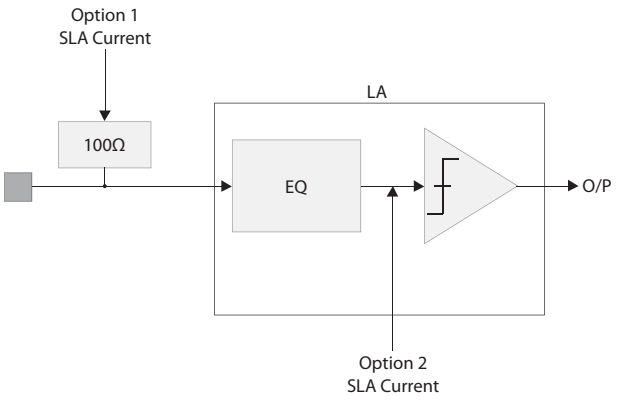


Figure 4-2: Slice Level Adjustment Insertion Points

RXLA_SLICE_ADJ_LO_RANGE should be set to 1 to apply the slice adjust after the equalization function.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG3	50	RXLA_SLICE_ADJ_LO_RANGE	1:1	RW	0	0-1	Selects slice level adjust point. When LOW, slicing point is option 1. When HIGH, slicing point is option 2.

4.2.3 Receive Equalization

The receive input implements an equalizer that provides peaking at 5.35GHz. This feature allows for optimal performance with extended reach connections, and allows for optimization of parameters such as dispersion penalty.

The equalizer implements 0dB to 14dB of high-frequency boost in fifteen steps, while achieving optimal receive sensitivity at any given equalization setting. The equalization setting is set through the **RXLA_BOOST_MSB** control. Additionally, the **RXLA_BOOST_LSB** control provides another 8 steps of fine tune control of the equalization gain at each **RXLA_BOOST_MSB** setting.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG1	48	RXLA_BOOST_MSB	3:0	RW	0000	0-15	RXLA boost control bit MSBs: 0 = 0dB to 15 = 14dB
RX_REG16	63	RXLA_BOOST_LSB	2:0	RW	000	0-7	RXLA boost control bit LSBs for fine tuning gain with smaller step size.

When the equalization setting is 0dB, the equalization function is bypassed and the receive sensitivity performance is the same as that of a limiting amplifier.

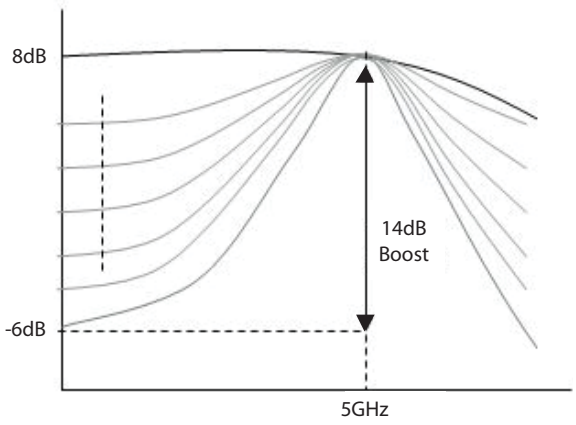


Figure 4-3: Receive Equalization

4.2.4 Rx PLL Variable Loop Bandwidth

The loop bandwidth of the receive Phase Locked Loops (PLLs) can be varied through the digital control interface. The loop bandwidths (LBW) are individually controlled, and can cover a range of 2.6MHz to 13MHz through the following 5-bit registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG1	20	RX_PLL_LBW_POS_ADJ	4:0	RW	11101	0-31	Adjusts LBW positive temperature coefficient control.
RXPLL_REG2	21	RX_PLL_LBW_NEG_ADJ	4:0	RW	00111	0-31	Adjusts LBW negative temperature coefficient control.

The temperature coefficient of the loop bandwidth can be adjusted by a weighted summation of **RX_PLL_LBW_POS_ADJ**, which has a positive temperature coefficient, and **RX_PLL_LBW_NEG_ADJ**, which has a negative temperature coefficient.

Table 4-1 shows the recommended settings for a flat loop bandwidth temperature coefficient:

Table 4-1: Rx Loop Bandwidth

RX_PLL_LBW_POS_ADJ	RX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
2	0	2	2.047
4	3	7	3.280
7	5	12	4.513
10	7	17	5.700
13	9	22	6.700
15	11	26	7.500
18	13	31	8.500
21	15	36	9.500
24	17	41	10.250
27	19	46	11.000

Table 4-1: Rx Loop Bandwidth (Continued)

RX_PLL_LBW_POS_ADJ	RX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
29	20	49	11.375
31	22	53	11.875
31	31	62	13.000

4.2.5 Rx CDR Input Jitter Tolerance

The input jitter tolerance of the Rx CDR is configurable to allow power optimization for required performance. Three modes of operation are supported as follows:

- **Mode 1:** Recommended for power-optimized applications. This mode supports the lowest power, but it is not guaranteed to meet the SONET IJT mask
- **Mode 2:** Recommended for most applications, including SONET, Ethernet and Fibre Channel. In this mode, the device is guaranteed to meet the SONET IJT mask.
- **Mode 3:** Recommended for SONET applications that require large margins on SONET IJT mask. This mode consumes extra power.

The RxCDR IJT mode is configured through the following registers. By default, the device is configured in Mode 3.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG9	28	RX_PLL_SELECT_HIGH_IJT	3:3	RW	1	0-1	When HIGH, selects high-margin Sonet IJT mode in conjunction with the RX_PLL_SONET_IJT_SETTING.
RXPLL_REG8	27	RX_PLL_SONET_IJT_SETTING	7:3	RW	00010	0-31	Control for Sonet IJT performance. Used in conjunction with Sonet IJT modes 2 and 3 to set IJT performance. Gradually increase setting for increased margins.
RXPWRDN_REG4	137	RX_PD_SONET_IJT	0:0	RW	0	0-1	When HIGH, powers-down the Rx path Sonet IJT feature to save power.

Table 4-2 shows the recommended settings for above registers for the three IJT modes:

Table 4-2: IJT Mode Settings

IJT Mode	RX_PD_SONET_IJT	RX_PLL_SELECT_HIGH_IJT	RX_PLL_SONET_IJT_SETTING[4:0]
1	1	x	x
2	0	0	2 (or higher, based on user preference)
3	0	1	3 (or higher, based on user preference)

Figure 4-4 shows that Mode 2 and Mode 3 SIJT performance is comparable with maximum LBW settings, with >3UI margin at 400kHz:

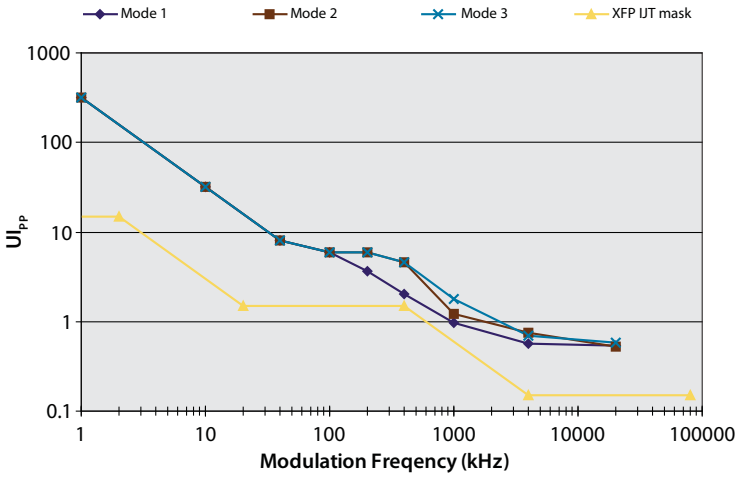


Figure 4-4: S-IJT Mode 1, 2 & 3 (Loop Bandwidth = 6.2MHz)

With higher LBW settings, Mode 2 can be used to meet and exceed S-IJT mask with lower power than Mode 3. Note that in either Mode 2 or Mode 3, the **RX_PLL_SONET_IJT_SETTING** can be adjusted beyond the values provided in Table 4-2 to further optimize SIJT performance margins.

4.2.6 Emphasis Driver with Auto-Mute

The receive path driver is a non-clocked emphasis driver that can be used to compensate for losses in the connector and trace between the module and ASIC. The emphasis operates regardless of the status or state of the Rx CDR. The output swing can be set from 100mV to 800mV in steps of 50mV through the **RX_SDO_SWING[3:0]** register. The emphasis amplitude can be varied from 1dB to 6dB in 16 steps through **RX_SDO_EMPHASIS[3:0]**.

Note: The Rx emphasis in disabled by default. To enable the emphasis, set **RX_PD_RXSDO_EMPHASIS** to 0 to power-on the Rx emphasis block. When emphasis is enabled, the output driver is still limited to approximately 800mV$_{ppd}$ output. Therefore, at some swings settings (i.e. >400mV$_{ppd}$), the full 6dB emphasis may not be realized. See Figure 4-5 for more information.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXSDO_REG1	75	RX_SDO_SWING	3:0	RW	0110	0-15	Driver swing: 100mV$_{ppd}$ to 850mV$_{ppd}$. Default = 6 = 400mV$_{ppd}$.
RXSDO_REG2	76	RX_SDO_EMPHASIS	3:0	RW	0000	0-15	Driver emphasis control.
RXPWRDN_REG1	134	RX_PD_RXSDO_EMPHASIS	3:3	RW	1	0-1	When HIGH, power-down for the trace driver emphasis.

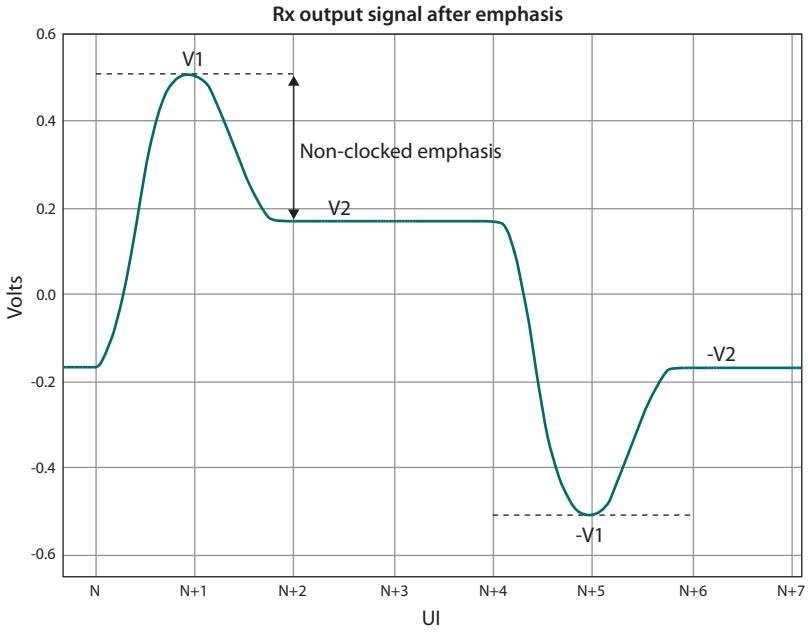


Figure 4-5: Emphasis Waveform Description when Enabled

Figure 4-5 above shows the emphasis waveform. Amplitudes V1, V2 and emphasis in dB are defined as follows:

V1, **V2** and **Emphasis** are defined as follows:

V1 = **RX_SDO_EMPHASIS** setting, which represents the "peak", or superposition of the **RX_SDO_SWING** setting and the **RX_SDO_EMPHASIS** setting.

V2 = **RX_SDO_SWING** setting, which is the DC or Steady State swing, same as when no emphasis is enabled.

Emphasis [dB] = 20 x log(V1/V2). As a guideline, 2 x V1 should be less than or equal to 800mV.

The output can be configured to automatically mute if Receive LOS is detected through the following registers. When muted, the output driver remains powered-up, and the output common mode is maintained. The output driver can be configured to power-down when muted by setting the **RX_SDO_PWR_DN_ON_MUTE** bit:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXSDO_REG3	77	RX_SDO_FORCE_MUTE	0:0	RW	0	0-1	Mutes driver to CM when not in auto mute mode.
		RX_SDO_AUTO_MUTE_EN	1:1	RW	1	0-1	Enables muting the driver upon LOS.
		RX_SDO_PWR_DN_ON_MUTE	2:2	RW	1	0-1	Enables power-down on mute for output stage.

4.2.7 Output Polarity Invert

Polarity inversion is implemented at the SDO input. Input to the CDR is not affected by polarity inversion. The output polarity can be inverted through the following register:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG5	24	RX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.

4.3 Transmit Path

The transmit path is comprised of a trace equalizer, a multi-rate CDR and a DML driver.

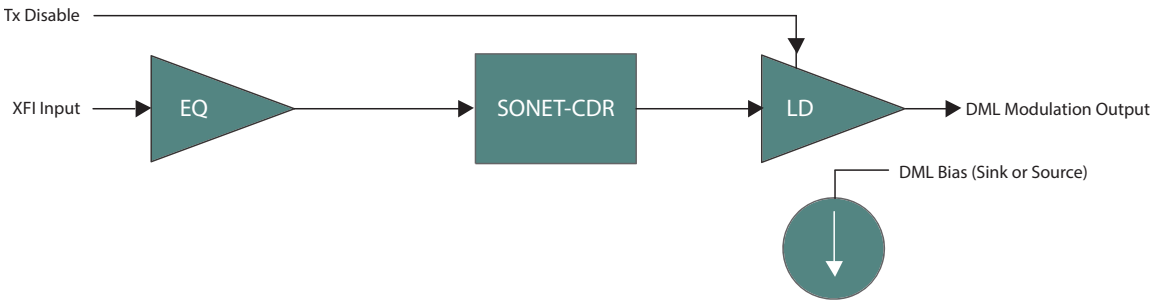


Figure 4-6: Transmit Path

4.3.1 Equalizer

The the transmit path input has an XFI equalizer with up to 6dB gain at 5.35GHz. The equalizer can be controlled through the following register:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TX_REG3	33	TX_EQ_BOOST	1:0	RW	11	0-3	Controls the Tx path input equalization setting: 00 = 0dB 01 = 2dB 10 = 4dB 11 = 6dB

4.3.2 Tx PLL Variable Loop Bandwidth

The loop bandwidth of the transmit Phase Locked Loops (PLLs) can be varied through the digital control interface. The loop bandwidths are individually controlled, and can cover the range of 1MHz to 10MHz through the following 5-bit registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG1	10	TX_PLL_LBW_POS_ADJ	4:0	RW	01110	0-31	Adjusts LBW positive temperature coefficient control.
TXPLL_REG2	11	TX_PLL_LBW_NEG_ADJ	4:0	RW	00010	0-31	Adjusts LBW negative temperature coefficient control.

The temperature coefficient of the loop bandwidth can be adjusted by weighted summation of **TX_PLL_LBW_POS_ADJ**, which has a positive temperature coefficient and **TX_PLL_LBW_NEG_ADJ**, which has a negative temperature coefficient.

Table 4-3 shows the recommended settings for a flat loop bandwidth temperature coefficient:

Table 4-3: Tx Loop Bandwidth

TX_PLL_LBW_POS_ADJ	TX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
2	0	2	1.413
4	3	7	2.480
7	5	12	3.547
10	7	17	4.555
13	9	22	5.330
15	11	26	5.950
18	13	31	6.725
21	15	36	7.500
24	17	41	8.050
27	19	46	8.600
29	20	49	8.919
31	22	53	9.344
31	31	62	10.300

4.3.3 Tx Jitter Filter Mode

The Tx CDR supports a jitter filter mode to aid in the optimization of jitter generation performance and reduction of jitter present at the Tx CDR input. The jitter filter mode is configured using the following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPWRDN_REG4	133	TX_PD_JIT_FILT	0:0	RW	1	0-1	When HIGH, power-down for the Tx jitter filter.
TXPLL_REG1	10	TX_PLL_LBW_POS_ADJ	4:0	RW	01110	0-31	Adjusts the LBW positive temperature coefficient control.
TXPLL_REG2	11	TX_PLL_LBW_NEG_ADJ	4:0	RW	00010	0-31	Adjusts the LBW negative temperature coefficient control.
TXPLL_REG8	17	TX_JIT_FILT_TRACK_ADJUST	7:3	RW	00010	0-31	Sets the tracking capability when Tx jitter filter mode is enabled.

Note: This feature does not impact the jitter generation performance of the Tx Laser Driver. The jitter generation performance of the laser driver and external TOSA must still be properly optimized separately.

To enable Tx jitter filter mode, set **TX_PD_JIT_FILT** LOW. Once enabled, **TX_PLL_LBW_POS_ADJ** and **TX_PLL_LBW_NEG_ADJ** are used to set the jitter filter bandwidth, and can be optimized for the desired jitter generation/filtering performance. Lastly, **TX_JIT_FILT_TRACK_ADJUST** is used to set the tracking capability of an internal clock with respect to the Tx input data. This allows for optimization of wander tolerance.

4.4 Laser Driver

4.4.1 DML Driver

The GN2042 has an integrated DML driver with eye-shaping features, and an integrated Automatic Power Control (APC) loop.

The DML laser driver can provide up to 80mA$_{pp}$ modulation current into a 25Ω load. The following registers can be used to set the modulation current with 10-bit resolution. Note that the **TXSDO_IMOD_LO** must be written to first, followed by a write to **TXSDO_IMOD_HI**. The new value only takes effect after a write to **TXSDO_IMOD_HI**.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG10	87	TXSDO_IMOD_LO	7:0	RW	00000000	0-255	LD modulation current LSB.
TXSDO_REG11	88	TXSDO_IMOD_HI	1:0	RW	00	0-3	LD modulation current MSB.

4.4.1.1 Jitter Generation Optimization Using Laser Driver Phase Adjust

The jitter optimization feature in the laser driver is intended to optimize module level jitter. This includes jitter from the GN2042, external pull-up inductors, board parasitic and the laser diode. This feature can also be used to improve jitter generation performance for SONET applications. The following registers can be used to optimize jitter generation through TxSDO phase adjust:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG13	90	TXSDO_PHASE_ADJUST	7:0	RW	00000000	0-255	LD phase adjust—compensation for jitter generation due to Sonet header.
TXSDO_REG25	99	TXSDO_PHASEADJ_DIR	1:1	RW	0	0-1	LD phase adjust (Z0) compensation direction E/L:0/1.
PWRDN_REG1	138	PD_TXSDO_PHASE_ADJ	2:2	RW	1	0-1	When HIGH, power-down for LD phase adjust (Z0) compensation.

TXSDO_PHASEADJ_DIR controls the direction in which the jitter generation optimization using phase adjust is applied. The direction depends on the jitter signature present at the output of the module. **TXSDO_PHASE_ADJUST** controls the magnitude of the jitter generation optimization. To enable the feature, **PD_TXSDO_PHASE_ADJ** must be set LOW. The Tx CDR must be powered-on for the phase adjust feature to work.

4.4.1.2 Crossing Point Adjust

The crossing point adjust feature allows the user to adjust the cross point as shown in Figure 4-7 below. The crossing point adjust features can set the output crossing point from 20% to 80%, with a 6-bit control through following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG12	89	TXSDO_CPA	5:0	RW	011111	0-63	LD crossing point adjust: 0~ = >80% 31 = 50% 63~ = <20%
PWRDN_REG1	138	PD_TXSDO_CPA	3:3	RW	1	0-1	When HIGH, power-down for LD crossing point adjust.

To enable the feature, **PD_TXSDO_CPA** must be set LOW.

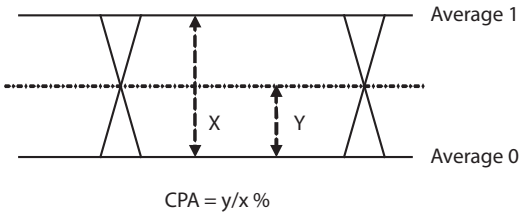


Figure 4-7: Definition of Cross Point Adjust Percentage

4.4.1.3 Laser Driver Shutdown

The laser driver supports several modes of shutdown including:

- Manual mute (with optional output stage power-down)
- Automatic mute upon LOS detection (with optional output stage power-down)
- Modulation squelch
- TxDSBL through control register

The following registers can be used to configure and invoke the above shutdown modes:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG25	99	TXSDO_MOD_SQUELCH	0:0	RW	0	0-1	When HIGH, LD modulation is squelched.
		TXSDO_FORCE_TXDSBL	2:2	RW	0	0-1	When HIGH, shuts down the LD mod, bias and APC.
		TXSDO_FORCE_MUTE	3:3	RW	0	0-1	When HIGH, mutes driver to CM when not in auto mute mode.
		TXSDO_AUTO_MUTE_EN	4:4	RW	1	0-1	When HIGH, enables muting the driver upon LOS.
		TXSDO_PWR_DN_ON_MUTE	5:5	RW	1	0-1	When HIGH, enables power-down on mute for the output stage.

4.4.2 Laser Driver Bias Current

The laser driver bias current can be configured as either a sink or a source current. By default, the bias current is configured as a source. It is important to avoid configuring the bias current in a mode that will not be used by the intended application. If a bias current sink is required by the application, the device must be configured to make the bias current a sink after power-up. If a bias current source is required by the application, no configuration is necessary, as the device is configured as a source by default.

The following registers can be used to configure the bias current as either a source or a sink:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG26	100	TXSDO_BIAS_SOURCE_EN	3:3	RW	1	0-1	LD bias source is enabled when HIGH. TXSDO_BIAS_SINK_EN must be LOW.
		TXSDO_BIAS_SINK_EN	4:4	RW	0	0-1	LD bias sink is enabled when HIGH. TXSDO_BIAS_SOURCE_EN must be LOW.

The laser driver bias current is controlled by the Automatic Power Control or APC loop by default. The next section describes the operation of the APC loop. However, the laser driver bias current may be set manually by overriding the APC loop. The following registers allow a fixed laser driver bias current to be programmed manually:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range (Dec)	Function
APC_REG4	106	APC_DAC_OVR_VAL_LO	7:0	RW	00000000	0-255	Override value for the APC DAC counter [7:0]. Sets the LD bias current manually when used with APC_DAC_OVR_VAL_HI, and when APC_OVR is HIGH. Step size is approximately 0.15mA.
APC_REG5	107	APC_DAC_OVR_VAL_HI	1:0	RW	00	0-3	Override APC DAC [9:8]. A write triggers an update.
		APC_OVR	2:2	RW	0	0-1	When HIGH, overrides the APC loop with the DAC override value to set the LD bias current manually.

When **APC_OVR** is set HIGH, the APC control loop is bypassed and the 10-bit bias current control **APC_DAC_OVR_VAL_LO/HI** takes effect. Note that the LOW value must be written first, followed by a write to the HIGH value. The new value only takes effect after a write to the HIGH value. The APC must still be enabled when using the override mode.

Note: With **APC_OVR** set HIGH, TxDSBL assert will set the LD bias current to shut off. After TxDSBL is de-asserted, the **APC_DAC_OVR_VAL_LO/HI** registers must be re-written to turn on the LD bias current. When **APC_OVR** is set HIGH, it is recommended to write the **APC_DAC_OVR_VAL_LO/HI** registers immediately following TxDSBL negation to minimize the negate time.

4.4.3 Automatic Power Control Loop

The GN2042 integrates an Automatic Power Control or APC loop to control the bias current for the laser diode in the TOSA, thereby reducing the external components required. The photo current from the TOSA (IPHOTO) is converted to a voltage (VPHOTO), through an on-chip, selectable resistor. The resistor selection is based on the maximum IPHOTO from the TOSA. There are four possible settings available through **IPH_RANGE_SEL[1:0]**. IPHOTO is then used as an indicator of the average transmit power. The user can define a set point for IPHOTO to achieve a certain average transmit power. The APC loop operates to achieve and maintain the set point over operating conditions.

The APC uses 10 bits of resolution to define the bias current to ensure minimal variation of average transmit power. To accommodate different TOSAs configurations, IPHOTO can be configured to source a current from the GN2042 or sink a current from the TOSA.

The APC loop is enabled by default. The following registers can be used to enable and configure the APC loop. When the APC loop is disabled and re-enabled, it must be reset.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
APC_REG1	104	APC_EN	0:0	RW	1	0-1	When HIGH, enables the APC.
		APC_RESET	3:3	RW	0	0-1	When HIGH, the APC control is reset.
		APC_SEL_HIGH_REF	4:4	RW	0	0-1	When HIGH, IPHOTO is sourced from the GN2042 and is sunk in the TOSA. When LOW, IPHOTO is sourced from the TOSA and is sunk in the GN2042.
TXSDO_REG5	82	IPH_RANGE_SEL	1:0	RW	10	0-3	IPHOTO range select: 00 = 0mA to 0.25mA 01 = 0.25mA to 0.75mA 10 = 0.75mA to 1.25mA 11 = 1.25mA to 2.14mA

4.4.3.1 APC Loop Dynamics

The APC loop is designed to meet the TxDSBL assert time of <10µs, and the TxDSBL negate time of <2ms. In addition, the APC loop supports a highly-configurable loop dynamics upon TxDSBL negate to minimize the time to achieve the desired output average power level, without any overshoots on output average power.

The loop dynamics upon Reset or TxDSBL negation is configured through two sets of parameters as follows:

1. APC Thresholds
   - APC_TH_HI
   - Set Point (IPHOTO for desired average transmit power)
2. APC Slew Rates
   - Fast Rate—LD bias current updates rate when IPHOTO is < APC_TH_HI
   - Slow Rate—LD bias current updates rate when IPHOTO is > APC_TH_HI

Figure 4-8 shows the loop dynamics and impact of each of the above parameters.

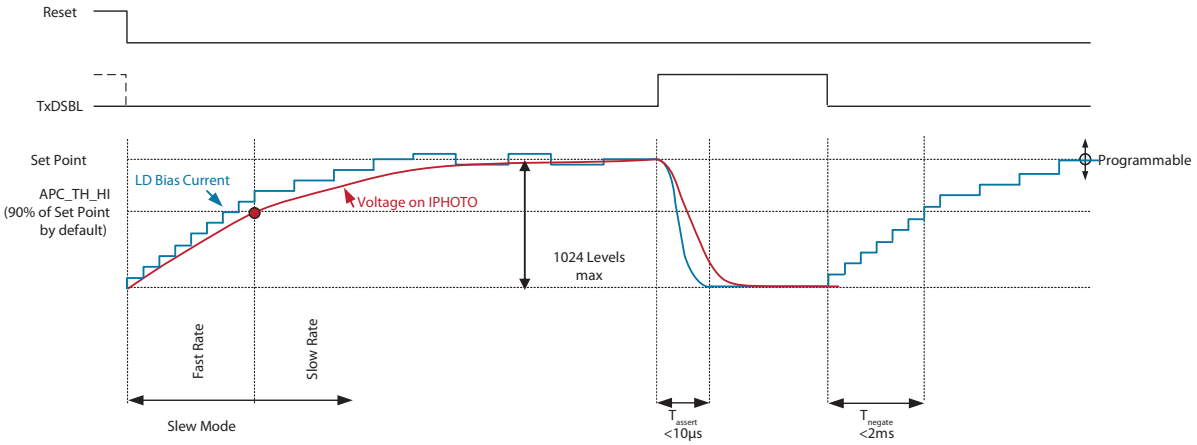


Figure 4-8: APC Loop Dynamics

Upon negation of Reset or TxDSBL, the difference between IPHOTO and the set point (error) is large. In this region, a fast rate for LD bias current can be selected to minimize the negate time without risk of overshooting the set point. As the error reduces, it is desirable to slow down the LD bias current rate to avoid overshoot. The threshold **APC_TH_HI** defines the region of fast and slow ramp up rates. Initially, the LD Bias current will ramp-up at a fast rate because it is below **APC_TH_HI**. When the LD Bias current exceeds **APC_TH_HI**, it will ramp-up at the slow rate. This controlled ramp-up ensures robust stability and avoids overshoots while meeting the negate time of <2ms. By default, **APC_TH_HI** is set to 90% of the set point, but it can be adjusted if necessary. It is generally recommended to use the default APC configuration settings.

The following registers control the APC thresholds:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
APC_REG6	108	APC_REF_DAC_CTRL	7:0	RW	00000000	0-255	Sets APC final target reference threshold (0V to 1V range in steps of 4mV).
APC_REG8	110	APC_TH_HI	5:0	RW	110110	0-63	APC Threshold Hi setting 110110 (default) - 0.9x of setpoint 1 LSB = 0.0167x of setpoint.

The following registers control the APC slew rates:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
APC_REG2	105	APC_CLK_RATE_FAST_DIV	3:2	RW	00	0-3	APC fast rate divide ratio: 0-3 = 32-256, default = 32
		APC_CLK_RATE_SLOW_DIV	6:4	RW	101	0-7	APC slow rate divide ratio: 0-3 = 32-4k, default = 1k

Note: The default update rate is approximately 20MHz.

4.5 Status Indicators

The GN2042 supports three status indicators: Loss of Signal (LOS), Loss of Lock (LOL) and Module Not Ready (MODNR). LOS and LOL indicators are available on both the receive and the transmit paths.

4.5.1 Receive Loss of Signal (LOS)

The receive path Loss Of Signal indicator status is available through a register and the LOSL pin. The LOSL pin is by default open-drain, active-high 1.8V – 3.3V LVCMOS compatible. However, the pin can be configured in a 1.8V LVCMOS-compliant compatible mode by setting **OPEN_DRAIN_LOSL** to 0. In addition, LOSL can be configured to be active-low by setting **POLINV_LOSL** HIGH. The status of RxLOS can be read out through **RX_PLL_LOS**. Additionally, the LOSL pin can be configured to provide other status information as per the table below. By default, LOSL only provides status information for RxLOS. If other status indicators are enabled, the LOSL output is the logical OR of all enabled indicators.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TOP_REG2	2	POLINV_LOSL	1:1	RW	0	0-1	When HIGH, inverts polarity of the LOSL output.
		OPEN_DRAIN_LOSL	2:2	RW	1	0-1	When HIGH, makes the LOSL output driver open-drain.
		LOSL_MASK_RXLOS	4:4	RW	0	0-1	When HIGH, masks-out RxLOS from asserting LOSL.
		LOSL_MASK_RXLOL	5:5	RW	1	0-1	When HIGH, masks-out RxLOL from asserting LOSL.
		LOSL_MASK_TXLOS	6:6	RW	1	0-1	When HIGH, masks-out TxLOS from asserting LOSL.
		LOSL_MASK_TXLOL	7:7	RW	1	0-1	When HIGH, masks-out TxLOL from asserting LOSL.
RXPLL_REG10	29	RX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.

The LOS assert threshold can be set from 5mV to 400mV in three distinct ranges. The LOS assert threshold is a function of the **RXLA_BOOST_MSB** setting. Table 4-4 describes the selection of **RXLOS_RANGE** based on the required LOS assert threshold and **RXLA_BOOST_MSB** settings.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG12	59	RXLOS_RANGE	1:0	RW	01	0-3	LOS range: 0 = highest 3 = lowest

Table 4-4: LOS Assert Ranges

RXLA_BOOST_MSB [3:0]	LOS Assert Threshold Range		RXLOS_RANGE[1:0]	Resolution (controlled by RXLOS_TH_NEG/POS)	Unit
	Min	Max			
	5	400	LOS Threshold - Total Range	—	mV_{ppd}
0-7	—	—	11 - Unused	—	—
0-7	5	30	10 - Low Range	<0.1mV	mV_{ppd}
0-7	30	100	01 - Mid Range	<1.0mV	mV_{ppd}
0-7	100	400	00 - High Range	<2.0mV	mV_{ppd}
8-15	5	30	11 - Low Range	<0.1mV	mV_{ppd}
8-15	30	100	10 - Mid Range	<1.0mV	mV_{ppd}
8-15	—	—	01 - Unused	—	—
8-15	100	400	00 - High Range	<2.0mV	mV_{ppd}

4.5.1.1 Rx LOS Threshold

The LOS assert threshold is set using the following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG9	56	RXLOS_TH_NEG	7:0	RW	01001001	0-255	Negative tempco LOS threshold setting.
RX_REG10	57	RXLOS_TH_POS	7:0	RW	00000000	0-255	Positive tempco LOS threshold setting.

Figure 4-9 to Figure 4-12 shows the typical recommended range of Rx LOS Assert thresholds and corresponding **RX_LOS_TH_NEG[7:0]** setting to achieve these thresholds. It is recommended to keep **RX_LOS_POS[7:0]** = 0. The Rx LOS De-assert thresholds are the same as the Rx LOS Assert thresholds for a hysteresis setting of 0.

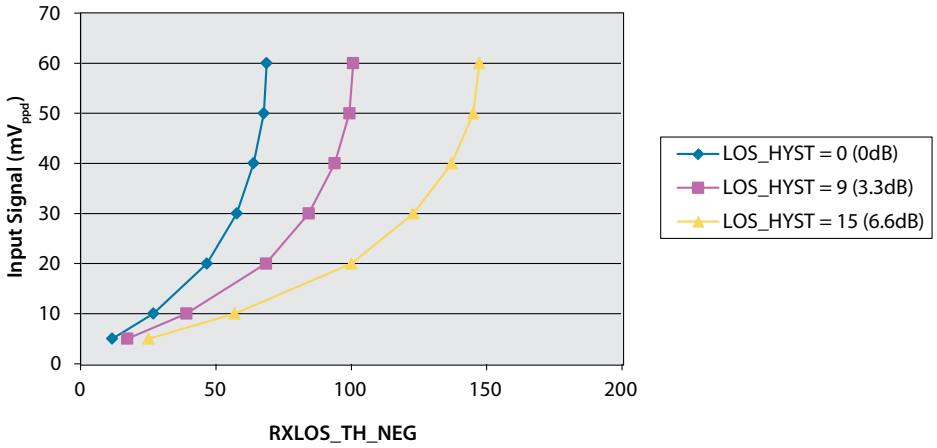


Figure 4-9: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = LOW)

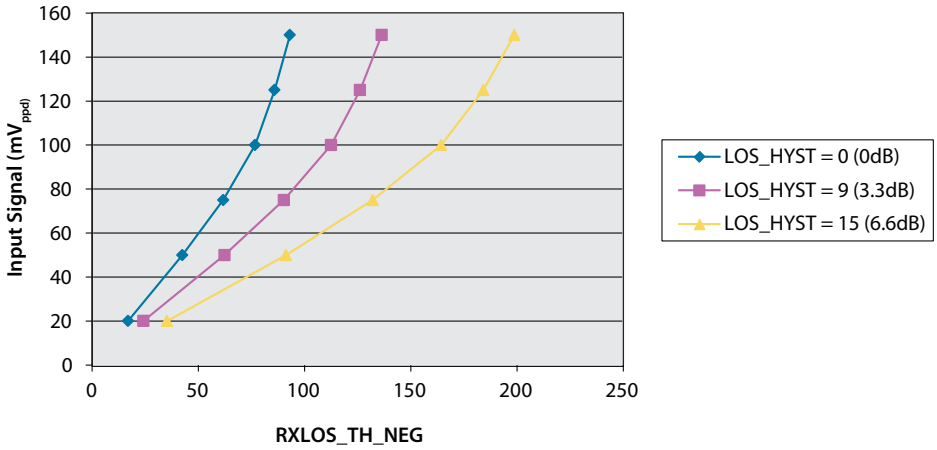


Figure 4-10: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = MID)

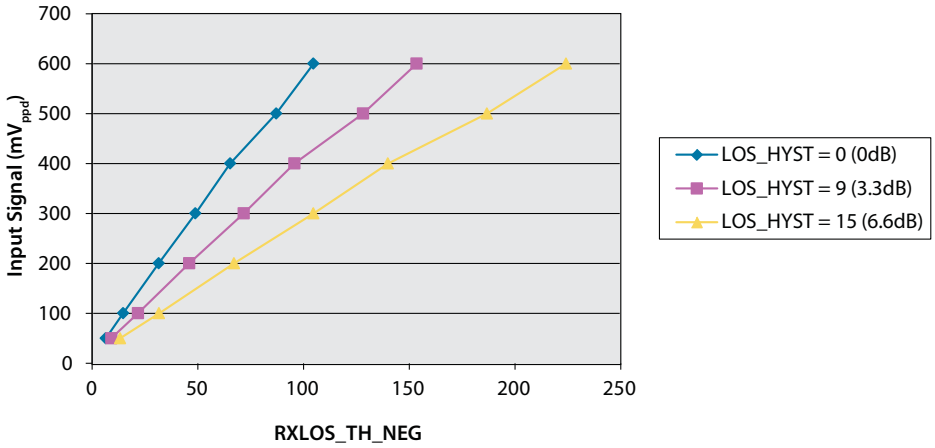


Figure 4-11: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = HIGH)

The LOS threshold has a slight dependence on the input data rate. Figure 4-12 below gives an indication of the typical variation of data rate, between 9.95Gb/s to 11.3Gb/s.

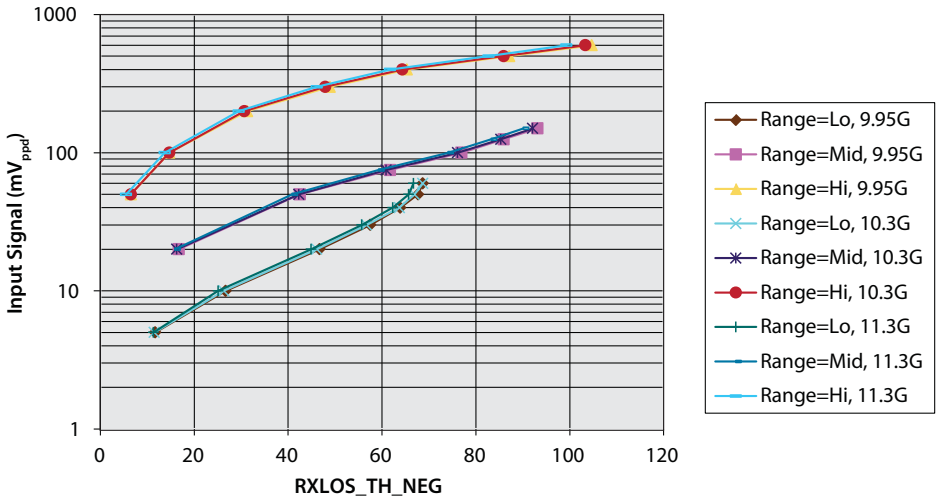


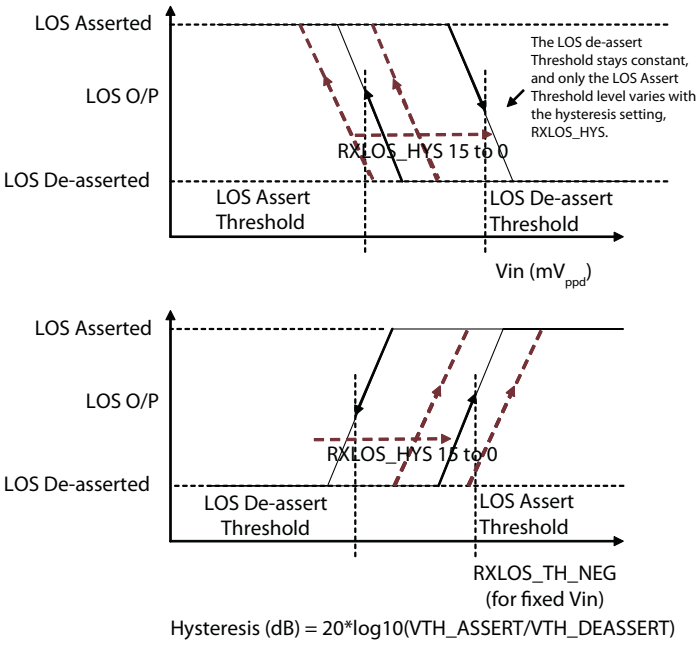
Figure 4-12: Rx LOS Assert Threshold Variation Over Data Rates

4.5.1.2 Rx LOS Hysteresis

The LOS detector supports programmable hysteresis ranging from 0dB to 6dB, adjustable in steps of less than 0.5dB. The following register can be used to program the hysteresis. Note that the effective hysteresis is somewhat dependent on the threshold value:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG11	58	RXLOS_HYS	3:0	RW	1001	0-15	Hysteresis control 0-15 -> 0-6dB. Default = 9 = 3dB.

Hysteresis control only affects the assert threshold. The LOS de-assert threshold is set by **RXLOS_TH_NEG** and **RXLOS_TH_POS** controls only. Figure 4-13 shows the hysteresis characteristics and the impact of **RXLOS_HYS[3:0]**:



RXLOS_HYS	Hysteresis (dB)
0	0.1
1	0.3
2	0.7
3	1.1
4	1.4
5	1.8
6	2.1
7	2.5
8	3.0
9	3.4
10	3.9
11	4.4
12	4.8
13	5.4
15	6.7

Figure 4-13: Rx LOS Hysteresis

To support system diagnostics, a manual LOS assert feature is available through the following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG12	59	RXLOS_FORCE_ASSERT	2:2	RW	0	0-1	Directly sets the state of RXLOS accordingly if RXLOS_FORCE_ASSERT_EN is HIGH.
		RXLOS_FORCE_ASSERT_EN	3:3	RW	0	0-1	When HIGH, LOS is controlled by RXLOS_FORCE_ASSERT.

4.5.2 Transmit Loss of Signal

The transmit path LOS indicator status is available through a register. If desired, its status can be included in the generation of the MODNR or LOSL output pins. The LOS assert threshold can be set from 20mV to 100mV in <1mV steps. In addition the temperature coefficient of the LOS threshold can be adjusted to ensure consistent LOS operation over temperature. The LOS also has hysteresis that is programmable from 0dB to 6dB in steps of less than 0.5dB. A manual LOS assert feature is supported for system diagnostics.

The following registers are used to control the transmit LOS feature:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TX_REG9	39	TXLOS_TH_NEG	7:0	RW	00011011	0-255	Negative temperature coefficient LOS threshold setting.
TX_REG10	40	TXLOS_TH_POS	7:0	RW	00000000	0-255	Positive temperature coefficient LOS threshold setting.
TX_REG11	41	TXLOS_HYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB.
TX_REG12	42	TXLOS_FORCE_ASSERT	3:3	RW	0	0-1	Directly sets the state of TXLOS accordingly if TXLOS_FORCE_ASSERT_EN is HIGH.
		TXLOS_FORCE_ASSERT_EN	4:4	RW	0	0-1	When HIGH, LOS is controlled by TXLOS_FORCE_ASSERT.

4.5.2.1 Tx LOS Threshold

Figure 4-14 and Figure 4-15 show the typical recommended range of Tx LOS assert thresholds and corresponding **TXLOS_TH_NEG[7:0]** setting to achieve these thresholds. It is recommended to keep **TXLOS_TH_POS[7:0]** = 0 to achieve a flat temperature coefficient for LOS threshold. The Tx LOS de-assert thresholds are the same as the Tx LOS assert thresholds for a hysteresis setting of 0.

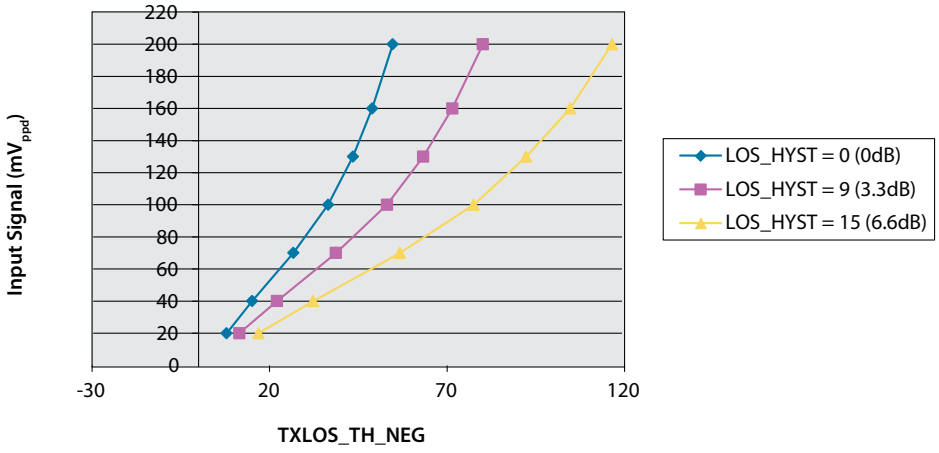


Figure 4-14: Tx LOS Assert Threshold – Typical @ 9.95Gb/s

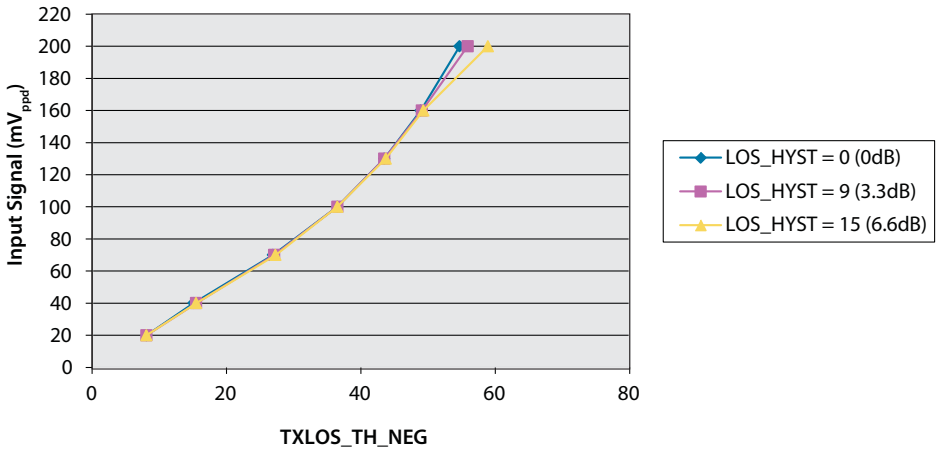


Figure 4-15: Tx LOS De-Assert Threshold – Typical @ 9.95Gb/s

The LOS threshold will have a slight dependence on data rate.

4.5.3 Loss of Lock

The receive path and transmit path LOSS of LOCK (LOL) status indicators are both available in registers as indicated below. These bits can also be included in the MODNR or LOSL outputs:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG10	19	TX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
RXPLL_REG10	29	RX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.

4.5.4 MODNR - Module Not Ready

Various status indicator pins are combined to generate a single MODNR indicator output. The MODNR output is, by default, an open-drain 1.8V – 3.3V LVCMOS-compatible output. It can be configured in a 1.8V LVCMOS-compliant mode through Register 2, bit 3—**OPEN_DRAIN_MODNR**.

The MODNR output is active-high by default. Its polarity can be changed to make it active-LOW through Register 2, bit 0—**POLINV_MODNR**. When set HIGH, MODNR is configured as an active-low output.

The following status indicator controls can be combined to generate the MODNR output. Each of the indicators can be independently masked through register controls. By default, the MODNR output combines (OR's) the status of all indicators.

The following registers control the masking of the various indicators for MODNR and the configuration of MODNR pin.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG1	1	MODNR_MASK_RXLOS	0:0	RW	0	0-1	When HIGH, masks-out RxLOS from asserting MODNR.
		MODNR_MASK_RXLOL	1:1	RW	0	0-1	When HIGH, masks-out RxLOL from asserting MODNR.
		MODNR_MASK_TXLOS	2:2	RW	0	0-1	When HIGH, masks-out TxLOS from asserting MODNR.
		MODNR_MASK_TXLOL	3:3	RW	0	0-1	When HIGH, masks-out TxLOL from asserting MODNR.
		MODNR_MASK_TXFAULT	4:4	RW	0	0-1	When HIGH, masks-out TxFault from asserting MODNR.
TOP_REG2	2	POLINV_MODNR	0:0	RW	0	0-1	When HIGH, inverts polarity of MODNR output.
		OPEN_DRAIN_MODNR	3:3	RW	1	0-1	When HIGH, makes the MODNR output driver open-drain.

4.6 Test Features

The GN2042 contains built-in test features that can be used during module bring-up or for debug purposes. The test features are not guaranteed and are only meant as functional tests under typical conditions. It is not advised to use these features during mission mode operation.

4.6.1 PRBS Generator and Checker

The GN2042 has a built-in PRBS7 generator and checker. The generator and checker are disabled by default to save power, and can be enabled through the digital control interface. There are multiple ways to use the PRBS generator/checker. The PRBS Generator frequency is controlled by the **PRBS_GENERATOR_DATA_RATE_CONTROL[5:0]** register. The PRBS generator and checker are meant to be used only as functional debug tests. The register setting of **PRBS_GENERATOR_DATA_RATE_CONTROL[5:0]** = 20 corresponds to a data rate of typically 10.3Gb/s. The PRBS checker uses the recovered clock from the Tx CDR. Refer to Table 4-5 for more details.

Note: PRBS7 input to the PRBS checker must be non-inverted for the checker to operate correctly. As such, care must be taken when using the polarity invert feature in conjunction with external loop back to PRBS checker to ensure that the data polarity to the checker is correct. Internal loop-back paths are not affected by the polarity invert feature.

The following registers enable and configure the PRBS Generator and Checker:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG3	3	PRBS_GEN_START	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts off the PRBS Generator.
		PRBS_CHK_CLEAR_ERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from the Checker.
TOP_REG6	6	PRBS_CHK_STATUS	0:0	RO	0	0-1	When HIGH, checker detected an error.
LOOPBK_REG1	7	LB_RX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Rx Driver.
		LB_RX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects PRBS generator output into Rx Driver.
LOOPBK_REG2	8	PRBS_CHK_CLK_SEL	1:1	RW	0	0-1	When HIGH, selects the Tx recovered clock. When LOW, selects the Rx recovered clock.
		LB_TX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Tx Driver.
		LB_TX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects PRBS generator output into the Tx Driver.
LOOPBK_REG3	9	PRBS_GENERATOR_DATA_ RATE_CONTROL	5:0	RW	0	0-63	PRBS Generator Frequency Tuning Control. The tuning range is 9.9GHz to 10.4GHz from minimum to maximum setting.
PWRDN_REG2	139	PD_PRBS_GEN	1:1	RW	1	0-1	When HIGH, power-down the PRBS generator and associated buffers.
		PD_PRBS_CHK	2:2	RW	1	0-1	When HIGH, power-down the PRBS checker and associated buffers.

To ensure proper operation of the PRBS7 generator, **PRBS_GEN_START** needs to be set HIGH and then LOW once after the generator is powered-up through **PD_PRBS_GEN**.

To ensure proper operation of the PRBS7 checker, **PRBS_CHK_CLEAR_ERR** needs to be set HIGH and then LOW after application of valid PRBS7 pattern to clear any spurious errors. **PRBS_CHK_STATUS**, may be polled to check for errors flagged by the checker.

The PRBS generator can be configured to apply a PRBS7 pattern to RxSDO or TxSDO.

Table 4-5: PRBS Generator/Checker Configuration

Loopback Mode	Description	PD_PRBS_GEN	PD_PRBS_CHK	PRBS_CHK_CLK_SEL	LB_TX_OUT_PRBS_GEN	LB_RX_OUT_PRBS_GEN	LB_TX_OUT_EN	LB_RX_OUT_EN
PRBS Disabled	Default Mission mode	1	1	X	0	0	0	0
PRBS GEN → Rx Driver → Tx Equalizer → Tx CDR → PRBS CHECKER	External Rx Loopback (tests Tx CDR)	0	0	1	0	1	0	1

4.6.2 Loopback

The GN2042 allows four different loopback paths, and supports loopback on both the electrical side and the optical side. The loopback paths are shown in Table 4-6. The blocks referenced in the different loopback paths are shown in Figure 4-16.

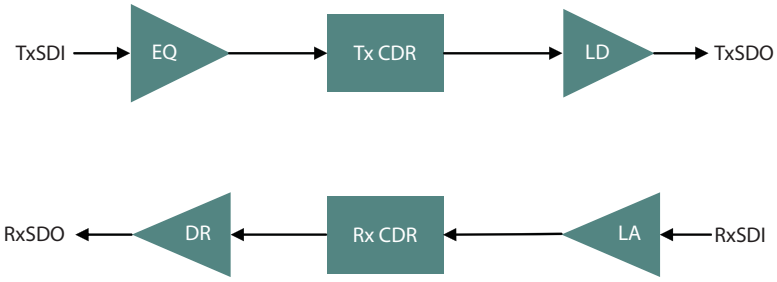


Figure 4-16: Simultaneous Loopback

Table 4-6: Loopback Paths

Mode #	Loopback Path
1	RxSDI → LA→ LD → TxSDO
2	RxSDI → LA → RxCDR → LD → TxSDO
3	TxSDI → EQ → DR → RxSDO
4	TxSDI → EQ → TxCDR → DR → RxSDO

When loopback is enabled, the standard data path is not interrupted. For example: in Mode 1, the input to RxSDI will also be accessible at RxSDO. When using loopback modes, the automute feature for RxSDO or TxSDO may have to be disabled if the corresponding RxSDI or TxSDI inputs are unused.

The relevant parameters and their values required to enable each of the loopback options indicated above, are shown in Table 4-7.

The selection of a loopback path impacts the following features:

- Polarity inversion
- Phase adjust for jitter optimization for TxSDO (LD)

Table 4-7 also captures the impact on these features in each loopback mode.

Table 4-7: Loopback Options

Loop Back Mode (see Table 4-6)	LB_RX_OUT_EN	LB_RX_OUT_TX_DATA	LB_RX_OUT_PRBS_GEN	LB_RX_OUT_RX_CLK	RX_PLL_BYPASS	LB_TX_OUT_EN	LB_TX_OUT_RX_DATA	LB_TX_OUT_PRBS_GEN	LB_TX_OUT_TX_CLK	TX_PLL_BYPASS	TX_PLL_POLINV Effective	TX_SDO_PHADJ Available	RX_PLL_POLINV Effective
1	0	0	0	0	1	1	1	0	0	0	Y	N	N
2	0	0	0	0	0	1	1	0	0	0	Y	N	N
3	1	1	0	0	0	0	0	0	0	1	N	—	Y
4	1	1	0	0	0	0	0	0	0	0	N	—	Y
Control Register Address	7	7	7	7	24	8	8	8	8	14	—	—	—
Associated Bit Slice	4	5	6	7	2	4	5	6	7	2	—	—	—

4.7 Digital Diagnostics

The GN2042 has an on-chip ADC to provide diagnostic information through the digital interface. Refer to the GN204x Family ADC Application Note (PDS-060373) for more details.

4.8 Power-Down Options

The GN2042 provides a high-degree of flexibility in configuring the device for optimal power through power-down registers. Typical usage scenarios are shown. For further description on each of the individual control bits, see Table 5-1, registers **134** to **137**. This section describes the power-down controls for the following sub-systems:

1. Rx LA Power-Down
2. Rx CDR & SDO Power-Down
3. Tx CDR Power-Down
4. Tx SDO Power-Down

Table 4-8: Rx LA Power-Down

RX_PD_PATH	RX_PD_LA	RX_PD_LOS	RX_PD_SLICE_ADJ	Description
1	x	1	1	Completely powers-down the Rx LA.
x	1	1	1	Completely powers-down the Rx LA.
0	0	0	0	All features on. This is diagnostic mode.
0	0	0	1	Powers-down the slice adjust mode.
0	0	1	1	Powers down the SLA and LOS feature for lowest power mode.

Table 4-9: Rx CDR & SDO Power-Down

RX_PLL_BYPASS	RX_PD_PATH	RX_PD_RXCDR	RX_PD_SONET_IJT	RX_PD_RXSDO	RX_PD_RXSDO_EMPHASIS	Description
0	1	x	x	1	1	Completely powers-down the Rx CDR and Rx SDO.
0	x	1	x	1	1	Completely powers-down the Rx CDR and Rx SDO
1	0	x	x	0	1	Main data path through Rx CDR and RxSDO is powered-up for bypass mode. (RxLA has to be powered-up).
0	0	0	1	0	1	Standard operating mode, Rx CDR & SDO enabled in low-power mode. High IJT mode and emphasis are disabled.
0	0	0	0	0	0	Standard operating mode, Rx CDR & SDO enabled. High IJT mode and emphasis are enabled. IJT performance is set by RX_PLL_SELECT_HIGH_IJT registers.
0	0	0	1	0	0	Rx CDR & SDO are enabled. High IJT mode is powered-down. Emphasis is enabled.

Table 4-10: Tx CDR Power-Down

TX_PLL_BYPASS	TX_PD_TXPATH	TX_PD_TXCDR	TX_PD_JIT_FILT	TX_PD_TXSDO	PD_TXSDO_PHASE_ADJ	Description
0	1	1	x	1	x	Completely powers-down the Tx CDR and Tx path.
1	0	1	x	0	1	Main data path through Tx CDR is powered-up for bypass mode. (TxEq has to be powered-up).
0	0	0	1	0	1	Standard operating mode, Tx CDR is enabled in standard mode. Tx SDO jitter optimization through phase adjust is powered-down.
0	0	0	0	0	1	Standard operating mode, Tx CDR is enabled in jitter filter mode. (Requires appropriate configuration of jitter filter controls. See Section 4.3.3).
0	0	0	1	0	0	Standard operating mode, Tx SDO jitter optimization feature through phase adjust is enabled. (Requires appropriate configuration of Tx SDO controls).

Table 4-11: Tx SDO Power-Down

TX_PD_TXPATH	TX_PD_TXSDO	TX_PD_TXCDR	PD_TXSDO_PHASE_ADJ	PD_TXSDO_CPA	PD_APC	Description
1	x	x	x	x	x	Completely powers-down the Tx SDO.
x	1	x	x	x	x	Completely powers-down the Tx SDO.
0	0	0	0	x	x	Enables the Tx SDO jitter optimization through phase adjust feature.
0	0	x	x	1	x	Independently powers-down the Tx SDO cross point adjust feature.
0	0	x	x	x	1	Independently powers-down the Tx SDO Automatic Power Control loop.
0	0	0	0	0	0	Standard operating mode with Tx SDO jitter optimization, crossing point adjust and APC loop enabled.
0	0	0	0	0	0	Tx SDO with all features enabled.

4.9 Device Reset

$\overline{\text{RESET}}$ is an active-low signal with LVTTL/LVCMOS-compatible signalling levels. Due to the timing requirements of $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ to $\overline{\text{RESET}}$, it is recommended that $\overline{\text{RESET}}$ be driven by the Micro on the module. An external 10kΩ pull-down resistor is also recommended on the $\overline{\text{RESET}}$ line. $\overline{\text{RESET}}$ does not have a Schmitt trigger since reset negation is internally synchronized. See Figure 3-10.

4.9.1 Reset State During Power-up

The device requires $\overline{\text{RESET}}$ to be continuously pulled tor GND during power ramp-up. $\overline{\text{RESET}}$ must continue to remain in that state for the minimum specified time after all of the power supplies have reached 90% of their final settling value. Following a $\overline{\text{RESET}}$ assertion at power-up, the device may be reset again at any time with the minimum specified pulse width on $\overline{\text{RESET}}$. Refer to Figure 4-17.

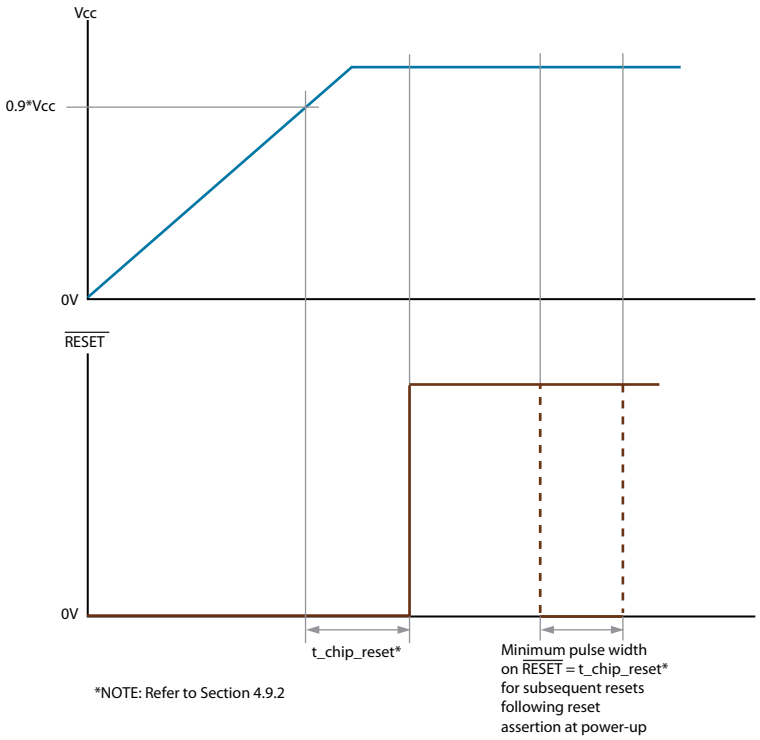


Figure 4-17: Reset State During Power-up

4.9.2 $\overline{\text{RESET}}$ Timing

The following $\overline{\text{RESET}}$ timing specifications apply:

- **t_chip_reset: 10µs**
  Defined as the minimum duration that $\overline{\text{RESET}}$ must be asserted after the supply has reached 90% of final settling value
- **t_ISELb_setup: 500ns**
  Defined as the minimum duration that the $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ pin must be asserted HIGH to select the SPI mode before $\overline{\text{RESET}}$ is negated
- **t_SPI_ready: 500ns**

  Defined as the minimum duration before an SPI/I^2C operation may be initiated, after $\overline{\text{RESET}}$ negation

When I^2C mode is desired, the $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ pin is recommended to be pulled to ground throughout operation of the device.

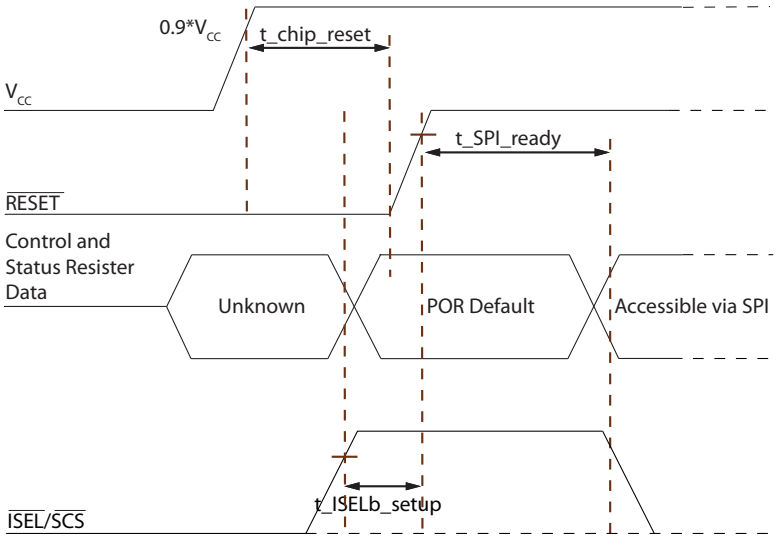


Figure 4-18: GN2042 Device Reset Timing Diagram

4.9.3 I/O and Register States During and After Reset

All configuration registers are set to their post-reset defaults state immediately following $\overline{\text{RESET}}$ assertion.

The following I/O states are applicable upon $\overline{\text{RESET}}$ assertion:

Table 4-12: I/O and Register States During and After Reset

Pin Name	I/O State upon $\overline{\text{RESET}}$ Assertion
SDA/SDIO/MISO	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance with a weak pull-down of 5µA.
SCL/SCLK and SSEL/MOSI	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted, and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance with a weak pull-down of 5µA.
MODNR	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. The loss of lock indicators will assert MODNR HIGH. This output will be high-impedance, and it's state will depend on the external pull-up.
LOSL	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. If a signal is present, the output will be pulled LOW. Otherwise, this output will be high-impedance and it's state will depend on the external pull-up.

4.10 Digital Control Interface

The GN2042 has a tri-mode serial control interface to communicate with the part. Either an I^2C or SPI 3-wire, or SPI 4-wire protocol can be used. The protocol is selected using the $\overline{ISEL}/\overline{SCS}$ and SSEL pins at the time of reset de-assertion.

When pin $\overline{ISEL}/\overline{SCS}$ is held LOW, or left unconnected, and the $\overline{RESET}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in I^2C mode. After reset de-assertion, the state of the $\overline{ISEL}/\overline{SCS}$ pin is a 'don't care'. However, it is recommended that if the pin is not left unconnected, then it be driven LOW.

When the $\overline{ISEL}/\overline{SCS}$ pin is held HIGH, and the SSEL pin is held LOW or left unconnected, and the $\overline{RESET}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in a three-wire SPI mode. After reset de-assertion, the $\overline{ISEL}/\overline{SCS}$ pin functions as the $\overline{SCS}$ pin of a three-wire SPI interface.

When the $\overline{ISEL}/\overline{SCS}$ pin is held HIGH, and the SSEL pin is held HIGH, and the $\overline{RESET}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in a four-wire SPI mode. After reset de-assertion, the $\overline{ISEL}/\overline{SCS}$ pin functions as the $\overline{SCS}$ pin, and the SSEL/MOSI functions as the slave data input pin, and the SDA/SDIO/MISO functions as the slave data output of a four-wire SPI interface.

4.10.1 I^2C Host Interface Mode

The I^2C mode supports standard-mode (100kHz) and fast-mode (400kHz) signalling. The device only supports slave mode. The pins SDA/SDIO and SCL/SCLK are used for bi-directional serial data and clock respectively. Signalling rates lower than the standard-mode and fast-mode rates are also supported by the device.

The GN2042 device slave address is 24_h.

The I^2C protocol is implemented as per the following description:

Each access begins with a 7-bit I^2C slave address word, an 8-bit register address word, followed by one 8-bit data word in a write command, or the device slave address with the read/write bit plus one 8-bit data word in the read command.

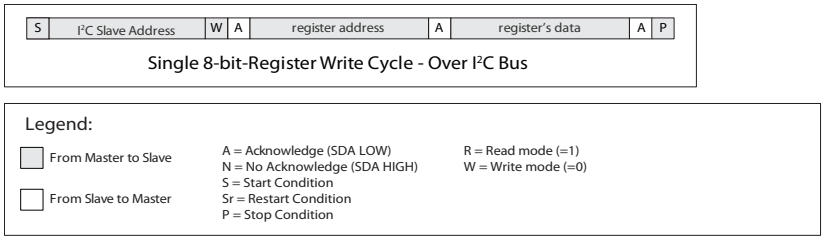


Figure 4-19: Single Register Write Cycle over I²C Bus

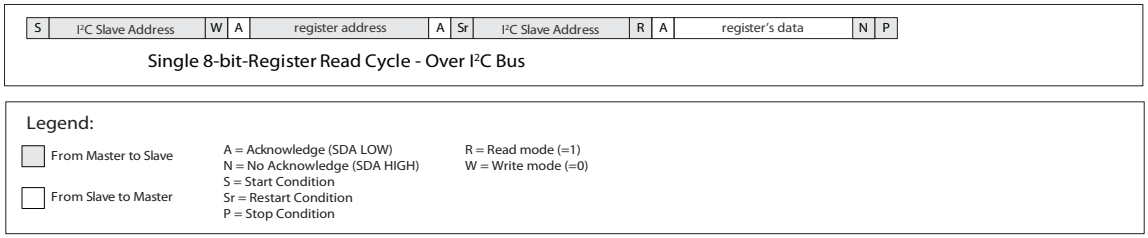


Figure 4-20: Single Register Read Cycle over I²C Bus

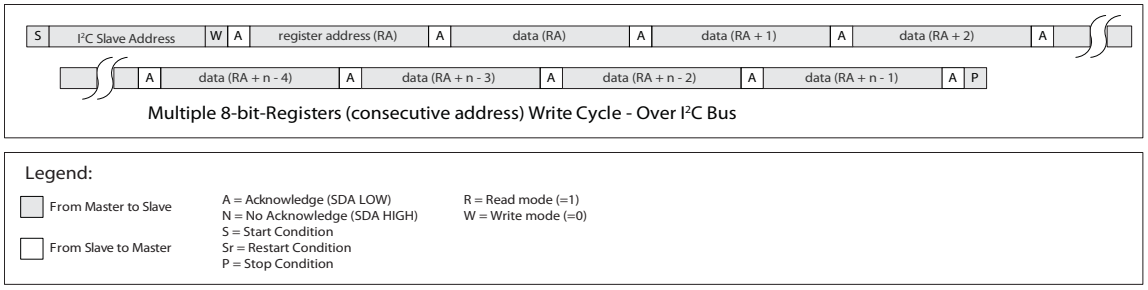


Figure 4-21: Bulk Register Write Cycle over I²C Bus

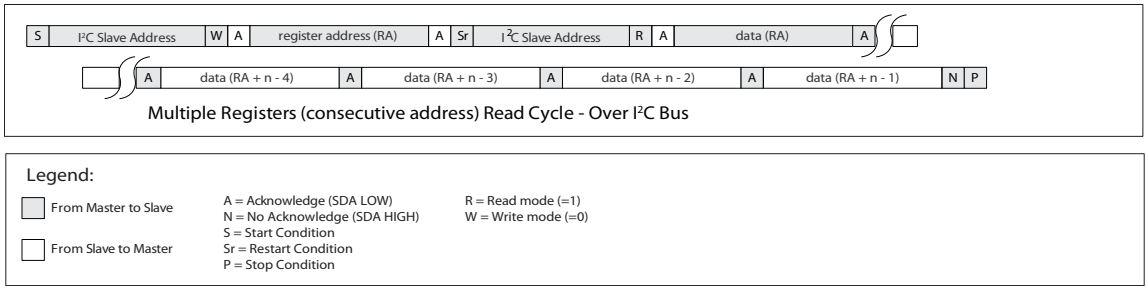


Figure 4-22: Bulk Register Read Cycle over I²C Bus

4.10.2 SPI Host Interface Mode

The GN2042 uses either a 3-wire or a 4-wire SPI protocol. The 3-wire SPI protocol's serial communication takes place via the bi-directional serial data signal (SDA/SDIO). The 4-wire SPI protocol's serial communication uses SSEL/MOSI as its data input and SDA/SDIO as its data output. In both modes, SCL/SCLK is the clock input and $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ is the chip select.

The signalling rate can be up to 10Mb/s. The interface uses 8-bit data and 16-bit address + control.

The 16-bit address + control is made up of an 8-bit address, 1-bit command, 1-bit for auto-increment and 6 unused bits. The 3-wire SPI protocol is implemented as per Figure 4-23 and Figure 4-24. The signal sdo_oen_o is an internal signal indicating the direction of the SDIN_SDOUT pin. When '1', the SDIN_SDOUT pin is configured as an input, when '0', its configured as an output. The 4-wire SPI protocol is implemented as per Figure 4-25.

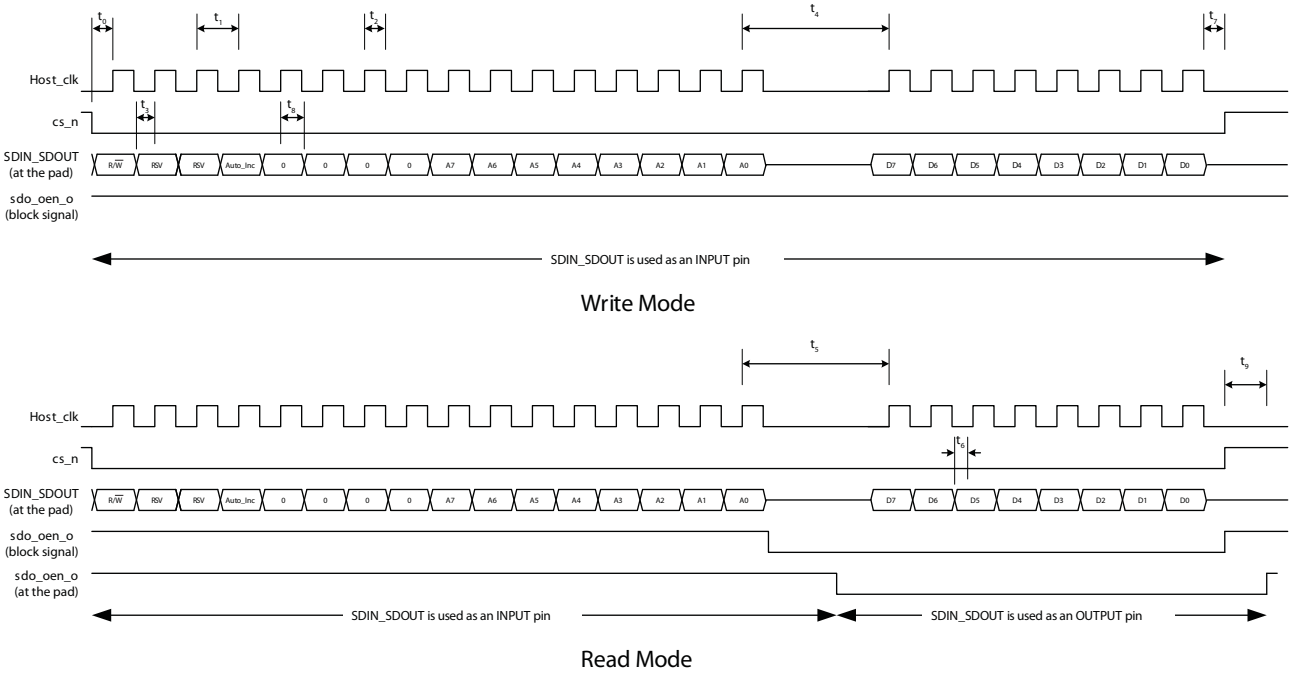


Figure 4-23: SPI Write and Read Timing Diagrams (Single Transaction)

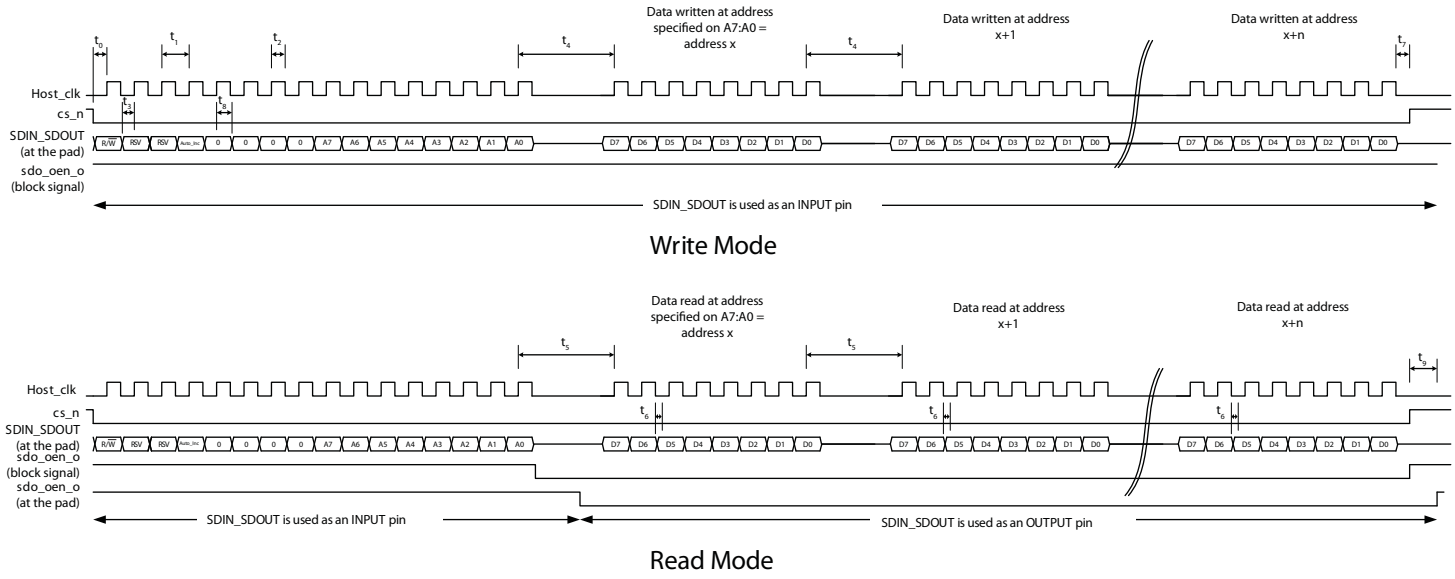


Figure 4-24: SPI Write and Read Timing Diagrams (Auto-Increment Transaction)

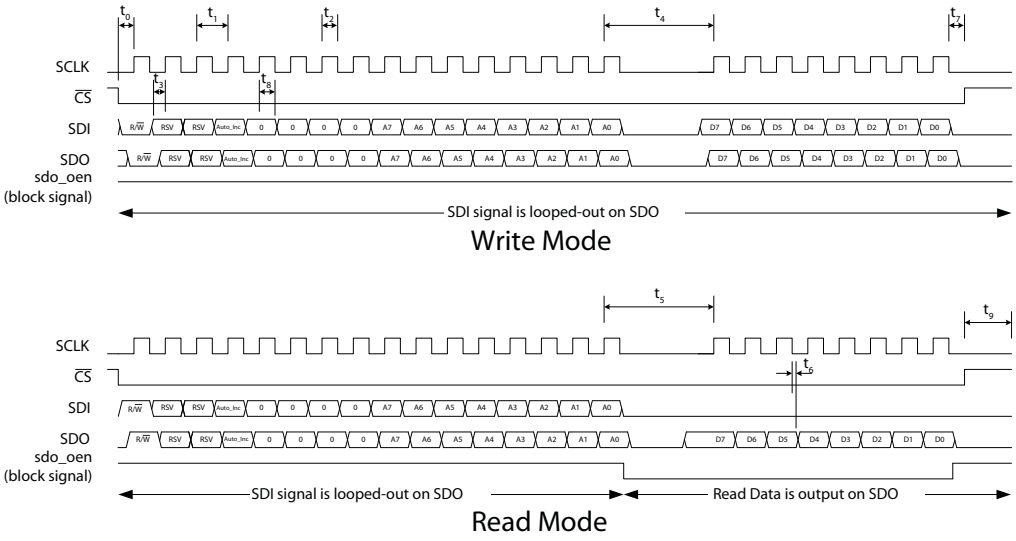


Figure 4-25: SPI Write and Read Timing Diagrams (4-wire)

Table 4-13: SPI Host Interface Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CS_N low before HOST_CLK rising edge	t_0	50% levels; 1.8V operation	1.5	—	—	ns
HOST_CLK period	t_1		100	—	—	ns
HOST_CLK duty cycle	t_2		40	50	60	%
Input data setup time	t_3		1.5	—	—	ns
Time between end of command word (or data in Auto Increment mode) and the first host_clk of the following data word write cycle	t_4		93.5	—	—	ns
Time between end of command word (or data in Auto Increment mode) and the first host_clk of the following data wordread cycle	t_5		420	—	—	ns
Output hold time (15pF load)	t_6		1.5	—	—	ns
CS_N high after last host_clk rising edge	t_7		93.5	—	—	ns
Input data hold time	t_8		1.5	—	—	ns
CS_N high time	t_9		233.6	—	—	ns
CS_N input rise/fall time*	—	20% to 80%	10	—	—	ns

In Figure 4-23, Figure 4-24, and Figure 4-25, CS_N = $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$, HOST_CLK = SCL/SCLK, SDIN_SDOUT = SDA/SDIO, SDI = SSEL/MOSI, and SDO = SDA/SDIO.

There is an auto-increment bit in the command (bit 12) allowing for write burst and read burst transactions.

*The specified minimum rise/fall time must be met to avoid degrading receive sensitivity.

4.10.3 Digital I/O (Schmitt Trigger)

A Schmitt trigger is available on the following signals:

- $\overline{ISEL}/\overline{SCS}$
- SDA/SDIO in input mode
- SCL/SCK in input mode SSEL/MOSI
- SSEL/MOSI

The transfer characteristics of the Schmitt Trigger buffer are shown in Figure 4-26 below:

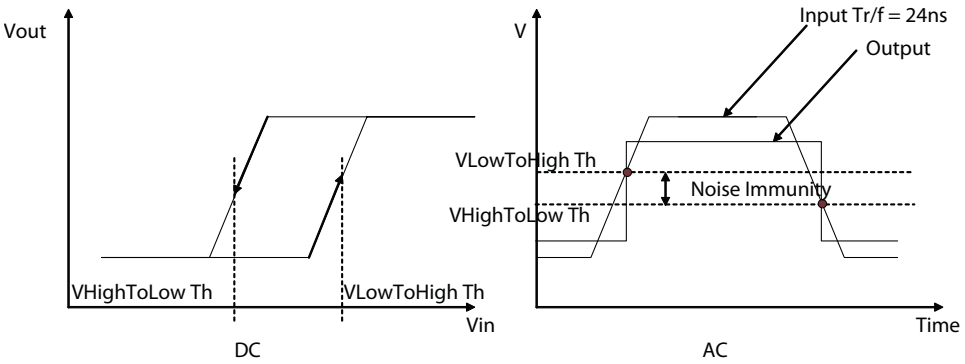


Figure 4-26: Schmitt Trigger Transfer Characteristics

The DC and AC thresholds are shown in Table 2-2: DC Electrical Characteristics.

5. Register Descriptions

Table 5-1: Register Descriptions

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
0	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
1	TOP_REG1	RSVD	7:6	—	0	0-3	Reserved – do not change.
		SPIOUT_OPEN_DRAIN	5:5	RW	0	0-1	0 = Normal SPI operation 1 = Enables SPI output driver open-drain configuration
		MODNR_MASK_TXFAULT	4:4	RW	0	0-1	When HIGH, masks-out TxFault from asserting MODNR.
		MODNR_MASK_TXLOL	3:3	RW	1	0-1	When HIGH, masks-out TxLOL from asserting MODNR.
		MODNR_MASK_TXLOS	2:2	RW	0	0-1	When HIGH, masks-out TxLOS from asserting MODNR.
		MODNR_MASK_RXLOL	1:1	RW	1	0-1	When HIGH, masks-out RxLOL from asserting MODNR.
		MODNR_MASK_RXLOS	0:0	RW	0	0-1	When HIGH, masks-out RxLOS from asserting MODNR.
2	TOP_REG2	LOSL_MASK_TXLOL	7:7	RW	1	0-1	When HIGH, masks-out TxLOL from asserting LOSL.
		LOSL_MASK_TXLOS	6:6	RW	1	0-1	When HIGH, masks-out TxLOS from asserting LOSL.
		LOSL_MASK_RXLOL	5:5	RW	1	0-1	When HIGH, masks-out RxLOL from asserting LOSL.
		LOSL_MASK_RXLOS	4:4	RW	0	0-1	When HIGH, masks-out RxLOS from asserting LOSL.
		OPEN_DRAIN_MODNR	3:3	RW	1	0-1	When HIGH, makes the MODNR output driver open-drain.
		OPEN_DRAIN_LOSL	2:2	RW	1	0-1	When HIGH, makes the LOSL output driver open-drain.
		POLINV_LOSL	1:1	RW	0	0-1	When HIGH, inverts the polarity of the LOSL output.
		POLINV_MODNR	0:0	RW	0	0-1	When HIGH, inverts the polarity of the MODNR output.
3	TOP_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		PRBS_CHK_CLEAR_ERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from the PRBS Checker.
		PRBS_GEN_START	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts the PRBS Generator.
4	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.
5	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
6	TOP_REG6	RSVD	7:1	—	0	0-127	Reserved – do not change.
		PRBS_CHK_STATUS	0:0	RO	0	0-1	When HIGH, the PRBS Checker has detected an error.
7	LOOPBK_REG1	LB_RX_OUT_RX_CLK	7:7	RW	0	0-1	Selects the Rx Clk into the Rx Driver.
		LB_RX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects the PRBS Generator O/P into the Rx Driver.
		LB_RX_OUT_TX_DATA	5:5	RW	0	0-1	Selects the Tx data into the Rx Driver.
		LB_RX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Rx Driver.
		RSVD	3:0	—	0	0-15	Reserved – do not change.
8	LOOPBK_REG2	LB_TX_OUT_TX_CLK	7:7	RW	0	0-1	Selects the Tx Clock into the Tx Driver.
		LB_TX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects the PRBS Generator O/P into the Tx Driver.
		LB_TX_OUT_RX_DATA	5:5	RW	0	0-1	Selects the Rx data into the Tx Driver.
		LB_TX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into Tx Driver.
		RSVD	3:2	—	0	0-3	Reserved – do not change.
		PRBS_CHK_CLK_SEL	1:1	RW	0	0-1	When HIGH, selects the Tx recovered clock. When LOW, selects the Rx recovered clock.
		RSVD	0:0	—	0	0-1	Reserved – do not change.
9	LOOPBK_REG3	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PRBS_GENERATOR_DATA_RATE_CONTROL	5:0	RW	0	0-63	PRBS Generator frequency tuning control. See Section 4.6.1.
10	TXPLL_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TX_PLL_LBW_POS_ADJ	4:0	RW	1110	0-31	Adjusts LBW positive temperature coefficient control. See Section 4.3.2.
11	TXPLL_REG2	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TX_PLL_LBW_NEG_ADJ	4:0	RW	10	0-31	Adjusts LBW negative temperature coefficient control. See Section 4.3.2.
12	RSVD_REG	RSVD	7:0	—	00010010	0-255	Reserved – do not change.
13	RSVD_REG	RSVD	7:0	—	00000101	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
14	TXPLL_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		TX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Tx CDR into bypass mode.
		RSVD	1:1	—	0	0-1	Reserved – do not change.
		TX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.
15	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
16	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
17	TXPLL_REG8	TX_JIT_FILT_TRACK_ADJUST	7:3	RW	00010	0-31	Sets the tracking capability when Tx jitter filter mode is enabled. See Section 4.3.3.
		RSVD	2:0	—	101	0-7	Reserved – do not change.
18	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
19	TXPLL_REG10	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		TX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.
20	RXPLL_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		RX_PLL_LBW_POS_ADJ	4:0	RW	11101	0-31	Adjusts LBW positive temperature coefficient control. See Section 4.2.4.
21	RXPLL_REG2	RSVD	7:5	—	0	0-7	Reserved – do not change.
		RX_PLL_LBW_NEG_ADJ	4:0	RW	111	0-31	Adjusts LBW negative temperature coefficient control. See Section 4.2.4.
22	RSVD_REG	RSVD	7:0	—	00010010	0-255	Reserved – do not change.
23	RSVD_REG	RSVD	7:0	—	00000101	0-255	Reserved – do not change.
24	RXPLL_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the CDR into bypass mode.
		RSVD	1:1	—	0	0-1	Reserved – do not change.
		RX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.
25 to 26	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
27	RXPLL_REG8	RX_PLL_SONET_IJT_SETTING	7:3	RW	10	0-31	Control for Sonet IJT performance. Used in conjunction with Sonet IJT modes 2 and 3 to set IJT performance. Gradually increase setting for increased margins. See Section 4.2.5.
		RX_PLL_LOCK_DCD_TOL_DIS	2:2	RW	1	0-1	When LOW, enables tolerance of data duty cycle distortion for locking.
		RSVD	1:0	—	1	0-3	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
28	RXPLL_REG9	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_PLL_SELECT_HIGH_IJT	3:3	RW	1	0-1	When HIGH, selects high-margin Sonet IJT mode in conjunction with RX_PLL_SONET_IJT_SETTING. See Section 4.2.5.
		RSVD	2:0	—	0	0-7	Reserved – do not change.
29	RXPLL_REG10	RSVD	7:2	—	0	0-63	Reserved – do not change.
		RX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		RX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.
30	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
31	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
32	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
33	TX_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TX_EQ_BOOST	1:0	RW	11	0-3	Controls the Tx path input equalization setting: 00 = 0dB 01 = 2dB 10 = 4dB 11 = 6dB
34	RSVD_REG	RSVD	7:0	—	111111	0-255	Reserved – do not change.
35	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
36	RSVD_REG	RSVD	7:0	—	101	0-255	Reserved – do not change.
37	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
38	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
39	TX_REG9	TXLOS_TH_NEG	7:0	RW	11011	0-255	Negative temperature coefficient LOS threshold setting. Refer to Section 4.5.2.
40	TX_REG10	TXLOS_TH_POS	7:0	RW	0	0-255	Positive temperature coefficient LOS threshold setting. Refer to Section 4.5.2.
41	TX_REG11	RSVD	7:4	—	0	0-15	Reserved – do not change.
		TXLOS_HYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB.
42	TX_REG12	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TXLOS_FORCE_ASSERT_EN	4:4	RW	0	0-1	When HIGH, LOS is controlled by TXLOS_FORCE_ASSERT.
		TXLOS_FORCE_ASSERT	3:3	RW	0	0-1	Directly sets the state of TXLOS accordingly if TXLOS_FORCE_ASSERT_EN is HIGH.
		RSVD	2:0	—	0	0-7	Reserved – do not change.
43	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
44	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
45	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
46	RSVD_REG	RSVD	7:0	—	1111	0-255	Reserved – do not change.
47	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
48	RX_REG1	RSVD	7:4	—	111	0-15	Reserved – do not change.
		RXLA_BOOST_MSB	3:0	RW	0	0-15	RXLA boost control bit MSBs. 0 = 0dB to 15 = 14dB
49	RX_REG2	RXLA_SLICE_ADJ	7:0	RW	0	0-255	Slice adjust magnitude control.
50	RX_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		RXLA_SLICE_ADJ_LO_RANGE	1:1	RW	0	0-1	Selects slice level adjust point. When LOW, slicing point is option 1. When HIGH, slicing point is option 2. See Section 4.2.2.
		RXLA_SLICE_ADJ_POL	0:0	RW	0	0-1	Slice adjust polarity. When HIGH, slice adjust is positive.
51	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
52	RX_REG5	RSVD	7:1	—	1000	0-127	Reserved – do not change.
		RXLA_MANUAL_SLICE_ADJ_EN	0:0	R/W	0	0-1	When HIGH, enables user to adjust slice level at Rx input. See Section 4.2.2.
53	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
54	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
56	RX_REG9	RXLOS_TH_NEG	7:0	RW	1001001	0-255	Negative tempco LOS threshold setting.
57	RX_REG10	RXLOS_TH_POS	7:0	RW	0	0-255	Positive tempco LOS threshold setting.
58	RX_REG11	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RXLOS_HYS	3:0	RW	1001	0-15	Hysteresis control 0-15 -> 0-6dB. Default 9 = 3dB.
59	RX_REG12	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RXLOS_FORCE_ASSERT_EN	3:3	RW	0	0-1	When HIGH, LOS is controlled by RXLOS_FORCE_ASSERT.
		RXLOS_FORCE_ASSERT	2:2	RW	0	0-1	Directly sets the state of RXLOS accordingly if RXLOS_FORCE_ASSERT_EN is HIGH.
		RXLOS_RANGE	1:0	RW	1	0-3	LOS range: 0 = highest 3 = lowest
60	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
61	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
62	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
63	RX_REG16	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RXLA_BOOST_LSB	2:0	RW	0	0-7	RXLA boost control bit LSBs for fine tuning gain with smaller step size. See Section 4.2.3.
64 to 74	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
75	RXSDO_REG1	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_SDO_SWING	3:0	RW	110	0-15	Driver swing: 100mV$_{ppd}$ to 850mV$_{ppd}$, Default = 6 = 400mV$_{ppd}$
76	RXSDO_REG2	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_SDO_EMPHASIS	3:0	RW	0	0-15	Driver emphasis control.
77	RXSDO_REG3	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_SDO_PWR_DN_ON_MUTE	2:2	RW	1	0-1	Enables power-down on mute for output stage.
		RX_SDO_AUTO_MUTE_EN	1:1	RW	1	0-1	Enables muting the driver upon LOS.
		RX_SDO_FORCE_MUTE	0:0	RW	0	0-1	Mutes driver to CM when not in auto mute mode.
78	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
79	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
80	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
81	RSVD_REG	RSVD	7:0	—	11110001	0-255	Reserved – do not change.
82	TXSDO_REG5	RSVD	7:2	—	0	0-63	Reserved – do not change.
		IPH_RANGE_SEL	1:0	RW	10	0-3	IPHOTO range select: 00 = 0mA to 0.25mA 01 = 0.25mA to 0.75mA 10 = 0.75mA to 1.25mA 11 = 1.25mA to 2.14mA
83	RSVD_REG	RSVD	7:0	—	110	0-255	Reserved – do not change.
84	RSVD_REG	RSVD	7:0	—	110110	0-255	Reserved – do not change.
85	TXSDO_REG8	RSVD	7:4	—	0	0-15	Reserved – do not change.
		TXSDO_BIAS_MON_EN	3:3	RW	0	0-1	Enables the laser driver bias monitor circuitry.
		TXSDO_MOD_MON_EN	2:2	RW	0	0-1	Enables the laser driver modulation monitor circuitry.
		RSVD	1:0	—	11	0-3	Reserved – do not change.
86	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
87	TXSDO_REG10	TXSDO_IMOD_LO	7:0	RW	0	0-255	LD modulation current LSB.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
88	TXSDO_REG11	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TXSDO_IMOD_HI	1:0	RWC	0	0-3	LD modulation current MSB.
89	TXSDO_REG12	RSVD	7:6	—	0	0-3	Reserved – do not change.
		TXSDO_CPA	5:0	RW	11111	0-63	LD crossing point adjust: 0~ = > 80% 31 = 50% 63~ = < 20%
90	TXSDO_REG13	TXSDO_PHASE_ADJUST	7:0	RW	0	0-255	LD phase adjust—compensation for jitter generation due to Sonet header.
91	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
92	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
93	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
94	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
95	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
96	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
97	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
98	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
99	TXSDO_REG25	RSVD	7:6	—	0	0-255	Reserved – do not change.
		TXSDO_PWR_DN_ON_MUTE	5:5	RW	1	0-1	When HIGH, enables power-down on mute for output stage.
		TXSDO_AUTO_MUTE_EN	4:4	RW	1	0-1	When HIGH, enables muting the driver upon LOS.
		TXSDO_FORCE_MUTE	3:3	RW	0	0-1	When HIGH, mutes driver to CM when not in auto mute mode.
		TXSDO_FORCE_TXDSBL	2:2	RW	0	0-1	When HIGH, shuts down the LD mod, bias and APC.
		TXSDO_PHASEADJ_DIR	1:1	RW	0	0-1	LD phase adjust (Z0) compensation direction E/L:0/1.
		TXSDO_MOD_SQUELCH	0:0	RW	0	0-1	When HIGH, LD modulation is squelched.
100	TXSDO_REG26	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TXSDO_BIAS_SINK_EN	4:4	RW	0	0-1	LD bias sink is enabled when HIGH. TXSDO_BIAS_SOURCE_EN must be LOW.
		TXSDO_BIAS_SOURCE_EN	3:3	RW	1	0-1	LD bias source is enabled when HIGH. TXSDO_BIAS_SINK_EN must be LOW.
		RSVD	2:0	—	001	0-7	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
101	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
102	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
103	RSVD_REG	RSVD	7:0	—	11000010	0-255	Reserved – do not change.
104	APC_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		APC_SEL_HIGH_REF	4:4	RW	0	0-1	When HIGH, IPHOTO is sourced from the GN2042 and is sunk in the TOSA. When LOW, IPHOTO is sourced from the TOSA and is sunk in the GN2042.
		APC_RESET	3:3	RW	0	0-1	When HIGH, the APC control loop is reset.
		RSVD	2:1	—	0	0-3	Reserved – do not change.
		APC_EN	0:0	RW	1	0-1	When HIGH, enables the APC.
105	APC_REG2	RSVD	7:7	—	0	0-1	Reserved – do not change.
		APC_CLK_RATE_SLOW_DIV	6:4	RW	101	0-7	APC update rate3 divide ratio: 0 = 32 1 = 64 2 = 128 3 = 256 4 = 512 5 = 1024 (default) 6 = 2048 7 = 4096
		APC_CLK_RATE_FAST_DIV	3:2	RW	0	0-3	APC update rate2 divide ratio: 0 = 32 (default) 1 = 64 2 = 128 3 = 256
		RSVD	1:0	—	0	0-3	Reserved – do not change.
106	APC_REG4	APC_DAC_OVR_VAL_LO	7:0	RW	0	0-255	Override value for the APC DAC counter [7:0]. Sets the LD bias current manually when used with APC_DAC_OVR_VAL_HI, and when APC_OVR is HIGH. Step size is approximately 0.15mA.
107	APC_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		APC_OVR	2:2	RW	0	0-1	When HIGH, overrides the APC loop with the DAC override value to set the LD bias current manually.
		APC_DAC_OVR_VAL_HI	1:0	RWC	0	0-3	Override APC DAC [9:8]. A write triggers an update.
108	APC_REG6	APC_REF_DAC_CTRL	7:0	RW	0	0-255	Sets the APC final target reference threshold.
109	APC_REG7	RSVD	7:0	—	01000110	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
110	APC_REG8	RSVD	7:7	—	0	0-1	Reserved – do not change.
		APC_TH_HI_BYPASS	6:6	RW	0	0-1	When HIGH, bypasses Threshold Hi and associated APC clock rate.
		APC_TH_HI	5:0	RW	110110	0-63	APC Threshold Hi setting 110110 (default) - 0.9x of setpoint 1 LSB = 0.0167x of setpoint.
111	APC_REG9	RSVD	7:2	—	0	0-63	Reserved – do not change.
		APC_DAC_VAL_LO	1:0	RO	0	0-3	Read out value from the APC DAC counter [1:0].
112	APC_REG10	APC_DAC_VAL_HI	7:0	RO	0	0-255	Read out value from the APC DAC counter [9:3].
113	TXFLT_REG1	RSVD	7:7	—	0	0-1	Reserved – do not change.
		TXFAULT_CLEAR_STATUS	6:6	RW	0	0-1	When HIGH, clears the latched Tx fault status.
		TXFAULT_DISABLE_EN	5:5	RW	0	0-1	When HIGH, a TxDisable assertion triggers a fault.
		TXFAULT_LD_IPHOTO_EN	4:4	RW	1	0-1	Enables IPHOTO monitoring for Fault.
		TXFAULT_LDMOD_CUR_EN	3:3	RW	1	0-1	Enables LD Modulation monitoring for fault.
		TXFAULT_LDBIAS_CUR_EN	2:2	RW	1	0-1	Enables LD Bias Current monitoring for Fault.
		TXFAULT_LDBIAS_V_EN	1:1	RW	1	0-1	Enables LD Bias Voltage monitoring for Fault.
		TXFAULT_EN	0:0	RW	1	0-1	Enable all Tx Faults.
114	TXFLT_REG2	RSVD	7:3	—	0	0-31	Reserved – do not change.
		TXFAULT_LDBIAS_VTH	2:0	RW	0	0-7	Fault threshold for LD Bias minimum voltage. The fault threshold covers a range of 0 to 800mV on the LDBias pin, in steps of 100mV typical. If LDBias is set to source mode, the fault threshold covers V_{CC} to V_{CC}-800mV in 100mV steps.
115	TXFLT_REG3	TXFAULT_LDBIAS_CUR_TH	7:0	RW	11111111	0-255	Fault threshold for LD Bias maximum current. The fault threshold covers a range of 147mA of LD bias current in steps of 0.575mA typical.
116	TXFLT_REG4	TXFAULT_LDMOD_CUR_TH	7:0	RW	11111111	0-255	Fault threshold for LD Mod maximum current. The fault threshold covers a range of 0-100mA$_{pp}$ LD modulation current in steps of 0.4mA$_{pp}$ typical.
117	TXFLT_REG5	TXFAULT_LD_IPHOTO_TH	7:0	RW	11111111	0-255	Fault threshold for APC IPHOTO maximum voltage.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
118	TXFLT_REG6	RSVD	7:6	—	0	0-3	Reserved – do not change.
		TXFAULT_MUTE_EN	5:5	RW	0	0-1	When HIGH, mutes fault output, faults reported through register status only.
		TXDISABLE_TO_CLEAR_FAULT	4:4	RW	0	0-1	When HIGH, TxDSBL clears faults.
		RSVD	3:0	—	1111	0-15	Reserved – do not change.
119	TXFLT_REG7	RSVD	7:7	—	0	0-1	Reserved – do not change.
		TXFAULT_MODNR	6:6	RO	0	0-1	Reflects the status of the MODNR pin due to TxFault. It can be used to identify the source of the MODNR assertion.
		RSVD	5:5	—	0	0-1	Reserved – do not change.
		TXFAULT_DRV_DISABLE	4:4	RO	0	0-1	Fault status of TxDisable. When HIGH, there is a fault condition.
		TXFAULT_LD_IPHOTO	3:3	RO	0	0-1	Fault status of IPHOTO. When HIGH, there is a fault condition.
		TXFAULT_LDMOD_CUR	2:2	RO	0	0-1	Fault status of LD Mod Current. When HIGH, there is a fault condition.
		TXFAULT_LDBIAS_CUR	1:1	RO	0	0-1	Fault status of LD Bias Current. When HIGH, there is a fault condition.
		TXFAULT_LDBIAS_V	0:0	RO	0	0-1	Fault status of the LD Bias Voltage node. When HIGH, there is a fault condition.
120	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
121	ADC_REG0	RSVD	7:4	—	0	0-15	Reserved – do not change.
		ADC_AUTO_CALIBRATION_EN	3:3	RW	1	0-1	1 = Enables Auto ADC Calibration mode 0 = Disables Auto ADC Calibration mode
		ADC_JUST_LSB	2:2	RW	1	0-1	When HIGH, justify towards LSB. When LOW justify towards MSB.
		ADC_AUTO_CONV_EN	1:1	RW	1	0-1	When HIGH, enables auto conversion, set LOW for manual.
		ADC_RESET	0:0	RW	1	0-1	Reset for the ADC.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
		RSVD	7:4	—	0	0-15	Reserved – do not change.
122	ADC_REG1	ADC_SRC_SEL	3:0	RW	0	0-15	Selects ADC source used for measurement: 0000 = ADC reference voltage 0001 = Laser driver bias monitor 0010 = Photo diode voltage at IPHOTO 0011 = Laser driver modulation monitor 0100 = Temperature sensor (vbe@255µA) 0101 = Temperature sensor (vbe@2.55µA) 0110 = V3p3 supply (0.75*v3p3) 0111 = V1p8 supply (0.5*v1p8) See Section .
123	ADC_REG2	RSVD	7:7	—	0	0-1	Reserved – do not change.
		ADC_CLK_RATE	6:3	RW	11	0-15	ADC clock divide ratio. See Section .
		ADC_RESOLUTION	2:0	RWC	11	0-7	ADC resolution control: 0-6 -> 4,6,8,10,12,14,16 bits. See Section .
124	ADC_REG3	RSVD	7:1	—	0	0-127	Reserved – do not change.
		ADC_START_CONV	0:0	RWC	0	0-1	ADC start conversion.
125	ADC_REG4	RSVD	7:1	—	0	0-127	Reserved – do not change.
		ADC_DONE_CONV	0:0	RO	0	0-1	ADC conversion done flag.
126	ADC_REG5	ADC_OUT_LO	7:0	RO	0	0-255	ADC output low MSB.
127	ADC_REG6	ADC_OUT_HI	7:0	RO	0	0-255	ADC output high MSB.
128	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
129	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
130	TXPWRDN_REG1	RSVD	7:3	—	0	0-31	Reserved – do not change.
		TX_PD_TXSDO	2:2	RW	0	0-1	When HIGH, power-down for the entire laser driver.
		TX_PD_TXCDR	1:1	RW	0	0-1	When HIGH, power-down for the entire Tx CDR.
		TX_PD_TXPATH	0:0	RW	0	0-1	When HIGH, Power-down for the entire Tx path.
131	TXPWRDN_REG2	RSVD	7:2	—	100000	0-63	Reserved – do not change.
		TX_PD_LOS	1:1	RW	0	0-1	When HIGH, power-down for the Tx LOS.
		TX_PD_EQ	0:0	RW	0	0-1	When HIGH, power-down for the Tx input Equalizer.
132	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
133	TXPWRDN_REG4	RSVD	7:1	—	0000111	0-127	Reserved – do not change.
		TX_PD_JIT_FILT	0:0	RW	1	0-1	When HIGH, power-down for the Tx jitter filter.
134	RXPWRDN_REG1	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_PD_RXSDO_EMPHASIS	3:3	RW	1	0-1	When HIGH, power-down for the trace driver pre-emphasis.
		RX_PD_RXSDO	2:2	RW	0	0-1	When HIGH, power-down for the Rx path trace driver.
		RX_PD_RXCDR	1:1	RW	0	0-1	When HIGH, power-down for the entire Rx CDR.
		RX_PD_PATH	0:0	RW	0	0-1	When HIGH, power-down for the entire Rx path.
135	RXPWRDN_REG2	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_PD_LOS	2:2	RW	0	0-1	When HIGH, power-down for the Rx path LOS.
		RX_PD_SLICE_ADJ	1:1	RW	1	0-1	When HIGH, power-down for the LA slice adjust.
		RX_PD_LA	0:0	RW	0	0-1	When HIGH, power-down for the Rx path LA.
136	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
137	RXPWRDN_REG4	RSVD	7:1	—	111	0-127	Reserved – do not change.
		RX_PD_SONET_IJT	0:0	RW	0	0-1	When HIGH, powers-down the Rx path Sonet IJT feature to save power.
138	PWRDN_REG1	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PD_APC	5:5	RW	0	0-1	When HIGH, power-down for APC blocks.
		RSVD	4:4	—	1	0-1	Reserved – do not change.
		PD_TXSDO_CPA	3:3	RW	1	0-1	When HIGH, power-down for the LD crossing point adjust.
		PD_TXSDO_PHASE_ADJ	2:2	RW	1	0-1	When HIGH, power-down for the LD phase adjust (Z0) compensation.
		RSVD	1:1	—	1	0-1	Reserved – do not change.
		PD_TXSDO_PREEMPH	0:0	RW	1	0-1	When HIGH, power-down for the LD pre-emphasis on the rising edge.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
139	PWRDN_REG2	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PD_ADC	5:5	RW	1	0-1	When HIGH, power-down for the ADC.
		PD_SUPPLY_SENSOR	4:4	RW	1	0-1	When HIGH, power-down for the supply sensor.
		PD_TEMP_SENSOR	3:3	RW	1	0-1	When HIGH, power-down for the temperature sensor(s).
		PD_PRBS_CHK	2:2	RW	1	0-1	When HIGH, power-down for the PRBS Checker and associated buffers.
		PD_PRBS_GEN	1:1	RW	1	0-1	When HIGH, power-down for the PRBS Generator and associated buffers.
		RSVD	0:0	—	1	0-1	Reserved – do not change.
140 to 153	RSVD_REG	RSVD	All	—	0	0-255	Reserved – do not change.
154	TXLBW_REG1	RSVD	7:1	—	0	0-127	Reserved – do not change.
		TX_DYN_LBW_ENABLE	0:0	RW	1	0-1	Tx dynamic loop bandwidth block enable: 0 = disabled 1 = enabled
155	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.
156	RSVD_REG	RSVD	7:0	—	00000011	0-255	Reserved – do not change.
157	RSVD_REG	RSVD	7:0	—	00011111	0-255	Reserved – do not change.
158	RSVD_REG	RSVD	7:0	—	00000100	0-255	Reserved – do not change.
159	RXLBW_REG1	RSVD	7:1	—	0	0-127	Reserved – do not change.
		RX_DYN_LBW_ENABLE	0:0	RW	1	0-1	Rx dynamic loop bandwidth block enable: 0 = Disabled 1 = Enabled
160 to 221	RSVD_REG	RSVD	All	—	0	0-255	Reserved – do not change.

6. Applications Information

6.1 Typical Application Circuit

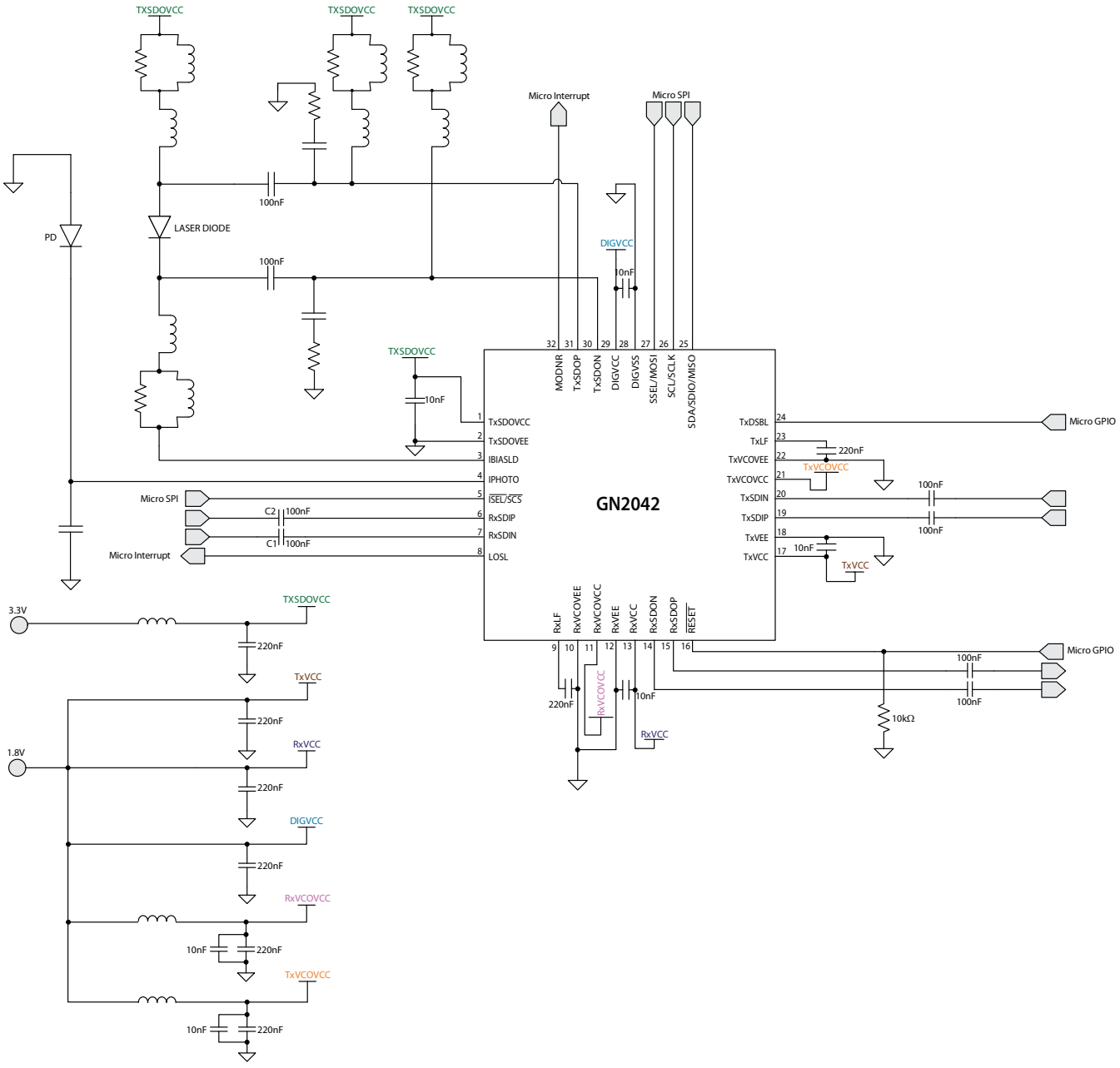


Figure 6-1: Typical Application Circuit

- Use high-quality, temperature-stable LF capacitors. For example, silicon, tantalum or C0G dielectric ceramic capacitors. Lower quality capacitors such as X7R are more sensitive to environmental conditions and may not perform adequately across conditions for this node. Silicone conformal coating can be used with such capacitors as an effective way to mitigate environmental sensitivity

  Note: Please refer to the document "Preventing Loop Filter Capacitor Leakage Current" (PDS-060519) for more information.

- Place lowest value decoupling capacitor closest to the device
- Component values for the TOSA interface must be optimized for the TOSA type
- VCC referenced VPHOTO configuration for APC is shown for a typical TOSA with grounded PD anode. VEE referenced VPHOTO configuration is also supported
- Status indicator connections are shown for a LVCMOS/LVTTL compatible mode. These I/Os can be configured as open-drain with pull-up
- Host interface is shown configured for SPI mode. I^2C mode is also supported

6.2 Power Supply Filter Recommendations

RC filters for isolating supplies are not recommended due to the large currents drawn from each supply.

- The Tx and Rx VCOs do not have independent supplies; additional filtering for the VCOs is not required

For improved isolation between the Tx and Rx paths, and to achieve the best Rx sensitivity and Tx jitter generation, a supply filter such as the one shown in Figure 6-2 is recommended.

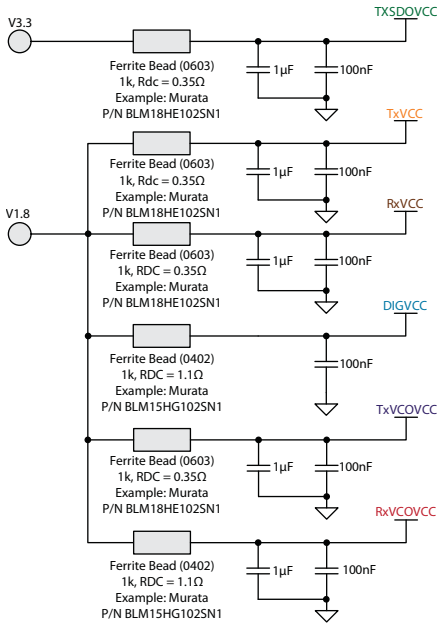


Figure 6-2: Power Supply Filter Recommendations

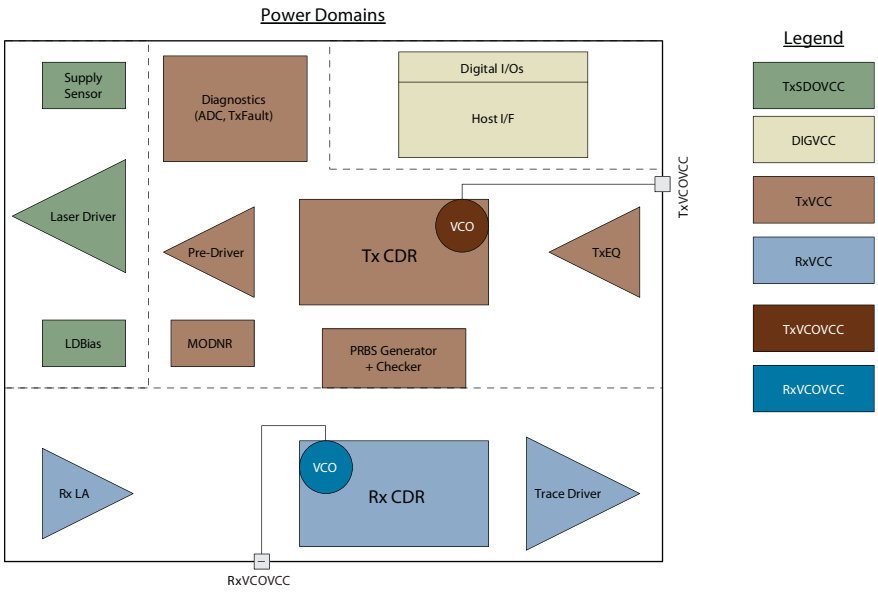


Figure 6-3: Power Supply Domains

6.3 Layout Considerations

The following high-frequency design rules should be considered to achieve optimum performance of the GN2042:

- Use carefully designed controlled-impedance transmission lines with minimal local discontinuities for all high-speed data signals
- Place decoupling capacitors as close as possible to the supply pins
- For optimal electrical and thermal performance, the QFN's exposed pad should be soldered to the module ground plane
- It is recommended to have LF cap ground and VCO caps ground to be common with multiple stitching of vias to ground. Capacitors should be placed from smallest value to largest value away from chip. In addition, the connection from the LF pin to the capacitor should be as small as possible with no vias. Figure 6-4 below demonstrates this technique:

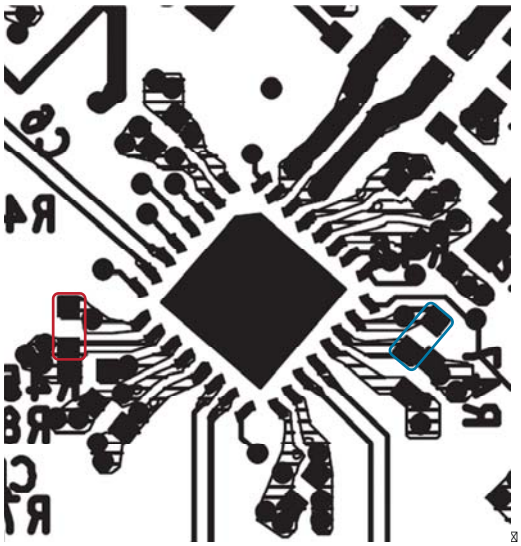


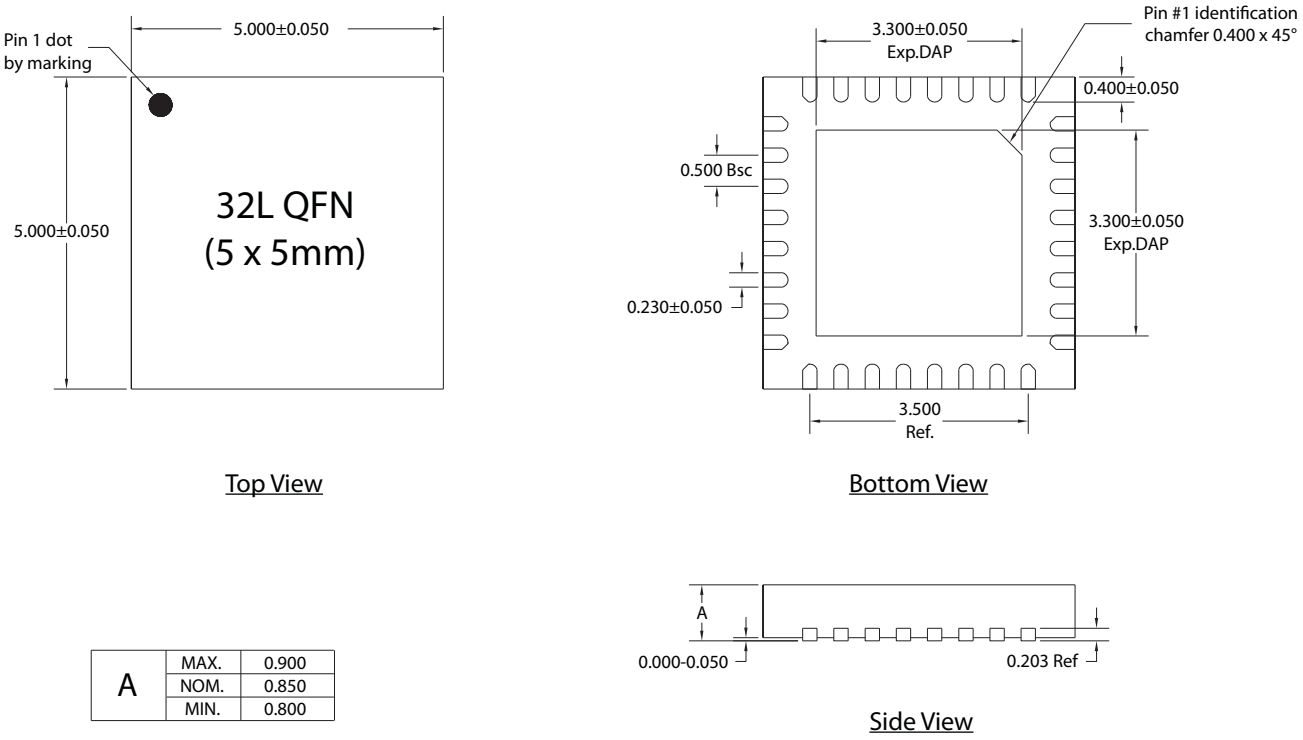
Figure 6-4: Loop Filter Capacitor PCB Layout

- All supply decoupling capacitors should have multiple vias to ground/power planes, and placed as close to chip as possible
- All supplies/grounds should be routed to corresponding decoupling capacitors pads, and never to the centre pad
- The recommended PCB layout for the GN2042 device is shown in Figure 7-2
- Use high-quality, temperature-stable LF capacitors (i.e. capacitors connected to pins 9 and 23). For example: X7R or C0G dielectrics for ceramic capacitors. Lower-quality capacitors with smaller package sizes (e.g. 0201) are more sensitive to environmental conditions and may not perform adequately across conditions for this node. Silicone conformal coating is also an effective way to mitigate environmental sensitivity

7. Package and Ordering Information

7.1 Package Dimensions

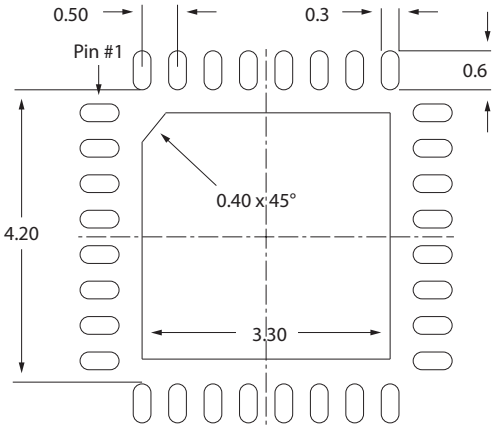
The GN2042 is a 5mm x 5mm, 32-pin QFN.



A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800

Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint



Notes:
1. All dimensions in mm.
2. Drawing not to scale.
3. 16 thermal relief pins, evenly spaced on centre paddle, connected to ground plane.
4. Drill size: 0.254mm.

Figure 7-2: Recommended PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	32-pin QFN / 5mm x 5mm / 0.5mm pad pitch
Moisture Sensitivity Level	1
Junction to Case Thermal Resistance, θ_{j-c}	17.8°C/W
Junction to Air Thermal Resistance (at zero airflow), θ_{j-a}	26.4°C/W
Psi = Junction-to-Top (of Package) Characterization Parameter, Ψ	0.4°C/W
Pb-free and RoHS compliant	Yes

7.4 Solder Reflow Profile

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 7-3.

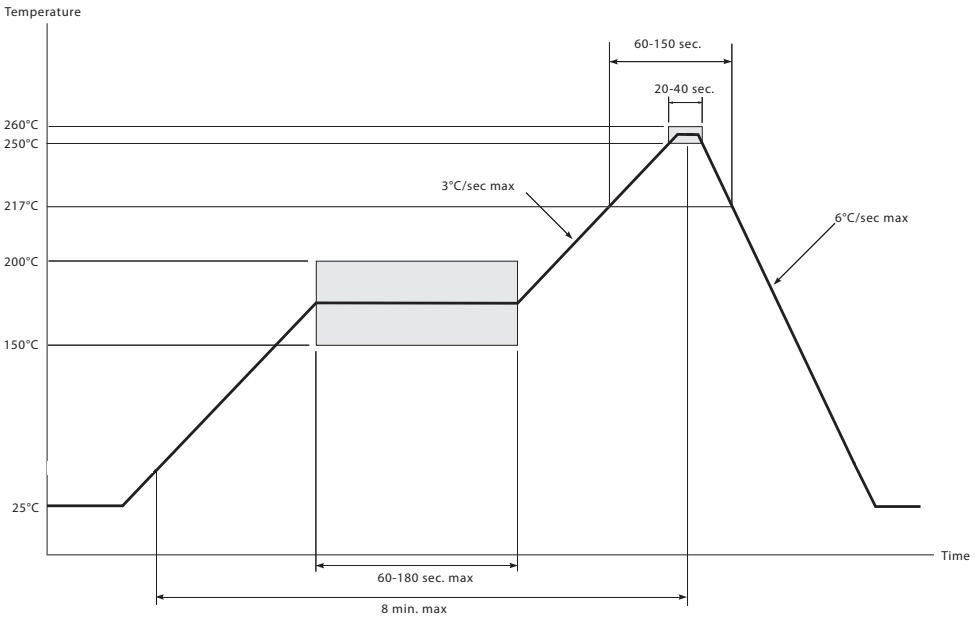


Figure 7-3: Maximum Pb-free Solder Reflow Profile

7.5 Marking Diagram

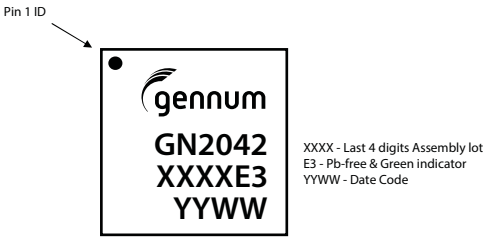


Figure 7-4: Marking Diagram

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Package	Case Temperature Range
GN2042-INE3	32-pin QFN	-40°C to +100°C
GN2042-INTE3D	32-pin QFN (500pc tape and reel)	-40°C to +100°C

DOCUMENT IDENTIFICATION
FINAL DATA SHEET
The product is in production. Semtech reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

GN2044

Dual-CDR Multi-rate Transceiver with EML Driver

Features

- Dual CDR with 9.8 to 11.3Gb/s reference-free operation and integrated EAM/EML laser driver
- Low power to enable SFP+ <1.5W 40km SONET modules
- Integrated Jitter Filter to ensure robust jitter generation performance and margin to the OC192 standards
- APC loop improvements, including:
  - High dynamic range photodiode current detector
- Integrated limiting amplifier with typical sensitivity of 2.5mV
- Digital control through I^2C or SPI interface
- Programmable Jitter Transfer bandwidth
- Bi-directional loopback
- Highly-configurable, including the following programmable features:
  - Limiting Amplifier Equalization
  - Transmit Input Equalization
  - Input Slice Level Adjust
  - LOS with adjustable threshold and hysteresis
  - Tx Fault signalling
  - Polarity invert and mute in both directions
  - Rx Output De-emphasis
  - Tx Output Eye Shaping
- Integrated analog to digital converter, which provides access to digital diagnostic information on supply voltage, die temperature, transmit optical power, modulation current, biasing current, etc.
- Integrated laser safety features
- Pb-free/RoHS-compliant

Applications

- XFP & SFP+ 10Gb/s SONET optical transceivers
- XFP & SFP+ 10GBase-ER/ZR optical transceivers
- XFP DWDM optical transceivers

General Description

The GN2044 is an integrated bi-directional CDR, EML laser driver and limiting amplifier designed specifically to enable low power SFP+ re-timed modules for SONET. Based on the Semtech ClearEdge™ technology, the GN2044 delivers best in class eye quality.

In addition to enabling lower power modules, the GN2044 offers a selectable jitter filter to ensure margin to difficult to meet jitter generation specifications. The GN2044 also features an improved APC loop with extended dynamic range and increased resolution to support a wide variety of TOSAs.

The transmit path consists of optional input equalization, a multi-rate Tx CDR, and an EML laser driver. The receive path is comprised of a limiting amplifier with programmable equalization, a multi-rate Rx CDR, and output de-emphasis. The transmit direction offers a highly-configurable eye shaping feature, including programmable pre-emphasis, which allows for an optimal electrical and optical output. Both directions offer the option for polarity-invert, loopback, and output mute.

The GN2044 has an integrated analog to digital converter, which through the serial interface, provides digital diagnostic information on supply voltage, die temperature, and transmit optical power. The GN2044 also offers integrated laser safety features.

By integrating the laser driver, the GN2044 offers an extremely low-power solution for EML based optical modules. It consumes only 790mW typical from a 3.3V supply and a 1.7V supply, with the laser driver biased at 80mA bias current and $1.9V_{pp}$ single-ended swing.

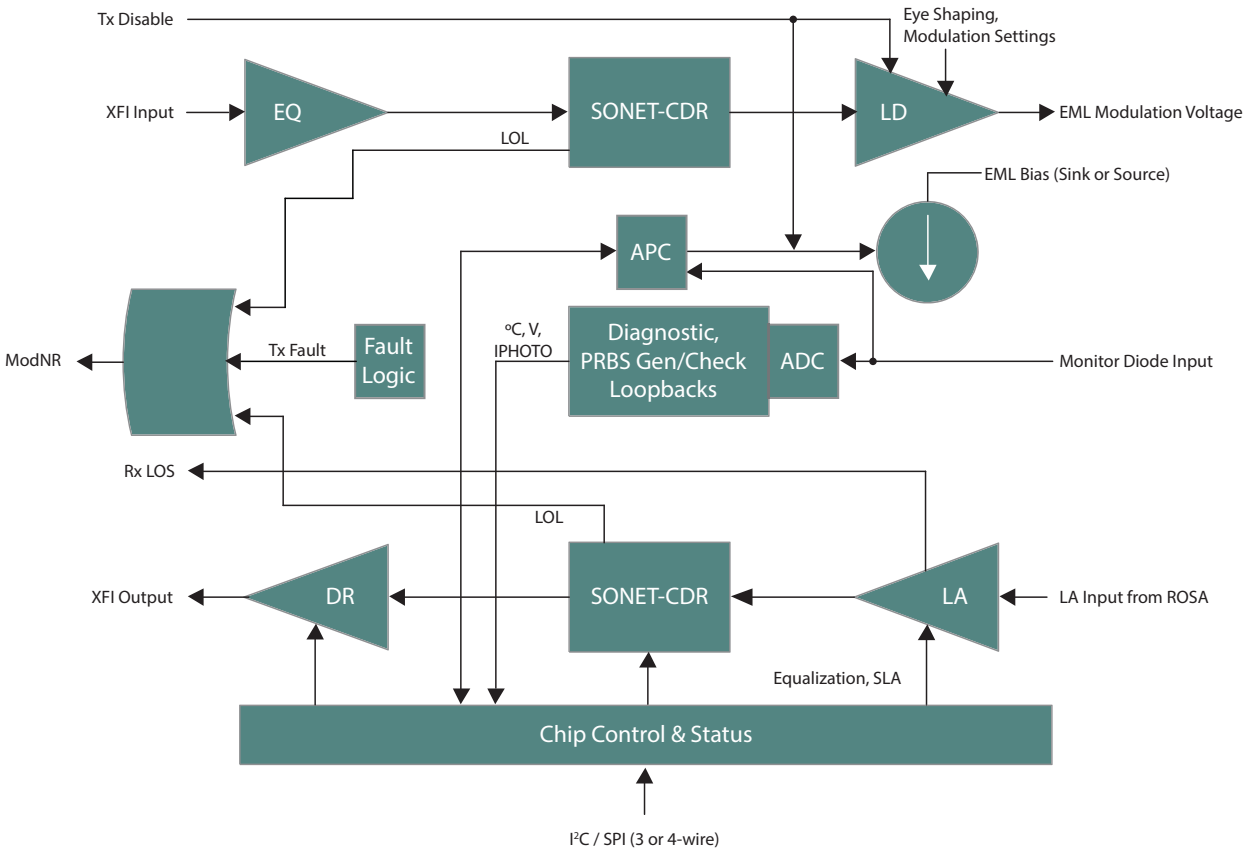


Figure A: GN2044 Functional Block Diagram

EML Laser Driver Features

- Low power EML driver
- Laser bias current up to 120mA
- Option for source or sink bias current
- Modulation swing of up to 2.5V_{pp} single-ended
- 2x 50Ω single-ended terminations
- Transmitter disable pin
- Crossing point adjustment
- Programmable analog pre-emphasis with peaking control
- Jitter Optimization with Phase Adjust feature
- Optional on-chip APC loop
- Programmable Tx Fault signalling

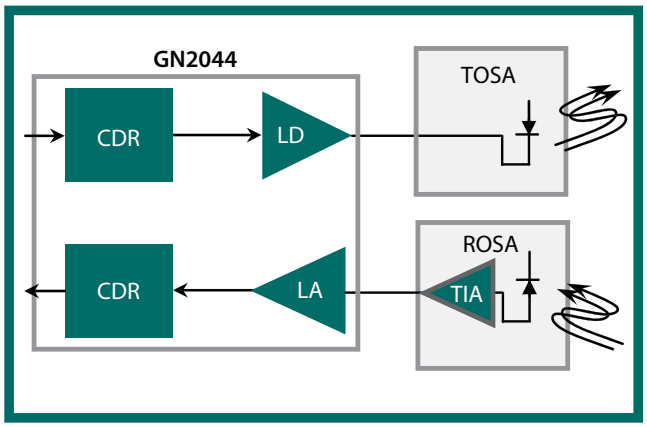


Figure B: Typical Usage - XFP or SFP+ 1310nm to 1550nm Optical Module

Revision History

Version	ECO	Date	Changes and / or Modifications
4	025195	April 2015	Updated Data Rate parameter in Table 2-5: AC Electrical Characteristics.
3	024595	March 2015	Updates.
2	022966	November 2014	Correction to Table 2-2: DC Electrical Characteristics and Table 2-5: AC Electrical Characteristics.
1	021596	November 2014	Converted document to Final Data Sheet. Updates to Electrical Characteristics. Added Power Dissipation and Power Features sections.
0	018845	May 2014	Converted document to Preliminary Data Sheet. Updated document template.
B	015335	September 2013	Updates: Added content to Detailed Description and Register Descriptions.
A	158539	October 2012	New document.

Contents

1. Pin Out

1.1 Pin Assignment

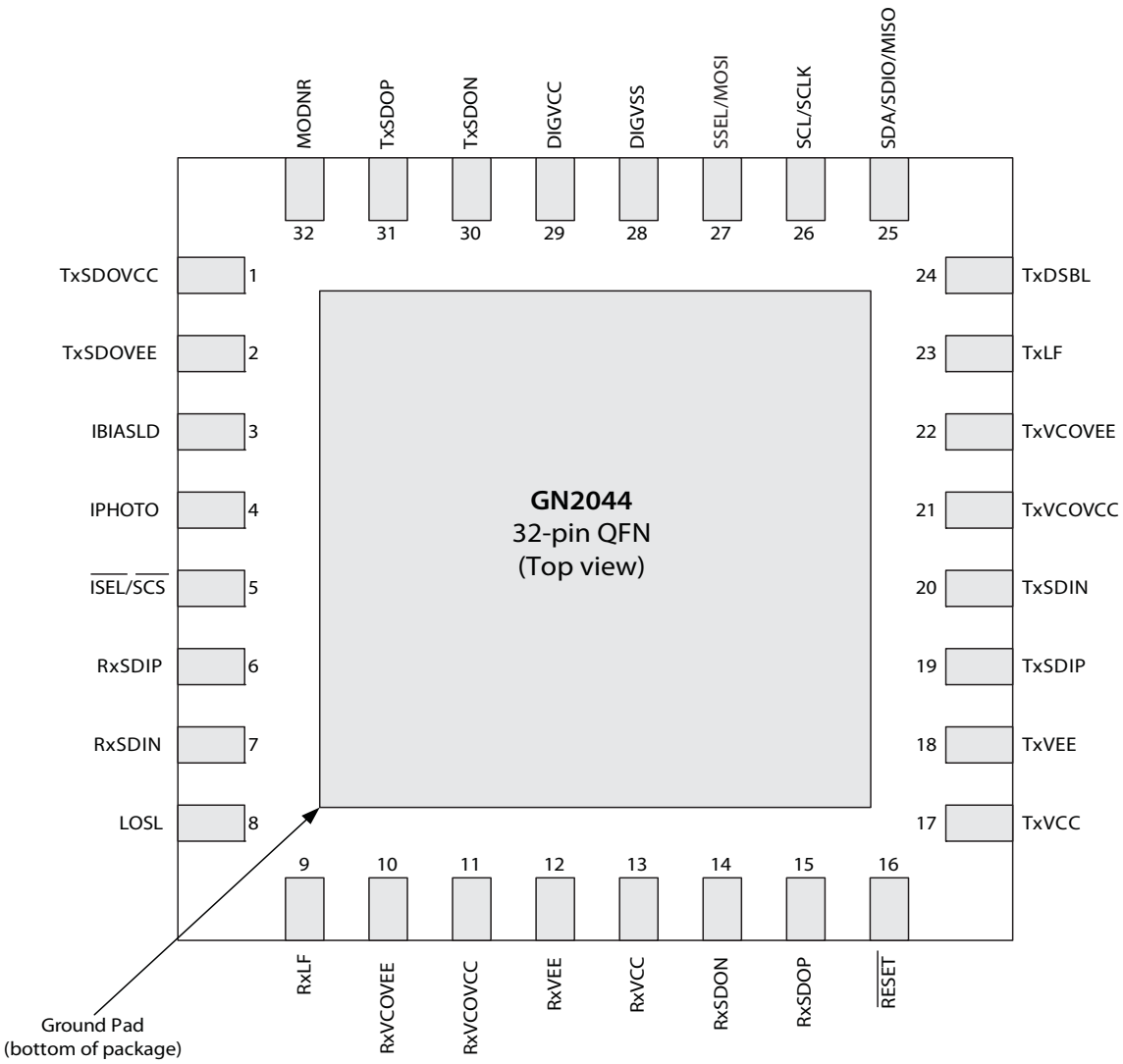


Figure 1-1: Pin Assignment

1.2 Pin Description

Table 1-1: Pin Description

Pin #	Name	Type	Description
1	TxSDOVCC	Power	3.3V power supply for the transmit signal path output.
2	TxSDOVEE	Ground	Ground for the transmit signal path output.
3	IBIASLD	Analog Output	Current sink/source output for external laser DC bias.
4	IPHOTO	Analog Input	Photodiode Monitor Current input. Photodiode current is sensed at the IPHOTO pin. IPHOTO can be configured to sink or source photodiode current, when the photodiode is referenced from a positive supply.
5	$\overline{\text{ISEL}}$/$\overline{\text{SCS}}$	Digital Input	Digital active-low LVTTL/LVCMOS-compliant input. $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ selects the host interface mode during a device reset. When LOW or left unconnected, this pin selects I^2C host interface mode. When HIGH, this pin selects SPI host interface mode on device power-on or reset. $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ is an SPI-compliant active-low chip-select pin in SPI host interface mode. $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ is not used in I^2C host interface mode.
6, 7	RxSDIP, RxSDIN	Input	High-speed input for the receive signal path.
8	LOSL	Digital Output	XFP/SFP+ compliant, active-high. Open-collector Loss-Of-Signal indicator requires an external pull-up resistor. When LOSL is LOW, the transmit and receive signal paths are operating properly. When LOSL is high-impedance, the device has detected a condition that indicates invalid data in the transmit and/or receive signal paths. It consists of a logical OR of the following signals: • Receive signal path CDR Loss of Signal (included by default) • Receive signal path CDR Loss of Lock (masked by default) • Transmit signal path CDR Loss of Signal (masked by default) • Transmit signal path CDR Loss of Lock (masked by default) Loss-of-signal/loss-of-lock inputs from either signal path can be masked or enabled.
9	RxLF	Passive	Loop filter capacitor connection for the receive signal path.
10	RxVCOVEE	Ground	Ground for the receive signal path VCO.
11	RxVCOVCC	Passive	1.8V power supply for the receive signal path VCO.
12	RxVEE	Ground	Ground for the receive signal path and output.
13	RxVCC	Power	1.8V power supply for the receive signal path and output.
14, 15	RxSDON, RxSDOP	Output	High-speed differential output for the receive signal path.
16	$\overline{\text{RESET}}$	Digital Input	Digital active-low 1.8V CMOS-compliant input. Device reset control pin. This is an active pull-down. It is recommended that $\overline{\text{RESET}}$ be pulled down by an external 10kΩ resistor and be driven by the Micro on the module.
17	TxVCC	Power	1.8V power supply for the transmit signal path.
18	TxVEE	Ground	Ground for the transmit signal path.
19, 20	TxSDIP, TxSDIN	Input	High-speed input for the transmit signal path.

Table 1-1: Pin Description (Continued)

Pin #	Name	Type	Description
21	TxVCOVCC	Passive	1.8V power supply for the transmit signal path VCO.
22	TxVCOVEE	Ground	Ground for the transmit signal path VCO.
23	TxLF	Passive	Loop filter capacitor connection for the transmit signal path.
24	TxDSBL	Digital Input	Digital active-high XFP and SFP+ compliant input. When left unconnected or held HIGH, this pin disables the transmit signal path high-speed differential output and the laser DC bias current. When held LOW, the transmit signal path and laser DC bias outputs behave normally. Includes a weak internal pull-up current to disable the laser DC bias current, should this pin be externally disconnected.
25	SDA/SDIO/MISO	Digital Input/ Output	Digital active-high serial data signal for the host interface. Schmitt triggered in input mode. Bi-directional, I^2C-compliant, open-drain driver/receiver in I^2C host-interface mode. Bi-directional, 1.8V CMOS-compliant driver/receiver in 3-wire SPI host-interface mode. 1.8V CMOS-compliant active-high output driver in 4-wire SPI host-interface mode.
26	SCL/SCLK	Digital Input	Digital active-high clock input signal for the serial host interface. Schmitt triggered in input mode. Bi-directional, I^2C-compliant, open-drain driver/receiver in I^2C host-interface mode (SCL). 1.8V CMOS-compliant input in either SPI host-interface mode (SCLK).
27	SSEL/MOSI	Digital Input	Digital active-high 1.8V CMOS-compliant input. SSEL selects the SPI port style when SPI host interface mode is selected: When LOW or left unconnected during device reset, this pin selects 3-wire SPI host interface mode. When HIGH during device reset, this pin selects 4-wire SPI host interface mode on device power on or reset. Following device reset, SSEL/MOSI is an active-high SPI-compliant receiver. SSEL/MOSI is not used in I^2C host interface mode.
28	DIGVSS	Ground	Ground for the low-speed digital I/O and internal logic.
29	DIGVCC	Power	1.8V power supply for the low-speed digital I/O.
30, 31	TxSDON, TxSDOP	Output	High-speed differential output for the transmit signal path. Use TxSDOP to drive the EML TOSA.
32	MODNR	Digital Output	XFP/SFP+-compliant active-high digital output. Open-collector Module-Not-Ready indicator. Requires an external pull-up resistor. When MODNR is LOW, the transmit and receive signal paths are operating properly. When MODNR is high-impedance, the device has detected a condition that indicates invalid data in the transmit and/or receive signal paths. It consists of a logical OR of the following signals: • Transmit signal path CDR Loss of Lock • Transmit signal path CDR Loss of Signal • Transmitter Laser Fault • Receive signal path CDR Loss of Lock • Receive signal path CDR Loss of Signal

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
3.3V Supply Voltage	-0.5 to +3.6V_{DC}
1.8V Supply Voltage	-0.5 to +2.1V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_A < 125°C
Input Voltage Range (any input pin)	-0.3 to (V_{CC} + 0.3)V_{DC}
Solder Reflow Temperature	260°C

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = 1.6V to 1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Power	Bias/Mod Voltage = 0mA/0V_{ppse} Jitter filter mode off		—	279	330	mW	
	Bias/Mod Voltage = 80mA/1.875V_{ppse} Jitter filter mode off		—	790	840	mW	1
	Bias/Mod Voltage = 90mA/2.5V_{ppse} Jitter filter mode off		—	906	963	mW	
Control Logic Input Specifications							
Input Low Voltage		V_{IL}	0	—	0.8	V	—
Input High Voltage		V_{IH}	2.0	—	V_{CC}	V	—
Input Low Current	V_{IL} = 0V	I_{IL}	—	-100	—	µA	—
Input High Current	V_{IH} = 3.3V, V_{CC} = 3.3V	I_{IH}	—	100	—	µA	—

Table 2-2: DC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = 1.6V to 1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Schmitt Trigger Thresholds							
DC Low-to-High Threshold	V_{CC} = 1.9V		0.93	1.05	1.16	V	2
DC High-to-Low Threshold			0.51	0.70	0.85	V	2
DC Low-to-High Threshold	V_{CC} = 1.8V		0.88	0.99	1.13	V	3
DC High-to-Low Threshold			0.41	0.67	0.77	V	3
DC Low-to-High Threshold	V_{CC} = 1.7V		0.83	0.94	1.07	V	—
DC High-to-Low Threshold			0.36	0.59	0.73	V	—
AC Low-to-High Threshold	$V_{CC\_1.8}$ = 1.7V or $V_{CC\_3.3}$ = 3.13V		0.76	0.91	1.06	V	—
AC High-to-Low Threshold			0.44	0.57	0.69	V	—
AC Low-to-High Threshold	$V_{CC\_1.8}$ = 1.9V or $V_{CC\_3.3}$ = 3.46V		0.93	1.06	1.19	V	—
AC High-to-Low Threshold			0.70	0.82	0.93	V	—
Status Indicator Output Specifications							
Indicator Output Logic LOW	I_{SINK}(max) = 3mA	V_{OL}	—	0.2	0.4	V	—
Rx Side Specification							
Input Termination (RxSDIP/N)	Differential		80	100	120	Ω	—
Output Termination (RxSDOP/N)	Differential		80	100	120	Ω	—
Tx Side Specification							
Input Termination (TxSDIP/N)	Differential		80	100	120	Ω	—
Output Termination (TxSDOP/N)	Single-ended		—	50	—	Ω	—
Maximum Laser Modulation Voltage	AC-coupled, single-ended load, $V_{CC} \geq 3.13V$		2.5	3	—	V_{pp}	—
	AC-coupled, single-ended load, $V_{CC} \geq 2.8V$		2	2.5	—	V_{pp}	—
	AC-coupled, single-ended load, $V_{CC} \geq 2.6$		1.5	2	—	V_{pp}	—

Table 2-2: DC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = 1.6V to 1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Maximum Laser Bias Current			120	—	—	mA	—
IPHOTO Range	Minimum setting		—	0.025	—	mA	4
	Maximum setting		—	2	—	mA	
TxDSBL, Input HIGH		V_{IH}	1.2	—	V_{CC} + 0.3	V	—
TxDSBL, Input LOW		V_{IL}	-0.3	—	0.7	V	—

Notes:

1. Each output terminated and power includes dissipation of external 50Ω resistor on non-TOSA side. Typical power is specified at VCC_1.8 = 1.7V and VCC_3.3 = 3.3V. Maximum power is specified at VCC_1.8 = 1.8V and VCC_3.3 = 3.3V.
2. Typical Noise Immunity = 0.34V.
3. Typical Noise Immunity = 0.43V.
4. Can be configured to sink or source photodiode current at the IPHOTO pin when the photodiode is referenced from a positive supply.

2.2.1 Power Dissipation

Table 2-3: Power Dissipation

$V_{CC\_1.8}$	$V_{CC\_3.3}$	Modulation Swing	Bias Current	$V_{CC\_1.8}$ Current	$V_{CC\_3.3}$ Current	Total Current	Total Power
V	V	V_{pp}	mA	mA	mA	mA	mW
1.6	2.6	1.5	0	159	60	219	410
1.7	2.6	1.5	0	164	60	224	435
1.8	2.6	1.5	0	170	60	230	462
1.6	2.6	1.875	0	159	75	234	449
1.7	2.6	1.875	0	164	75	239	474
1.8	2.6	1.875	0	170	75	245	501
1.6	2.6	1.875	80	159	155	314	657
1.7	2.6	1.875	80	164	155	319	682
1.8	2.6	1.875	80	170	155	325	709
1.6	2.8	0	0	159	0	159	255
1.6	2.8	1.875	80	159	155	314	689
1.6	2.8	2.5	90	159	190	349	787
1.7	3.3	0	0	164	0	164	279

Table 2-3: Power Dissipation (Continued)

$V_{CC\_1.8}$	$V_{CC\_3.3}$	Modulation Swing	Bias Current	$V_{CC\_1.8}$ Current	$V_{CC\_3.3}$ Current	Total Current	Total Power
1.7	3.3	1.875	80	164	155	319	790
1.7	3.3	2.5	90	164	190	354	906
1.8	3.3	0	0	170	0	170	306
1.8	3.3	1.875	80	170	155	325	818
1.8	3.3	2.5	90	170	190	360	933

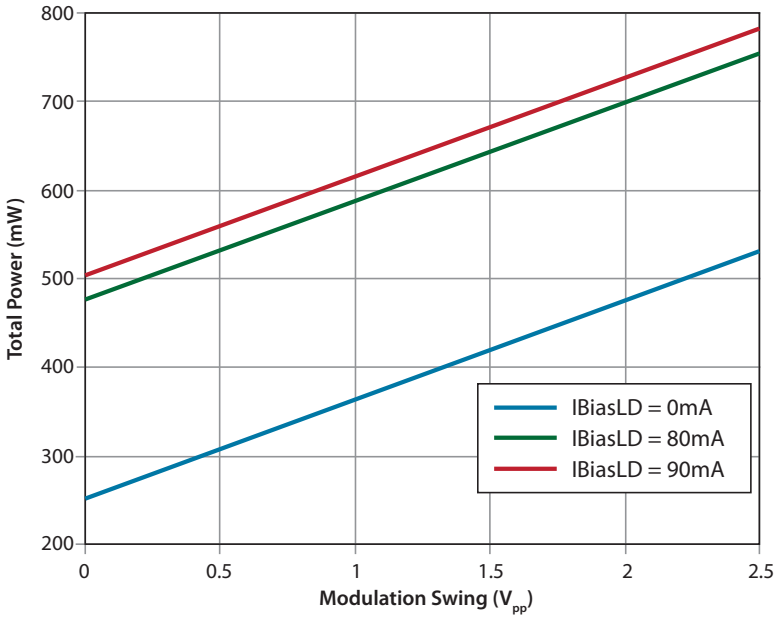


Figure 2-1: Typical Total Power vs. Modulation Voltage and Bias Current for 1.6V/2.8V Setting

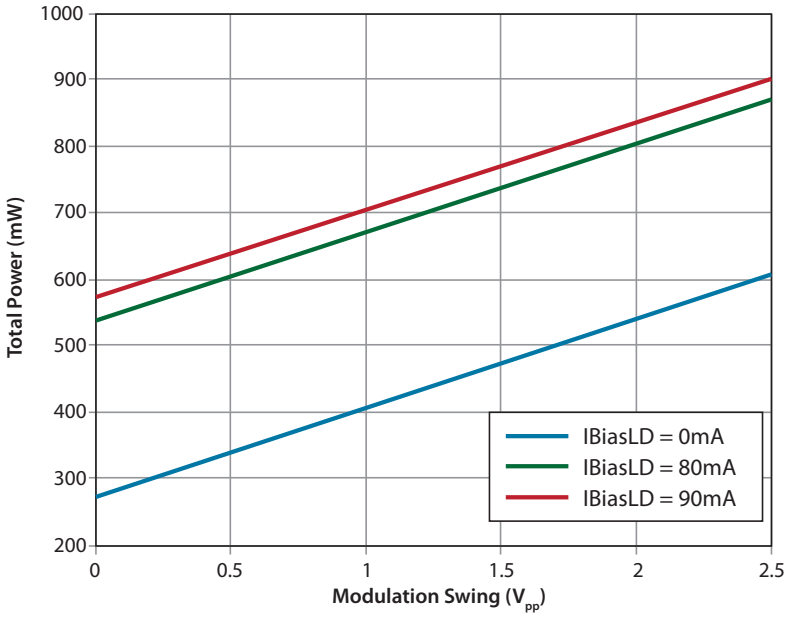


Figure 2-2: Typical Total Power vs. Modulation Voltage and Bias Current for 1.7V/3.3V Setting

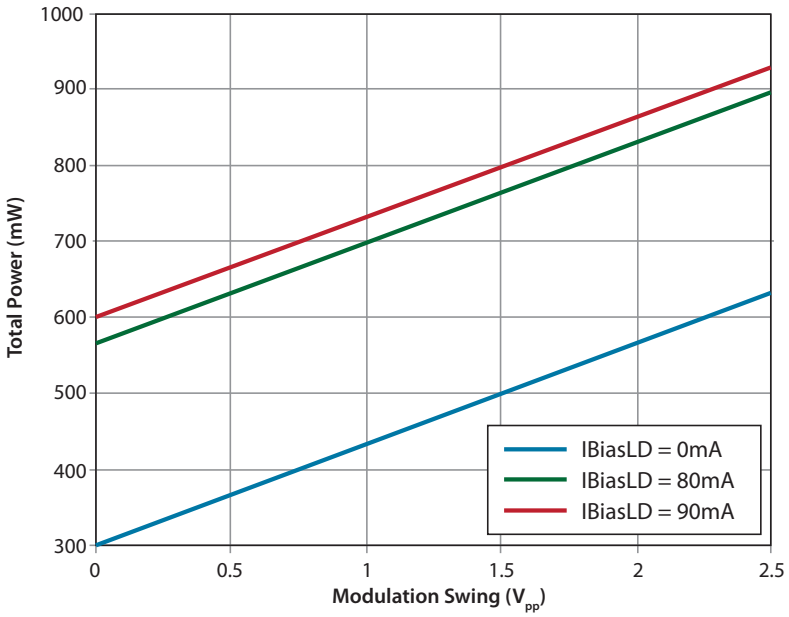


Figure 2-3: Typical Total Power vs. Modulation Voltage and Bias Current for 1.8V/3.3V Setting

2.2.2 Power Features

Table 2-4: Power Features

Feature	Description	Typical Baseline Power (mW)	Typical Delta Power (mW)
Base Power	**V_{mod} = 2.5V_{ppse}, Bias = 90mA**	**906**	
Incremental Power Features			
LA Boost at Maximum			0
Slice Adjust at Maximum			12.3
PRBS7 Generator	Path for PRBS7 Generator to RxSDO is on		40
PRBS7 Checker	PRBS7 Checker is on		56
Diag + ADC	Temperature, Supply Sensor, ADC		7.6
LD CPA at Maximum	Laser Driver Crossing Point Adjust is at maximum		10.3
LD Jitter Optimization with Phase Adjust at Maximum	Jitter optimization through phase adjust is enabled for laser driver		18.8
LD Rise Pre-emphasis at Maximum Setting			27.4
Tx Jitter Filter Mode Enabled	Tx jitter filter tracking capability set to maximum		9.5
Rx Swing at Maximum			122.7
Power Saving Features			
with Rx CDR Bypassed and Powered-down			-64.1
with Rx and Tx CDR Bypassed and Powered-down			-124.7
with Rx Path Powered-down			-103.6
RxSDO Muted			-25.1
TxSDO Muted			-344.4
Rx IJT Mode 1			-18.5
Rx IJT Mode 2			-15

2.3 AC Electrical Characteristics

Table 2-5: AC Electrical Characteristics

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Data Rate	Default configuration, $V_{CC\_1.8V} \geq 1.71V$		9.8	10.3125	11.35	Gb/s	—
	Default configuration, $V_{CC\_1.8V} < 1.71V$		9.8	10.3125	11.3	Gb/s	—
Rx Side Specification							
Input Sensitivity			—	2.5	8	mV_{ppd}	—
Input Overload			1200	—	—	mV_{ppd}	—
Limiting Amplifier Equalization	Max EQ setting		14	—	—	dB	1
Input Sinusoidal Jitter Tolerance	f = 100kHz		20	30	—	UI_{pp}	2, 3
	f = 400kHz		2.5	8	—	UI_{pp}	3
	f = 4MHz		0.5	1.4	—	UI_{pp}	3
	f = 80MHz		0.3	0.5	—	UI_{pp}	3
Jitter Transfer Bandwidth Setting Range	Minimum programmable setting		—	2.2	—	MHz	—
	Maximum programmable setting		—	13	—	MHz	—
Jitter Peaking	With 6MHz LBW, loop filter capacitor = 220nF		—	—	0.03	dB	—
RxSDO Output Total Jitter	PRBS31 data, BER = 10^{-12}, 11.3Gb/s with optimized boost and swing settings	TJ	—	0.08	0.16	UI_{pp}	—
RxSDO Output Deterministic Jitter	PRBS31 data, BER = 10^{-12}, 11.3Gb/s with optimized boost and swing settings	DJ	—	0.05	0.088	UI_{pp}	—

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
RxSDO Output Rise/Fall Time	20% to 80%	t_r, t_f	—	—	24	ps	4
RxLOS De-assert Threshold Level Setting Range	Minimum programmable setting		—	5	—	mV_{ppd}	—
	Maximum programmable setting		—	400	—	mV_{ppd}	—
RxLOS Threshold Level Variation	1 sigma IC to IC, RXLOSRANGE = 0,1		—	1.0	—	dB	—
	1 sigma IC to IC, RXLOSRANGE = 2		—	2.0	—	dB	—
	Over V_{CC} range		—	1.0	—	dB	—
	Over temperature range -40°C to +95°C, threshold level > $20mV_{ppd}$		—	1.5	—	dB	—
RxLOS Threshold Level Hysteresis Setting Range	Electrical		0	—	6	dB	—
RxLOS Response Time			3	5	20	µs	—
Slice Level Adjust Range	Maximum setting		200	—	—	mV	—
Rx CDR Lock Time	Default mode: loop filter cap = 220nF, minimum LBW		—	—	1	ms	—
Differential Output Voltage Setting Range	Minimum swing setting		90	120	130	mV_{ppd}	—
	Maximum swing setting		630	800	910	mV_{ppd}	—
Output Pre-emphasis Setting Range	Maximum pre-emphasis setting. Output swing = $350mV_{ppd}$		6	—	—	dB	—
RxSDI Differential Return Loss	<5GHz		—	-14	—	dB	—
	5GHz to 10GHz		—	-10	—	dB	—
RxSDO Differential Return Loss	<5GHz		—	-16	—	dB	—
	5GHz to 10GHz		—	-8	—	dB	—

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Tx Side Specification							
Input Sensitivity			—	15	30	mV_{ppd}	—
Input Overload			1200	—	—	mV_{ppd}	—
LOS Threshold Level Setting Range	Minimum programmable setting		—	20	—	mV_{ppd}	—
	Maximum programmable setting		—	100	—	mV_{ppd}	—
Equalization Gain	Maximum programmable setting		—	6	—	dB	5
Input Sinusoidal Jitter Tolerance – jitter filter mode off	f = 120kHz, maximum LBW		7	10	—	UI_{pp}	6, 7
	f = 4MHz		0.4	0.6	—	UI_{pp}	7
	f = 80MHz		0.35	0.5	—	UI_{pp}	7
Input Sinusoidal Jitter Tolerance – jitter filter mode on	f = 120kHz, maximum LBW		10	16	—	UI_{pp}	6, 7
	f = 4MHz		0.4	0.6	—	UI_{pp}	7
	f = 80MHz		0.35	0.5	—	UI_{pp}	7
Jitter Transfer Bandwidth Setting Range	Minimum programmable setting		—	1.5	—	MHz	—
	Maximum programmable setting		—	10.3	—	MHz	—
Jitter Peaking	With 6MHz LBW, loop filter capacitor = 220nF		—	—	0.03	dB	—
Jitter Generation	50kHz to 80MHz		—	34	—	mUI_{pp}	9
	4MHz to 80MHz		—	22	—	mUI_{pp}	9

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Total Output Jitter	TXSDOIMOD = $1.9V_{pp}$, PRBS31 data, BER = 10^{-12}, 11.3G, with optimized phase adjust; measured on TxSDOP	TJ	—	0.1	0.18	UI_{pp}	—
Tx CDR Lock Time			—	—	1	ms	8
TxSDO Output Rise/Fall Time	20% to 80%	t_r, t_f	—	26	35	ps	—
TxSDI Differential Return Loss	<5GHz		—	-15	—	dB	—
	5GHz to 10GHz		—	-13	—	dB	—
TxSDO Differential Return Loss	<5GHz		—	-16	—	dB	—
	5GHz to 10GHz		—	-8	—	dB	—
Output Crossing Point Adjust Setting Range	Minimum setting		—	20	—	%	—
	Maximum setting		—	80	—	%	—
Maximum Phase Adjust for Jitter Optimization			—	30	—	ps	—
Tx Output Pre-emphasis Amplitude	Tx Mod Voltage = $1.9V_{ppse}$		0	500	—	mV_{ppse}	9

Notes:

1. At 5.35GHz.
2. At jitter frequencies <100kHz, the GN2044 jitter tolerance performance exceeds the SONET GR-253 RX Tolerance specifications.
3. With default loop bandwidth setting, IJT mode 3 and IJT setting 31.
4. Measured at host-side of XFP or SFP+ connector.
5. At 5.35GHz (dielectric loss).
6. At jitter frequencies <120kHz, the GN2044 jitter tolerance performance exceeds the XFI module transmitter input telecom sinusoidal jitter tolerance specifications (XFP MSA Revision 4.0, Figure 16).
7. In addition to XFI input jitter tolerance requirements.
8. No signal-to-signal (PRBS31 pattern).
9. Measured on TxSDOP channel with optimized phase adjust.

3. Input/Output Circuits

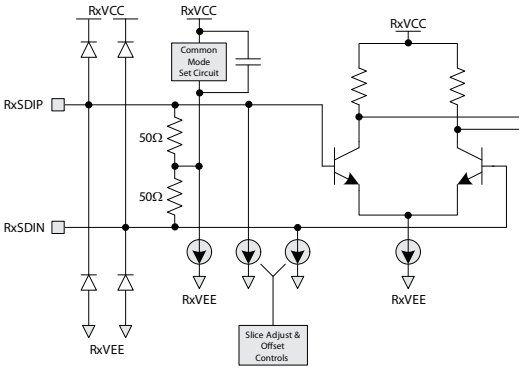


Figure 3-1: RxSDI

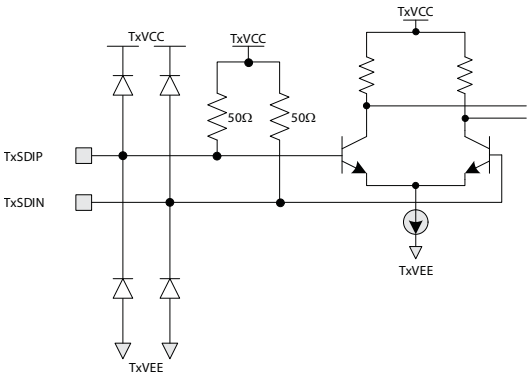


Figure 3-2: TxSDI

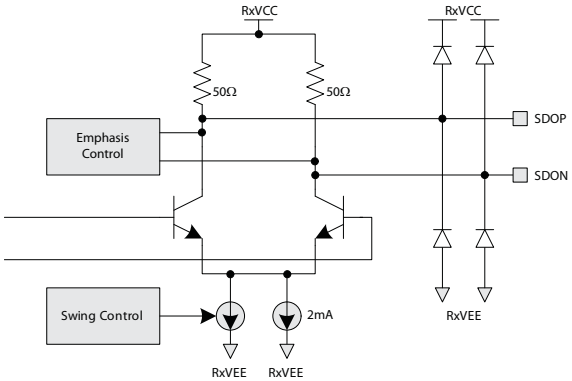


Figure 3-3: RxSDO

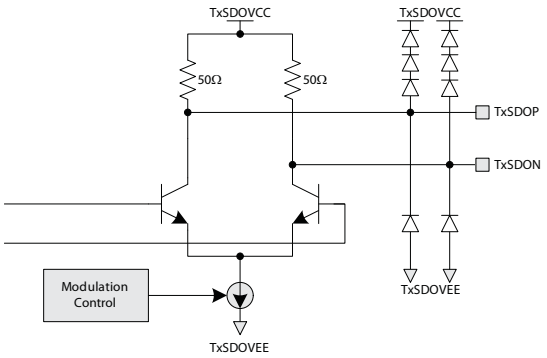


Figure 3-4: TxSDO

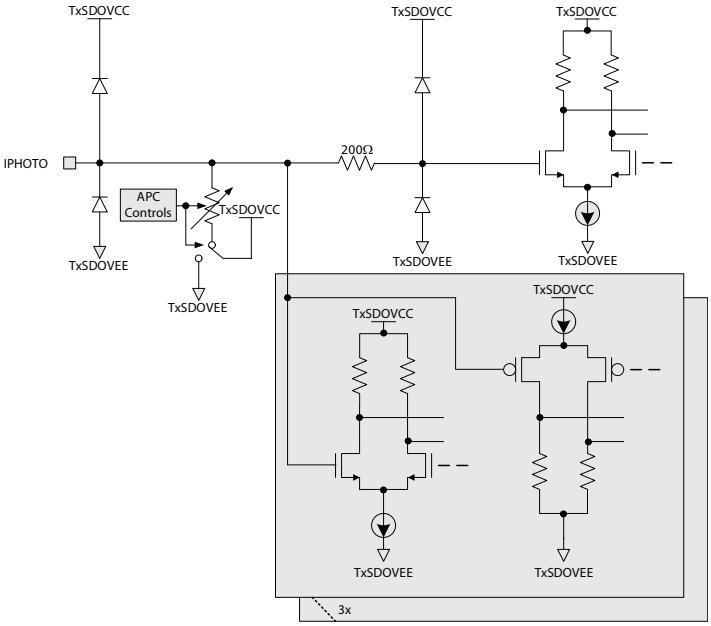


Figure 3-5: IPHOTO

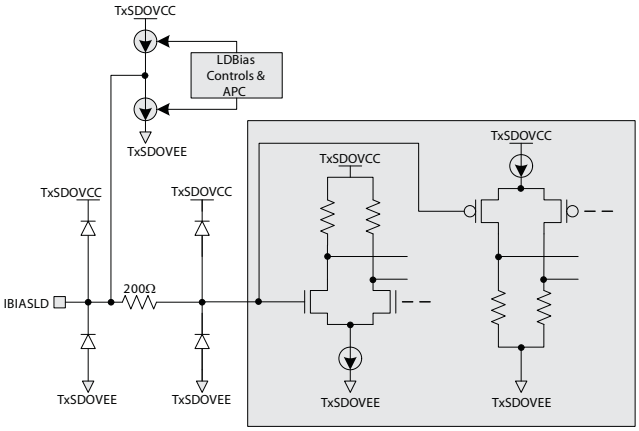
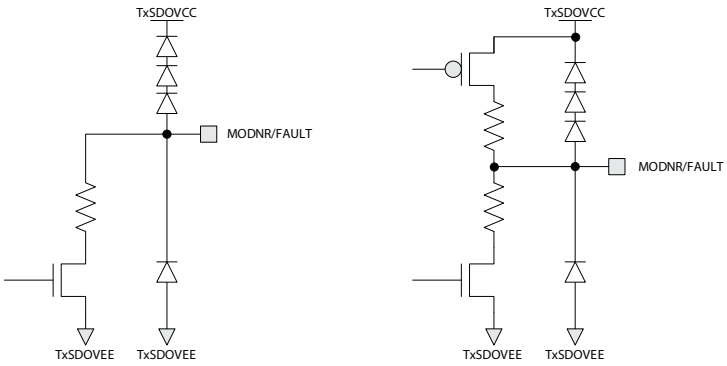


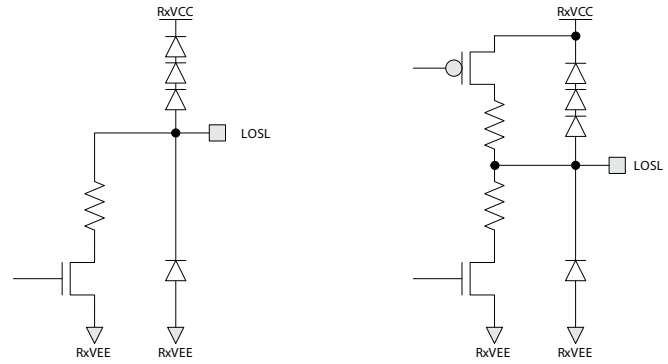
Figure 3-6: IBIASLD



Configured as open-drain

Configured as LVCMOS

Figure 3-7: MODNR/FAULT



Configured as open-drain

Configured as LVCMOS

Figure 3-8: LOSL

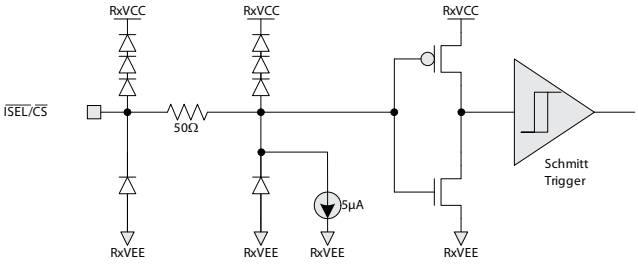


Figure 3-9: $\overline{\text{ISEL}}/\overline{\text{SCS}}$

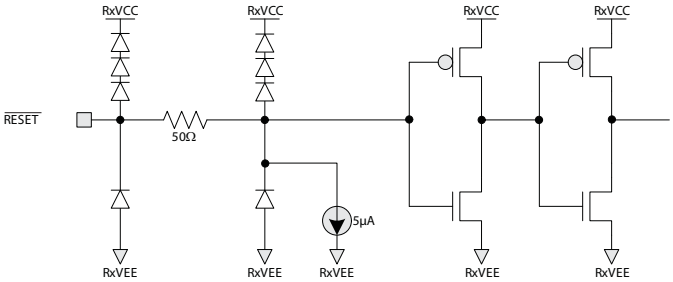


Figure 3-10: $\overline{\text{RESET}}$

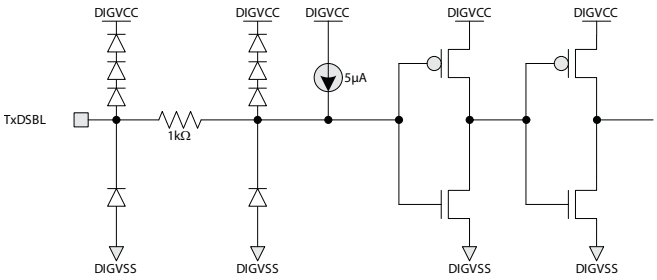


Figure 3-11: TxDSBL

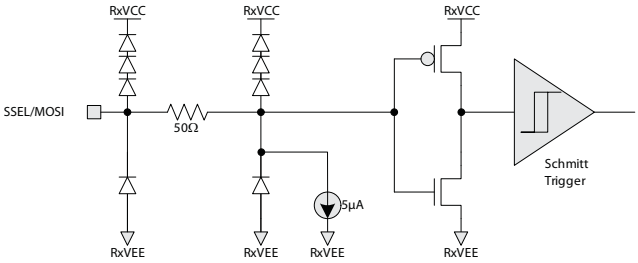


Figure 3-12: SSEL/MOSI

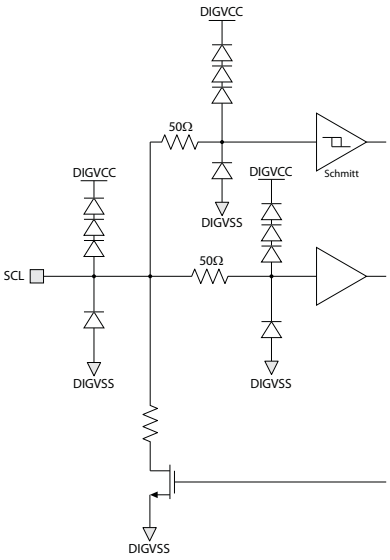


Figure 3-13: SCL

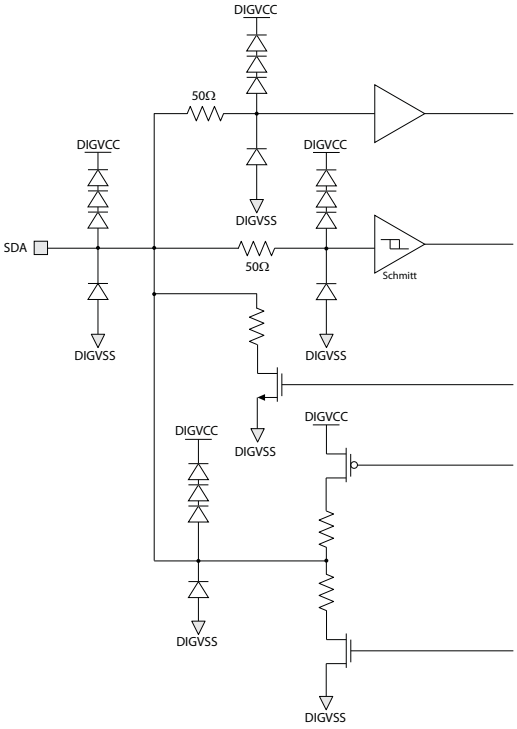


Figure 3-14: SDA

4. Detailed Description

4.1 Multirate CDR Functionality

The GN2044 supports a range of data rates, so that a single part can be used for multiple applications. The GN2044 does not require a reference clock. Some example applications are as follows:

- 10Gb/s Ethernet (10.3Gb/s)
- 10Gb/s Ethernet with FEC (11.1Gb/s)
- 10G Fibre Channel (10.5Gb/s)
- 10G Fibre Channel with FEC (11.3Gb/s)
- SONET OC192 (9.95Gb/s)
- 9.8Gb/s CPRI

4.1.1 Retimer Bypass

The device can be configured to manually bypass each of the Rx and Tx CDRs through the **TX_PLL_BYPASS** and **RX_PLL_BYPASS** controls.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG5	14	TX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Tx CDR into bypass mode.
RXPLL_REG5	24	RX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Rx CDR into bypass mode.

4.2 Receive Path

The GN2044 receive path contains a high-sensitivity limiting amplifier with optional equalization, a multi-rate CDR, and an emphasis driver.

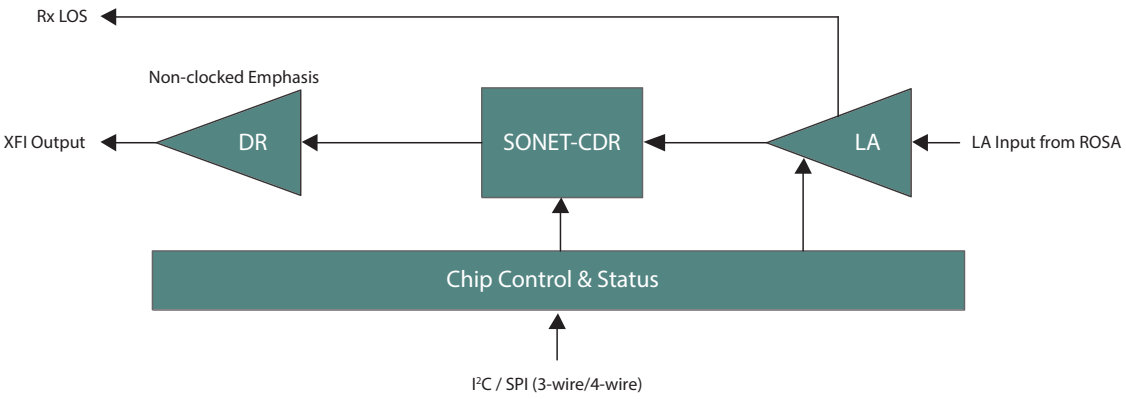


Figure 4-1: Receive Path

4.2.1 Integrated Limiting Amplifier

The GN2044 has an integrated Limiting Amplifier (LA), with better than 10mV sensitivity. Additional features are; slice level adjust and optional equalization on the limiting amplifier input.

4.2.2 Slice Level Adjust

The slicing level of the limiting amplifier can be configured in two modes of operation:

1. Automatic offset correction.
2. Manual slice adjust with a fixed slice level.

By default, the limiting amplifier is configured in automatic offset correction mode, and will slice the incoming signal at the 50% point.

The LA can be configured to allow a user-specified fixed slice level. In this mode, the slice level can be varied by ±200mV from the 50% point in 1mV increments. To enable this mode, **RX_PD_SLICE_ADJ** (shown below) should be set to 0.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPWRDN_REG2	135	RX_PD_SLICE_ADJ	1:1	RW	1	0-1	When HIGH, power-down for LA slice adjust.

To enable the user to adjust the slice level manually, **RX_PD_SLICE_ADJ** must be set to 0 and **RX_MANUAL_SLICE_ADJ_EN** must be set to 1.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG5	52	RXLA_MANUAL_SLICE_ADJ_EN	0:0	RW	0	0-1	When HIGH, enables user to adjust slice level at the Rx input.

The following controls allow the slice adjust polarity and magnitude to be set manually:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG2	49	RXLA_SLICE_ADJ	7:0	RW	00000000	0-255	Slice adjust magnitude control.
RX_REG3	50	RXLA_SLICE_ADJ_POL	0:0	RW	0	0-1	Slice adjust polarity. When HIGH, slice level adjust is positive.

The slice level adjustment can be applied before or after the equalization function (covered in Section 4.2.3). This flexibility allows the device to maintain optimal receive sensitivity performance while optimizing slice adjust. Figure 4-2 shows the two possible insertion points for slice level adjustment:

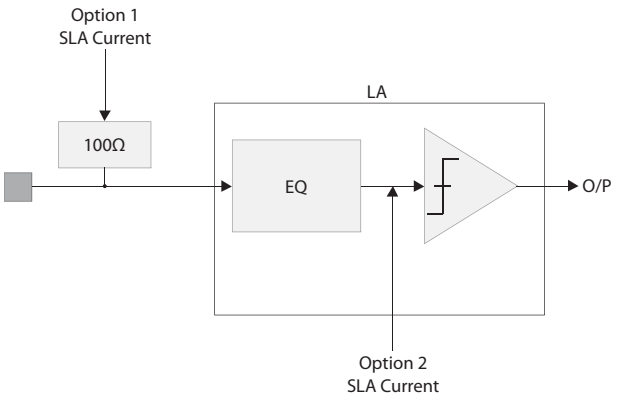


Figure 4-2: Slice Level Adjustment Insertion Points

RXLA_SLICE_ADJ_LO_RANGE should be set to 1 to apply the slice adjust after the equalization function.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG3	50	RXLA_SLICE_ADJ_LO_RANGE	1:1	RW	0	0-1	Selects slice level adjust point. When LOW, slicing point is option 1. When HIGH, slicing point is option 2.

4.2.3 Receive Equalization

The receive input implements an equalizer that provides peaking at 5.35GHz. This feature allows for optimal performance with extended reach connections, and allows for optimization of parameters such as dispersion penalty.

The equalizer implements 0dB to 14dB of high-frequency boost in fifteen steps, while achieving optimal receive sensitivity at any given equalization setting. The equalization setting is set through the **RXLA_BOOST_MSB** control. Additionally, the **RXLA_BOOST_LSB** control provides another 8 steps of fine tune control of the equalization gain at each **RXLA_BOOST_MSB** setting.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG1	48	RXLA_BOOST_MSB	3:0	RW	0000	0-15	RXLA boost control bit MSBs: 0 = 0dB to 15 = 14dB
RX_REG16	63	RXLA_BOOST_LSB	2:0	RW	000	0-7	RXLA boost control bit LSBs for fine tuning gain with smaller step size.

When the equalization setting is 0dB, the equalization function is bypassed and the receive sensitivity performance is the same as that of a limiting amplifier.

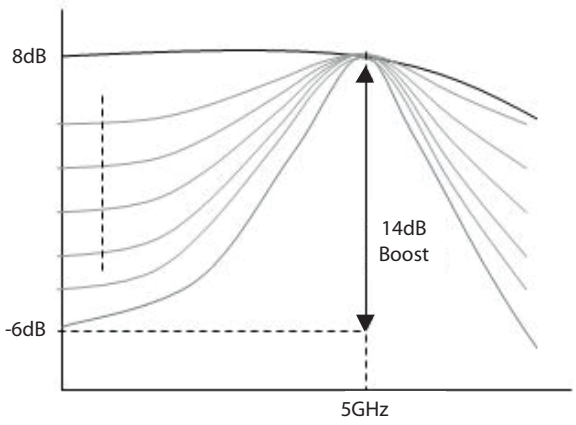


Figure 4-3: Receive Equalization

4.2.4 Rx PLL Variable Loop Bandwidth

The loop bandwidth of the receive Phase Locked Loops (PLLs) can be varied through the digital control interface. The loop bandwidths (LBW) are individually controlled, and can cover a range of 2.6MHz to 13MHz through the following 5-bit registers:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
RXPLL_REG1	20	RX_PLL_LBW_POS_ADJ	4:0	RW	11101	0-31	Adjusts LBW positive temperature coefficient control.
RXPLL_REG2	21	RX_PLL_LBW_NEG_ADJ	4:0	RW	00111	0-31	Adjusts LBW negative temperature coefficient control.

The temperature coefficient of the loop bandwidth can be adjusted by a weighted summation of **RX_PLL_LBW_POS_ADJ**, which has a positive temperature coefficient, and **RX_PLL_LBW_NEG_ADJ**, which has a negative temperature coefficient.

Table 4-1 shows the recommended settings for a flat loop bandwidth temperature coefficient:

Table 4-1: Rx Loop Bandwidth

RX_PLL_LBW_POS_ADJ	RX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
2	0	2	2.047
4	3	7	3.280
7	5	12	4.513
10	7	17	5.700
13	9	22	6.700
15	11	26	7.500
18	13	31	8.500
21	15	36	9.500
24	17	41	10.250
27	19	46	11.000

Table 4-1: Rx Loop Bandwidth (Continued)

RX_PLL_LBW_POS_ADJ	RX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
29	20	49	11.375
31	22	53	11.875
31	31	62	13.000

4.2.5 Rx CDR Input Jitter Tolerance

The input jitter tolerance of the Rx CDR is configurable to allow power optimization for required performance. Three modes of operation are supported as follows:

- **Mode 1:** Recommended for power-optimized applications. This mode supports the lowest power, but it is not guaranteed to meet the SONET IJT mask
- **Mode 2:** Recommended for most applications, including SONET, Ethernet and Fibre Channel. In this mode, the device is guaranteed to meet the SONET IJT mask.
- **Mode 3:** Recommended for SONET applications that require large margins on SONET IJT mask. This mode consumes extra power.

The RxCDR IJT mode is configured through the following registers. By default, the device is configured in Mode 3.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG9	28	RX_PLL_SELECT_HIGH_IJT	3:3	RW	1	0-1	When HIGH, selects high-margin Sonet IJT mode in conjunction with the RX_PLL_SONET_IJT_SETTING.
RXPLL_REG8	27	RX_PLL_SONET_IJT_SETTING	7:3	RW	00010	0-31	Control for Sonet IJT performance. Used in conjunction with Sonet IJT modes 2 and 3 to set IJT performance. Gradually increase setting for increased margins.
RXPWRDN_REG4	137	RX_PD_SONET_IJT	0:0	RW	0	0-1	When HIGH, powers-down the Rx path Sonet IJT feature to save power.

Table 4-2 shows the recommended settings for above registers for the three IJT modes:

Table 4-2: IJT Mode Settings

IJT Mode	RX_PD_SONET_IJT	RX_PLL_SELECT_HIGH_IJT	RX_PLL_SONET_IJT_SETTING[4:0]
1	1	x	x
2	0	0	2 (or higher, based on user preference)
3	0	1	3 (or higher, based on user preference)

Figure 4-4 shows that Mode 2 and Mode 3 SIJT performance is comparable with maximum LBW settings, with >3UI margin at 400kHz:

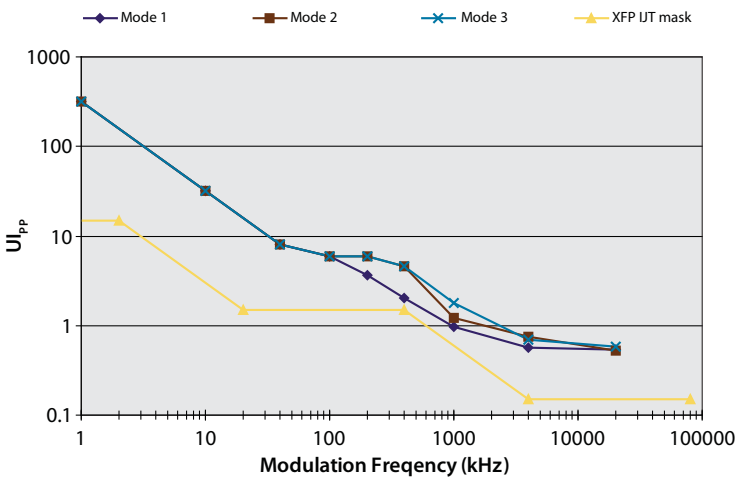


Figure 4-4: S-IJT Mode 1, 2 & 3 (Loop Bandwidth = 6.2MHz)

With higher LBW settings, Mode 2 can be used to meet and exceed S-IJT mask with lower power than Mode 3. Note that in either Mode 2 or Mode 3, the **RX_PLL_SONET_IJT_SETTING** can be adjusted beyond the values provided in Table 4-2 to further optimize SIJT performance margins.

4.2.6 Emphasis Driver with Auto-Mute

The receive path driver is a non-clocked emphasis driver that can be used to compensate for losses in the connector and trace between the module and ASIC. The emphasis operates regardless of the status or state of the Rx CDR. The output swing can be set from 100mV to 800mV in steps of 50mV through the **RX_SDO_SWING[3:0]** register. The emphasis amplitude can be varied from 1dB to 6dB in 16 steps through **RX_SDO_EMPHASIS[3:0]**.

Note: The Rx emphasis in disabled by default. To enable the emphasis, set **RX_PD_RXSDO_EMPHASIS** to 0 to power-on the Rx emphasis block. When emphasis is enabled, the output driver is still limited to approximately 800mV$_{ppd}$ output. Therefore, at some swings settings (i.e. >400mV$_{ppd}$), the full 6dB emphasis may not be realized. See Figure 4-5 for more information.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXSDO_REG1	75	RX_SDO_SWING	3:0	RW	0110	0-15	Driver swing: 100mV$_{ppd}$ to 850mV$_{ppd}$. Default = 6 = 400mV$_{ppd}$.
RXSDO_REG2	76	RX_SDO_EMPHASIS	3:0	RW	0000	0-15	Driver emphasis control.
RXPWRDN_REG1	134	RX_PD_RXSDO_EMPHASIS	3:3	RW	1	0-1	When HIGH, power-down for the trace driver emphasis.

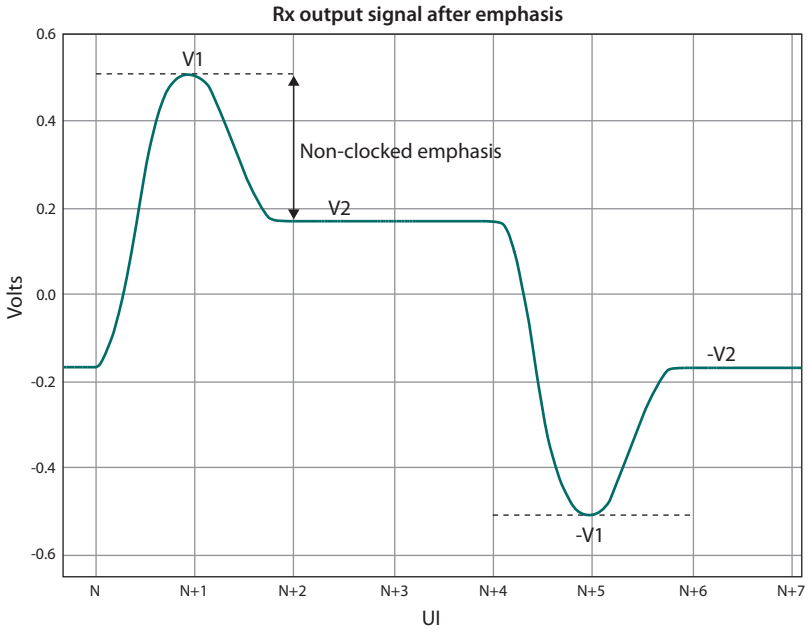


Figure 4-5: Emphasis Waveform Description when Enabled

Figure 4-5 above shows the emphasis waveform. Amplitudes V1, V2 and emphasis in dB are defined as follows:

V1, **V2** and **Emphasis** are defined as follows:

V1 = **RX_SDO_EMPHASIS** setting, which represents the "peak", or superposition of the **RX_SDO_SWING** setting and the **RX_SDO_EMPHASIS** setting.

V2 = **RX_SDO_SWING** setting, which is the DC or Steady State swing, same as when no emphasis is enabled.

Emphasis [dB] = 20 x log(V1/V2). As a guideline, 2 x V1 should be less than or equal to 800mV.

The output can be configured to automatically mute if Receive LOS is detected through the following registers. When muted, the output driver remains powered-up, and the output common mode is maintained. The output driver can be configured to power-down when muted by setting the **RX_SDO_PWR_DN_ON_MUTE** bit:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXSDO_REG3	77	RX_SDO_FORCE_MUTE	0:0	RW	0	0-1	Mutes driver to CM when not in auto mute mode.
		RX_SDO_AUTO_MUTE_EN	1:1	RW	1	0-1	Enables muting the driver upon LOS.
		RX_SDO_PWR_DN_ON_MUTE	2:2	RW	1	0-1	Enables power-down on mute for output stage.

4.2.7 Output Polarity Invert

Polarity inversion is implemented at the SDO input. Input to the CDR is not affected by polarity inversion. The output polarity can be inverted through the following register:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG5	24	RX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.

4.3 Transmit Path

The transmit path is comprised of a trace equalizer, a multi-rate CDR and an EML driver.

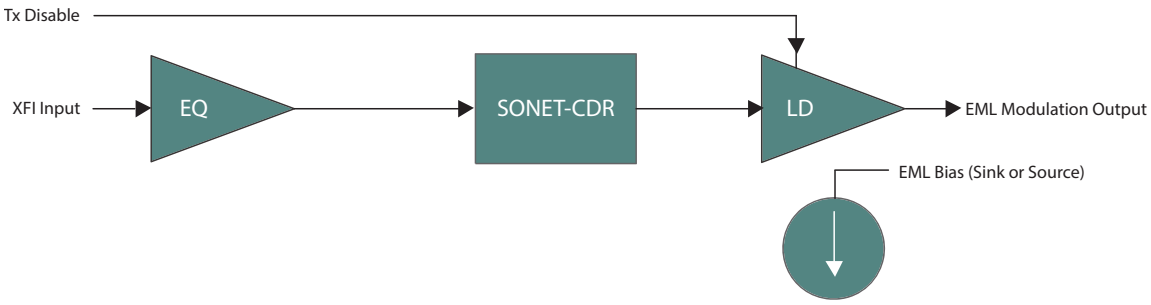


Figure 4-6: Transmit Path

4.3.1 Equalizer

The the transmit path input has an XFI equalizer with up to 6dB gain at 5.35GHz. The equalizer can be controlled through the following register:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TX_REG3	33	TX_EQ_BOOST	1:0	RW	11	0-3	Controls the Tx path input equalization setting: 00 = 0dB 01 = 2dB 10 = 4dB 11 = 6dB

4.3.2 Tx PLL Variable Loop Bandwidth

The loop bandwidth of the transmit Phase Locked Loops (PLLs) can be varied through the digital control interface. The loop bandwidths are individually controlled, and can cover the range of 1MHz to 10MHz through following 5-bit registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG1	10	TX_PLL_LBW_POS_ADJ	4:0	RW	01110	0-31	Adjusts LBW positive temperature coefficient control.
TXPLL_REG2	11	TX_PLL_LBW_NEG_ADJ	4:0	RW	00010	0-31	Adjusts LBW negative temperature coefficient control.

The temperature coefficient of the loop bandwidth can be adjusted by weighted summation of **TX_PLL_LBW_POS_ADJ**, which has a positive temperature coefficient and **TX_PLL_LBW_NEG_ADJ**, which has a negative temperature coefficient.

Table 4-3 shows the recommended settings for a flat loop bandwidth temperature coefficient:

Table 4-3: Tx Loop Bandwidth

TX_PLL_LBW_POS_ADJ	TX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
2	0	2	1.413
4	3	7	2.480
7	5	12	3.547
10	7	17	4.555
13	9	22	5.330
15	11	26	5.950
18	13	31	6.725
21	15	36	7.500
24	17	41	8.050
27	19	46	8.600
29	20	49	8.919
31	22	53	9.344
31	31	62	10.300

4.3.3 Tx Jitter Filter Mode

The Tx CDR supports a jitter filter mode to aid in the optimization of jitter generation performance and reduction of jitter present at the Tx CDR input. The jitter filter mode is configured using the following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPWRDN_REG4	133	TX_PD_JIT_FILT	0:0	RW	1	0-1	When HIGH, power-down for the Tx jitter filter.
TXPLL_REG1	10	TX_PLL_LBW_POS_ADJ	4:0	RW	01110	0-31	Adjusts the LBW positive temperature coefficient control.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TXPLL_REG2	11	TX_PLL_LBW_NEG_ADJ	4:0	RW	00010	0-31	Adjusts the LBW negative temperature coefficient control.
TXPLL_REG8	17	TX_JIT_FILT_TRACK_ADJUST	7:3	RW	00010	0-31	Sets the tracking capability when Tx jitter filter mode is enabled.

Note: This feature does not impact the jitter generation performance of the Tx Laser Driver. The jitter generation performance of the laser driver and external TOSA must still be properly optimized separately.

To enable Tx jitter filter mode, set **TX_PD_JIT_FILT** LOW. Once enabled, **TX_PLL_LBW_POS_ADJ** and **TX_PLL_LBW_NEG_ADJ** are used to set the jitter filter bandwidth, and can be optimized for the desired jitter generation/filtering performance. Lastly, **TX_JIT_FILT_TRACK_ADJUST** is used to set the tracking capability of an internal clock with respect to the Tx input data. This allows for optimization of wander tolerance.

4.4 Laser Driver

4.4.1 EML Driver

The GN2044 has an integrated EML driver with eye-shaping features, and an integrated Automatic Power Control (APC) loop.

The EML laser driver can provide up to $2.5V_{pp}$ modulation. The following registers can be used to set the modulation current with 10-bit resolution. Note that the **TXSDO_IMOD_LO** must be written to first, followed by a write to **TXSDO_IMOD_HI**. The new value only takes effect after a write to **TXSDO_IMOD_HI**.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TXSDO_REG10	87	TXSDO_IMOD_LO	7:0	RW	00000000	0-255	LD modulation current LSB.
TXSDO_REG11	88	TXSDO_IMOD_HI	1:0	RW	00	0-3	LD modulation current MSB.

4.4.1.1 Jitter Generation Optimization Using Laser Driver Phase Adjust

The jitter optimization feature in the laser driver is intended to optimize module level jitter. This includes jitter from the GN2044, external pull-up inductors, board parasitic and the laser diode. This feature can also be used to improve jitter generation performance for SONET applications. The following registers can be used to optimize jitter generation through TxSDO phase adjust:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG13	90	TXSDO_PHASE_ADJUST	7:0	RW	00000000	0-255	LD phase adjust—compensation for jitter generation due to Sonet header.
TXSDO_REG25	99	TXSDO_PHASEADJ_DIR	1:1	RW	0	0-1	LD phase adjust (Z0) compensation direction E/L:0/1.
PWRDN_REG1	138	PD_TXSDO_PHASE_ADJ	2:2	RW	1	0-1	When HIGH, power-down for LD phase adjust (Z0) compensation.

TXSDO_PHASEADJ_DIR controls the direction in which the jitter generation optimization using phase adjust is applied. The direction depends on the jitter signature present at the output of the module. **TXSDO_PHASE_ADJUST** controls the magnitude of the jitter generation optimization. To enable the feature, **PD_TXSDO_PHASE_ADJ** must be set LOW. The Tx CDR must be powered-on for the phase adjust feature to work.

4.4.1.2 Crossing Point Adjust

The crossing point adjust feature allows the user to adjust the cross point as shown in Figure 4-7 below. The crossing point adjust features can set the output crossing point from 20% to 80%, with a 6-bit control through following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG12	89	TXSDO_CPA	5:0	RW	011111	0-63	LD crossing point adjust: 0~ = >80% 31 = 50% 63~ = <20%
PWRDN_REG1	138	PD_TXSDO_CPA	3:3	RW	1	0-1	When HIGH, power-down for LD crossing point adjust.

To enable the feature, **PD_TXSDO_CPA** must be set LOW.

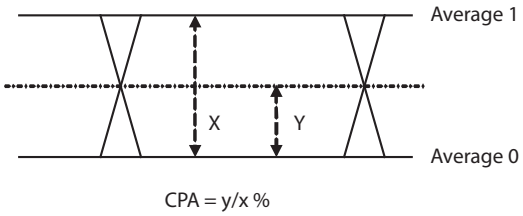


Figure 4-7: Definition of Cross Point Adjust Percentage

4.4.1.3 Pre-Emphasis

The laser driver supports pre-emphasis. The pre-emphasis is applied to both the rising and falling edges simultaneously. It can be used to optimize the optical eye and improve the mask margin. The amplitude of the pre-emphasis can be varied. The following registers are used to program the pre-emphasis:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TxSDO_REG14	91	TXDSO_PREEMPH_AMP	4:0	RW	00000	0-31	LD pre-emphasis amplitude control.
PWRDN_REG1	138	PD_TXSDO_PREEMPH	0:0	RW	1	0-1	Power-down for LD pre-emphasis.

4.4.1.4 Laser Driver Shutdown

The laser driver supports several modes of shutdown including:

- Manual mute (with optional output stage power-down)
- Automatic mute upon LOS detection (with optional output stage power-down)
- Modulation squelch
- TxDSBL through control register

The following registers can be used to configure and invoke the above shutdown modes:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG25	99	TXSDO_MOD_SQUELCH	0:0	RW	0	0-1	When HIGH, LD modulation is squelched.
		TXSDO_FORCE_TXDSBL	2:2	RW	0	0-1	When HIGH, shuts down the LD mod, bias and APC.
		TXSDO_FORCE_MUTE	3:3	RW	0	0-1	When HIGH, mutes driver to CM when not in auto mute mode.
		TXSDO_AUTO_MUTE_EN	4:4	RW	1	0-1	When HIGH, enables muting the driver upon LOS.
		TXSDO_PWR_DN_ON_MUTE	5:5	RW	1	0-1	When HIGH, enables power-down on mute for the output stage.

4.4.2 Laser Driver Bias Current

The laser driver bias current can be configured as either a sink or a source current. By default, the bias current is configured as a source. It is important to avoid configuring the bias current in a mode that will not be used by the intended application. If a bias current sink is required by the application, the device must be configured to make the bias current a sink after power-up. If a bias current source is required by the application, no configuration is necessary, as the device is configured as a source by default.

The following registers can be used to configure the bias current as either a source or a sink:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG26	100	TXSDO_BIAS_SOURCE_EN	3:3	RW	1	0-1	LD bias source is enabled when HIGH. TXSDO_BIAS_SINK_EN must be LOW.
		TXSDO_BIAS_SINK_EN	4:4	RW	0	0-1	LD bias sink is enabled when HIGH. TXSDO_BIAS_SOURCE_EN must be LOW.

The laser driver bias current is controlled by the Automatic Power Control or APC loop by default. The next section describes the operation of the APC loop. However, the laser driver bias current may be set manually by overriding the APC loop. The following registers allow a fixed laser driver bias current to be programmed manually:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
APC_REG4	106	APC_DAC_OVR_VAL_LO	7:0	RW	00000000	0-255	Override value for the APC DAC counter [7:0]. Sets the LD bias current manually when used with APC_DAC_OVR_VAL_HI, and when APC_OVR is HIGH. Step size is approximately 0.15mA.
APC_REG5	107	APC_DAC_OVR_VAL_HI	1:0	RW	00	0-3	Override APC DAC [9:8]. A write triggers an update.
		APC_OVR	2:2	RW	0	0-1	When HIGH, overrides the APC loop with the DAC override value to set the LD bias current manually.

When **APC_OVR** is set HIGH, the APC control loop is bypassed and the 10-bit bias current control **APC_DAC_OVR_VAL_LO/HI** takes effect. Note that the LOW value must be written first, followed by a write to the HIGH value. The new value only takes effect after a write to the HIGH value. The APC must still be enabled when using the override mode.

Note: With **APC_OVR** set HIGH, TxDSBL assert will set the LD bias current to shut off. After TxDSBL is de-asserted, the **APC_DAC_OVR_VAL_LO/HI** registers must be re-written to turn on the LD bias current. When **APC_OVR** is set HIGH, it is recommended to write the **APC_DAC_OVR_VAL_LO/HI** registers immediately following TxDSBL negation to minimize the negate time.

4.4.3 Automatic Power Control Loop

The GN2044 integrates an Automatic Power Control or APC loop to control the bias current for the laser diode in the TOSA, thereby reducing the external components required. The photo current from the TOSA (IPHOTO) is converted to a voltage (VPHOTO), through an on-chip, selectable resistor. The resistor selection is based on the maximum IPHOTO from the TOSA. There are four possible settings available through **IPH_RANGE_SEL[1:0]**. IPHOTO is then used as an indicator of the average transmit power. The user can define a set point for IPHOTO to achieve a certain average transmit power. The APC loop operates to achieve and maintain the set point over operating conditions.

The APC uses 10 bits of resolution to define the bias current to ensure minimal variation of average transmit power. To accommodate different TOSAs configurations, IPHOTO can be configured to source a current from the GN2044 or sink a current from the TOSA.

The APC loop is enabled by default. The following registers can be used to enable and configure the APC loop. When the APC loop is disabled and re-enabled, it must be reset.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
APC_REG1	104	APC_EN	0:0	RW	1	0-1	When HIGH, enables the APC.
		APC_RESET	3:3	RW	0	0-1	When HIGH, the APC control is reset.
		APC_SEL_HIGH_REF	4:4	RW	0	0-1	When HIGH, IPHOTO is sourced from the GN2044 and is sunk in the TOSA. When LOW, IPHOTO is sourced from the TOSA and is sunk in the GN2044.
TXSDO_REG5	82	IPH_RANGE_SEL	1:0	RW	10	0-3	IPHOTO range select: 00 = 0mA to 0.25mA 01 = 0.25mA to 0.75mA 10 = 0.75mA to 1.25mA 11 = 1.25mA to 2.14mA

4.4.3.1 APC Loop Dynamics

The APC loop is designed to meet the TxDSBL assert time of <10µs, and the TxDSBL negate time of <2ms. In addition, the APC loop supports a highly-configurable loop dynamics upon TxDSBL negate to minimize the time to achieve the desired output average power level, without any overshoots on output average power.

The loop dynamics upon Reset or TxDSBL negation is configured through two sets of parameters as follows:

1. APC Thresholds
   - APC_TH_HI
   - Set Point (IPHOTO for desired average transmit power)
2. APC Slew Rates
   - Fast Rate—LD bias current updates rate when IPHOTO is < APC_TH_HI
   - Slow Rate—LD bias current updates rate when IPHOTO is > APC_TH_HI

Figure 4-8 shows the loop dynamics and impact of each of the above parameters.

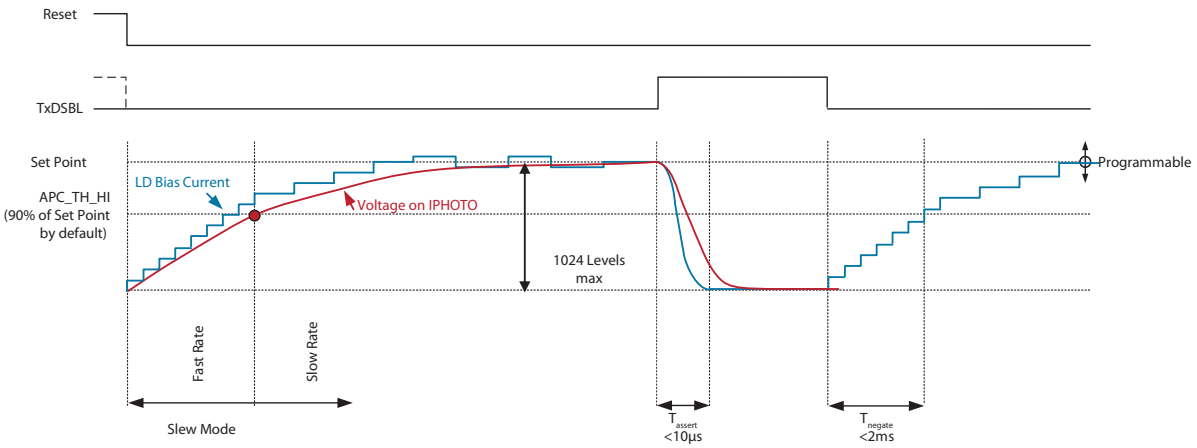


Figure 4-8: APC Loop Dynamics

Upon negation of Reset or TxDSBL, the difference between IPHOTO and the set point (error) is large. In this region, a fast rate for LD bias current can be selected to minimize the negate time without risk of overshooting the set point. As the error reduces, it is desirable to slow down the LD bias current rate to avoid overshoot. The threshold **APC_TH_HI** defines the region of fast and slow ramp up rates. Initially, the LD Bias current will ramp-up at a fast rate because it is below **APC_TH_HI**. When the LD Bias current exceeds **APC_TH_HI**, it will ramp-up at the slow rate. This controlled ramp-up ensures robust stability and avoids overshoots while meeting the negate time of <2ms. By default, **APC_TH_HI** is set to 90% of the set point, but it can be adjusted if necessary. It is generally recommended to use the default APC configuration settings.

The following registers control the APC thresholds:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
APC_REG6	108	APC_REF_DAC_CTRL	7:0	RW	00000000	0-255	Sets APC final target reference threshold (0V to 1V range in steps of 4mV).
APC_REG8	110	APC_TH_HI	5:0	RW	110110	0-63	APC Threshold Hi setting 110110 (default) - 0.9x of setpoint 1 LSB = 0.0167x of setpoint.

The following registers control the APC slew rates:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
APC_REG2	105	APC_CLK_RATE_FAST_DIV	3:2	RW	00	0-3	APC fast rate divide ratio: 0-3 = 32-256, default = 32
		APC_CLK_RATE_SLOW_DIV	6:4	RW	101	0-7	APC slow rate divide ratio: 0-3 = 32-4k, default = 1k

Note: The default update rate is approximately 20MHz.

4.5 Status Indicators

The GN2044 supports three status indicators: Loss of Signal (LOS), Loss of Lock (LOL) and Module Not Ready (MODNR). LOS and LOL indicators are available on both the receive and the transmit paths.

4.5.1 Receive Loss of Signal (LOS)

The receive path Loss Of Signal indicator status is available through a register and the LOSL pin. The LOSL pin is by default open-drain, active-high 1.8V – 3.3V LVCMOS compatible. However, the pin can be configured in a 1.8V LVCMOS-compliant compatible mode by setting **OPEN_DRAIN_LOSL** to 0. In addition, LOSL can be configured to be active-low by setting **POLINV_LOSL** HIGH. The status of RxLOS can be read out through **RX_PLL_LOS**. Additionally, the LOSL pin can be configured to provide other status information as per the table below. By default, LOSL only provides status information for RxLOS. If other status indicators are enabled, the LOSL output is the logical OR of all enabled indicators.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TOP_REG2	2	POLINV_LOSL	1:1	RW	0	0-1	When HIGH, inverts polarity of the LOSL output.
		OPEN_DRAIN_LOSL	2:2	RW	1	0-1	When HIGH, makes the LOSL output driver open-drain.
		LOSL_MASK_RXLOS	4:4	RW	0	0-1	When HIGH, masks-out RxLOS from asserting LOSL.
		LOSL_MASK_RXLOL	5:5	RW	1	0-1	When HIGH, masks-out RxLOL from asserting LOSL.
		LOSL_MASK_TXLOS	6:6	RW	1	0-1	When HIGH, masks-out TxLOS from asserting LOSL.
		LOSL_MASK_TXLOL	7:7	RW	1	0-1	When HIGH, masks-out TxLOL from asserting LOSL.
RXPLL_REG10	29	RX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.

The LOS assert threshold can be set from 5mV to 400mV in three distinct ranges. The LOS assert threshold is a function of the **RXLA_BOOST_MSB** setting. Table 4-4 describes the selection of **RXLOS_RANGE** based on the required LOS assert threshold and **RXLA_BOOST_MSB** settings.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG12	59	RXLOS_RANGE	1:0	RW	01	0-3	LOS range: 0 = highest 3 = lowest

Table 4-4: LOS Assert Ranges

RXLA_BOOST_MSB [3:0]	LOS Assert Threshold Range		RXLOS_RANGE[1:0]	Resolution (controlled by RXLOS_TH_NEG/POS)	Unit
	Min	Max			
	5	400	LOS Threshold - Total Range	—	mV_{ppd}
0-7	—	—	11 - Unused	—	—
0-7	5	30	10 - Low Range	<0.1mV	mV_{ppd}
0-7	30	100	01 - Mid Range	<1.0mV	mV_{ppd}
0-7	100	400	00 - High Range	<2.0mV	mV_{ppd}
8-15	5	30	11 - Low Range	<0.1mV	mV_{ppd}
8-15	30	100	10 - Mid Range	<1.0mV	mV_{ppd}
8-15	—	—	01 - Unused	—	—
8-15	100	400	00 - High Range	<2.0mV	mV_{ppd}

4.5.1.1 Rx LOS Threshold

The LOS assert threshold is set using the following registers:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
RX_REG9	56	RXLOS_TH_NEG	7:0	RW	01001001	0-255	Negative tempco LOS threshold setting.
RX_REG10	57	RXLOS_TH_POS	7:0	RW	00000000	0-255	Positive tempco LOS threshold setting.

Figure 4-9 to Figure 4-12 shows the typical recommended range of Rx LOS Assert thresholds and corresponding **RX_LOS_TH_NEG[7:0]** setting to achieve these thresholds. It is recommended to keep **RX_LOS_POS[7:0]** = 0. The Rx LOS De-assert thresholds are the same as the Rx LOS Assert thresholds for a hysteresis setting of 0.

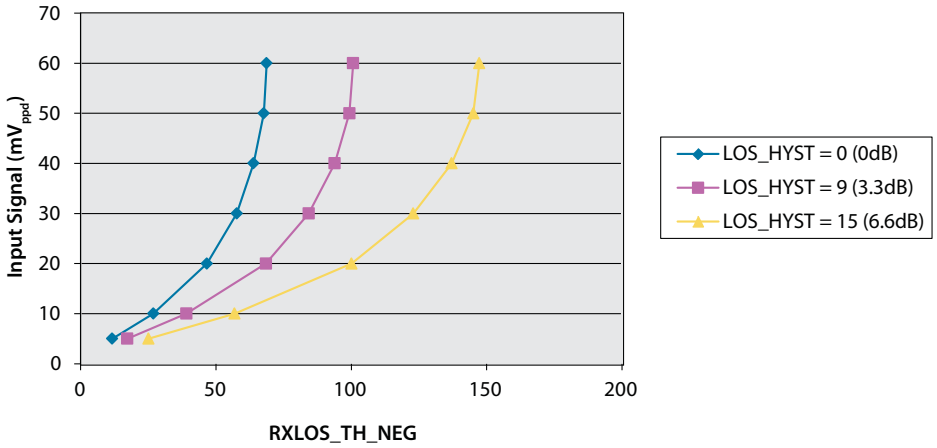


Figure 4-9: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = LOW)

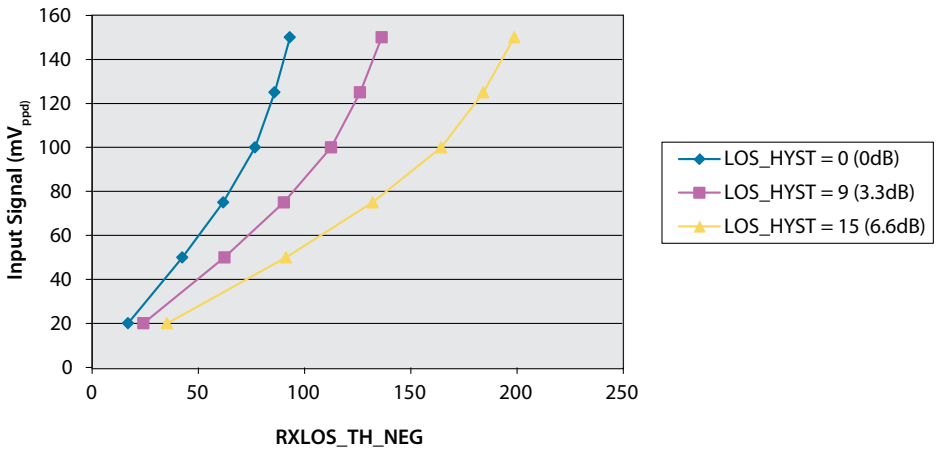


Figure 4-10: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = MID)

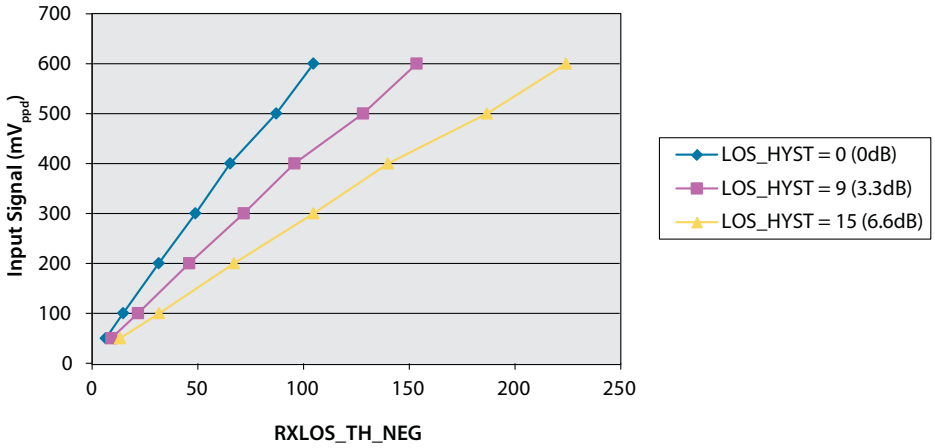


Figure 4-11: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = HIGH)

The LOS threshold has a slight dependence on the input data rate. Figure 4-12 below gives an indication of the typical variation of data rate, between 9.95Gb/s to 11.3Gb/s.

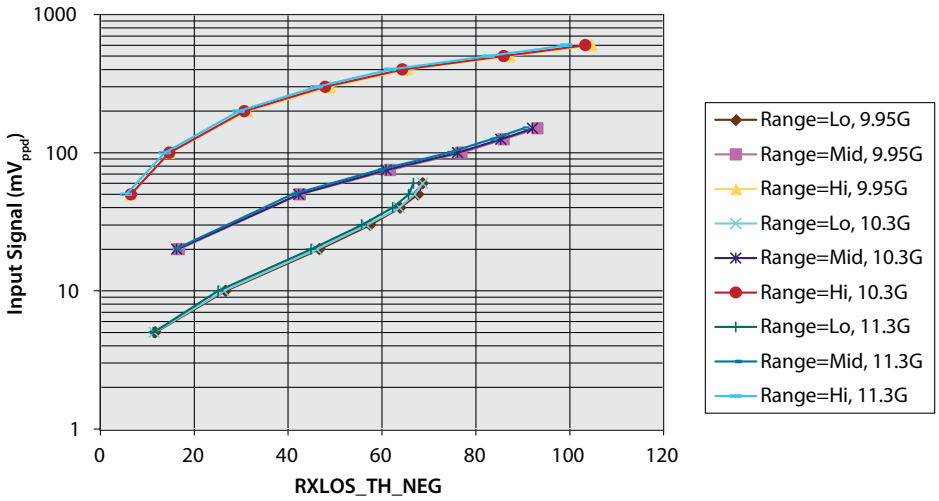


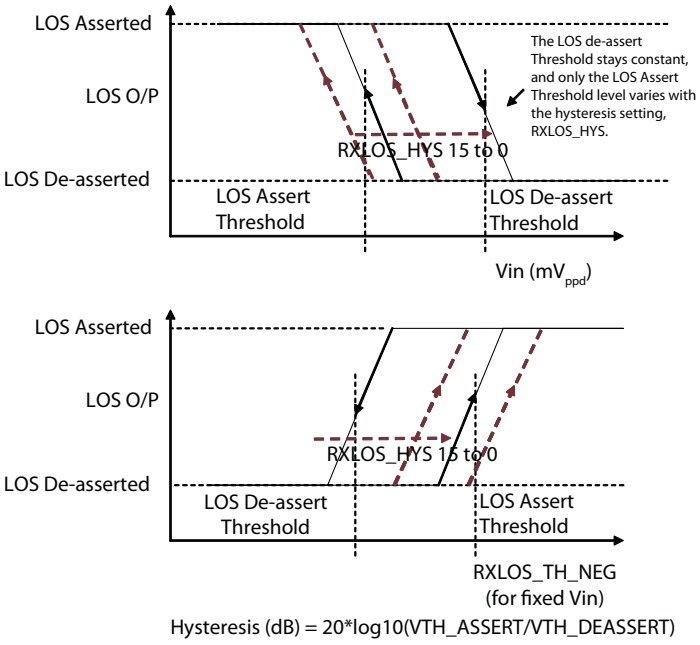
Figure 4-12: Rx LOS Assert Threshold Variation Over Data Rates

4.5.1.2 Rx LOS Hysteresis

The LOS detector supports programmable hysteresis ranging from 0dB to 6dB, adjustable in steps of less than 0.5dB. The following register can be used to program the hysteresis. Note that the effective hysteresis is somewhat dependent on the threshold value:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG11	58	RXLOS_HYS	3:0	RW	1001	0-15	Hysteresis control 0-15 -> 0-6dB. Default = 9 = 3dB.

Hysteresis control only affects the assert threshold. The LOS de-assert threshold is set by **RXLOS_TH_NEG** and **RXLOS_TH_POS** controls only. Figure 4-13 shows the hysteresis characteristics and the impact of **RXLOS_HYS[3:0]**:



RXLOS_HYS	Hysteresis (dB)
0	0.1
1	0.3
2	0.7
3	1.1
4	1.4
5	1.8
6	2.1
7	2.5
8	3.0
9	3.4
10	3.9
11	4.4
12	4.8
13	5.4
15	6.7

Figure 4-13: Rx LOS Hysteresis

To support system diagnostics, a manual LOS assert feature is available through the following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG12	59	RXLOS_FORCE_ASSERT	2:2	RW	0	0-1	Directly sets the state of RXLOS accordingly if RXLOS_FORCE_ASSERT_EN is HIGH.
		RXLOS_FORCE_ASSERT_EN	3:3	RW	0	0-1	When HIGH, LOS is controlled by RXLOS_FORCE_ASSERT.

4.5.2 Transmit Loss of Signal

The transmit path LOS indicator status is available through a register. If desired, its status can be included in the generation of the MODNR or LOSL output pins. The LOS assert threshold can be set from 20mV to 100mV in <1mV steps. In addition the temperature coefficient of the LOS threshold can be adjusted to ensure consistent LOS operation over temperature. The LOS also has hysteresis that is programmable from 0dB to 6dB in steps of less than 0.5dB. A manual LOS assert feature is supported for system diagnostics.

The following registers are used to control the transmit LOS feature:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TX_REG9	39	TXLOS_TH_NEG	7:0	RW	00011011	0-255	Negative temperature coefficient LOS threshold setting.
TX_REG10	40	TXLOS_TH_POS	7:0	RW	00000000	0-255	Positive temperature coefficient LOS threshold setting.
TX_REG11	41	TXLOS_HYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB.
TX_REG12	42	TXLOS_FORCE_ASSERT	3:3	RW	0	0-1	Directly sets the state of TXLOS accordingly if TXLOS_FORCE_ASSERT_EN is HIGH.
		TXLOS_FORCE_ASSERT_EN	4:4	RW	0	0-1	When HIGH, LOS is controlled by TXLOS_FORCE_ASSERT.

4.5.2.1 Tx LOS Threshold

Figure 4-14 and Figure 4-15 show the typical recommended range of Tx LOS assert thresholds and corresponding **TXLOS_TH_NEG[7:0]** setting to achieve these thresholds. It is recommended to keep **TXLOS_TH_POS[7:0]** = 0 to achieve a flat temperature coefficient for LOS threshold. The Tx LOS de-assert thresholds are the same as the Tx LOS assert thresholds for a hysteresis setting of 0.

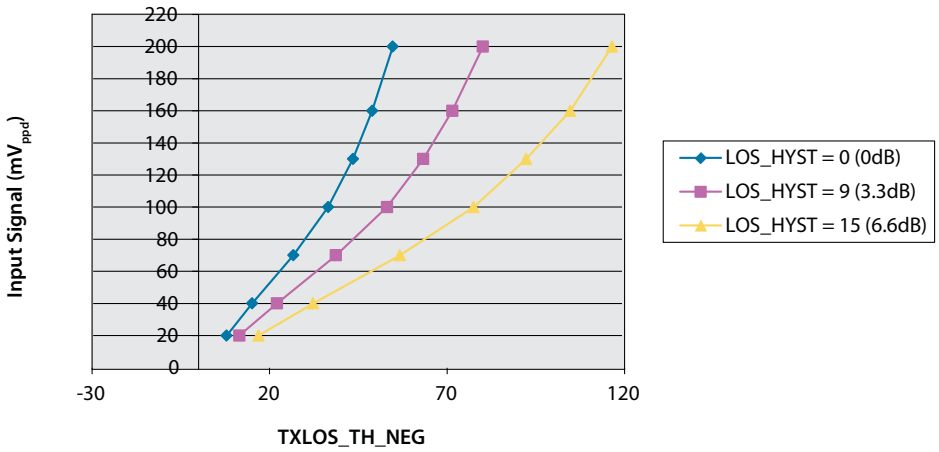


Figure 4-14: Tx LOS Assert Threshold – Typical @ 9.95Gb/s

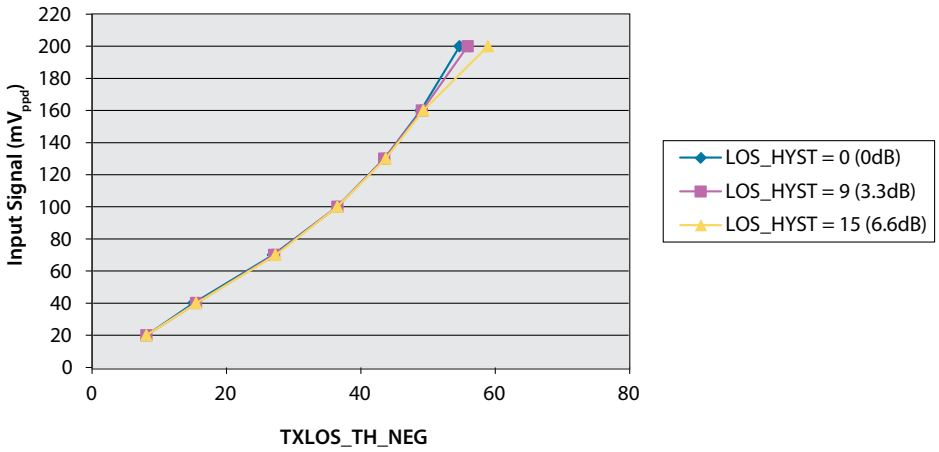


Figure 4-15: Tx LOS De-Assert Threshold – Typical @ 9.95Gb/s

The LOS threshold will have a slight dependence on data rate.

4.5.3 Loss of Lock

The receive path and transmit path LOSS of LOCK (LOL) status indicators are both available in registers as indicated below. These bits can also be included in the MODNR or LOSL outputs:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG10	19	TX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
RXPLL_REG10	29	RX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.

4.5.4 MODNR - Module Not Ready

Various status indicator pins are combined to generate a single MODNR indicator output. The MODNR output is, by default, an open-drain 1.8V – 3.3V LVCMOS-compatible output. It can be configured in a 1.8V LVCMOS-compliant mode through Register 2, bit 3—**OPEN_DRAIN_MODNR**.

The MODNR output is active-high by default. Its polarity can be changed to make it active-LOW through Register 2, bit 0—**POLINV_MODNR**. When set HIGH, MODNR is configured as an active-low output.

The following status indicator controls can be combined to generate the MODNR output. Each of the indicators can be independently masked through register controls. By default, the MODNR output combines (OR's) the status of all indicators.

The following registers control the masking of the various indicators for MODNR and the configuration of MODNR pin.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG1	1	MODNR_MASK_RXLOS	0:0	RW	0	0-1	When HIGH, masks-out RxLOS from asserting MODNR.
		MODNR_MASK_RXLOL	1:1	RW	0	0-1	When HIGH, masks-out RxLOL from asserting MODNR.
		MODNR_MASK_TXLOS	2:2	RW	0	0-1	When HIGH, masks-out TxLOS from asserting MODNR.
		MODNR_MASK_TXLOL	3:3	RW	0	0-1	When HIGH, masks-out TxLOL from asserting MODNR.
		MODNR_MASK_TXFAULT	4:4	RW	0	0-1	When HIGH, masks-out TxFault from asserting MODNR.
TOP_REG2	2	POLINV_MODNR	0:0	RW	0	0-1	When HIGH, inverts polarity of MODNR output.
		OPEN_DRAIN_MODNR	3:3	RW	1	0-1	When HIGH, makes the MODNR output driver open-drain.

4.6 Test Features

The GN2044 contains built-in test features that can be used during module bring-up or for debug purposes. The test features are not guaranteed and are only meant as functional tests under typical conditions. It is not advised to use these features during mission mode operation.

4.6.1 PRBS Generator and Checker

The GN2044 has a built-in PRBS7 generator and checker. The generator and checker are disabled by default to save power, and can be enabled through the digital control interface. There are multiple ways to use the PRBS generator/checker. The PRBS Generator frequency is controlled by the **PRBS_GENERATOR_DATA_RATE_CONTROL[5:0]** register. The PRBS generator and checker are meant to be used only as functional debug tests. The register setting of **PRBS_GENERATOR_DATA_RATE_CONTROL[5:0]** = 20 corresponds to a data rate of typically 10.3Gb/s. The PRBS checker uses the recovered clock from the Tx CDR. Refer to Table 4-5 for more details.

Note: PRBS7 input to the PRBS checker must be non-inverted for the checker to operate correctly. As such, care must be taken when using the polarity invert feature in conjunction with external loop back to PRBS checker to ensure that the data polarity to the checker is correct. Internal loop-back paths are not affected by the polarity invert feature.

The following registers enable and configure the PRBS generator and checker:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG3	3	PRBS_GEN_START	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts off the PRBS Generator.
		PRBS_CHK_CLEAR_ERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from the Checker.
TOP_REG6	6	PRBS_CHK_STATUS	0:0	RO	0	0-1	When HIGH, checker detected an error.
LOOPBK_REG1	7	LB_RX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Rx Driver.
		LB_RX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects PRBS generator output into Rx Driver.
LOOPBK_REG2	8	PRBS_CHK_CLK_SEL	1:1	RW	0	0-1	When HIGH, selects the Tx recovered clock. When LOW, selects the Rx recovered clock.
		LB_TX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Tx Driver.
		LB_TX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects PRBS generator output into the Tx Driver.
LOOPBK_REG3	9	PRBS_GENERATOR_DATA_ RATE_CONTROL	5:0	RW	0	0-63	PRBS Generator Frequency Tuning Control. The tuning range is 9.9GHz to 10.4GHz from minimum to maximum setting.
PWRDN_REG2	139	PD_PRBS_GEN	1:1	RW	1	0-1	When HIGH, power-down the PRBS generator and associated buffers.
		PD_PRBS_CHK	2:2	RW	1	0-1	When HIGH, power-down the PRBS checker and associated buffers.

To ensure proper operation of the PRBS7 generator, **PRBS_GEN_START** needs to be set HIGH and then LOW once after the generator is powered-up through **PD_PRBS_GEN**.

To ensure proper operation of the PRBS7 checker, **PRBS_CHK_CLEAR_ERR** needs to be set HIGH and then LOW after application of valid PRBS7 pattern to clear any spurious errors. **PRBS_CHK_STATUS**, may be polled to check for errors flagged by the checker.

The PRBS generator can be configured to apply a PRBS7 pattern to RxSDO or TxSDO.

Table 4-5: PRBS Generator/Checker Configuration

Loopback Mode	Description	PD_PRBS_GEN	PD_PRBS_CHK	PRBS_CHK_CLK_SEL	LB_TX_OUT_PRBS_GEN	LB_RX_OUT_PRBS_GEN	LB_TX_OUT_EN	LB_RX_OUT_EN
PRBS Disabled	Default Mission mode	1	1	X	0	0	0	0
PRBS GEN → Rx Driver→ Tx Equalizer → Tx CDR → PRBS CHECKER	External Rx Loopback (tests TX CDR)	0	0	1	0	1	0	1

4.6.2 Loopback

The GN2044 allows four different loopback paths, and supports loopback on both the electrical side and the optical side. The loopback paths are shown in Table 4-6. The blocks referenced in the different loopback paths are shown in Figure 4-16.

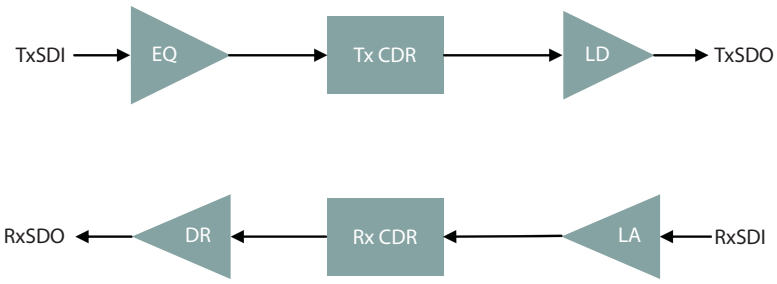


Figure 4-16: Simultaneous Loopback

Table 4-6: Loopback Paths

Mode #	Loopback Path
1	RxSDI → LA → LD → TxSDO
2	RxSDI → LA → RxCDR → LD → TxSDO
3	TxSDI → EQ → DR → RxSDO
4	TxSDI → EQ → TxCDR → DR → RxSDO

When loopback is enabled, the standard data path is not interrupted. For example: in Mode 1, the input to RxSDI will also be accessible at RxSDO. When using loopback modes, the automute feature for RxSDO or TxSDO may have to be disabled if the corresponding RxSDI or TxSDI inputs are unused.

The relevant parameters and their values required to enable each of the loopback options indicated above, are shown in Table 4-7.

The selection of a loopback path impacts the following features:

- Polarity inversion
- Phase adjust for jitter optimization for TxSDO (LD)

Table 4-7 also captures the impact on these features in each loopback mode.

Table 4-7: Loopback Options

Loop Back Mode (see Table 4-6)	LB_RX_OUT_EN	LB_RX_OUT_TX_DATA	LB_RX_OUT_PRBS_GEN	LB_RX_OUT_RX_CLK	RX_PLL_BYPASS	LB_TX_OUT_EN	LB_TX_OUT_RX_DATA	LB_TX_OUT_PRBS_GEN	LB_TX_OUT_TX_CLK	TX_PLL_BYPASS	TX_PLL_POLINV Effective	TX_SDO_PHADJ Available	RX_PLL_POLINV Effective
1	0	0	0	0	1	1	1	0	0	0	Y	N	N
2	0	0	0	0	0	1	1	0	0	0	Y	N	N
3	1	1	0	0	0	0	0	0	0	1	N	—	Y
4	1	1	0	0	0	0	0	0	0	0	N	—	Y
Control Register Address	7	7	7	7	24	8	8	8	8	14	—	—	—
Associated Bit Slice	4	5	6	7	2	4	5	6	7	2	—	—	—

4.7 Digital Diagnostics

The GN2044 has an on-chip ADC to provide diagnostic information through the digital interface. Refer to the GN204x Family ADC Application Note (PDS-060373) for more details.

4.8 Power-Down Options

The GN2044 provides a high-degree of flexibility in configuring the device for optimal power through power-down registers. Typical usage scenarios are shown. For further description on each of the individual control bits, see Table 5-1, registers **134** to **137**. This section describes the power-down controls for the following sub-systems:

1. Rx LA Power-Down
2. Rx CDR & SDO Power-Down
3. Tx CDR Power-Down
4. Tx SDO Power-Down

Table 4-8: Rx LA Power-Down

RX_PD_PATH	RX_PD_LA	RX_PD_LOS	RX_PD_SLICE_ADJ	Description
1	x	1	1	Completely powers-down the Rx LA.
x	1	1	1	Completely powers-down the Rx LA.
0	0	0	0	All features on. This is diagnostic mode.
0	0	0	1	Powers-down the slice adjust mode.
0	0	1	1	Powers down the SLA and LOS feature for lowest power mode.

Table 4-9: Rx CDR & SDO Power-Down

RX_PLL_BYPASS	RX_PD_PATH	RX_PD_RXCDR	RX_PD_SONET_IJT	RX_PD_RXSDO	RX_PD_RXSDO_EMPHASIS	Description
0	1	x	x	1	1	Completely powers-down the Rx CDR and Rx SDO.
0	x	1	x	1	1	Completely powers-down the Rx CDR and Rx SDO
1	0	x	x	0	1	Main data path through Rx CDR and RxSDO is powered-up for bypass mode. (RxLA has to be powered-up).
0	0	0	1	0	1	Standard operating mode, Rx CDR & SDO enabled in low-power mode. High IJT mode and emphasis are disabled.
0	0	0	0	0	0	Standard operating mode, Rx CDR & SDO enabled. High IJT mode and emphasis are enabled. IJT performance is set by RX_PLL_SELECT_HIGH_IJT registers.
0	0	0	1	0	0	Rx CDR & SDO are enabled. High IJT mode is powered-down. Emphasis is enabled.

Table 4-10: Tx CDR Power-Down

TX_PLL_BYPASS	TX_PD_TXPATH	TX_PD_TXCDR	TX_PD_JIT_FILT	TX_PD_TXSDO	PD_TXSDO_PHASE_ADJ	Description
0	1	1	x	1	x	Completely powers-down the Tx CDR and Tx path.
1	0	1	x	0	1	Main data path through Tx CDR is powered-up for bypass mode. (TxEq has to be powered-up).
0	0	0	1	0	1	Standard operating mode, Tx CDR is enabled in standard mode. Tx SDO jitter optimization through phase adjust is powered-down.
0	0	0	0	0	1	Standard operating mode, Tx CDR is enabled in jitter filter mode. (Requires appropriate configuration of jitter filter controls. See Section 4.3.3).
0	0	0	1	0	0	Standard operating mode, Tx SDO jitter optimization feature through phase adjust is enabled. (Requires appropriate configuration of Tx SDO controls).

Table 4-11: Tx SDO Power-Down

TX_PD_TXPATH	TX_PD_TXSDO	TX_PD_TXCDR	PD_TXSDO_PHASE_ADJ	PD_TXSDO_CPA	PD_APC	Description
1	x	x	x	x	x	Completely powers-down the Tx SDO.
x	1	x	x	x	x	Completely powers-down the Tx SDO.
0	0	0	0	x	x	Enables the Tx SDO jitter optimization through phase adjust feature.
0	0	x	x	1	x	Independently powers-down the Tx SDO cross point adjust feature.
0	0	x	x	x	1	Independently powers-down the Tx SDO Automatic Power Control loop.
0	0	0	0	0	0	Standard operating mode with Tx SDO jitter optimization, crossing point adjust and APC loop enabled.
0	0	0	0	0	0	Tx SDO with all features enabled.

4.9 Device Reset

$\overline{\text{RESET}}$ is an active-low signal with LVTTL/LVCMOS-compatible signalling levels. Due to the timing requirements of $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ to $\overline{\text{RESET}}$, it is recommended that $\overline{\text{RESET}}$ be driven by the Micro on the module. An external 10kΩ pull-down resistor is also recommended on the $\overline{\text{RESET}}$ line. $\overline{\text{RESET}}$ does not have a Schmitt trigger since reset negation is internally synchronized. See Figure 3-10.

4.9.1 Reset State During Power-up

The device requires $\overline{\text{RESET}}$ to be continuously pulled to GND during power ramp-up. $\overline{\text{RESET}}$ must continue to remain in that state for the minimum specified time after all of the power supplies have reached 90% of their final settling value. Following a $\overline{\text{RESET}}$ assertion at power-up, the device may be reset again at any time with the minimum specified pulse width on $\overline{\text{RESET}}$. Refer to Figure 4-17.

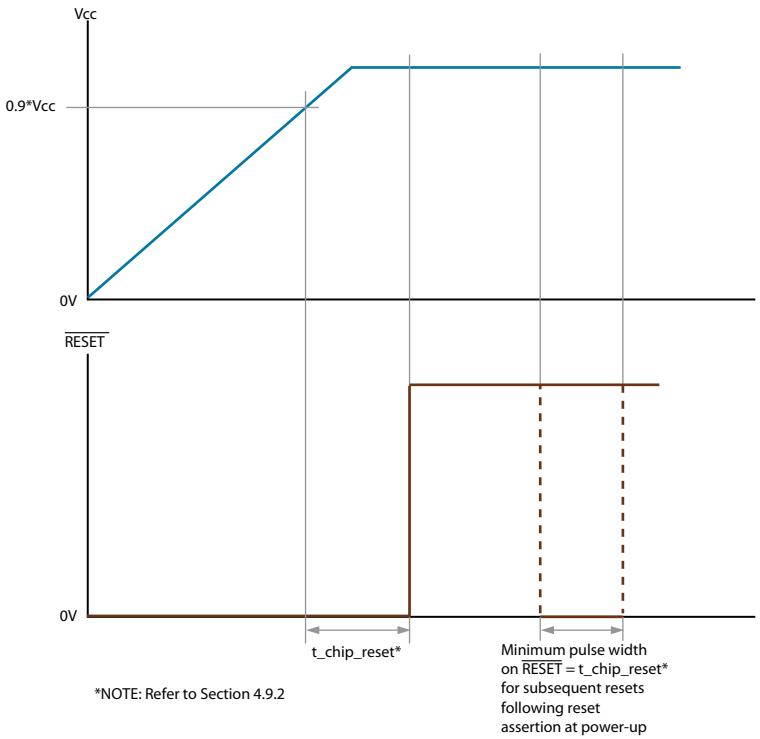


Figure 4-17: Reset State During Power-up

4.9.2 $\overline{\text{RESET}}$ Timing

The following $\overline{\text{RESET}}$ timing specifications apply:

- **t_chip_reset: 10µs**
  Defined as the minimum duration that $\overline{\text{RESET}}$ must be asserted after the supply has reached 90% of final settling value
- **t_ISELb_setup: 500ns**
  Defined as the minimum duration that the $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ pin must be asserted HIGH to select the SPI mode before $\overline{\text{RESET}}$ is negated

- **t_SPI_ready: 500ns**

  Defined as the minimum duration before an SPI/I^2C operation may be initiated, after $\overline{\text{RESET}}$ negation

When I^2C mode is desired, the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin is recommended to be pulled to ground throughout operation of the device.

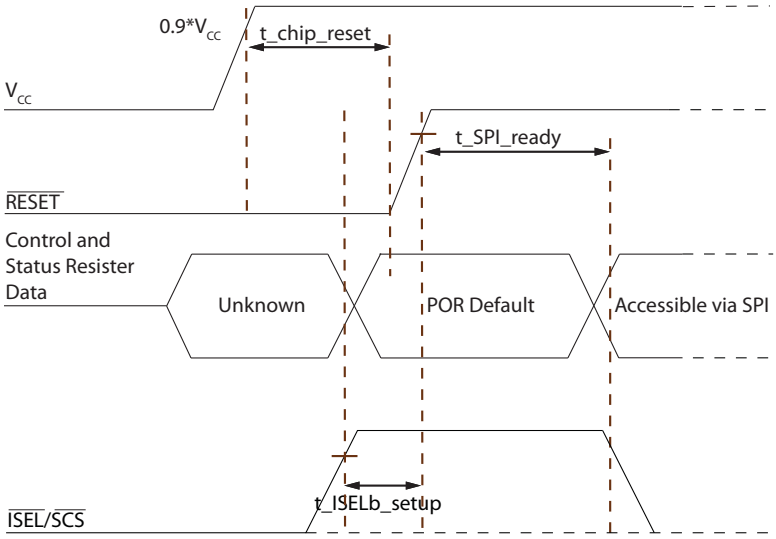


Figure 4-18: GN2044 Device Reset Timing Diagram

4.9.3 I/O and Register States During and After Reset

All configuration registers are set to their post-reset defaults state immediately following $\overline{\text{RESET}}$ assertion.

The following I/O states are applicable upon $\overline{\text{RESET}}$ assertion:

Table 4-12: I/O and Register States During and After Reset

Pin Name	I/O State upon $\overline{\text{RESET}}$ Assertion
SDA/SDIO/MISO	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance with a weak pull-down of 5µA.
SCL/SCLK and SSEL/MOSI	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted, and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance with a weak pull-down of 5µA.
MODNR	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. The loss of lock indicators will assert MODNR HIGH. This output will be high-impedance, and it's state will depend on the external pull-up.
LOSL	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. If a signal is present, the output will be pulled LOW. Otherwise, this output will be high-impedance and it's state will depend on the external pull-up.

Note: While the device is in reset, the SDA/SDI/MISO pin will output the state of the SSEL/MOSI pin. This can inhibit the ability for the master to communicate with other slave devices on the bus.

4.10 Digital Control Interface

The GN2044 has a tri-mode serial control interface to communicate with the part. Either an I^2C or SPI 3-wire, or SPI 4-wire protocol can be used. The protocol is selected using the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ and SSEL pins at the time of reset de-assertion.

When pin $\overline{\text{ISEL}}/\overline{\text{SCS}}$ is held LOW, or left unconnected, and the $\overline{\text{RESET}}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in I^2C mode. After reset de-assertion, the state of the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin is a 'don't care'. However, it is recommended that if the pin is not left unconnected, then it be driven LOW.

When the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin is held HIGH, and the SSEL pin is held LOW or left unconnected, and the $\overline{\text{RESET}}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in a three-wire SPI mode. After reset de-assertion, the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin functions as the $\overline{\text{SCS}}$ pin of a three-wire SPI interface.

When the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin is held HIGH, and the SSEL pin is held HIGH, and the $\overline{\text{RESET}}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in a four-wire SPI mode. After reset de-assertion, the $\overline{\text{ISEL}}/\overline{\text{SCS}}$ pin functions as the $\overline{\text{SCS}}$ pin, and the SSEL/MOSI functions as the slave data input pin, and the SDA/SDIO/MISO functions as the slave data output of a four-wire SPI interface.

4.10.1 I^2C Host Interface Mode

The I^2C mode supports standard-mode (100kHz) and fast-mode (400kHz) signalling. The device only supports slave mode. The pins SDA/SDIO and SCL/SCLK are used for bi-directional serial data and clock respectively. Signalling rates lower than the standard-mode and fast-mode rates are also supported by the device.

The GN2044 device slave address is 24_h.

The I^2C protocol is implemented as per the following description:

Each access begins with a 7-bit I^2C slave address word, an 8-bit register address word, followed by one 8-bit data word in a write command, or the device slave address with the read/write bit plus one 8-bit data word in the read command.

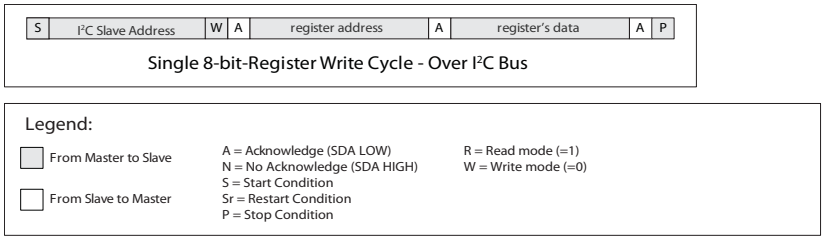


Figure 4-19: Single Register Write Cycle over I²C Bus

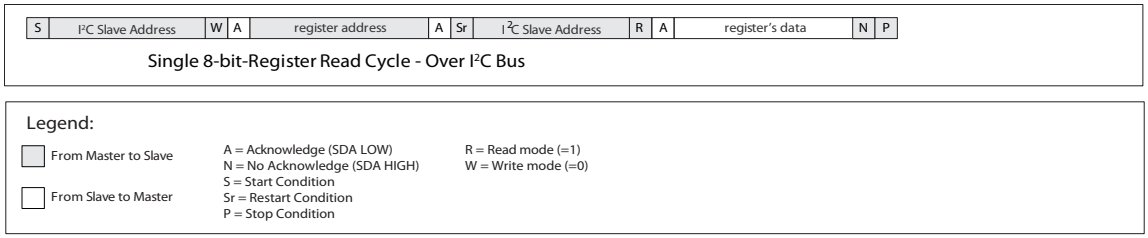


Figure 4-20: Single Register Read Cycle over I²C Bus

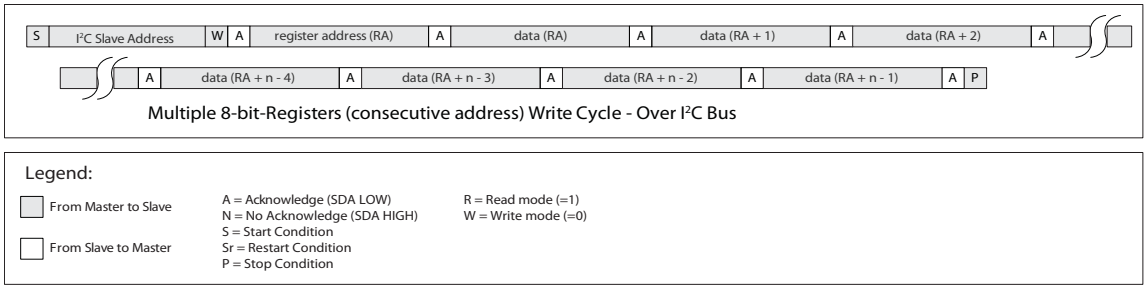


Figure 4-21: Bulk Register Write Cycle over I²C Bus

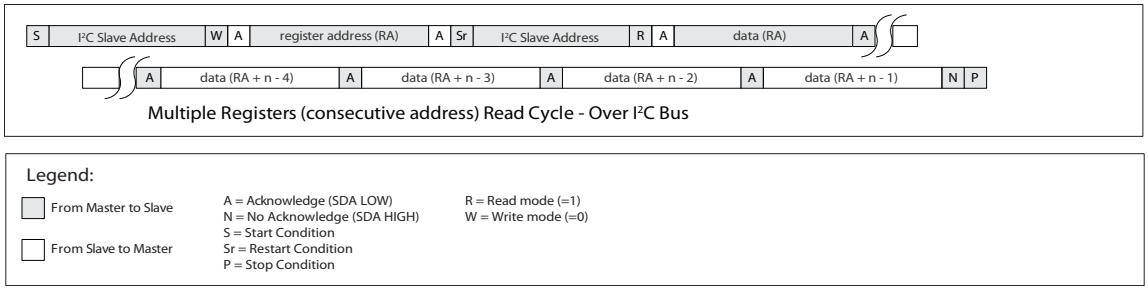


Figure 4-22: Bulk Register Read Cycle over I²C Bus

4.10.2 SPI Host Interface Mode

The GN2044 uses either a 3-wire or a 4-wire SPI protocol. The 3-wire SPI protocol's serial communication takes place via the bi-directional serial data signal (SDA/SDIO). The 4-wire SPI protocol's serial communication uses SSEL/MOSI as its data input and SDA/SDIO as its data output. In both modes, SCL/SCLK is the clock input and $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ is the chip select.

The signalling rate can be up to 10Mb/s. The interface uses 8-bit data and 16-bit address + control.

The 16-bit address + control is made up of an 8-bit address, 1-bit command, 1-bit for auto-increment and 6 unused bits. The 3-wire SPI protocol is implemented as per Figure 4-23 and Figure 4-24. The signal sdo_oen_o is an internal signal indicating the direction of the SDIN_SDOUT pin. When '1', the SDIN_SDOUT pin is configured as an input, when '0', its configured as an output. The 4-wire SPI protocol is implemented as per Figure 4-25.

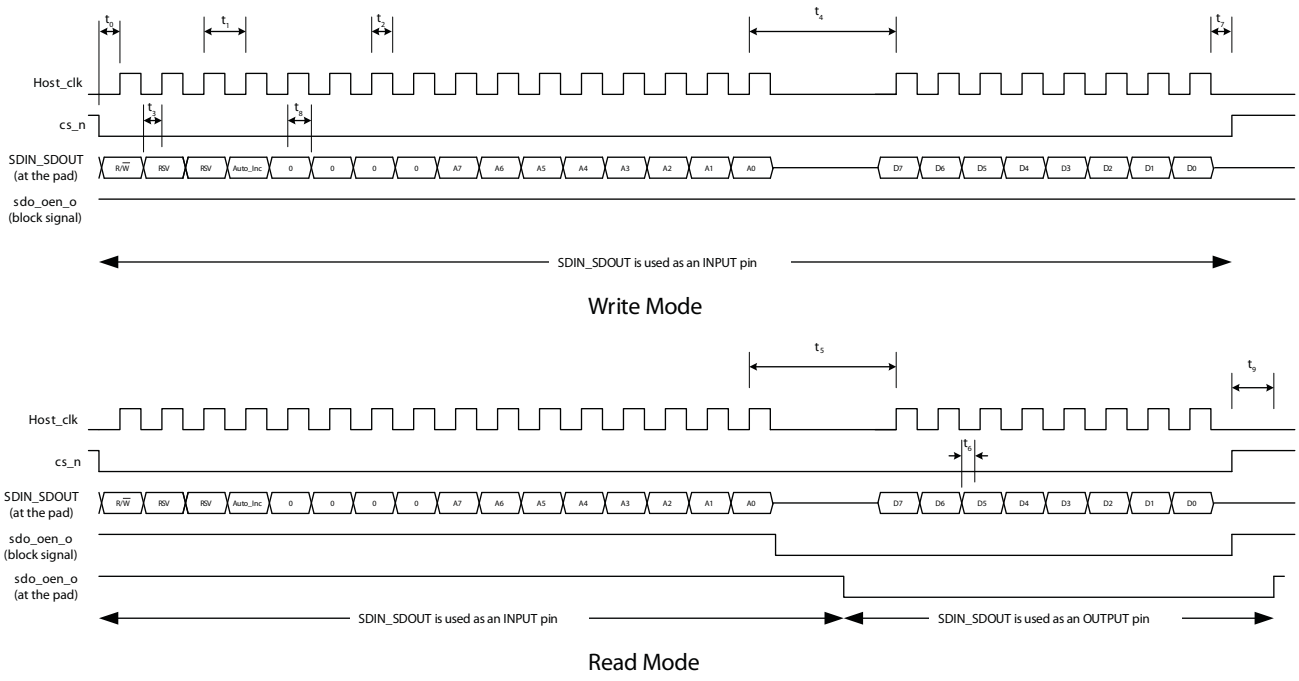


Figure 4-23: SPI Write and Read Timing Diagrams (Single Transaction)

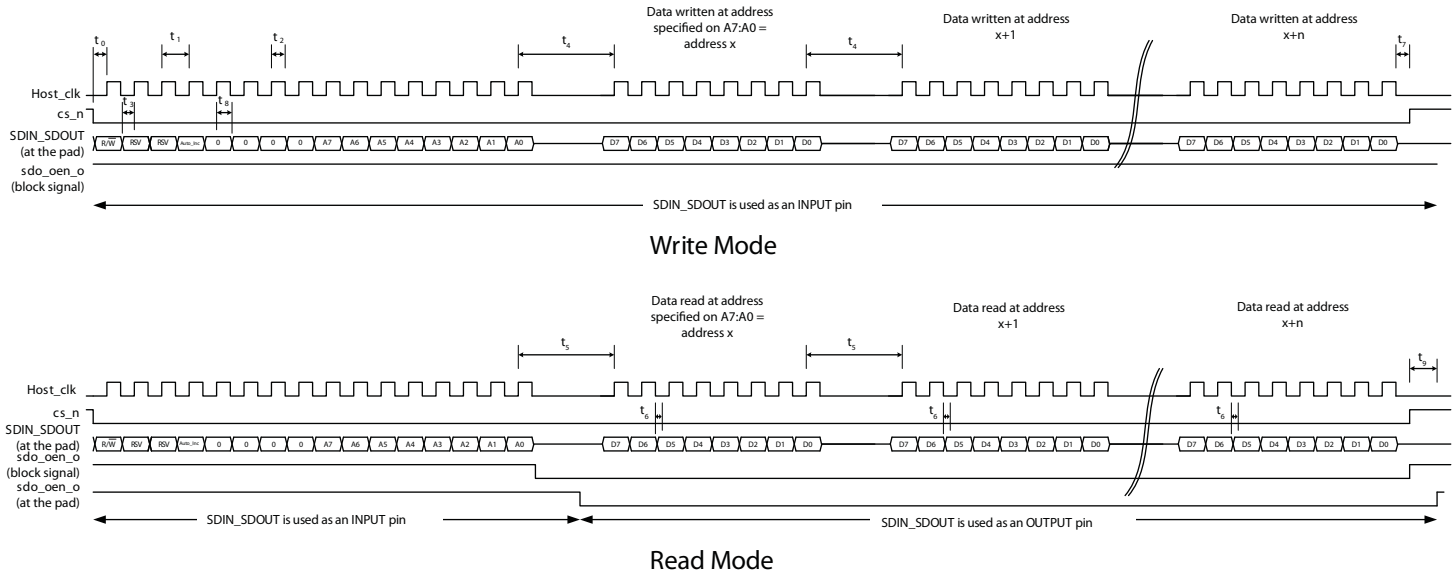


Figure 4-24: SPI Write and Read Timing Diagrams (Auto-Increment Transaction)

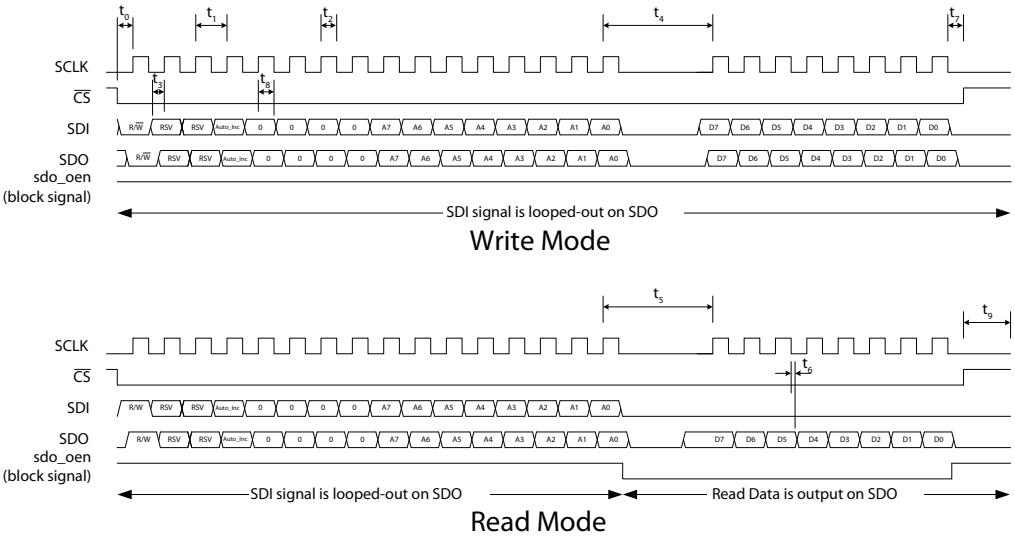


Figure 4-25: SPI Write and Read Timing Diagrams (4-wire)

Table 4-13: SPI Host Interface Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CS_N low before HOST_CLK rising edge	t_0	50% levels; 1.8V operation	1.5	—	—	ns
HOST_CLK period	t_1		100	—	—	ns
HOST_CLK duty cycle	t_2		40	50	60	%
Input data setup time	t_3		1.5	—	—	ns
Time between end of command word (or data in Auto Increment mode) and the first host_clk of the following data word write cycle	t_4		93.5	—	—	ns
Time between end of command word (or data in Auto Increment mode) and the first host_clk of the following data wordread cycle	t_5		420	—	—	ns
Output hold time (15pF load)	t_6		1.5	—	—	ns
CS_N high after last host_clk rising edge	t_7		93.5	—	—	ns
Input data hold time	t_8		1.5	—	—	ns
CS_N high time	t_9		233.6	—	—	ns
CS_N input rise/fall time*	—	20% to 80%	10	—	—	ns

In Figure 4-23, Figure 4-24, and Figure 4-25, CS_N = $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$, HOST_CLK = SCL/SCLK, SDIN_SDOUT = SDA/SDIO, SDI = SSEL/MOSI, and SDO = SDA/SDIO.

There is an auto-increment bit in the command (bit 12) allowing for write burst and read burst transactions.

*The specified minimum rise/fall time must be met to avoid degrading receive sensitivity.

4.10.3 Digital I/O (Schmitt trigger)

A Schmitt trigger is available on the following signals:

- $\overline{\text{ISEL}}/\overline{\text{SCS}}$
- SDA/SDIO in input mode
- SCL/SCK in input mode SSEL/MOSI
- SSEL/MOSI

The transfer characteristics of the Schmitt Trigger buffer are shown in Figure 4-26 below:

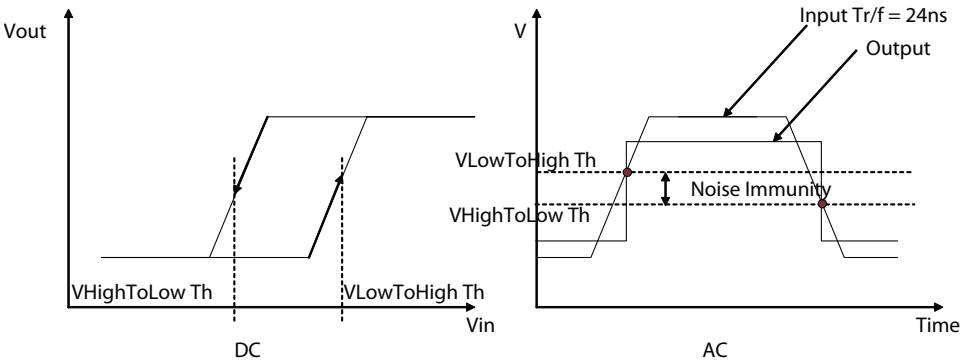


Figure 4-26: Schmitt Trigger Transfer Characteristics

The DC and AC thresholds are shown in Table 2-2: DC Electrical Characteristics.

5. Register Descriptions

Table 5-1: Register Descriptions

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
0	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
1	TOP_REG1	RSVD	7:6	—	0	0-3	Reserved – do not change.
		SPIOUT_OPEN_DRAIN	5:5	RW	0	0-1	0 = Normal SPI operation 1 = Enables SPI output driver open-drain configuration
		MODNR_MASK_TXFAULT	4:4	RW	0	0-1	When HIGH, masks-out TxFault from asserting MODNR.
		MODNR_MASK_TXLOL	3:3	RW	1	0-1	When HIGH, masks-out TxLOL from asserting MODNR.
		MODNR_MASK_TXLOS	2:2	RW	0	0-1	When HIGH, masks-out TxLOS from asserting MODNR.
		MODNR_MASK_RXLOL	1:1	RW	1	0-1	When HIGH, masks-out RxLOL from asserting MODNR.
		MODNR_MASK_RXLOS	0:0	RW	0	0-1	When HIGH, masks-out RxLOS from asserting MODNR.
2	TOP_REG2	LOSL_MASK_TXLOL	7:7	RW	1	0-1	When HIGH, masks-out TxLOL from asserting LOSL.
		LOSL_MASK_TXLOS	6:6	RW	1	0-1	When HIGH, masks-out TxLOS from asserting LOSL.
		LOSL_MASK_RXLOL	5:5	RW	1	0-1	When HIGH, masks-out RxLOL from asserting LOSL.
		LOSL_MASK_RXLOS	4:4	RW	0	0-1	When HIGH, masks-out RxLOS from asserting LOSL.
		OPEN_DRAIN_MODNR	3:3	RW	1	0-1	When HIGH, makes the MODNR output driver open-drain.
		OPEN_DRAIN_LOSL	2:2	RW	1	0-1	When HIGH, makes the LOSL output driver open-drain.
		POLINV_LOSL	1:1	RW	0	0-1	When HIGH, inverts the polarity of the LOSL output.
		POLINV_MODNR	0:0	RW	0	0-1	When HIGH, inverts the polarity of the MODNR output.
3	TOP_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		PRBS_CHK_CLEAR_ERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from the PRBS Checker.
		PRBS_GEN_START	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts the PRBS Generator.
4	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.
5	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
6	TOP_REG6	RSVD	7:1	—	0	0-127	Reserved – do not change.
		PRBS_CHK_STATUS	0:0	RO	0	0-1	When HIGH, the PRBS Checker has detected an error.
7	LOOPBK_REG1	LB_RX_OUT_RX_CLK	7:7	RW	0	0-1	Selects the Rx Clk into the Rx Driver.
		LB_RX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects the PRBS Generator O/P into the Rx Driver.
		LB_RX_OUT_TX_DATA	5:5	RW	0	0-1	Selects the Tx data into the Rx Driver.
		LB_RX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Rx Driver.
		RSVD	3:0	—	0	0-15	Reserved – do not change.
8	LOOPBK_REG2	LB_TX_OUT_TX_CLK	7:7	RW	0	0-1	Selects the Tx Clock into the Tx Driver.
		LB_TX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects the PRBS Generator O/P into the Tx Driver.
		LB_TX_OUT_RX_DATA	5:5	RW	0	0-1	Selects the Rx data into the Tx Driver.
		LB_TX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into Tx Driver.
		RSVD	3:2	—	0	0-3	Reserved – do not change.
		PRBS_CHK_CLK_SEL	1:1	RW	0	0-1	When HIGH, selects the Tx recovered clock. When LOW, selects the Rx recovered clock.
		RSVD	0:0	—	0	0-1	Reserved – do not change.
9	LOOPBK_REG3	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PRBS_GENERATOR_DATA_RATE_CONTROL	5:0	RW	0	0-63	PRBS Generator frequency tuning control. See Section 4.6.1.
10	TXPLL_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TX_PLL_LBW_POS_ADJ	4:0	RW	1110	0-31	Adjusts LBW positive temperature coefficient control. See Section 4.3.2.
11	TXPLL_REG2	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TX_PLL_LBW_NEG_ADJ	4:0	RW	10	0-31	Adjusts LBW negative temperature coefficient control. See Section 4.3.2.
12	RSVD_REG	RSVD	7:0	—	00010010	0-255	Reserved – do not change.
13	RSVD_REG	RSVD	7:0	—	00000101	0-255	Reserved – do not change.
14	TXPLL_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		TX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Tx CDR into bypass mode.
		RSVD	1:1	—	0	0-1	Reserved – do not change.
		TX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
15	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
16	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
17	TXPLL_REG8	TX_JIT_FILT_TRACK_ADJUST	7:3	RW	00010	0-31	Sets the tracking capability when Tx jitter filter mode is enabled. See Section 4.3.3.
		RSVD	2:0	—	101	0-7	Reserved – do not change.
18	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
19	TXPLL_REG10	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		TX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.
20	RXPLL_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		RX_PLL_LBW_POS_ADJ	4:0	RW	11101	0-31	Adjusts LBW positive temperature coefficient control. See Section 4.2.4.
21	RXPLL_REG2	RSVD	7:5	—	0	0-7	Reserved – do not change.
		RX_PLL_LBW_NEG_ADJ	4:0	RW	111	0-31	Adjusts LBW negative temperature coefficient control. See Section 4.2.4.
22	RSVD_REG	RSVD	7:0	—	00010010	0-255	Reserved – do not change.
23	RSVD_REG	RSVD	7:0	—	00000101	0-255	Reserved – do not change.
24	RXPLL_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the CDR into bypass mode.
		RSVD	1:1	—	0	0-1	Reserved – do not change.
		RX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.
25 to 26	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
27	RXPLL_REG8	RX_PLL_SONET_IJT_SETTING	7:3	RW	10	0-31	Control for Sonet IJT performance. Used in conjunction with Sonet IJT modes 2 and 3 to set IJT performance. Gradually increase setting for increased margins. See Section 4.2.5.
		RX_PLL_LOCK_DCD_TOL_DIS	2:2	RW	1	0-1	When LOW, enables tolerance of data duty cycle distortion for locking.
		RSVD	1:0	—	1	0-3	Reserved – do not change.
28	RXPLL_REG9	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_PLL_SELECT_HIGH_IJT	3:3	RW	1	0-1	When HIGH, selects high-margin Sonet IJT mode in conjunction with RX_PLL_SONET_IJT_SETTING. See Section 4.2.5.
		RSVD	2:0	—	0	0-7	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
29	RXPLL_REG10	RSVD	7:2	—	0	0-63	Reserved – do not change.
		RX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		RX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.
30	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
31	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
32	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
33	TX_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TX_EQ_BOOST	1:0	RW	11	0-3	Controls the Tx path input equalization setting: 00 = 0dB 01 = 2dB 10 = 4dB 11 = 6dB
34	RSVD_REG	RSVD	7:0	—	111111	0-255	Reserved – do not change.
35	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
36	RSVD_REG	RSVD	7:0	—	101	0-255	Reserved – do not change.
37	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
38	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
39	TX_REG9	TXLOS_TH_NEG	7:0	RW	11011	0-255	Negative temperature coefficient LOS threshold setting. Refer to Section 4.5.2.
40	TX_REG10	TXLOS_TH_POS	7:0	RW	0	0-255	Positive temperature coefficient LOS threshold setting. Refer to Section 4.5.2.
41	TX_REG11	RSVD	7:4	—	0	0-15	Reserved – do not change.
		TXLOS_HYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB.
42	TX_REG12	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TXLOS_FORCE_ASSERT_EN	4:4	RW	0	0-1	When HIGH, LOS is controlled by TXLOS_FORCE_ASSERT.
		TXLOS_FORCE_ASSERT	3:3	RW	0	0-1	Directly sets the state of TXLOS accordingly if TXLOS_FORCE_ASSERT_EN is HIGH.
		RSVD	2:0	—	0	0-7	Reserved – do not change.
43	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
44	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
45	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
46	RSVD_REG	RSVD	7:0	—	1111	0-255	Reserved – do not change.
47	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
48	RX_REG1	RSVD	7:4	—	111	0-15	Reserved – do not change.
		RXLA_BOOST_MSB	3:0	RW	0	0-15	RXLA boost control bit MSBs. 0 = 0dB to 15 = 14dB
49	RX_REG2	RXLA_SLICE_ADJ	7:0	RW	0	0-255	Slice adjust magnitude control.
50	RX_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		RXLA_SLICE_ADJ_LO_RANGE	1:1	RW	0	0-1	Selects slice level adjust point. When LOW, slicing point is option 1. When HIGH, slicing point is option 2. See Section 4.2.2.
		RXLA_SLICE_ADJ_POL	0:0	RW	0	0-1	Slice adjust polarity. When HIGH, slice adjust is positive.
51	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
52	RX_REG5	RSVD	7:1	—	1000	0-127	Reserved – do not change.
		RXLA_MANUAL_SLICE_ADJ_EN	0:0	R/W	0	0-1	When HIGH, enables user to adjust slice level at Rx input. See Section 4.2.2.
53	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
54	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
56	RX_REG9	RXLOS_TH_NEG	7:0	RW	1001001	0-255	Negative tempco LOS threshold setting.
57	RX_REG10	RXLOS_TH_POS	7:0	RW	0	0-255	Positive tempco LOS threshold setting.
58	RX_REG11	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RXLOS_HYS	3:0	RW	1001	0-15	Hysteresis control 0-15 -> 0-6dB. Default 9 = 3dB.
59	RX_REG12	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RXLOS_FORCE_ASSERT_EN	3:3	RW	0	0-1	When HIGH, LOS is controlled by RXLOS_FORCE_ASSERT.
		RXLOS_FORCE_ASSERT	2:2	RW	0	0-1	Directly sets the state of RXLOS accordingly if RXLOS_FORCE_ASSERT_EN is HIGH.
		RXLOS_RANGE	1:0	RW	1	0-3	LOS range: 0 = highest 3 = lowest
60	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
61	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
62	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
63	RX_REG16	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RXLA_BOOST_LSB	2:0	RW	0	0-7	RXLA boost control bit LSBs for fine tuning gain with smaller step size. See Section 4.2.3.
64	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
65 to 74	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
75	RXSDO_REG1	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_SDO_SWING	3:0	RW	110	0-15	Driver swing: 100mV$_{ppd}$ to 850mV$_{ppd}$, Default = 6 = 400mV$_{ppd}$
76	RXSDO_REG2	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_SDO_EMPHASIS	3:0	RW	0	0-15	Driver emphasis control.
77	RXSDO_REG3	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_SDO_PWR_DN_ON_MUTE	2:2	RW	1	0-1	Enables power-down on mute for output stage.
		RX_SDO_AUTO_MUTE_EN	1:1	RW	1	0-1	Enables muting the driver upon LOS.
		RX_SDO_FORCE_MUTE	0:0	RW	0	0-1	Mutes driver to CM when not in auto mute mode.
78	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
79	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
80	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
81	RSVD_REG	RSVD	7:0	—	11110001	0-255	Reserved – do not change.
82	TXSDO_REG5	RSVD	7:2	—	0	0-63	Reserved – do not change.
		IPH_RANGE_SEL	1:0	RW	10	0-3	IPHOTO range select: 00 = 0mA to 0.25mA 01 = 0.25mA to 0.75mA 10 = 0.75mA to 1.25mA 11 = 1.25mA to 2.14mA
83	RSVD_REG	RSVD	7:0	—	110	0-255	Reserved – do not change.
84	RSVD_REG	RSVD	7:0	—	110110	0-255	Reserved – do not change.
85	TXSDO_REG8	RSVD	7:4	—	0	0-15	Reserved – do not change.
		TXSDO_BIAS_MON_EN	3:3	RW	0	0-1	Enables the laser driver bias monitor circuitry.
		TXSDO_MOD_MON_EN	2:2	RW	0	0-1	Enables the laser driver modulation monitor circuitry.
		RSVD	1:0	—	11	0-3	Reserved – do not change.
86	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
87	TXSDO_REG10	TXSDO_IMOD_LO	7:0	RW	0	0-255	LD modulation current LSB.
88	TXSDO_REG11	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TXSDO_IMOD_HI	1:0	RWC	0	0-3	LD modulation current MSB.
89	TXSDO_REG12	RSVD	7:6	—	0	0-3	Reserved – do not change.
		TXSDO_CPA	5:0	RW	11111	0-63	LD crossing point adjust: 0~ = > 80% 31 = 50% 63~ = < 20%

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
90	TXSDO_REG13	TXSDO_PHASE_ADJUST	7:0	RW	0	0-255	LD phase adjust—compensation for jitter generation due to Sonet header.
91	TxSDO_REG14	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TXDSO_PREEMPH_AMP	4:0	RW	00000	0-31	LD pre-emphasis amplitude control.
92	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
93	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
94	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
95	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
96	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
97	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
98	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
99	TXSDO_REG25	RSVD	7:6	—	0	0-255	Reserved – do not change.
		TXSDO_PWR_DN_ON_MUTE	5:5	RW	1	0-1	When HIGH, enables power-down on mute for output stage.
		TXSDO_AUTO_MUTE_EN	4:4	RW	1	0-1	When HIGH, enables muting the driver upon LOS.
		TXSDO_FORCE_MUTE	3:3	RW	0	0-1	When HIGH, mutes driver to CM when not in auto mute mode.
		TXSDO_FORCE_TXDSBL	2:2	RW	0	0-1	When HIGH, shuts down the LD mod, bias and APC.
		TXSDO_PHASEADJ_DIR	1:1	RW	0	0-1	LD phase adjust (Z0) compensation direction E/L:0/1.
		TXSDO_MOD_SQUELCH	0:0	RW	0	0-1	When HIGH, LD modulation is squelched.
100	TXSDO_REG26	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TXSDO_BIAS_SINK_EN	4:4	RW	0	0-1	LD bias sink is enabled when HIGH. TXSDO_BIAS_SOURCE_EN must be LOW.
		TXSDO_BIAS_SOURCE_EN	3:3	RW	1	0-1	LD bias source is enabled when HIGH. TXSDO_BIAS_SINK_EN must be LOW.
		RSVD	2:0	—	001	0-7	Reserved – do not change.
101	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
102	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
103	RSVD_REG	RSVD	7:0	—	11000010	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
104	APC_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		APC_SEL_HIGH_REF	4:4	RW	0	0-1	When HIGH, IPHOTO is sourced from the GN2044 and is sunk in the TOSA. When LOW, IPHOTO is sourced from the TOSA and is sunk in the GN2044.
		APC_RESET	3:3	RW	0	0-1	When HIGH, the APC control loop is reset.
		RSVD	2:1	—	0	0-3	Reserved – do not change.
		APC_EN	0:0	RW	1	0-1	When HIGH, enables the APC.
105	APC_REG2	RSVD	7:7	—	0	0-1	Reserved – do not change.
		APC_CLK_RATE_SLOW_DIV	6:4	RW	101	0-7	APC update rate3 divide ratio: 0 = 32 1 = 64 2 = 128 3 = 256 4 = 512 5 = 1024 (default) 6 = 2048 7 = 4096
		APC_CLK_RATE_FAST_DIV	3:2	RW	0	0-3	APC update rate2 divide ratio: 0 = 32 (default) 1 = 64 2 = 128 3 = 256
		RSVD	1:0	—	0	0-3	Reserved – do not change.
106	APC_REG4	APC_DAC_OVR_VAL_LO	7:0	RW	0	0-255	Override value for the APC DAC counter [7:0]. Sets the LD bias current manually when used with APC_DAC_OVR_VAL_HI, and when APC_OVR is HIGH. Step size is approximately 0.15mA.
107	APC_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		APC_OVR	2:2	RW	0	0-1	When HIGH, overrides the APC loop with the DAC override value to set the LD bias current manually.
		APC_DAC_OVR_VAL_HI	1:0	RWC	0	0-3	Override APC DAC [9:8]. A write triggers an update.
108	APC_REG6	APC_REF_DAC_CTRL	7:0	RW	0	0-255	Sets the APC final target reference threshold.
109	APC_REG7	RSVD	7:0	—	01000110	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
110	APC_REG8	RSVD	7:7	—	0	0-1	Reserved – do not change.
		APC_TH_HI_BYPASS	6:6	RW	0	0-1	When HIGH, bypasses Threshold Hi and associated APC clock rate.
		APC_TH_HI	5:0	RW	110110	0-63	APC Threshold Hi setting 110110 (default) - 0.9x of setpoint 1 LSB = 0.0167x of setpoint.
111	APC_REG9	RSVD	7:2	—	0	0-63	Reserved – do not change.
		APC_DAC_VAL_LO	1:0	RO	0	0-3	Read out value from the APC DAC counter [1:0].
112	APC_REG10	APC_DAC_VAL_HI	7:0	RO	0	0-255	Read out value from the APC DAC counter [9:3].
113	TXFLT_REG1	RSVD	7:7	—	0	0-1	Reserved – do not change.
		TXFAULT_CLEAR_STATUS	6:6	RW	0	0-1	When HIGH, clears the latched Tx fault status.
		TXFAULT_DISABLE_EN	5:5	RW	0	0-1	When HIGH, a TxDisable assertion triggers a fault.
		TXFAULT_LD_IPHOTO_EN	4:4	RW	1	0-1	Enables IPHOTO monitoring for Fault.
		TXFAULT_LDMOD_CUR_EN	3:3	RW	1	0-1	Enables LD Modulation monitoring for fault.
		TXFAULT_LDBIAS_CUR_EN	2:2	RW	1	0-1	Enables LD Bias Current monitoring for Fault.
		TXFAULT_LDBIAS_V_EN	1:1	RW	1	0-1	Enables LD Bias Voltage monitoring for Fault.
		TXFAULT_EN	0:0	RW	1	0-1	Enable all Tx Faults.
114	TXFLT_REG2	RSVD	7:3	—	0	0-31	Reserved – do not change.
		TXFAULT_LDBIAS_VTH	2:0	RW	0	0-7	Fault threshold for LD Bias minimum voltage. The fault threshold covers a range of 0 to 800mV on the LDBias pin, in steps of 100mV typical. If LDBias is set to source mode, the fault threshold covers V_{CC} to V_{CC}-800mV in 100mV steps.
115	TXFLT_REG3	TXFAULT_LDBIAS_CUR_TH	7:0	RW	11111111	0-255	Fault threshold for LD Bias maximum current. The fault threshold covers a range of 147mA of LD bias current in steps of 0.575mA typical.
116	TXFLT_REG4	TXFAULT_LDMOD_CUR_TH	7:0	RW	11111111	0-255	Fault threshold for LD Mod maximum current. The fault threshold covers a range of 0-100mA$_{pp}$ LD modulation current in steps of 0.4mA$_{pp}$ typical.
117	TXFLT_REG5	TXFAULT_LD_IPHOTO_TH	7:0	RW	11111111	0-255	Fault threshold for APC IPHOTO maximum voltage.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
118	TXFLT_REG6	RSVD	7:6	—	0	0-3	Reserved – do not change.
		TXFAULT_MUTE_EN	5:5	RW	0	0-1	When HIGH, mutes fault output, faults reported through register status only.
		TXDISABLE_TO_CLEAR_FAULT	4:4	RW	0	0-1	When HIGH, TxDSBL clears faults.
		RSVD	3:0	—	1111	0-15	Reserved – do not change.
119	TXFLT_REG7	RSVD	7:7	—	0	0-1	Reserved – do not change.
		TXFAULT_MODNR	6:6	RO	0	0-1	Reflects the status of the MODNR pin due to TxFault. It can be used to identify the source of the MODNR assertion.
		RSVD	5:5	—	0	0-1	Reserved – do not change.
		TXFAULT_DRV_DISABLE	4:4	RO	0	0-1	Fault status of TxDisable. When HIGH, there is a fault condition.
		TXFAULT_LD_IPHOTO	3:3	RO	0	0-1	Fault status of IPHOTO. When HIGH, there is a fault condition.
		TXFAULT_LDMOD_CUR	2:2	RO	0	0-1	Fault status of LD Mod Current. When HIGH, there is a fault condition.
		TXFAULT_LDBIAS_CUR	1:1	RO	0	0-1	Fault status of LD Bias Current. When HIGH, there is a fault condition.
		TXFAULT_LDBIAS_V	0:0	RO	0	0-1	Fault status of the LD Bias Voltage node. When HIGH, there is a fault condition.
120	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
121	ADC_REG0	RSVD	7:4	—	0	0-15	Reserved – do not change.
		ADC_AUTO_CALIBRATION_EN	3:3	RW	1	0-1	1 = Enables Auto ADC Calibration mode 0 = Disables Auto ADC Calibration mode
		ADC_JUST_LSB	2:2	RW	1	0-1	When HIGH, justify towards LSB. When LOW justify towards MSB.
		ADC_AUTO_CONV_EN	1:1	RW	1	0-1	When HIGH, enables auto conversion, set LOW for manual.
		ADC_RESET	0:0	RW	1	0-1	Reset for the ADC.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
		RSVD	7:4	—	0	0-15	Reserved – do not change.
122	ADC_REG1	ADC_SRC_SEL	3:0	RW	0	0-15	Selects ADC source used for measurement: 0000 = ADC reference voltage 0001 = Laser driver bias monitor 0010 = Photo diode voltage at IPHOTO 0011 = Laser driver modulation monitor 0100 = Temperature sensor (vbe@255µA) 0101 = Temperature sensor (vbe@2.55µA) 0110 = V3p3 supply (0.75*v3p3) 0111 = V1p8 supply (0.5*v1p8)
123	ADC_REG2	RSVD	7:7	—	0	0-1	Reserved – do not change.
		ADC_CLK_RATE	6:3	RW	11	0-15	ADC clock divide ratio.
		ADC_RESOLUTION	2:0	RWC	11	0-7	ADC resolution control: 0-6 -> 4,6,8,10,12,14,16 bits.
124	ADC_REG3	RSVD	7:1	—	0	0-127	Reserved – do not change.
		ADC_START_CONV	0:0	RWC	0	0-1	ADC start conversion.
125	ADC_REG4	RSVD	7:1	—	0	0-127	Reserved – do not change.
		ADC_DONE_CONV	0:0	RO	0	0-1	ADC conversion done flag.
126	ADC_REG5	ADC_OUT_LO	7:0	RO	0	0-255	ADC output low MSB.
127	ADC_REG6	ADC_OUT_HI	7:0	RO	0	0-255	ADC output high MSB.
128	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
129	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
130	TXPWRDN_REG1	RSVD	7:3	—	0	0-31	Reserved – do not change.
		TX_PD_TXSDO	2:2	RW	0	0-1	When HIGH, power-down for the entire laser driver.
		TX_PD_TXCDR	1:1	RW	0	0-1	When HIGH, power-down for the entire Tx CDR.
		TX_PD_TXPATH	0:0	RW	0	0-1	When HIGH, Power-down for the entire Tx path.
131	TXPWRDN_REG2	RSVD	7:2	—	100000	0-63	Reserved – do not change.
		TX_PD_LOS	1:1	RW	0	0-1	When HIGH, power-down for the Tx LOS.
		TX_PD_EQ	0:0	RW	0	0-1	When HIGH, power-down for the Tx input Equalizer.
132	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
133	TXPWRDN_REG4	RSVD	7:1	—	0000111	0-127	Reserved – do not change.
		TX_PD_JIT_FILT	0:0	RW	1	0-1	When HIGH, power-down for the Tx jitter filter.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
134	RXPWRDN_REG1	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_PD_RXSDO_EMPHASIS	3:3	RW	1	0-1	When HIGH, power-down for the trace driver pre-emphasis.
		RX_PD_RXSDO	2:2	RW	0	0-1	When HIGH, power-down for the Rx path trace driver.
		RX_PD_RXCDR	1:1	RW	0	0-1	When HIGH, power-down for the entire Rx CDR.
		RX_PD_PATH	0:0	RW	0	0-1	When HIGH, power-down for the entire Rx path.
135	RXPWRDN_REG2	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_PD_LOS	2:2	RW	0	0-1	When HIGH, power-down for the Rx path LOS.
		RX_PD_SLICE_ADJ	1:1	RW	1	0-1	When HIGH, power-down for the LA slice adjust.
		RX_PD_LA	0:0	RW	0	0-1	When HIGH, power-down for the Rx path LA.
136	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
137	RXPWRDN_REG4	RSVD	7:1	—	111	0-127	Reserved – do not change.
		RX_PD_SONET_IJT	0:0	RW	0	0-1	When HIGH, powers-down the Rx path Sonet IJT feature to save power.
138	PWRDN_REG1	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PD_APC	5:5	RW	0	0-1	When HIGH, power-down for APC blocks.
		RSVD	4:4	—	1	0-1	Reserved – do not change.
		PD_TXSDO_CPA	3:3	RW	1	0-1	When HIGH, power-down for the LD crossing point adjust.
		PD_TXSDO_PHASE_ADJ	2:2	RW	1	0-1	When HIGH, power-down for the LD phase adjust (Z0) compensation.
		RSVD	1:1	—	1	0-1	Reserved – do not change.
		PD_TXSDO_PREEMPH	0:0	RW	1	0-1	When HIGH, power-down for the LD pre-emphasis.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
139	PWRDN_REG2	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PD_ADC	5:5	RW	1	0-1	When HIGH, power-down for the ADC.
		PD_SUPPLY_SENSOR	4:4	RW	1	0-1	When HIGH, power-down for the supply sensor.
		PD_TEMP_SENSOR	3:3	RW	1	0-1	When HIGH, power-down for the temperature sensor(s).
		PD_PRBS_CHK	2:2	RW	1	0-1	When HIGH, power-down for the PRBS Checker and associated buffers.
		PD_PRBS_GEN	1:1	RW	1	0-1	When HIGH, power-down for the PRBS Generator and associated buffers.
		RSVD	0:0	—	1	0-1	Reserved – do not change.
140 to 153	RSVD_REG	RSVD	All	—	0	0-255	Reserved – do not change.
154	TXLBW_REG1	RSVD	7:1	—	0	0-127	Reserved – do not change.
		TX_DYN_LBW_ENABLE	0:0	RW	1	0-1	Tx dynamic loop bandwidth block enable: 0 = disabled 1 = enabled
155	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.
156	RSVD_REG	RSVD	7:0	—	00000011	0-255	Reserved – do not change.
157	RSVD_REG	RSVD	7:0	—	00011111	0-255	Reserved – do not change.
158	RSVD_REG	RSVD	7:0	—	00000100	0-255	Reserved – do not change.
159	RXLBW_REG1	RSVD	7:1	—	0	0-127	Reserved – do not change.
		RX_DYN_LBW_ENABLE	0:0	RW	1	0-1	Rx dynamic loop bandwidth block enable: 0 = Disabled 1 = Enabled
160 to 221	RSVD_REG	RSVD	All	—	0	0-255	Reserved – do not change.

6. Applications Information

6.1 Typical Application Circuit

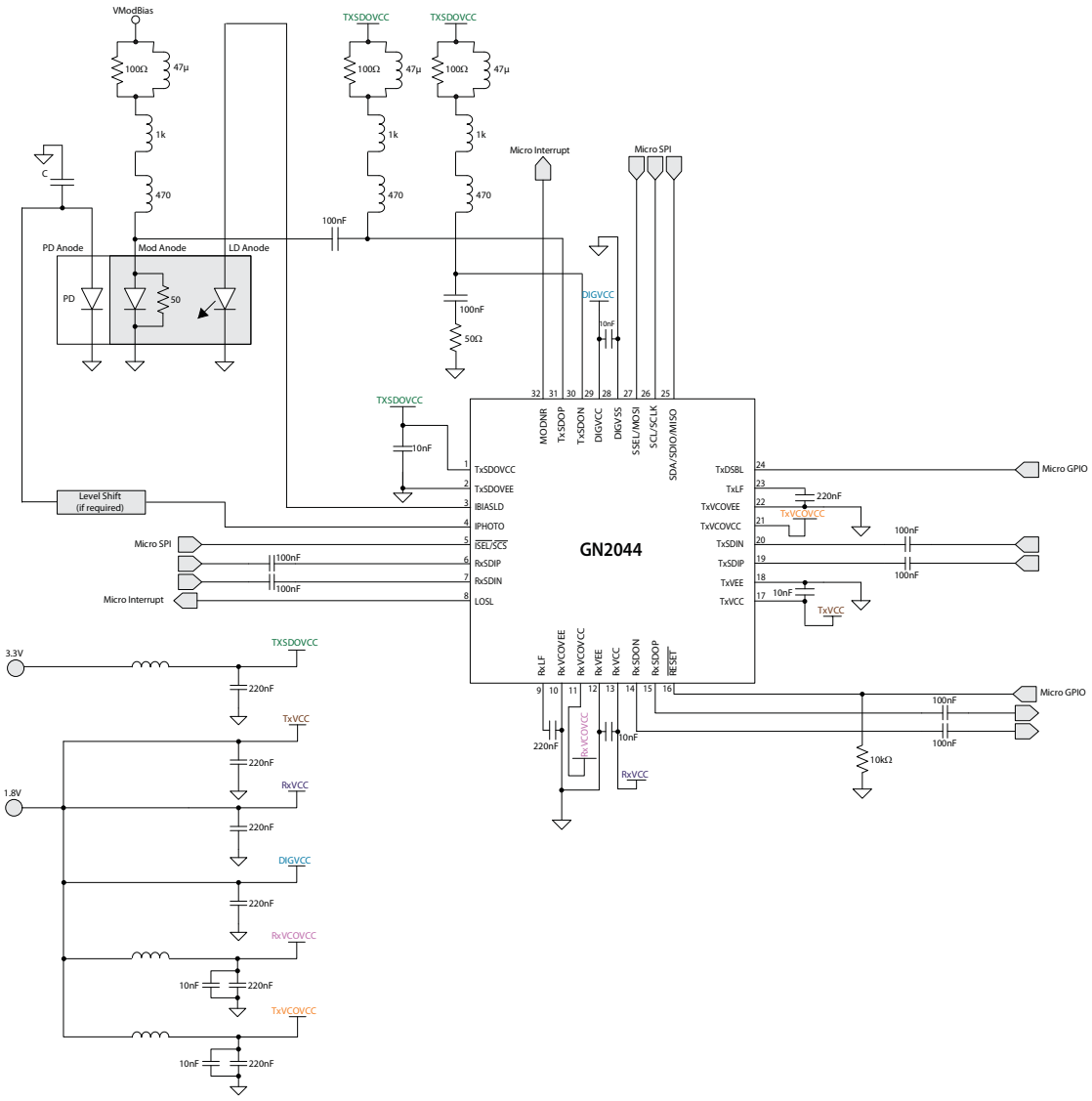


Figure 6-1: Typical Application Circuit

- Use high-quality, temperature-stable LF capacitors. For example, silicon, tantalum or C0G dielectric ceramic capacitors. Lower quality capacitors such as X7R are more sensitive to environmental conditions and may not perform adequately across conditions for this node. Silicone conformal coating can be used with such capacitors as an effective way to mitigate environmental sensitivity

  Note: Please refer to the document "Preventing Loop Filter Capacitor Leakage Current" (PDS-060519) for more information.

- Place lowest value decoupling capacitor closest to the device
- Component values for the TOSA interface must be optimized for the TOSA type
- Status indicator connections are shown for a LVCMOS/LVTTL compatible mode. These I/Os can be configured as open-drain with pull-up
- Host interface is shown configured for SPI mode. I^2C mode is also supported

6.2 Power Supply Filter Recommendations

RC filters for isolating supplies are not recommended due to the large currents drawn from each supply.

- The Tx and Rx VCOs do not have independent supplies; additional filtering for the VCOs is not required

For improved isolation between the Tx and Rx paths, and to achieve the best Rx sensitivity and Tx jitter generation, a supply filter such as the one shown in Figure 6-2 is recommended.

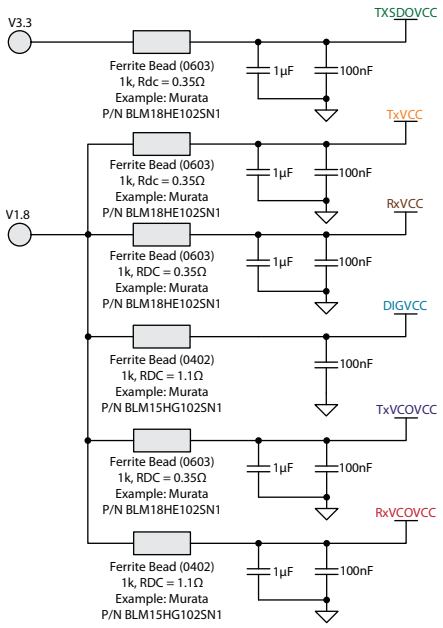


Figure 6-2: Power Supply Filter Recommendations

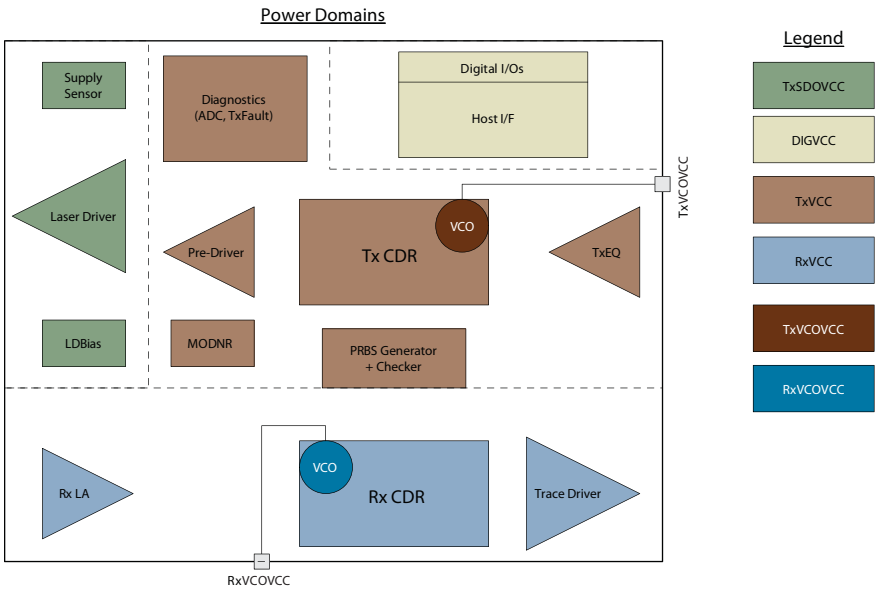


Figure 6-3: Power Supply Domains

6.3 Layout Considerations

The following high-frequency design rules should be considered to achieve optimum performance of the GN2044:

- Use carefully designed controlled-impedance transmission lines with minimal local discontinuities for all high-speed data signals
- Place decoupling capacitors as close as possible to the supply pins
- For optimal electrical and thermal performance, the QFN's exposed pad should be soldered to the module ground plane
- It is recommended to have LF cap ground and VCO caps ground to be common with multiple stitching of vias to ground. Capacitors should be placed from smallest value to largest value away from chip. In addition, the connection from the LF pin to the capacitor should be as small as possible with no vias. Figure 6-4 below demonstrates this technique:

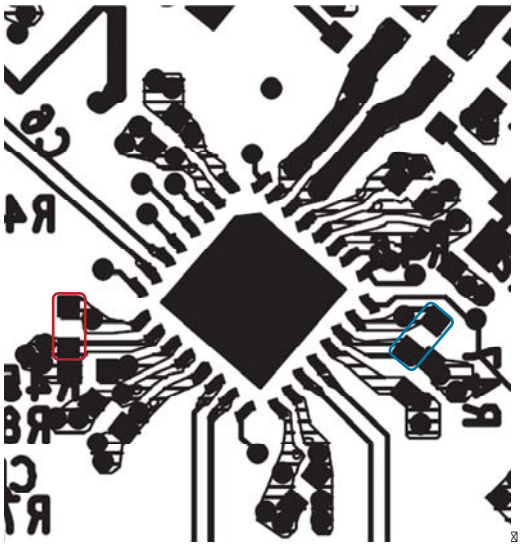


Figure 6-4: Loop Filter Capacitor PCB Layout

- All supply decoupling capacitors should have multiple vias to ground/power planes, and placed as close to chip as possible
- All supplies/grounds should be routed to corresponding decoupling capacitors pads, and never to the centre pad
- The recommended PCB layout for the GN2044 device is shown in Figure 7-2
- Use high-quality, temperature-stable LF capacitors (i.e. capacitors connected to pins 9 and 23). For example: X7R or C0G dielectrics for ceramic capacitors. Lower quality capacitors with smaller package sizes (e.g. 0201) are more sensitive to environmental conditions and may not perform adequately across conditions for this node. Silicone conformal coating is also an effective way to mitigate environmental sensitivity

7. Package and Ordering Information

7.1 Package Dimensions

The GN2044 is a 5mm x 5mm, 32-pin QFN.

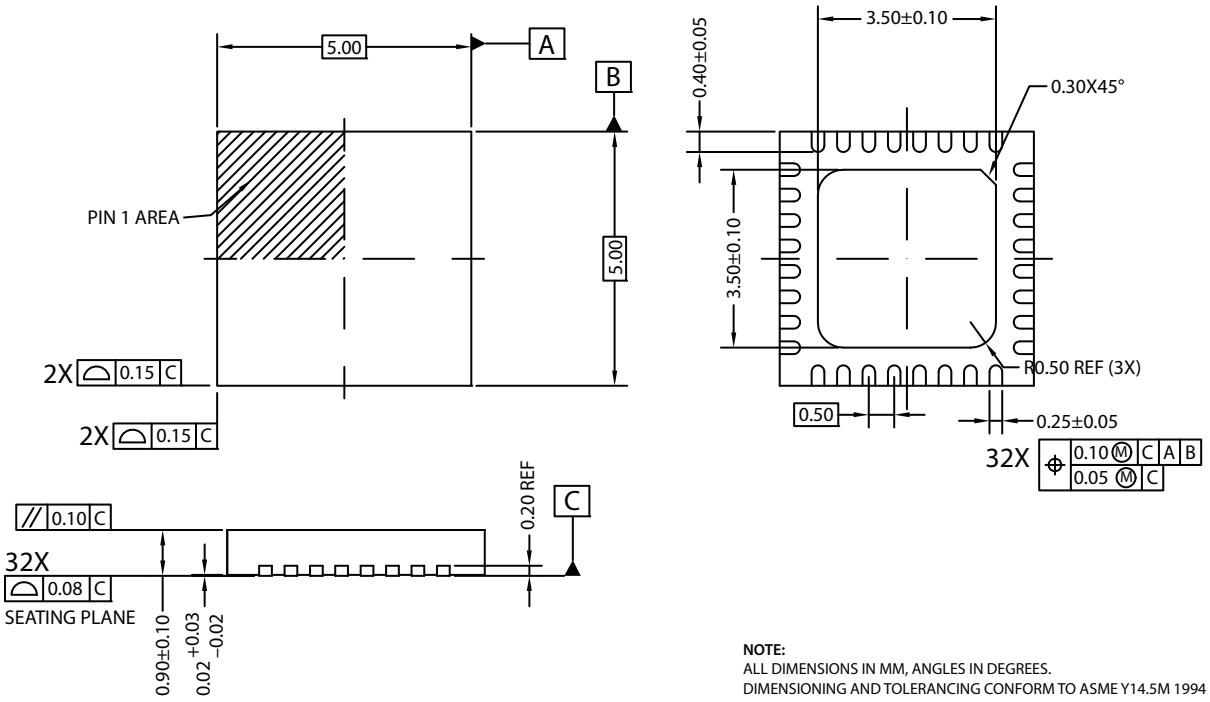
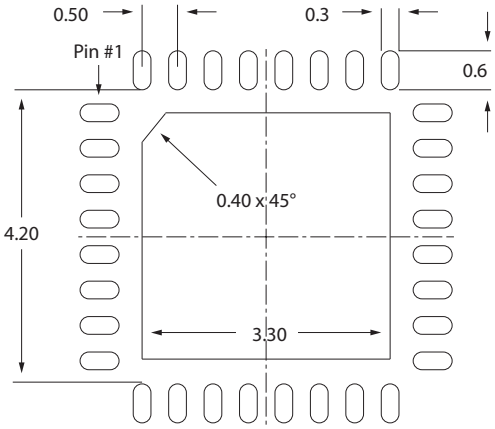


Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint



Notes:
1. All dimensions in mm.
2. Drawing not to scale.
3. 16 thermal relief pins, evenly spaced on centre paddle, connected to ground plane.
4. Drill size: 0.254mm.

Figure 7-2: Recommended PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	32-pin QFN / 5mm x 5mm / 0.5mm pad pitch
Moisture Sensitivity Level	1
Junction to Case Thermal Resistance, θ_{j-c}	17.8°C/W
Junction to Air Thermal Resistance (at zero airflow), θ_{j-a}	26.4°C/W
Psi = Junction-to-Top (of Package) Characterization Parameter, Ψ	0.4°C/W
Pb-free and RoHS compliant	Yes

7.4 Solder Reflow Profile

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 7-3.

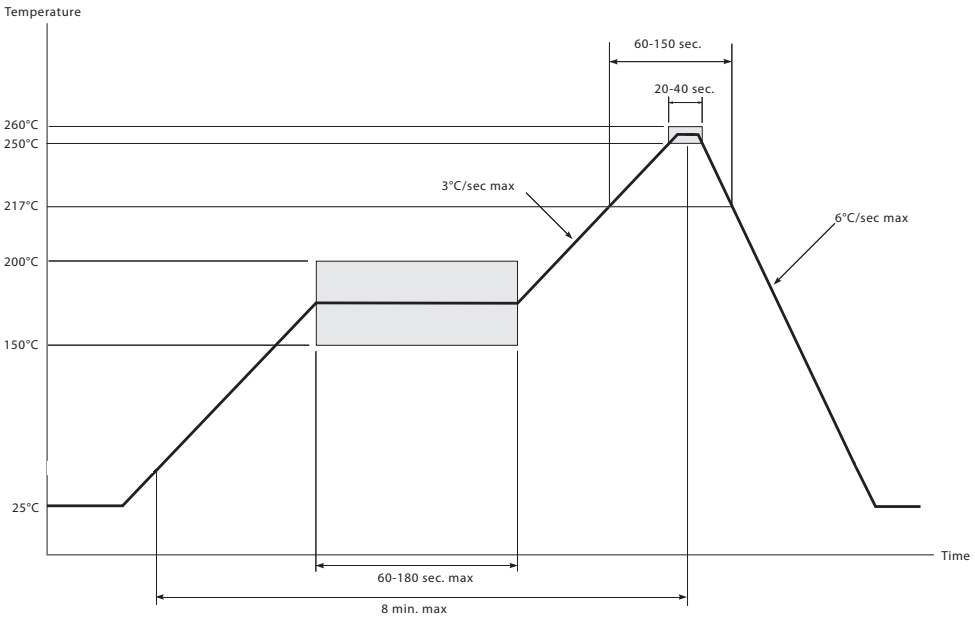


Figure 7-3: Maximum Pb-free Solder Reflow Profile

7.5 Marking Diagram

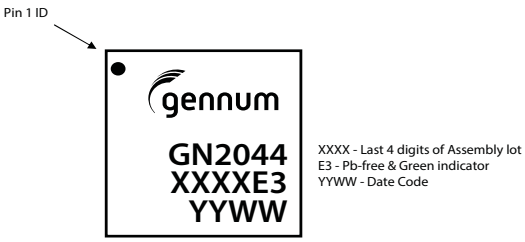


Figure 7-4: Marking Diagram

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Package	Case Temperature Range
GN2044-INE3	32-pin QFN	-40°C to +100°C
GN2044-INTE3D	32-pin QFN (500pc tape and reel)	-40°C to +100°C

DOCUMENT IDENTIFICATION
FINAL DATA SHEET
The product is in production. Semtech reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

GN2044S

Dual-CDR Multi-rate Transceiver with EML Driver

Features

- Dual CDR with 9.8 to 11.3Gb/s reference-free operation and integrated EAM/EML laser driver
- Low power to enable SFP+ <1.5W 40km SONET modules
- Integrated Jitter Filter to ensure robust jitter generation performance and margin to the OC192 standards
- APC loop improvements, including:
  - High dynamic range photodiode current detector
- Integrated limiting amplifier with typical sensitivity of 2.5mV
- Digital control through I^2C or SPI interface
- Programmable Jitter Transfer bandwidth
- Bi-directional loopback
- Highly-configurable, including the following programmable features:
  - Limiting Amplifier Equalization
  - Transmit Input Equalization
  - Input Slice Level Adjust
  - LOS with adjustable threshold and hysteresis
  - Tx Fault signalling
  - Polarity invert and mute in both directions
  - Rx Output De-emphasis
  - Tx Output Eye Shaping
- Integrated analog to digital converter, which provides access to digital diagnostic information on supply voltage, die temperature, transmit optical power, modulation current, biasing current, etc.
- Integrated laser safety features
- Pb-free/RoHS-compliant

Applications

- XFP & SFP+ 10Gb/s SONET optical transceivers
- XFP & SFP+ 10GBase-ER/ZR optical transceivers
- XFP DWDM optical transceivers

General Description

The GN2044S is an integrated bi-directional CDR, EML laser driver and limiting amplifier designed specifically to enable low power SFP+ re-timed modules for SONET. Based on the Semtech ClearEdge™ technology, the GN2044S delivers best in class eye quality.

In addition to enabling lower power modules, the GN2044S offers a selectable jitter filter to ensure margin to difficult to meet jitter generation specifications. The GN2044S also features an improved APC loop with extended dynamic range and increased resolution to support a wide variety of TOSAs.

The transmit path consists of optional input equalization, a multi-rate Tx CDR, and an EML laser driver. The receive path is comprised of a limiting amplifier with programmable equalization, a multi-rate Rx CDR, and output de-emphasis. The transmit direction offers a highly-configurable eye shaping feature, including programmable pre-emphasis, which allows for an optimal electrical and optical output. Both directions offer the option for polarity-invert, loopback, and output mute.

The GN2044S has an integrated analog to digital converter, which through the serial interface, provides digital diagnostic information on supply voltage, die temperature, and transmit optical power. The GN2044S also offers integrated laser safety features.

By integrating the laser driver, the GN2044S offers an extremely low-power solution for EML based optical modules. It consumes only 790mW typical from a 3.3V supply and a 1.7V supply, with the laser driver biased at 80mA bias current and $1.9V_{pp}$ single-ended swing.

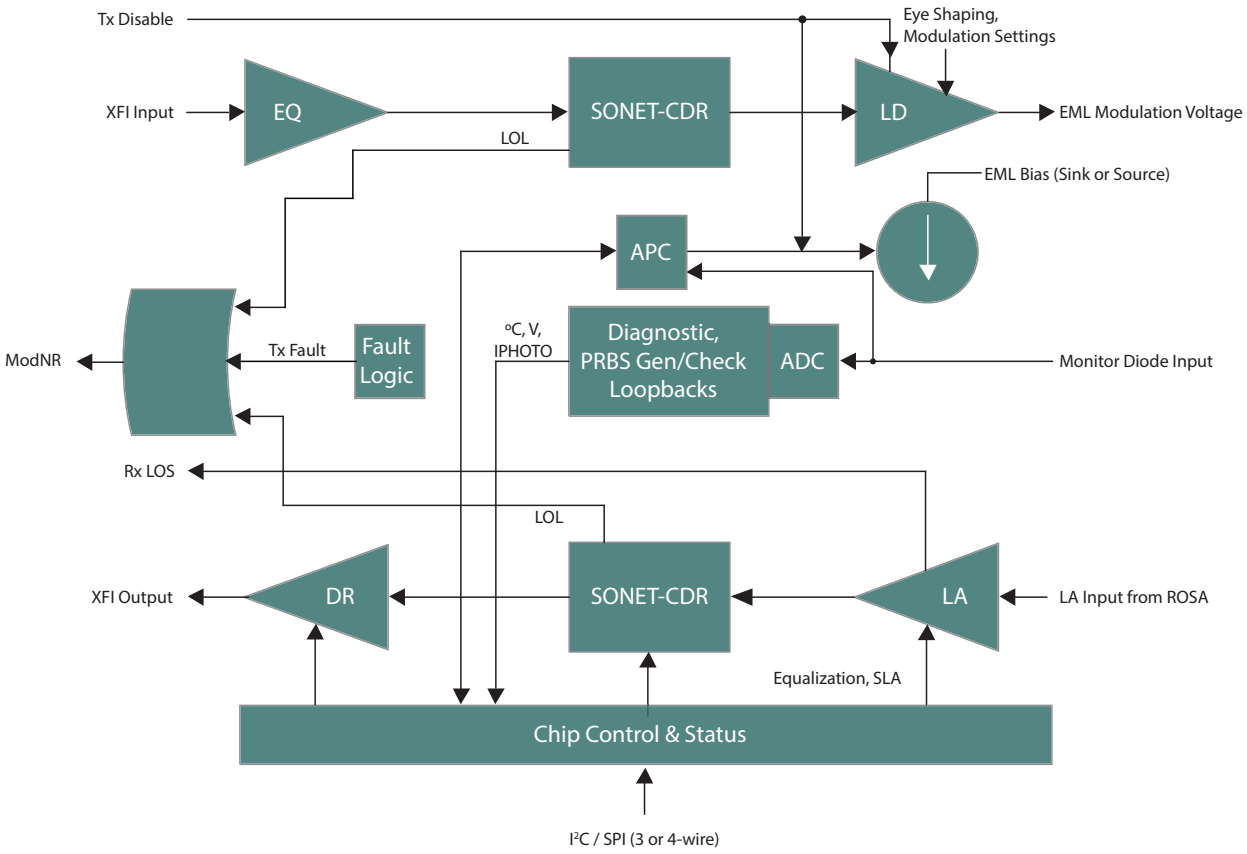


Figure A: GN2044S Functional Block Diagram

EML Laser Driver Features

- Low power EML driver
- Laser bias current up to 120mA
- Option for source or sink bias current
- Modulation swing of up to 2.5V_{pp} single-ended
- 2x 50Ω single-ended terminations
- Transmitter disable pin
- Crossing point adjustment
- Programmable analog pre-emphasis with peaking control
- Jitter Optimization with Phase Adjust feature
- Optional on-chip APC loop
- Programmable Tx Fault signalling

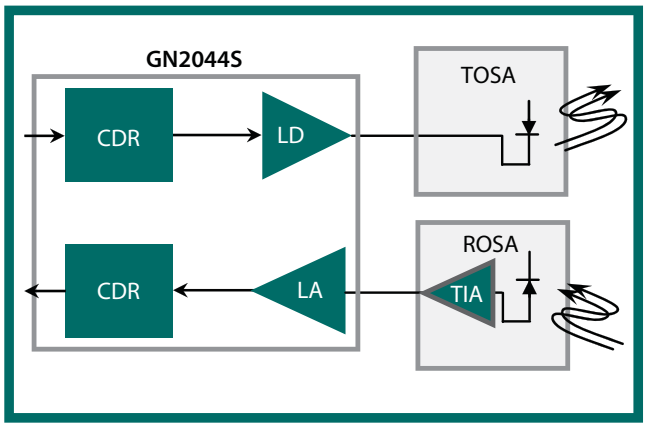


Figure B: Typical Usage - XFP or SFP+ 1310nm to 1550nm Optical Module

Revision History

Version	ECO	Date	Changes and / or Modifications
3	025194	April 2015	Updated Data Rate parameter in Table 2-5: AC Electrical Characteristics.
2	024600	March 2015	Updates.
1	022990	November 2014	Correction to Table 2-2: DC Electrical Characteristics and Table 2-5: AC Electrical Characteristics.
0	018595	November 2014	New document.

Contents

1. Pin Out

1.1 Pin Assignment

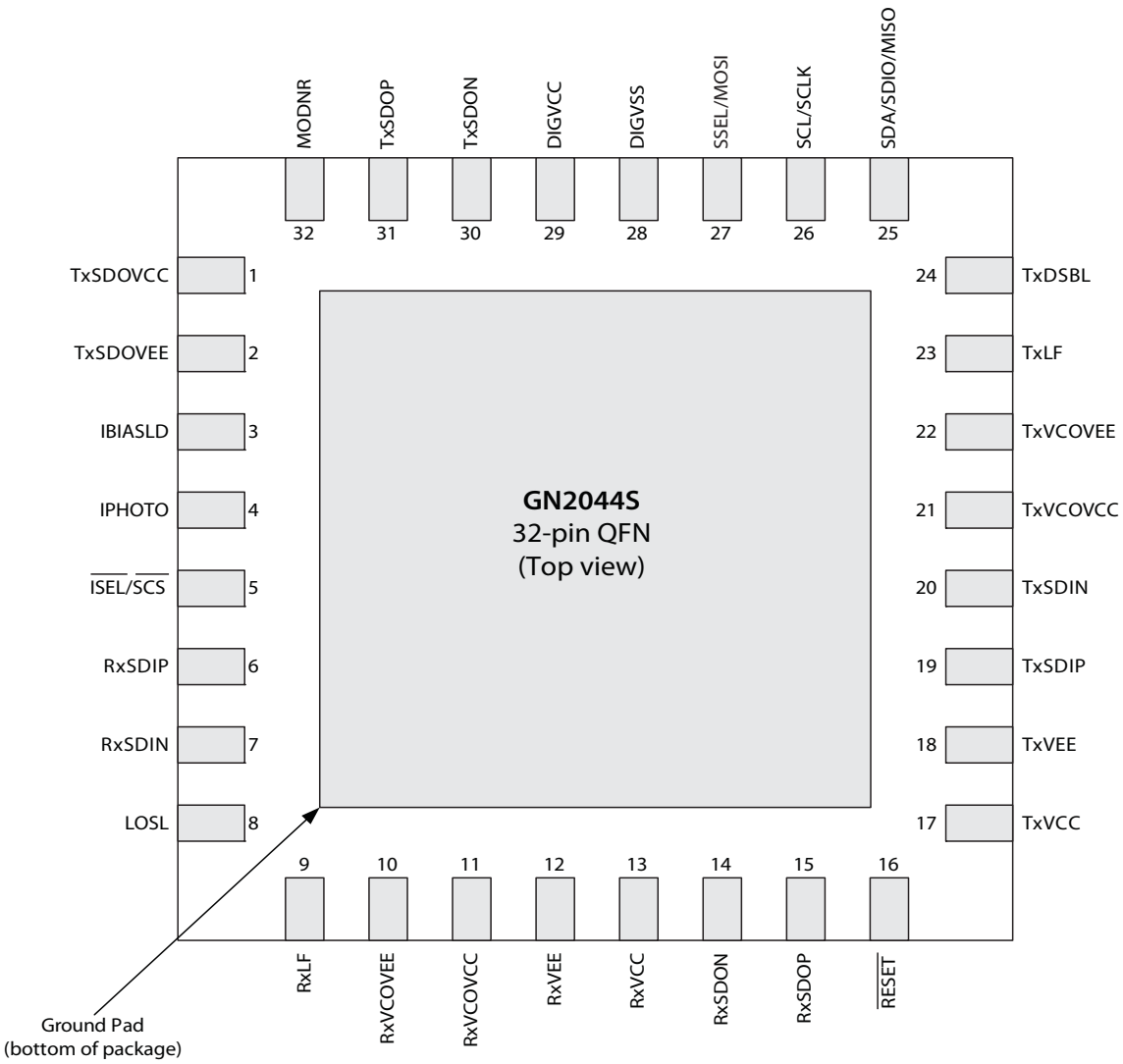


Figure 1-1: Pin Assignment

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin #	Name	Type	Description
1	TxSDOVCC	Power	3.3V power supply for the transmit signal path output.
2	TxSDOVEE	Ground	Ground for the transmit signal path output.
3	IBIASLD	Analog Output	Current sink/source output for external laser DC bias.
4	IPHOTO	Analog Input	Photodiode Monitor Current input. Photodiode current is sensed at the IPHOTO pin. IPHOTO can be configured to sink or source photodiode current, when the photodiode is referenced from a positive supply.
5	$\overline{\text{ISEL}}$/$\overline{\text{SCS}}$	Digital Input	Digital active-low LVTTL/LVCMOS-compliant input. $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ selects the host interface mode during a device reset. When LOW or left unconnected, this pin selects I^2C host interface mode. When HIGH, this pin selects SPI host interface mode on device power-on or reset. $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ is an SPI-compliant active-low chip-select pin in SPI host interface mode. $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ is not used in I^2C host interface mode.
6, 7	RxSDIP, RxSDIN	Input	High-speed input for the receive signal path.
8	LOSL	Digital Output	XFP/SFP+ compliant, active-high. Open-collector Loss-Of-Signal indicator requires an external pull-up resistor. When LOSL is LOW, the transmit and receive signal paths are operating properly. When LOSL is high-impedance, the device has detected a condition that indicates invalid data in the transmit and/or receive signal paths. It consists of a logical OR of the following signals: • Receive signal path CDR Loss of Signal (included by default) • Receive signal path CDR Loss of Lock (masked by default) • Transmit signal path CDR Loss of Signal (masked by default) • Transmit signal path CDR Loss of Lock (masked by default) Loss-of-signal/loss-of-lock inputs from either signal path can be masked or enabled.
9	RxLF	Passive	Loop filter capacitor connection for the receive signal path.
10	RxVCOVEE	Ground	Ground for the receive signal path VCO.
11	RxVCOVCC	Passive	1.8V power supply for the receive signal path VCO.
12	RxVEE	Ground	Ground for the receive signal path and output.
13	RxVCC	Power	1.8V power supply for the receive signal path and output.
14, 15	RxSDON, RxSDOP	Output	High-speed differential output for the receive signal path.
16	$\overline{\text{RESET}}$	Digital Input	Digital active-low 1.8V CMOS-compliant input. Device reset control pin. This is an active pull-down. It is recommended that $\overline{\text{RESET}}$ be pulled down by an external 10kΩ resistor and be driven by the Micro on the module.
17	TxVCC	Power	1.8V power supply for the transmit signal path.
18	TxVEE	Ground	Ground for the transmit signal path.
19, 20	TxSDIP, TxSDIN	Input	High-speed input for the transmit signal path.

Table 1-1: Pin Descriptions (Continued)

Pin #	Name	Type	Description
21	TxVCOVCC	Passive	1.8V power supply for the transmit signal path VCO.
22	TxVCOVEE	Ground	Ground for the transmit signal path VCO.
23	TxLF	Passive	Loop filter capacitor connection for the transmit signal path.
24	TxDSBL	Digital Input	Digital active-high XFP and SFP+ compliant input. When left unconnected or held HIGH, this pin disables the transmit signal path high-speed differential output and the laser DC bias current. When held LOW, the transmit signal path and laser DC bias outputs behave normally. Includes a weak internal pull-up current to disable the laser DC bias current, should this pin be externally disconnected.
25	SDA/SDIO/MISO	Digital Input/ Output	Digital active-high serial data signal for the host interface. Schmitt triggered in input mode. Bi-directional, I^2C-compliant, open-drain driver/receiver in I^2C host-interface mode. Bi-directional, 1.8V CMOS-compliant driver/receiver in 3-wire SPI host-interface mode. 1.8V CMOS-compliant active-high output driver in 4-wire SPI host-interface mode.
26	SCL/SCLK	Digital Input	Digital active-high clock input signal for the serial host interface. Schmitt triggered in input mode. Bi-directional, I^2C-compliant, open-drain driver/receiver in I^2C host-interface mode (SCL). 1.8V CMOS-compliant input in either SPI host-interface mode (SCLK).
27	SSEL/MOSI	Digital Input	Digital active-high 1.8V CMOS-compliant input. SSEL selects the SPI port style when SPI host interface mode is selected: When LOW or left unconnected during device reset, this pin selects 3-wire SPI host interface mode. When HIGH during device reset, this pin selects 4-wire SPI host interface mode on device power on or reset. Following device reset, SSEL/MOSI is an active-high SPI-compliant receiver. SSEL/MOSI is not used in I^2C host interface mode.
28	DIGVSS	Ground	Ground for the low-speed digital I/O and internal logic.
29	DIGVCC	Power	1.8V power supply for the low-speed digital I/O.
30, 31	TxSDON, TxSDOP	Output	High-speed differential output for the transmit signal path. Use TxSDOP to drive the EML TOSA.
32	MODNR	Digital Output	XFP/SFP+-compliant active-high digital output. Open-collector Module-Not-Ready indicator. Requires an external pull-up resistor. When MODNR is LOW, the transmit and receive signal paths are operating properly. When MODNR is high-impedance, the device has detected a condition that indicates invalid data in the transmit and/or receive signal paths. It consists of a logical OR of the following signals: • Transmit signal path CDR Loss of Lock • Transmit signal path CDR Loss of Signal • Transmitter Laser Fault • Receive signal path CDR Loss of Lock • Receive signal path CDR Loss of Signal

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
3.3V Supply Voltage	-0.5 to +3.6V_{DC}
1.8V Supply Voltage	-0.5 to +2.1V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_A < +125°C
Input Voltage Range (any input pin)	-0.3 to ($V_{CC\_3.3}$ + 0.3)V_{DC}
Solder Reflow Temperature	260°C

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = 1.6V to 1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31 data. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Power	Bias/Mod Voltage = 0mA/0V_{ppse} Jitter filter mode off		—	279	330	mW	
	Bias/Mod Voltage = 80mA/1.875V_{ppse} Jitter filter mode off		—	790	840	mW	1
	Bias/Mod Voltage = 90mA/2.5V_{ppse} Jitter filter mode off		—	906	963	mW	
Control Logic Input Specifications							
Input Low Voltage		V_{IL}	0	—	0.8	V	—
Input High Voltage		V_{IH}	2.0	—	V_{CC}	V	—
Input Low Current	V_{IL} = 0V	I_{IL}	—	-100	—	µA	—
Input High Current	V_{IH} = 3.3V, V_{CC} = 3.3V	I_{IH}	—	100	—	µA	—

Table 2-2: DC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = 1.6V to 1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31 data. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Schmitt Trigger Thresholds							
DC Low-to-High Threshold	V_{CC} = 1.9V		0.93	1.05	1.16	V	2
DC High-to-Low Threshold			0.51	0.70	0.85	V	2
DC Low-to-High Threshold	V_{CC} = 1.8V		0.88	0.99	1.13	V	3
DC High-to-Low Threshold			0.41	0.67	0.77	V	3
DC Low-to-High Threshold	V_{CC} = 1.7V		0.83	0.94	1.07	V	—
DC High-to-Low Threshold			0.36	0.59	0.73	V	—
AC Low-to-High Threshold	$V_{CC\_1.8}$ = 1.7V or $V_{CC\_3.3}$ = 3.13V		0.76	0.91	1.06	V	—
AC High-to-Low Threshold			0.44	0.57	0.69	V	—
AC Low-to-High Threshold	$V_{CC\_1.8}$ = 1.9V or $V_{CC\_3.3}$ = 3.46V		0.93	1.06	1.19	V	—
AC High-to-Low Threshold			0.70	0.82	0.93	V	—
Status Indicator Output Specifications							
Indicator Output Logic LOW	I_{SINK}(max) = 3mA	V_{OL}	—	0.2	0.4	V	—
Rx Side Specification							
Input Termination (RxSDIP/N)	Differential		80	100	120	Ω	—
Output Termination (RxSDOP/N)	Differential		80	100	120	Ω	—
Tx Side Specification							
Input Termination (TxSDIP/N)	Differential		80	100	120	Ω	—
Output Termination (TxSDOP/N)	Single-ended		—	50	—	Ω	—
Maximum Laser Modulation Voltage	AC-coupled, single-ended load, $V_{CC} \geq 3.13V$		2.5	3	—	V_{pp}	—
	AC-coupled, single-ended load, $V_{CC} \geq 2.8V$		2	2.5	—	V_{pp}	—
	AC-coupled, single-ended load, $V_{CC} \geq 2.6$		1.5	2	—	V_{pp}	—

Table 2-2: DC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = 1.6V to 1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31 data. Note: mA_{pp} refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Maximum Laser Bias Current			120	—	—	mA	—
IPHOTO Range	Minimum setting		—	0.025	—	mA	4
	Maximum setting		—	2	—	mA	
TxDSBL, Input HIGH		V_{IH}	1.2	—	V_{CC} + 0.3	V	—
TxDSBL, Input LOW		V_{IL}	-0.3	—	0.7	V	—

Notes:

1. Each output terminated and power includes dissipation of external 50Ω resistor on non-TOSA side. Typical power is specified at VCC_1.8 = 1.7V and VCC_3.3 = 3.3V. Maximum power is specified at VCC_1.8 = 1.8V and VCC_3.3 = 3.3V.
2. Typical Noise Immunity = 0.34V.
3. Typical Noise Immunity = 0.43V.
4. Can be configured to sink or source photodiode current at the IPHOTO pin when the photodiode is referenced from a positive supply.

2.2.1 Power Dissipation

Table 2-3: Power Dissipation

$V_{CC\_1.8}$	$V_{CC\_3.3}$	Modulation Swing	Bias Current	$V_{CC\_1.8}$ Current	$V_{CC\_3.3}$ Current	Total Current	Total Power
V	V	V_{pp}	mA	mA	mA	mA	mW
1.6	2.6	1.5	0	159	60	219	410
1.7	2.6	1.5	0	164	60	224	435
1.8	2.6	1.5	0	170	60	230	462
1.6	2.6	1.875	0	159	75	234	449
1.7	2.6	1.875	0	164	75	239	474
1.8	2.6	1.875	0	170	75	245	501
1.6	2.6	1.875	80	159	155	314	657
1.7	2.6	1.875	80	164	155	319	682
1.8	2.6	1.875	80	170	155	325	709
1.6	2.8	0	0	159	0	159	255
1.6	2.8	1.875	80	159	155	314	689
1.6	2.8	2.5	90	159	190	349	787
1.7	3.3	0	0	164	0	164	279

Table 2-3: Power Dissipation (Continued)

$V_{CC\_1.8}$	$V_{CC\_3.3}$	Modulation Swing	Bias Current	$V_{CC\_1.8}$ Current	$V_{CC\_3.3}$ Current	Total Current	Total Power
1.7	3.3	1.875	80	164	155	319	790
1.7	3.3	2.5	90	164	190	354	906
1.8	3.3	0	0	170	0	170	306
1.8	3.3	1.875	80	170	155	325	818
1.8	3.3	2.5	90	170	190	360	933

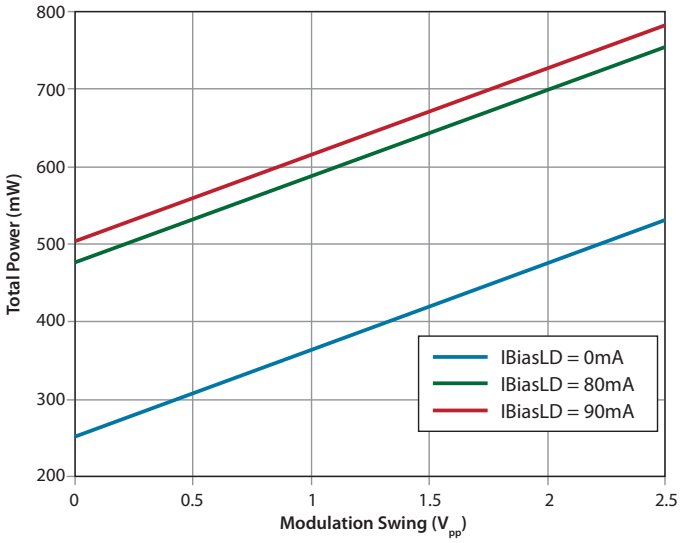


Figure 2-1: Typical Total Power vs. Modulation and Bias Current for 1.6V/2.8V Setting

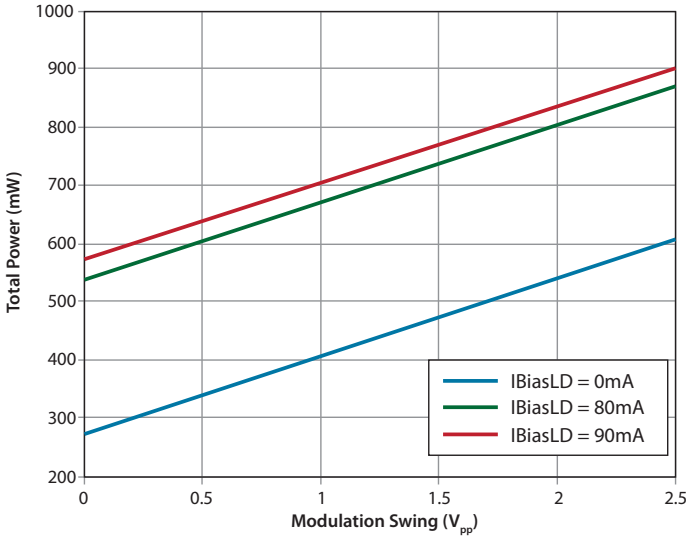


Figure 2-2: Typical Total Power vs. Modulation and Bias Current for 1.7V/3.3V Setting

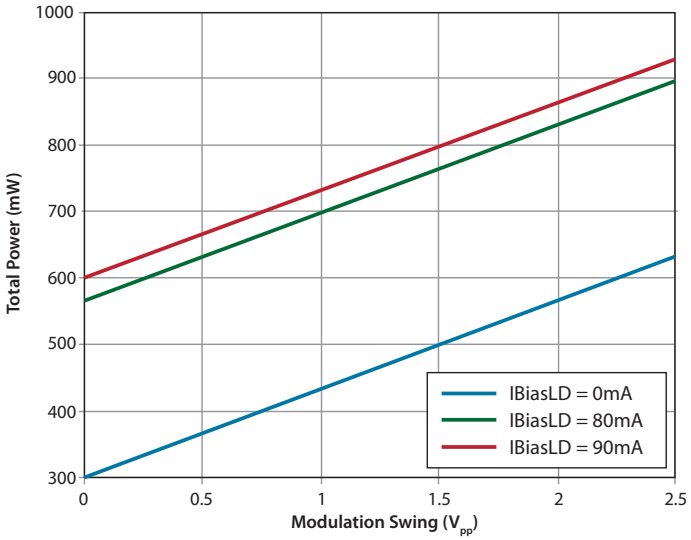


Figure 2-3: Typical Total Power vs. Modulation and Bias Current for 1.8V/3.3V Setting

2.2.2 Power Features

Table 2-4: Power Features

Feature	Description	Typical Baseline Power (mW)	Typical Delta Power (mW)
Base Power	**V_{mod} = 2.5V_{ppse}, Bias = 90mA**	**906**	
Incremental Power Features			
LA Boost at Maximum			0
Slice Adjust at Maximum			12.3
PRBS7 Generator	Path for PRBS7 Generator to RxSDO is on		40
PRBS7 Checker	PRBS7 Checker is on		56
Diag + ADC	Temperature, Supply Sensor, ADC		7.6
LD CPA at Maximum	Laser Driver Crossing Point Adjust is at maximum		10.3
LD Jitter Optimization with Phase Adjust at Maximum	Jitter optimization through phase adjust is enabled for laser driver		18.8
LD Rise Pre-emphasis at Maximum Setting			27.4
Tx Jitter Filter Mode Enabled	Tx jitter filter tracking capability set to maximum		9.5
Rx Swing at Maximum			122.7
Power Saving Features			
with Rx CDR Bypassed and Powered-down			-64.1
with Rx and Tx CDR Bypassed and Powered-down			-124.7
with Rx Path Powered-down			-103.6
RxSDO Muted			-25.1
TxSDO Muted			-344.4
Rx IJT Mode 1			-18.5
Rx IJT Mode 2			-15

2.3 AC Electrical Characteristics

Table 2-5: AC Electrical Characteristics

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Data Rate	Default configuration, $V_{CC\_1.8V} \geq 1.71V$		9.8	10.3125	11.35	Gb/s	—
	Default configuration, $V_{CC\_1.8V} < 1.71V$		9.8	10.3125	11.3	Gb/s	—
Rx Side Specification							
Input Sensitivity			—	2.5	10	mV_{ppd}	—
Input Overload			1200	—	—	mV_{ppd}	—
Limiting Amplifier Equalization	Max EQ setting		14	—	—	dB	1
Input Sinusoidal Jitter Tolerance	f = 100kHz		20	30	—	UI_{pp}	2, 3
	f = 400kHz		2.5	8	—	UI_{pp}	3
	f = 4MHz		0.5	1.4	—	UI_{pp}	3
	f = 80MHz		0.3	0.5	—	UI_{pp}	3
Jitter Transfer Bandwidth Setting Range	Minimum programmable setting		—	2.6	—	MHz	—
	Maximum programmable setting		—	13	—	MHz	—
Jitter Peaking	With 6MHz LBW, loop filter capacitor = 220nF		—	—	0.03	dB	—
RxSDO Output Total Jitter	PRBS31 data, BER = 10^{-12}, 11.3Gb/s with optimized boost and swing settings	TJ	—	0.08	0.16	UI_{pp}	—
RxSDO Output Deterministic Jitter	PRBS31 data, BER = 10^{-12}, 11.3Gb/s with optimized boost and swing settings	DJ	—	0.05	0.088	UI_{pp}	—
RxSDO Output Rise/Fall Time	20% to 80%	t_r, t_f	—	—	24	ps	4

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
RxLOS De-assert Threshold Level Setting Range	Minimum programmable setting		—	5	—	mV_{ppd}	—
	Maximum programmable setting		—	400	—	mV_{ppd}	—
RxLOS Threshold Level Variation	1 sigma IC to IC, RXLOSRANGE = 0,1		—	1.0	—	dB	—
	1 sigma IC to IC, RXLOSRANGE = 2		—	2.0	—	dB	—
	Over V_{CC} range		—	1.0	—	dB	—
	Over temperature range -40°C to +95°C, threshold level > $20mV_{ppd}$		—	1.5	—	dB	—
RxLOS Threshold Level Hysteresis Setting Range	Electrical		0	—	6	dB	—
RxLOS Response Time			3	5	20	µs	—
Slice Level Adjust Range	Maximum setting		200	—	—	mV	—
Rx CDR Lock Time	Default mode: loop filter cap = 220nF, minimum LBW		—	—	1	ms	—
Differential Output Voltage Setting Range	Minimum swing setting		90	120	130	mV_{ppd}	—
	Maximum swing setting		730	800	910	mV_{ppd}	—
Output De-emphasis Setting Range	Maximum pre-emphasis setting. Output swing = $350mV_{ppd}$		6	—	—	dB	—
RxSDI Differential Return Loss	<5GHz		—	-14	—	dB	—
	5GHz to 10GHz		—	-10	—	dB	—
RxSDO Differential Return Loss	<5GHz		—	-16	—	dB	—
	5GHz to 10GHz		—	-8	—	dB	—

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Tx Side Specification							
Input Sensitivity			—	15	30	mV_{ppd}	—
Input Overload			1200	—	—	mV_{ppd}	—
LOS Threshold Level Setting Range	Minimum programmable setting		—	20	—	mV_{ppd}	—
	Maximum programmable setting		—	100	—	mV_{ppd}	—
Equalization Gain	Maximum programmable setting		—	6	—	dB	5
Input Sinusoidal Jitter Tolerance – jitter filter mode off	f = 120kHz, maximum LBW		7	10	—	UI_{pp}	6, 7
	f = 4MHz		0.4	0.6	—	UI_{pp}	7
	f = 80MHz		0.35	0.5	—	UI_{pp}	7
Input Sinusoidal Jitter Tolerance – jitter filter mode on	f = 120kHz, maximum LBW		10	16	—	UI_{pp}	6, 7
	f = 4MHz		0.4	0.6	—	UI_{pp}	7
	f = 80MHz		0.35	0.5	—	UI_{pp}	7
Jitter Transfer Bandwidth Setting Range	Minimum programmable setting		—	1.5	—	MHz	—
	Maximum programmable setting		—	10.3	—	MHz	—
Jitter Peaking	With 6MHz LBW, loop filter capacitor = 220nF		—	—	0.03	dB	—
Jitter Generation	50kHz to 80MHz		—	34	—	mUI_{pp}	9
	4MHz to 80MHz		—	22	—	mUI_{pp}	9

Table 2-5: AC Electrical Characteristics (Continued)

$V_{CC\_3.3}$ = +2.6V to +3.47V, $V_{CC\_1.8}$ = +1.6V to +1.89V, T_C = -40°C to +100°C. Typical values are $V_{CC\_3.3}$ = +3.3V, $V_{CC\_1.8}$ = +1.8V and T_A = 25°C, unless otherwise specified. Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical data rate = 10.3Gb/s. Typical data pattern = PRBS 31. BER 1e-12.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Total Output Jitter	TXSDOIMOD = $1.9V_{pp}$, PRBS31 data, BER = 10^{-12}, 11.3G, with optimized phase adjust; measured on TxSDOP		—	0.1	0.18	UI_{pp}	—
Tx CDR Lock Time			—	—	1	ms	8
TxSDO Output Rise/Fall Time	20% to 80%	t_r, t_f	—	26	35	ps	—
TxSDI Differential Return Loss	<5GHz		—	-15	—	dB	—
	5GHz to 10GHz		—	-13	—	dB	—
TxSDO Differential Return Loss	<5GHz		—	-16	—	dB	—
	5GHz to 10GHz		—	-8	—	dB	—
Output Crossing Point Adjust Setting Range	Minimum setting		—	20	—	%	—
	Maximum setting		—	80	—	%	—
Maximum Phase Adjust for Jitter Optimization			—	30	—	ps	—
Tx Output Pre-emphasis Amplitude	Tx Mod Voltage = $1.9V_{ppse}$		0	500	—	mV_{ppse}	9

Notes:

1. At 5.35GHz.
2. At jitter frequencies <100kHz, the GN2044S jitter tolerance performance exceeds the SONET GR-253 RX Tolerance specifications.
3. With default loop bandwidth setting, IJT Mode 3 and IJT setting 31.
4. Measured at host-side of XFP or SFP+ connector.
5. At 5.35GHz (dielectric loss).
6. At jitter frequencies <120kHz, the GN2044S jitter tolerance performance exceeds the XFI module transmitter input telecom sinusoidal jitter tolerance specifications (XFP MSA Revision 4.0, Figure 16).
7. In addition to XFI input jitter tolerance requirements.
8. No signal-to-signal (PRBS31 pattern).
9. Measured on TxSDOP channel with optimized phase adjust.

3. Input/Output Circuits

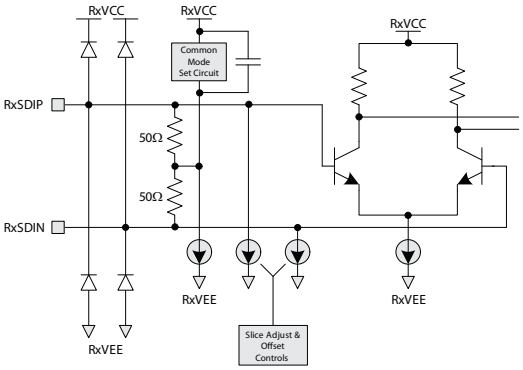


Figure 3-1: RxSDI

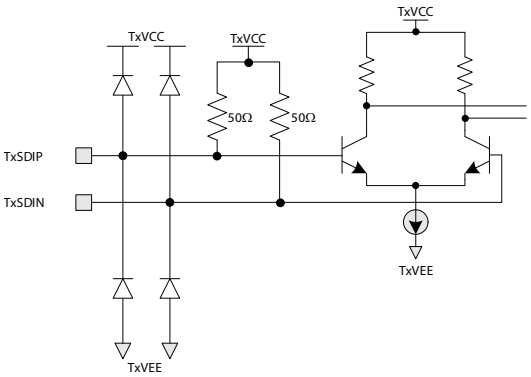


Figure 3-2: TxSDI

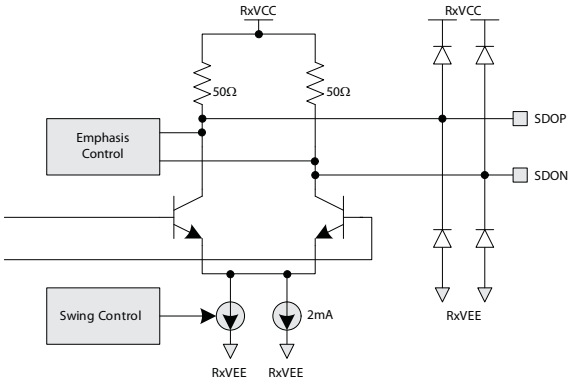


Figure 3-3: RxSDO

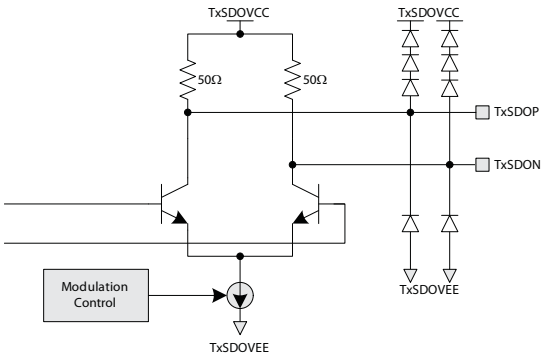


Figure 3-4: TxSDO

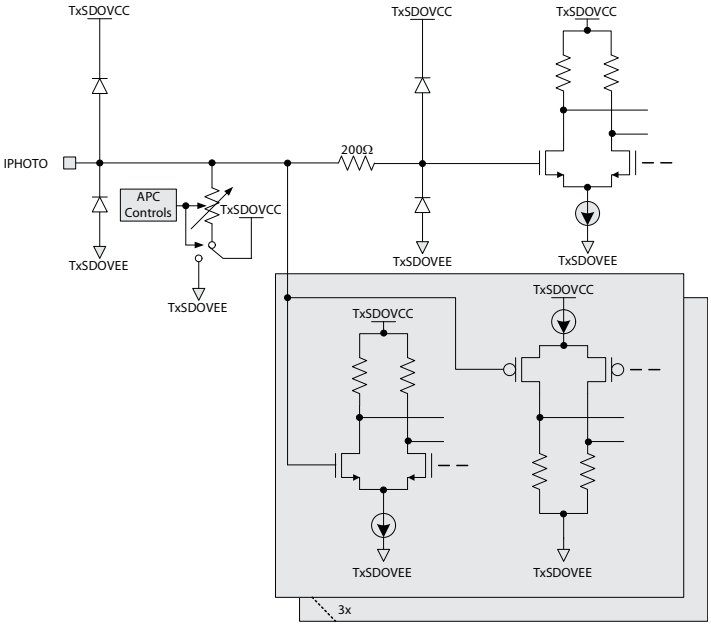


Figure 3-5: IPHOTO

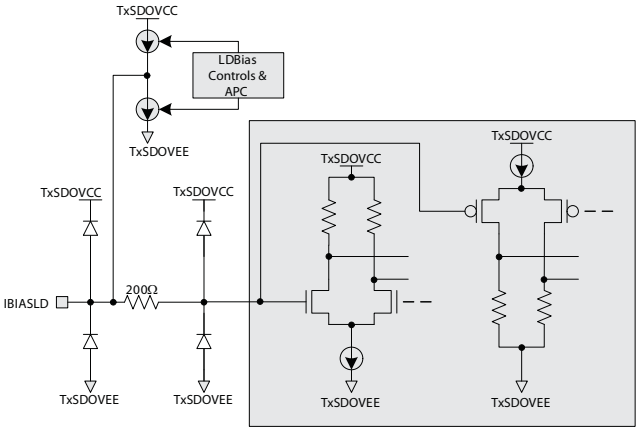
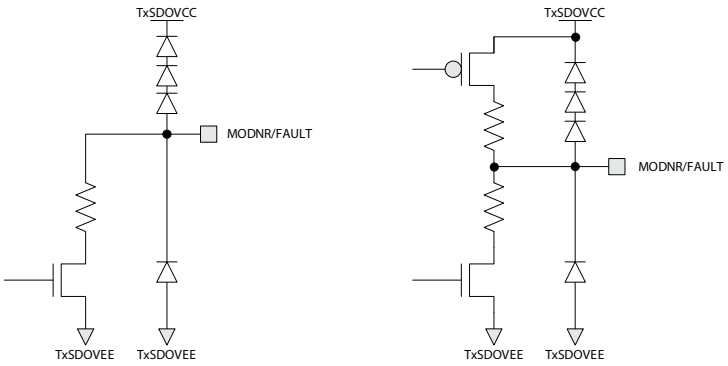


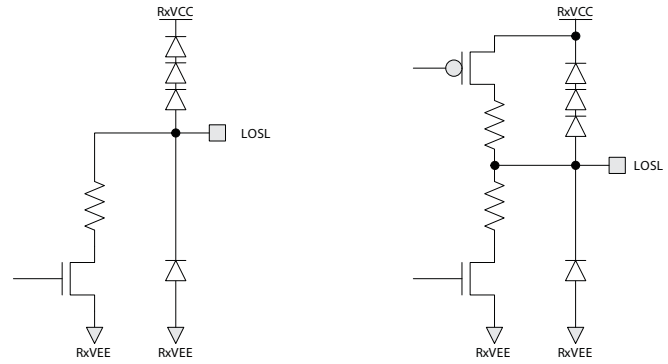
Figure 3-6: IBIASLD



Configured as open-drain

Configured as LVCMOS

Figure 3-7: MODNR/FAULT



Configured as open-drain

Configured as LVCMOS

Figure 3-8: LOSL

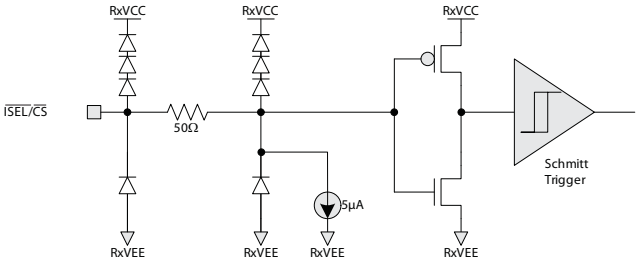


Figure 3-9: $\overline{\text{ISEL}}/\overline{\text{SCS}}$

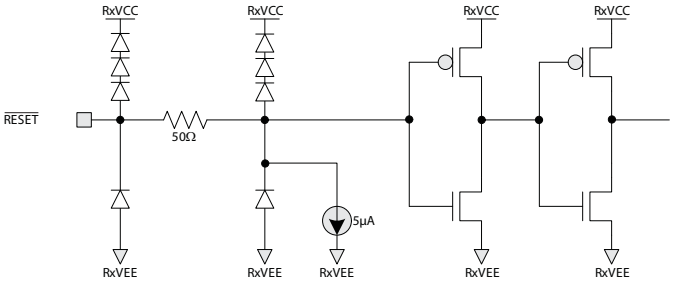


Figure 3-10: $\overline{\text{RESET}}$

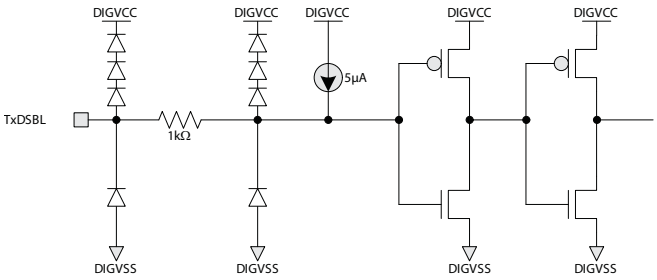


Figure 3-11: TxDSBL

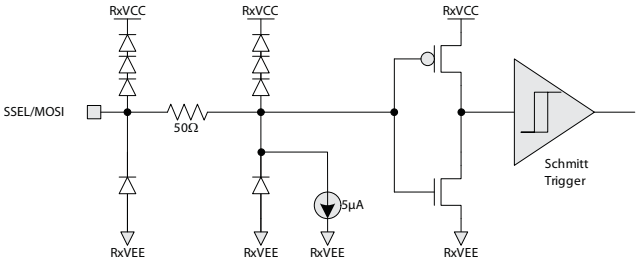


Figure 3-12: SSEL/MOSI

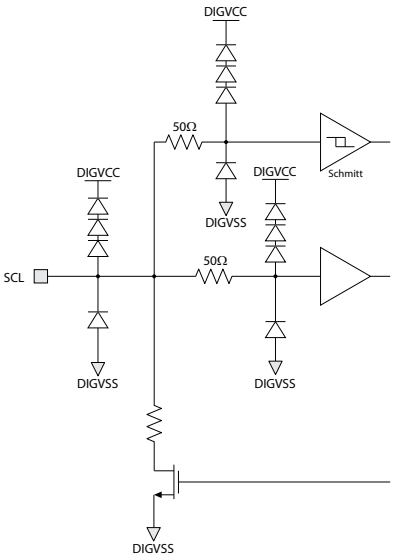


Figure 3-13: SCL

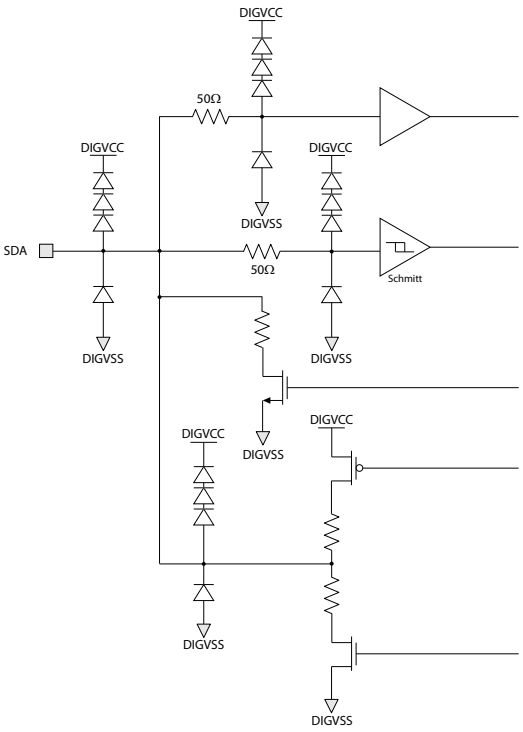


Figure 3-14: SDA

4. Detailed Description

4.1 Multirate CDR Functionality

The GN2044S supports a range of data rates, so that a single part can be used for multiple applications. The GN2044S does not require a reference clock. Some example applications are as follows:

- 10Gb/s Ethernet (10.3Gb/s)
- 10Gb/s Ethernet with FEC (11.1Gb/s)
- 10G Fibre Channel (10.5Gb/s)
- 10G Fibre Channel with FEC (11.3Gb/s)
- SONET OC192 (9.95Gb/s)
- 9.8Gb/s CPRI

4.1.1 Retimer Bypass

The device can be configured to manually bypass each of the Rx and Tx CDRs through the **TX_PLL_BYPASS** and **RX_PLL_BYPASS** controls.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG5	14	TX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Tx CDR into bypass mode.
RXPLL_REG5	24	RX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Rx CDR into bypass mode.

4.2 Receive Path

The GN2044S receive path contains a high-sensitivity limiting amplifier with optional equalization, a multi-rate CDR, and an emphasis driver.

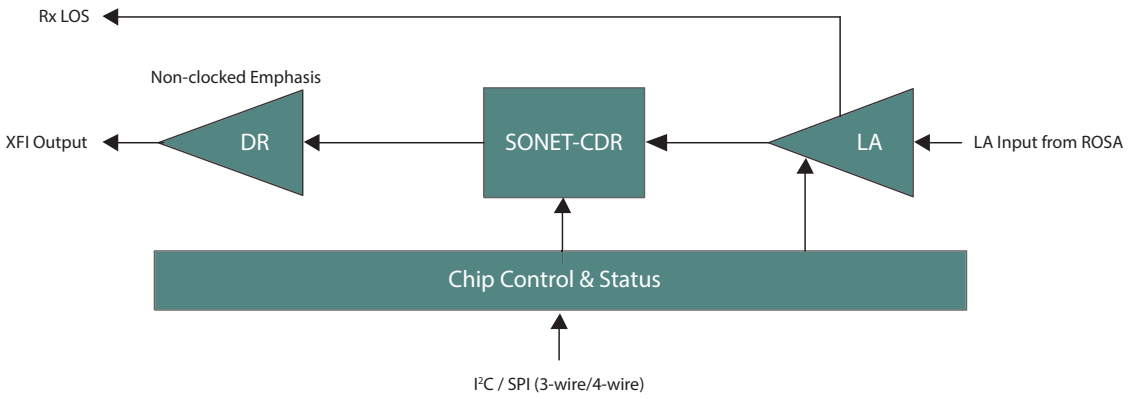


Figure 4-1: Receive Path

4.2.1 Integrated Limiting Amplifier

The GN2044S has an integrated Limiting Amplifier (LA), with better than 10mV sensitivity. Additional features are; slice level adjust and optional equalization on the limiting amplifier input.

4.2.2 Slice Level Adjust

The slicing level of the limiting amplifier can be configured in two modes of operation:

1. Automatic offset correction.
2. Manual slice adjust with a fixed slice level.

By default, the limiting amplifier is configured in automatic offset correction mode, and will slice the incoming signal at the 50% point.

The LA can be configured to allow a user-specified fixed slice level. In this mode, the slice level can be varied by ±200mV from the 50% point in 1mV increments. To enable this mode, **RX_PD_SLICE_ADJ** (shown below) should be set to 0.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPWRDN_REG2	135	RX_PD_SLICE_ADJ	1:1	RW	1	0-1	When HIGH, power-down for LA slice adjust.

To enable the user to adjust the slice level manually, **RX_PD_SLICE_ADJ** must be set to 0 and **RX_MANUAL_SLICE_ADJ_EN** must be set to 1.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG5	52	RXLA_MANUAL_SLICE_ADJ_EN	0:0	RW	0	0-1	When HIGH, enables user to adjust slice level at the Rx input.

The following controls allow the slice adjust polarity and magnitude to be set manually:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG2	49	RXLA_SLICE_ADJ	7:0	RW	00000000	0-255	Slice adjust magnitude control.
RX_REG3	50	RXLA_SLICE_ADJ_POL	0:0	RW	0	0-1	Slice adjust polarity. When HIGH, slice level adjust is positive.

The slice level adjustment can be applied before or after the equalization function (covered in Section 4.2.3). This flexibility allows the device to maintain optimal receive sensitivity performance while optimizing slice adjust. Figure 4-2 shows the two possible insertion points for slice level adjustment:

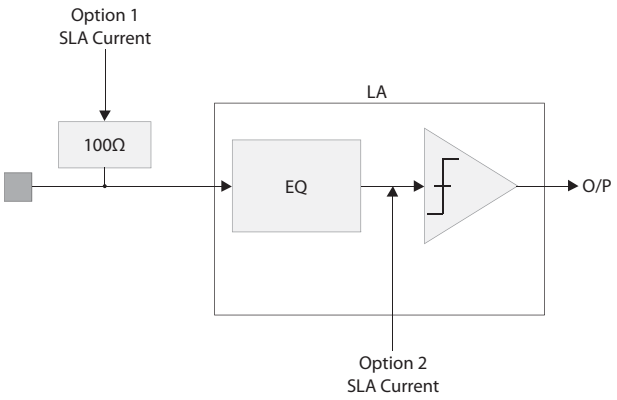


Figure 4-2: Slice Level Adjustment Insertion Points

RXLA_SLICE_ADJ_LO_RANGE should be set to 1 to apply the slice adjust after the equalization function.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG3	50	RXLA_SLICE_ADJ_LO_RANGE	1:1	RW	0	0-1	Selects slice level adjust point. When LOW, slicing point is option 1. When HIGH, slicing point is option 2.

4.2.3 Receive Equalization

The receive input implements an equalizer that provides peaking at 5.35GHz. This feature allows for optimal performance with extended reach connections, and allows for optimization of parameters such as dispersion penalty.

The equalizer implements 0dB to 14dB of high-frequency boost in fifteen steps, while achieving optimal receive sensitivity at any given equalization setting. The equalization setting is set through the **RXLA_BOOST_MSB** control. Additionally, the **RXLA_BOOST_LSB** control provides another 8 steps of fine tune control of the equalization gain at each **RXLA_BOOST_MSB** setting.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG1	48	RXLA_BOOST_MSB	3:0	RW	0000	0-15	RXLA boost control bit MSBs: 0 = 0dB to 15 = 14dB
RX_REG16	63	RXLA_BOOST_LSB	2:0	RW	000	0-7	RXLA boost control bit LSBs for fine tuning gain with smaller step size.

When the equalization setting is 0dB, the equalization function is bypassed and the receive sensitivity performance is the same as that of a limiting amplifier.

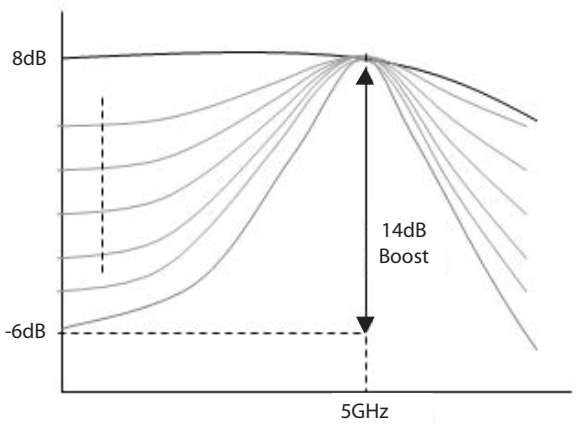


Figure 4-3: Receive Equalization

4.2.4 Rx PLL Variable Loop Bandwidth

The loop bandwidth of the receive Phase Locked Loops (PLL) can be varied through the digital control interface. The loop bandwidths (LBW) are individually controlled, and can cover a range of 2.6MHz to 13MHz through the following 5-bit registers:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
RXPLL_REG1	20	RX_PLL_LBW_POS_ADJ	4:0	RW	11101	0-31	Adjusts LBW positive temperature coefficient control.
RXPLL_REG2	21	RX_PLL_LBW_NEG_ADJ	4:0	RW	00111	0-31	Adjusts LBW negative temperature coefficient control.

The temperature coefficient of the loop bandwidth can be adjusted by a weighted summation of **RX_PLL_LBW_POS_ADJ**, which has a positive temperature coefficient, and **RX_PLL_LBW_NEG_ADJ**, which has a negative temperature coefficient.

Table 4-1 shows the recommended settings for a flat loop bandwidth temperature coefficient:

Table 4-1: Rx Loop Bandwidth

RX_PLL_LBW_POS_ADJ	RX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
2	0	2	2.047
4	3	7	3.280
7	5	12	4.513
10	7	17	5.700
13	9	22	6.700
15	11	26	7.500
18	13	31	8.500
21	15	36	9.500
24	17	41	10.250
27	19	46	11.000

Table 4-1: Rx Loop Bandwidth (Continued)

RX_PLL_LBW_POS_ADJ	RX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
29	20	49	11.375
31	22	53	11.875
31	31	62	13.000

4.2.5 Rx CDR Input Jitter Tolerance

The input jitter tolerance of the Rx CDR is configurable to allow power optimization for required performance. Three modes of operation are supported as follows:

- **Mode 1:** Recommended for power-optimized applications. This mode supports the lowest power, but it is not guaranteed to meet the SONET IJT mask
- **Mode 2:** Recommended for most applications, including SONET, Ethernet and Fibre Channel. In this mode, the device is guaranteed to meet the SONET IJT mask.
- **Mode 3:** Recommended for SONET applications that require large margins on SONET IJT mask. This mode consumes extra power.

The RxCDR IJT mode is configured through the following registers. By default, the device is configured in Mode 3.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG9	28	RX_PLL_SELECT_HIGH_IJT	3:3	RW	1	0-1	When HIGH, selects high-margin Sonet IJT mode in conjunction with the RX_PLL_SONET_IJT_SETTING.
RXPLL_REG8	27	RX_PLL_SONET_IJT_SETTING	7:3	RW	00010	0-31	Control for Sonet IJT performance. Used in conjunction with Sonet IJT modes 2 and 3 to set IJT performance. Gradually increase setting for increased margins.
RXPWRDN_REG4	137	RX_PD_SONET_IJT	0:0	RW	0	0-1	When HIGH, powers-down the Rx path Sonet IJT feature to save power.

Table 4-2 shows the recommended settings for above registers for the three IJT modes:

Table 4-2: IJT Mode Settings

IJT Mode	RX_PD_SONET_IJT	RX_PLL_SELECT_HIGH_IJT	RX_PLL_SONET_IJT_SETTING[4:0]
1	1	x	x
2	0	0	2 (or higher, based on user preference)
3	0	1	3 (or higher, based on user preference)

Figure 4-4 shows that Mode 2 and Mode 3 SIJT performance is comparable with maximum LBW settings, with >3UI margin at 400kHz:

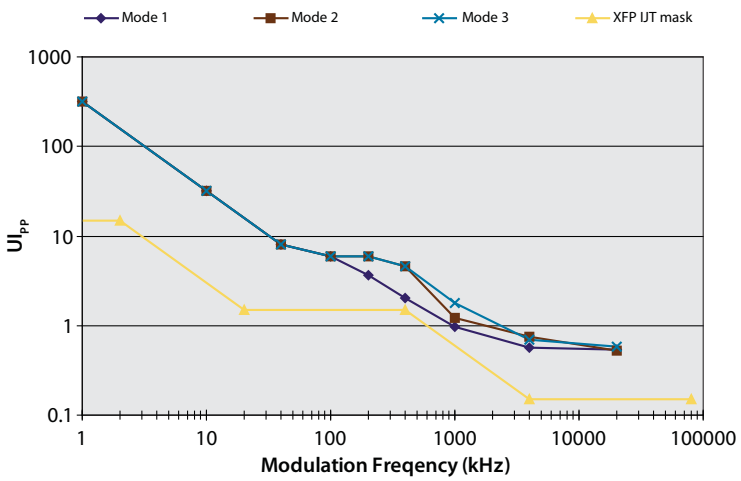


Figure 4-4: S-IJT Mode 1, 2 & 3 (Loop Bandwidth = 6.2MHz)

With higher LBW settings, Mode 2 can be used to meet and exceed S-IJT mask with lower power than Mode 3. Note that in either Mode 2 or Mode 3, the **RX_PLL_SONET_IJT_SETTING** can be adjusted beyond the values provided in Table 4-2 to further optimize SIJT performance margins.

4.2.6 Emphasis Driver with Auto-Mute

The receive path driver is a non-clocked emphasis driver that can be used to compensate for losses in the connector and trace between the module and ASIC. The emphasis operates regardless of the status or state of the Rx CDR. The output swing can be set from 100mV to 800mV in steps of 50mV through the **RX_SDO_SWING[3:0]** register. The emphasis amplitude can be varied from 1dB to 6dB in 16 steps through **RX_SDO_EMPHASIS[3:0]**.

Note: The Rx emphasis in disabled by default. To enable the emphasis, set **RX_PD_RXSDO_EMPHASIS** to 0 to power-on the Rx emphasis block. When emphasis is enabled, the output driver is still limited to approximately 800mV$_{ppd}$ output. Therefore, at some swings settings (i.e. >400mV$_{ppd}$), the full 6dB emphasis may not be realized. See Figure 4-5 for more information.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXSDO_REG1	75	RX_SDO_SWING	3:0	RW	0110	0-15	Driver swing: 100mV$_{ppd}$ to 850mV$_{ppd}$. Default = 6 = 400mV$_{ppd}$.
RXSDO_REG2	76	RX_SDO_EMPHASIS	3:0	RW	0000	0-15	Driver emphasis control.
RXPWRDN_REG1	134	RX_PD_RXSDO_EMPHASIS	3:3	RW	1	0-1	When HIGH, power-down for the trace driver emphasis.

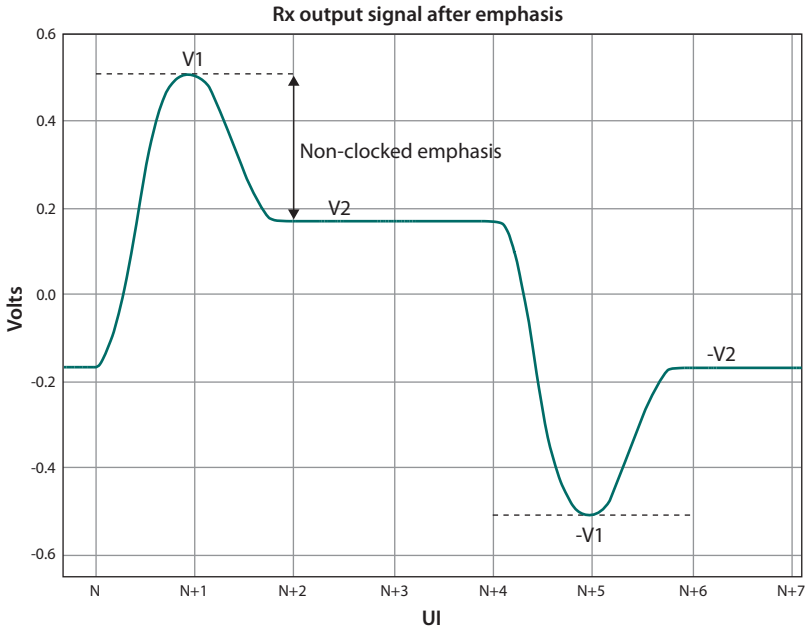


Figure 4-5: Emphasis Waveform Description when Enabled

Figure 4-5 above shows the emphasis waveform. Amplitudes V1, V2 and emphasis in dB are defined as follows:

V1, **V2** and **Emphasis** are defined as follows:

V1 = **RX_SDO_EMPHASIS** setting, which represents the "peak", or superposition of the **RX_SDO_SWING** setting and the **RX_SDO_EMPHASIS** setting.

V2 = **RX_SDO_SWING** setting, which is the DC or Steady State swing, same as when no emphasis is enabled.

Emphasis [dB] = 20 x log(V1/V2). As a guideline, 2V1 should be less than or equal to 800mV.

The output can be configured to automatically mute if Receive LOS is detected through the following registers. When muted, the output driver remains powered-up, and the output common mode is maintained. The output driver can be configured to power-down when muted by setting the **RX_SDO_PWR_DN_ON_MUTE** bit:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXSDO_REG3	77	RX_SDO_FORCE_MUTE	0:0	RW	0	0-1	Mutes driver to CM when not in auto mute mode.
		RX_SDO_AUTO_MUTE_EN	1:1	RW	1	0-1	Enables muting the driver upon LOS.
		RX_SDO_PWR_DN_ON_MUTE	2:2	RW	1	0-1	Enables power-down on mute for output stage.

4.2.7 Output Polarity Invert

Polarity inversion is implemented at the SDO input. Input to the CDR is not affected by polarity inversion. The output polarity can be inverted through the following register:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RXPLL_REG5	24	RX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.

4.3 Transmit Path

The transmit path is comprised of a trace equalizer, a multi-rate CDR and an EML driver.

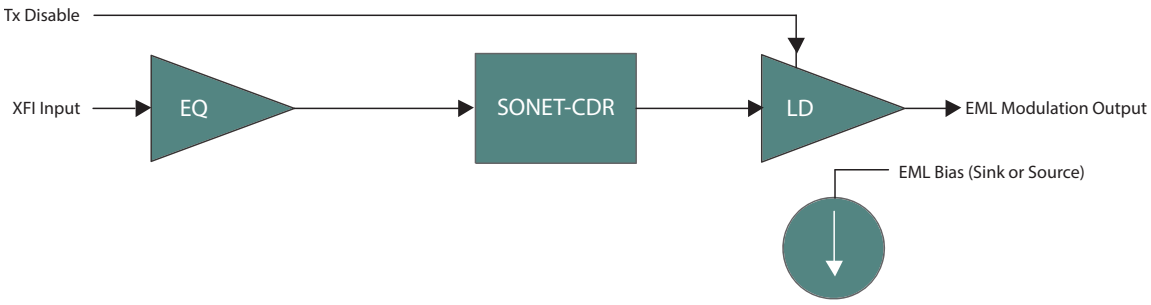


Figure 4-6: Transmit Path

4.3.1 Equalizer

The the transmit path input has an XFI equalizer with up to 6dB gain at 5.35GHz. The equalizer can be controlled through the following register:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TX_REG3	33	TX_EQ_BOOST	1:0	RW	11	0-3	Controls the Tx path input equalization setting: 00 = 0dB 01 = 2dB 10 = 4dB 11 = 6dB

4.3.2 Tx PLL Variable Loop Bandwidth

The loop bandwidth of the transmit Phase Locked Loops (PLL) can be varied through the digital control interface. The loop bandwidths are individually controlled, and can cover the range of less than 1MHz to 10MHz through following 5-bit registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG1	10	TX_PLL_LBW_POS_ADJ	4:0	RW	01110	0-31	Adjusts LBW positive temperature coefficient control.
TXPLL_REG2	11	TX_PLL_LBW_NEG_ADJ	4:0	RW	00010	0-31	Adjusts LBW negative temperature coefficient control.

The temperature coefficient of the loop bandwidth can be adjusted by weighted summation of **TX_PLL_LBW_POS_ADJ**, which has a positive temperature coefficient and **TX_PLL_LBW_NEG_ADJ**, which has a negative temperature coefficient.

Table 4-3 shows the recommended settings for a flat loop bandwidth temperature coefficient:

Table 4-3: Tx Loop Bandwidth

TX_PLL_LBW_POS_ADJ	TX_PLL_LBW_NEG_ADJ	LBWTotal	LBW (MHz)
2	0	2	1.413
4	3	7	2.480
7	5	12	3.547
10	7	17	4.555
13	9	22	5.330
15	11	26	5.950
18	13	31	6.725
21	15	36	7.500
24	17	41	8.050
27	19	46	8.600
29	20	49	8.919
31	22	53	9.344
31	31	62	10.300

4.3.3 Tx Jitter Filter Mode

The Tx CDR supports a jitter filter mode to aid in the optimization of jitter generation performance and reduction of jitter present at the Tx CDR input. The jitter filter mode is configured using the following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPWRDN_REG4	133	TX_PD_JIT_FILT	0:0	RW	1	0-1	When HIGH, power-down for the Tx jitter filter.
TXPLL_REG1	10	TX_PLL_LBW_POS_ADJ	4:0	RW	01110	0-31	Adjusts the LBW positive temperature coefficient control.
TXPLL_REG2	11	TX_PLL_LBW_NEG_ADJ	4:0	RW	00010	0-31	Adjusts the LBW negative temperature coefficient control.
TXPLL_REG8	17	TX_JIT_FILT_TRACK_ADJUST	7:3	RW	00010	0-31	Sets the tracking capability when Tx jitter filter mode is enabled.

Note: This feature does not impact the jitter generation performance of the Tx Laser Driver. The jitter generation performance of the laser driver and external TOSA must still be properly optimized separately.

To enable Tx jitter filter mode, set **TX_PD_JIT_FILT** LOW. Once enabled, **TX_PLL_LBW_POS_ADJ** and **TX_PLL_LBW_NEG_ADJ** are used to set the jitter filter bandwidth, and can be optimized for the desired jitter generation/filtering performance. Lastly, **TX_JIT_FILT_TRACK_ADJUST** is used to set the tracking capability of an internal clock with respect to the Tx input data. This allows for optimization of wander tolerance.

4.4 Laser Driver

4.4.1 EML Driver

The GN2044S has an integrated EML driver with eye-shaping features and an integrated Automatic Power Control (APC) loop.

The EML laser driver can provide up to $2.5V_{pp}$ modulation. The following registers can be used to set the modulation current with 10-bit resolution. Note that **TXSDO_IMOD_LO** must be written to first, followed by a write to **TXSDO_IMOD_HI**. The new value only takes effect after a write to **TXSDO_IMOD_HI**.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG10	87	TXSDO_IMOD_LO	7:0	RW	00000000	0-255	LD modulation current LSB.
TXSDO_REG11	88	TXSDO_IMOD_HI	1:0	RW	00	0-3	LD modulation current MSB.

4.4.1.1 Jitter Generation Optimization Using Laser Driver Phase Adjust

The jitter optimization feature in the laser driver is intended to optimize module level jitter. This includes jitter from the GN2044S, external pull-up inductors, board parasitic and the laser diode. This feature can also be used to improve jitter generation performance for SONET applications. The following registers can be used to optimize jitter generation through TxSDO phase adjust:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG13	90	TXSDO_PHASE_ADJUST	7:0	RW	00000000	0-255	LD phase adjust—compensation for jitter generation due to Sonet header.
TXSDO_REG25	99	TXSDO_PHASEADJ_DIR	1:1	RW	0	0-1	LD phase adjust (Z0) compensation direction: Early = 0, Late = 1.
PWRDN_REG1	138	PD_TXSDO_PHASE_ADJ	2:2	RW	1	0-1	When HIGH, power-down for LD phase adjust (Z0) compensation.

TXSDO_PHASEADJ_DIR controls the direction in which the jitter generation optimization using phase adjust is applied. The direction depends on the jitter signature present at the output of the module. **TXSDO_PHASE_ADJUST** controls the magnitude of the jitter generation optimization. To enable the feature, **PD_TXSDO_PHASE_ADJ** must be set LOW. The Tx CDR must be powered-on for the phase adjust feature to work.

4.4.1.2 Crossing Point Adjust

The crossing point adjust feature allows the user to adjust the cross point as shown in Figure 4-7 below. The crossing point adjust features can set the output crossing point from 20% to 80%, with a 6-bit control through following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG12	89	TXSDO_CPA	5:0	RW	011111	0-63	LD crossing point adjust: 0~ = >80% 31 = 50% 63~ = <20%
PWRDN_REG1	138	PD_TXSDO_CPA	3:3	RW	1	0-1	When HIGH, power-down for LD crossing point adjust.

To enable the feature, **PD_TXSDO_CPA** must be set LOW.

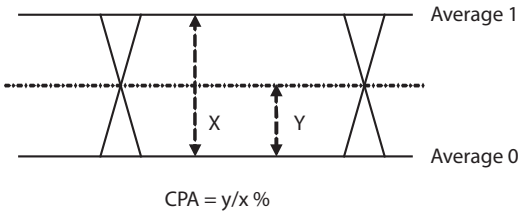


Figure 4-7: Definition of Cross Point Adjust Percentage

4.4.1.3 Pre-Emphasis

The laser driver supports pre-emphasis. The pre-emphasis is applied to both the rising and falling edges simultaneously. It can be used to optimize the optical eye and improve the mask margin. The amplitude of the pre-emphasis can be varied. The following registers are used to program the pre-emphasis:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TxSDO_REG14	91	TXDSO_PREEMPH_AMP	4:0	RW	00000	0-31	LD pre-emphasis amplitude control.
PWRDN_REG1	138	PD_TXSDO_PREEMPH	0:0	RW	1	0-1	Power-down for LD pre-emphasis.

4.4.1.4 Laser Driver Shutdown

The laser driver supports several modes of shutdown including:

- Manual mute (with optional output stage power-down)
- Automatic mute upon LOS detection (with optional output stage power-down)
- Modulation squelch
- TxDSBL through control register

The following registers can be used to configure and invoke the above shutdown modes:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG25	99	TXSDO_MOD_SQUELCH	0:0	RW	0	0-1	When HIGH, LD modulation is squelched.
		TXSDO_FORCE_TXDSBL	2:2	RW	0	0-1	When HIGH, shuts down the LD mod, bias and APC.
		TXSDO_FORCE_MUTE	3:3	RW	0	0-1	When HIGH, mutes driver to CM when not in auto mute mode.
		TXSDO_AUTO_MUTE_EN	4:4	RW	1	0-1	When HIGH, enables muting the driver upon LOS.
		TXSDO_PWR_DN_ON_MUTE	5:5	RW	1	0-1	When HIGH, enables power-down on mute for the output stage.

4.4.2 Laser Driver Bias Current

The laser driver bias current can be configured as either a sink or a source current. By default, the bias current is configured as a source. It is important to avoid configuring the bias current in a mode that will not be used by the intended application. If a bias current sink is required by the application, the device must be configured to make the bias current a sink after power-up. If a bias current source is required by the application, no configuration is necessary, as the device is configured as a source by default.

The following registers can be used to configure the bias current as either a source or a sink:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXSDO_REG26	100	TXSDO_BIAS_SOURCE_EN	3:3	RW	1	0-1	LD bias source is enabled when HIGH. TXSDO_BIAS_SINK_EN must be LOW.
		TXSDO_BIAS_SINK_EN	4:4	RW	0	0-1	LD bias sink is enabled when HIGH. TXSDO_BIAS_SOURCE_EN must be LOW.

The laser driver bias current is controlled by the Automatic Power Control or APC loop by default. The next section describes the operation of the APC loop. However, the laser driver bias current may be set manually by overriding the APC loop. The following registers allow a fixed laser driver bias current to be programmed manually:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range (Dec)	Function
APC_REG4	106	APC_DAC_OVR_VAL_LO	7:0	RW	00000000	0-255	Override value for the APC DAC counter [7:0]. Sets the LD bias current manually when used with APC_DAC_OVR_VAL_HI, and when APC_OVR is HIGH. Step size is approximately 0.15mA.
APC_REG5	107	APC_DAC_OVR_VAL_HI	1:0	RW	00	0-3	Override APC DAC [9:8]. A write triggers an update.
		APC_OVR	2:2	RW	0	0-1	When HIGH, overrides the APC loop with the DAC override value to set the LD bias current manually.

When **APC_OVR** is set HIGH, the APC control loop is bypassed and the 10-bit bias current control **APC_DAC_OVR_VAL_LO/HI** takes effect. Note that the LOW value must be written first, followed by a write to the HIGH value. The new value only takes effect after a write to the HIGH value. The APC must still be enabled when using the override mode.

Note: With **APC_OVR** set HIGH, TxDSBL assert will set the LD bias current to shut off. After TxDSBL is de-asserted, the **APC_DAC_OVR_VAL_LO/HI** registers must be re-written to turn on the LD bias current. When **APC_OVR** is set HIGH, it is recommended to write the **APC_DAC_OVR_VAL_LO/HI** registers immediately following TxDSBL negation to minimize the negate time.

4.4.3 Automatic Power Control Loop

The GN2044S integrates an Automatic Power Control or APC loop to control the bias current for the laser diode in the TOSA, thereby reducing the external components required. The photo current from the TOSA (IPHOTO) is converted to a voltage (VPHOTO), through an on-chip, selectable resistor. The resistor selection is based on the maximum IPHOTO from the TOSA. There are four possible settings available through IPH_RANGE_SEL[1:0]. IPHOTO is then used as an indicator of the average transmit power. The user can define a set point for IPHOTO to achieve a certain average transmit power. The APC loop operates to achieve and maintain the set point over operating conditions.

The APC uses 10 bits of resolution to define the bias current to ensure minimal variation of average transmit power. To accommodate different TOSAs configurations, IPHOTO can be configured to source a current from the GN2044S or sink a current from the TOSA.

The APC loop is enabled by default. The following registers can be used to enable and configure the APC loop. When the APC loop is disabled and re-enabled, it must be reset.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
APC_REG1	104	APC_EN	0:0	RW	1	0-1	When HIGH, enables the APC.
		APC_RESET	3:3	RW	0	0-1	When HIGH, the APC control is reset.
		APC_SEL_HIGH_REF	4:4	RW	0	0-1	When HIGH, IPHOTO is sourced from the GN2044S and is sunk in the TOSA. When LOW, IPHOTO is sourced from the TOSA and is sunk in the GN2044S.
TXSDO_REG5	82	IPH_RANGE_SEL	1:0	RW	10	0-3	IPHOTO range select: 00 = 0mA to 0.25mA 01 = 0.25mA to 0.75mA 10 = 0.75mA to 1.25mA 11 = 1.25mA to 2.14mA

4.4.3.1 APC Loop Dynamics

The APC loop is designed to meet the TxDSBL assert time of <10µs, and the TxDSBL negate time of <2ms. In addition, the APC loop supports a highly-configurable loop dynamics upon TxDSBL negate to minimize the time to achieve the desired output average power level, without any overshoots on output average power.

The loop dynamics upon Reset or TxDSBL negation is configured through two sets of parameters as follows:

1. APC Thresholds
   - APC_TH_HI
   - Set Point (IPHOTO for desired average transmit power)
2. APC Slew Rates
   - Fast Rate—LD bias current updates rate when IPHOTO is < APC_TH_HI
   - Slow Rate—LD bias current updates rate when IPHOTO is > APC_TH_HI

Figure 4-8 shows the loop dynamics and impact of each of the above parameters.

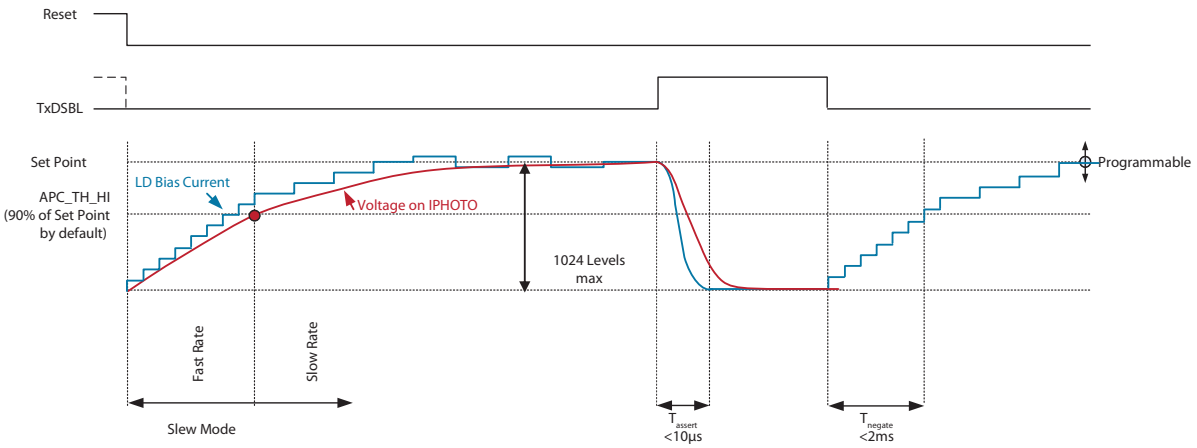


Figure 4-8: APC Loop Dynamics

Upon negation of Reset or TxDSBL, the difference between IPHOTO and the set point (error) is large. In this region, a fast rate for LD bias current can be selected to minimize the negate time without risk of overshooting the set point. As the error reduces, it is desirable to slow down the LD bias current rate to avoid overshoot. The threshold **APC_TH_HI** defines the region of fast and slow ramp up rates. Initially, the LD Bias current will ramp-up at a fast rate because it is below **APC_TH_HI**. When the LD Bias current exceeds **APC_TH_HI**, it will ramp-up at the slow rate. This controlled ramp-up ensures robust stability and avoids overshoots while meeting the negate time of <2ms. By default, **APC_TH_HI** is set to 90% of the set point, but it can be adjusted if necessary. It is generally recommended to use the default APC configuration settings.

The following registers control the APC thresholds:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
APC_REG6	108	APC_REF_DAC_CTRL	7:0	RW	00000000	0-255	Sets APC final target reference threshold (0V to 1V range in steps of 4mV).
APC_REG8	110	APC_TH_HI	5:0	RW	110110	0-63	APC Threshold Hi setting 110110 (default) - 0.9x of setpoint 1 LSB = 0.0167x of setpoint.

The following registers control the APC slew rates:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
APC_REG2	105	APC_CLK_RATE_FAST_DIV	3:2	RW	00	0-3	APC fast rate divide ratio: 0-3 = 32-256, default = 32
		APC_CLK_RATE_SLOW_DIV	6:4	RW	101	0-7	APC slow rate divide ratio: 0-3 = 32-4k, default = 1k

Note: The default update rate is approximately 20MHz.

4.5 Status Indicators

The GN2044S supports three status indicators: Loss of Signal (LOS), Loss of Lock (LOL) and Module Not Ready (MODNR). LOS and LOL indicators are available on both the receive and the transmit paths.

4.5.1 Receive Loss of Signal (LOS)

The receive path Loss Of Signal indicator status is available through a register and the LOSL pin. The LOSL pin is by default open-drain, active-high 1.8V – 3.3V LVCMOS compatible. However, the pin can be configured in a 1.8V LVCMOS-compliant compatible mode by setting **OPEN_DRAIN_LOSL** to 0. In addition, LOSL can be configured to be active-low by setting **POLINV_LOSL** HIGH. The status of RxLOS can be read out through **RX_PLL_LOS**. Additionally, the LOSL pin can be configured to provide other status information as per the table below. By default, LOSL only provides status information for RxLOS. If other status indicators are enabled, the LOSL output is the logical OR of all enabled indicators.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TOP_REG2	2	POLINV_LOSL	1:1	RW	0	0-1	When HIGH, inverts polarity of the LOSL output.
		OPEN_DRAIN_LOSL	2:2	RW	1	0-1	When HIGH, makes the LOSL output driver open-drain.
		LOSL_MASK_RXLOS	4:4	RW	0	0-1	When HIGH, masks-out RxLOS from asserting LOSL.
		LOSL_MASK_RXLOL	5:5	RW	1	0-1	When HIGH, masks-out RxLOL from asserting LOSL.
		LOSL_MASK_TXLOS	6:6	RW	1	0-1	When HIGH, masks-out TxLOS from asserting LOSL.
		LOSL_MASK_TXLOL	7:7	RW	1	0-1	When HIGH, masks-out TxLOL from asserting LOSL.
RXPLL_REG10	29	RX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.

The LOS assert threshold can be set from 5mV to 400mV in three distinct ranges. The LOS assert threshold is a function of the **RXLA_BOOST_MSB** setting. Table 4-4 describes the selection of **RXLOS_RANGE** based on the required LOS assert threshold and **RXLA_BOOST_MSB** settings.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG12	59	RXLOS_RANGE	1:0	RW	01	0-3	LOS range: 0 = highest 3 = lowest

Table 4-4: LOS Assert Ranges

RXLA_BOOST_MSB [3:0]	LOS Assert Threshold Range		RXLOS_RANGE[1:0]	Resolution (controlled by RXLOS_TH_NEG/POS)	Unit
	Min	Max			
	5	400	LOS Threshold - Total Range	—	mV_{ppd}
0-7	—	—	11 - Unused	—	—
0-7	5	30	10 - Low Range	<0.1mV	mV_{ppd}
0-7	30	100	01 - Mid Range	<1.0mV	mV_{ppd}
0-7	100	400	00 - High Range	<2.0mV	mV_{ppd}
8-15	5	30	11 - Low Range	<0.1mV	mV_{ppd}
8-15	30	100	10 - Mid Range	<1.0mV	mV_{ppd}
8-15	—	—	01 - Unused	—	—
8-15	100	400	00 - High Range	<2.0mV	mV_{ppd}

4.5.1.1 Rx LOS Threshold

The LOS assert threshold is set using the following registers:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
RX_REG9	56	RXLOS_TH_NEG	7:0	RW	01001001	0-255	Negative tempco LOS threshold setting.
RX_REG10	57	RXLOS_TH_POS	7:0	RW	00000000	0-255	Positive tempco LOS threshold setting.

Figure 4-9 to Figure 4-13 shows the typical recommended range of Rx LOS Assert thresholds and corresponding **RX_LOS_TH_NEG[7:0]** setting to achieve these thresholds. It is recommended to keep **RX_LOS_POS[7:0]** = 0. The Rx LOS De-assert thresholds are the same as the Rx LOS Assert thresholds for a hysteresis setting of 0.

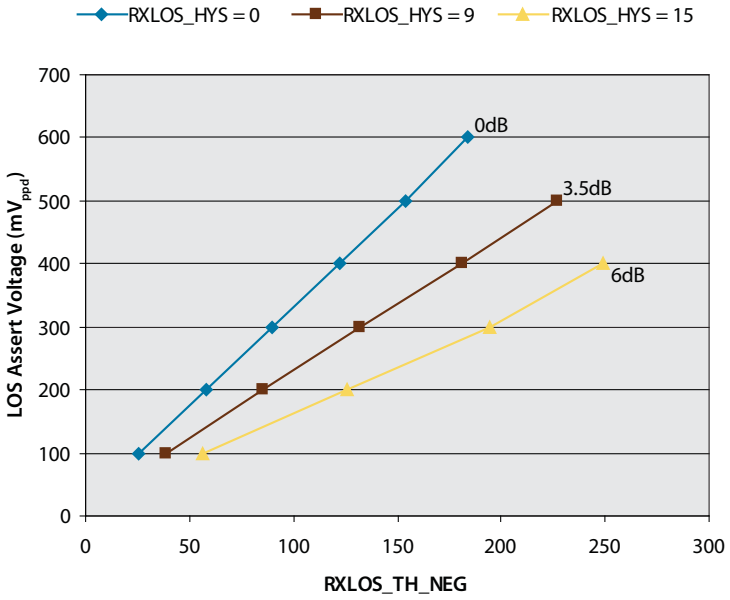


Figure 4-9: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = 0)

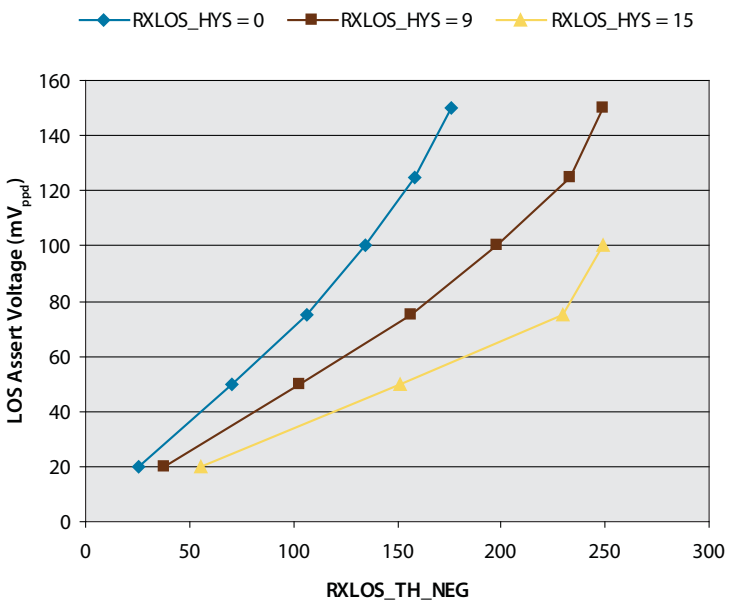


Figure 4-10: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = 1)

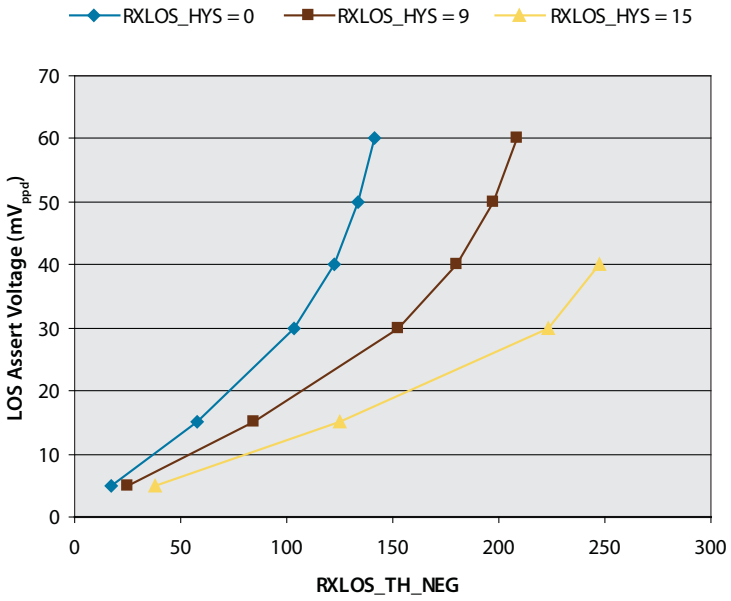


Figure 4-11: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = 2)

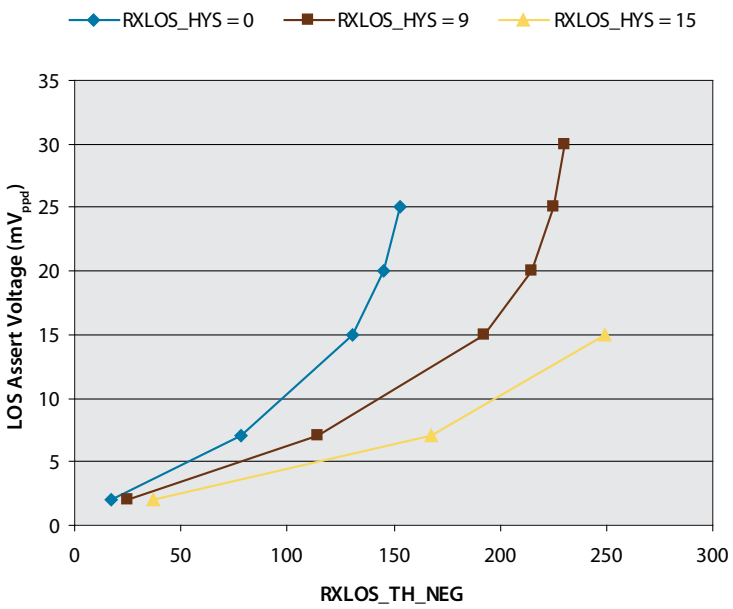


Figure 4-12: Rx LOS Threshold vs. Hysteresis (RXLOS_RANGE = 3)

The LOS threshold has a slight dependence on the input data rate. Figure 4-13 below gives an indication of the typical variation of data rate, between 9.95Gb/s to 11.3Gb/s.

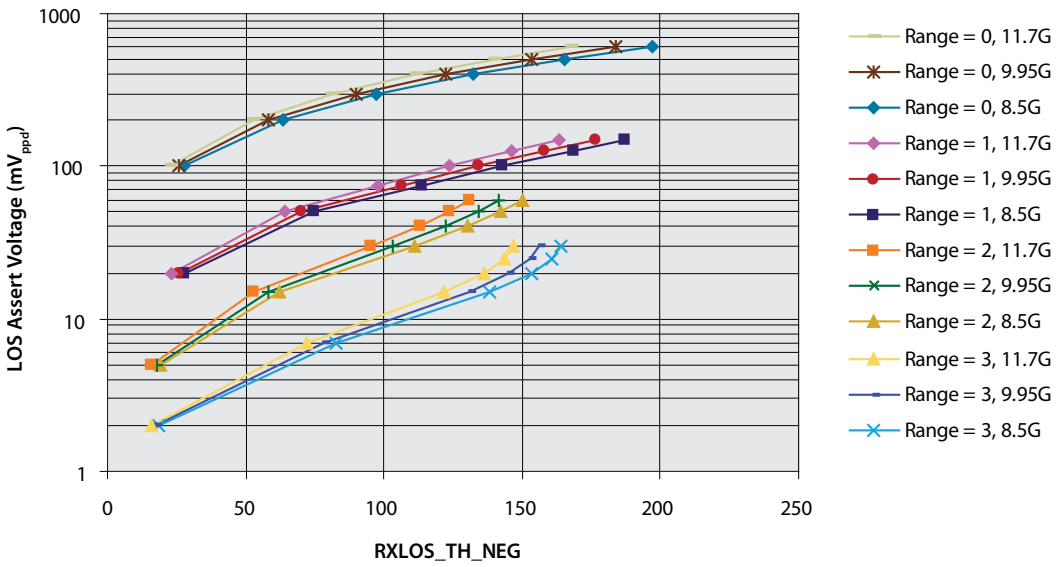


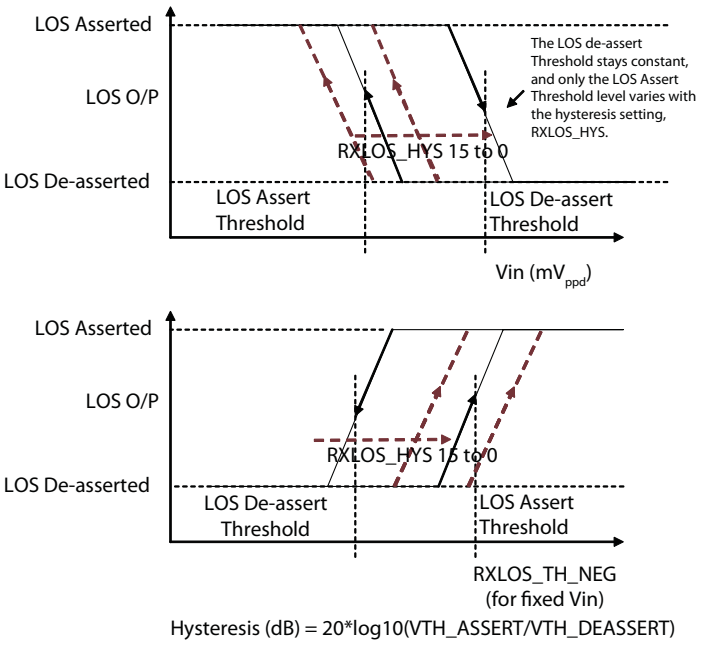
Figure 4-13: Rx LOS Assert Threshold Variation Over Data Rates

4.5.1.2 Rx LOS Hysteresis

The LOS detector supports programmable hysteresis ranging from 0dB to 6dB, adjustable in steps of less than 0.5dB. The following register can be used to program the hysteresis. Note that the effective hysteresis is somewhat dependent on the threshold value:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
RX_REG11	58	RXLOS_HYS	3:0	RW	1001	0-15	Hysteresis control 0-15 -> 0-6dB. Default = 9 = 3dB.

Hysteresis control only affects the assert threshold. The LOS de-assert threshold is set by **RXLOS_TH_NEG** and **RXLOS_TH_POS** controls only. Figure 4-14 shows the hysteresis characteristics and the impact of **RXLOS_HYS[3:0]**:



RXLOS_HYS	Hysteresis (dB)
0	0.1
1	0.3
2	0.7
3	1.1
4	1.4
5	1.8
6	2.1
7	2.5
8	3.0
9	3.4
10	3.9
11	4.4
12	4.8
13	5.4
15	6.7

Figure 4-14: Rx LOS Hysteresis

To support system diagnostics, a manual LOS assert feature is available through the following registers:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
RX_REG12	59	RXLOS_FORCE_ASSERT	2:2	RW	0	0-1	Directly sets the state of RXLOS accordingly if RXLOS_FORCE_ASSERT_EN is HIGH.
		RXLOS_FORCE_ASSERT_EN	3:3	RW	0	0-1	When HIGH, LOS is controlled by RXLOS_FORCE_ASSERT.

4.5.2 Transmit Loss of Signal

The transmit path LOS indicator status is available through a register. If desired, its status can be included in the generation of the MODNR or LOSL output pins. The LOS assert threshold can be set from 20mV to 100mV in <1mV steps. In addition the temperature coefficient of the LOS threshold can be adjusted to ensure consistent LOS operation over temperature. The LOS also has hysteresis that is programmable from 0dB to 6dB in steps of less than 0.5dB. A manual LOS assert feature is supported for system diagnostics.

The following registers are used to control the transmit LOS feature:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TX_REG9	39	TXLOS_TH_NEG	7:0	RW	00011011	0-255	Negative temperature coefficient LOS threshold setting.
TX_REG10	40	TXLOS_TH_POS	7:0	RW	00000000	0-255	Positive temperature coefficient LOS threshold setting.
TX_REG11	41	TXLOS_HYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB.
TX_REG12	42	TXLOS_FORCE_ASSERT	3:3	RW	0	0-1	Directly sets the state of TXLOS accordingly if TXLOS_FORCE_ASSERT_EN is HIGH.
		TXLOS_FORCE_ASSERT_EN	4:4	RW	0	0-1	When HIGH, LOS is controlled by TXLOS_FORCE_ASSERT.

4.5.2.1 Tx LOS Threshold

Figure 4-15 and Figure 4-16 show the typical recommended range of Tx LOS assert thresholds and corresponding **TXLOS_TH_NEG[7:0]** setting to achieve these thresholds. It is recommended to keep **TXLOS_TH_POS[7:0]** = 0 to achieve a flat temperature coefficient for LOS threshold. The Tx LOS de-assert thresholds are the same as the Tx LOS assert thresholds for a hysteresis setting of 0.

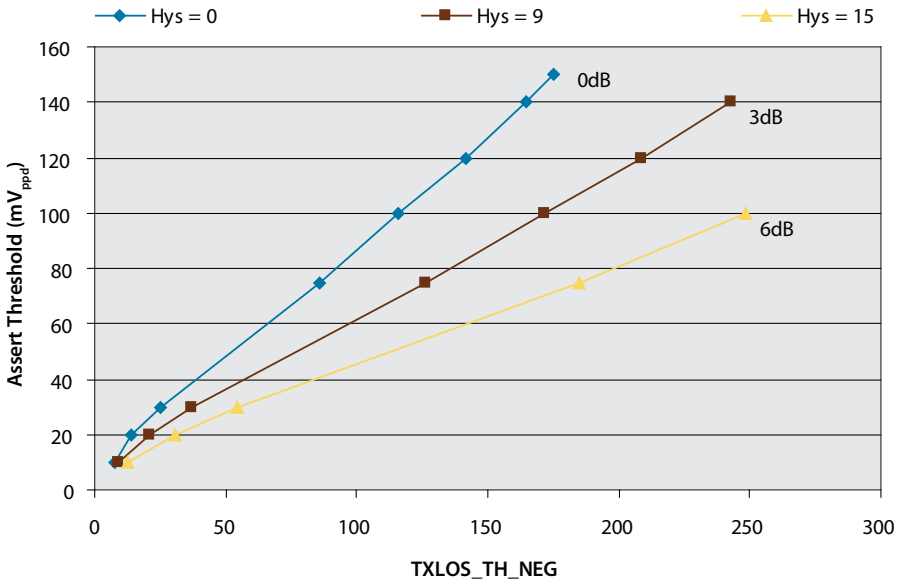


Figure 4-15: Tx LOS Assert Threshold – Typical @ 9.95Gb/s

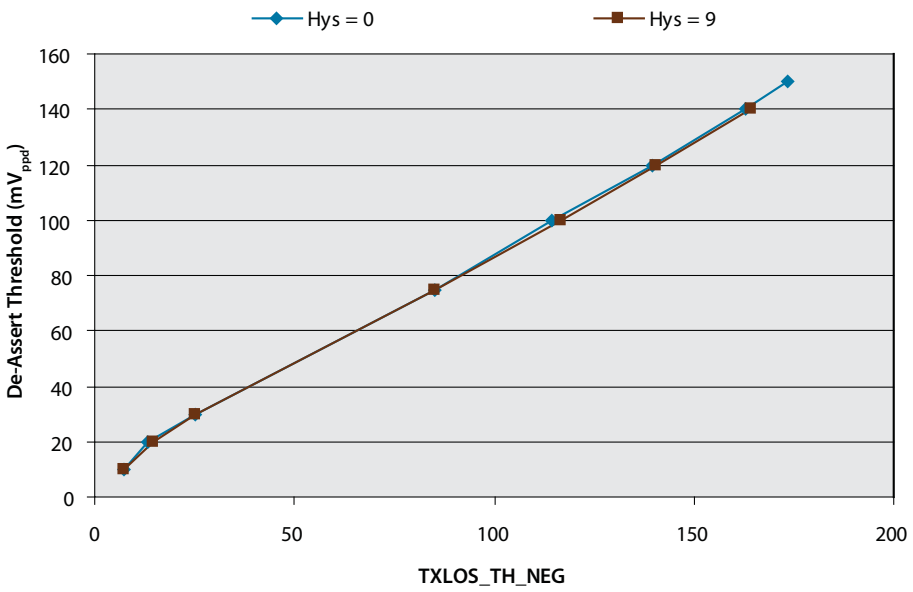


Figure 4-16: Tx LOS De-Assert Threshold – Typical @ 9.95Gb/s

The LOS threshold will have a slight dependence on data rate.

4.5.3 Loss of Lock

The receive path and transmit path LOSS of LOCK (LOL) status indicators are both available in registers as indicated below. These bits can also be included in the MODNR or LOSL outputs:

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TXPLL_REG10	19	TX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
RXPLL_REG10	29	RX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.

4.5.4 MODNR - Module Not Ready

Various status indicator pins are combined to generate a single MODNR indicator output. The MODNR output is, by default, an open-drain 1.8V – 3.3V LVCMOS-compatible output. It can be configured in a 1.8V LVCMOS-compliant mode through Register 2, bit 3 – **OPEN_DRAIN_MODNR**.

The MODNR output is active-high by default. Its polarity can be changed to make it active-LOW through Register 2, bit 0 – **POLINV_MODNR**. When set HIGH, MODNR is configured as an active-low output.

The following status indicator controls can be combined to generate the MODNR output. Each of the indicators can be independently masked through the register controls shown below. By default, the MODNR output combines (OR's) the status of all indicators.

The following registers control the masking of the various indicators for MODNR and the configuration of MODNR pin.

Register Name	Register Address$_d$	Parameter Name	Bit Position	Access	Reset Value$_b$	Valid Range$_d$	Function
TOP_REG1	1	MODNR_MASK_RXLOS	0:0	RW	0	0-1	When HIGH, masks-out RxLOS from asserting MODNR.
		MODNR_MASK_RXLOL	1:1	RW	0	0-1	When HIGH, masks-out RxLOL from asserting MODNR.
		MODNR_MASK_TXLOS	2:2	RW	0	0-1	When HIGH, masks-out TxLOS from asserting MODNR.
		MODNR_MASK_TXLOL	3:3	RW	0	0-1	When HIGH, masks-out TxLOL from asserting MODNR.
		MODNR_MASK_TXFAULT	4:4	RW	0	0-1	When HIGH, masks-out TxFault from asserting MODNR.
TOP_REG2	2	POLINV_MODNR	0:0	RW	0	0-1	When HIGH, inverts polarity of MODNR output.
		OPEN_DRAIN_MODNR	3:3	RW	1	0-1	When HIGH, makes the MODNR output driver open-drain.

4.6 Test Features

The GN2044S contains built-in test features that can be used during module bring-up or for debug purposes. The test features are not guaranteed and are only meant as functional tests under typical conditions. It is not advised to use these features during mission mode operation.

4.6.1 PRBS Generator and Checker

The GN2044S has a built-in PRBS7 generator and checker. The generator and checker are disabled by default to save power, and can be enabled through the digital control interface. There are multiple ways to use the PRBS generator/checker. The PRBS Generator frequency is controlled by the **PRBS_GENERATOR_DATA_RATE_CONTROL[5:0]** register. The PRBS generator and checker are meant to be used only as functional debug tests. The register setting of **PRBS_GENERATOR_DATA_RATE_CONTROL[5:0]** = 20 corresponds to a data rate of typically 10.3Gb/s. The PRBS checker uses the recovered clock from the Tx CDR. Refer to Table 4-5 for more details.

Note: PRBS7 input to the PRBS checker must be non-inverted for the checker to operate correctly. As such, care must be taken when using the polarity invert feature in conjunction with external loop back to PRBS checker to ensure that the data polarity to the checker is correct. Internal loop-back paths are not affected by the polarity invert feature.

The following registers enable and configure the PRBS generator and checker:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG3	3	PRBS_GEN_START	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts off the PRBS Generator.
		PRBS_CHK_CLEAR_ERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from the Checker.
TOP_REG6	6	PRBS_CHK_STATUS	0:0	RO	0	0-1	When HIGH, checker detected an error.
LOOPBK_REG1	7	LB_RX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Rx Driver.
		LB_RX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects PRBS generator output into Rx Driver.
LOOPBK_REG2	8	PRBS_CHK_CLK_SEL	1:1	RW	0	0-1	When HIGH, selects the Tx recovered clock. When LOW, selects the Rx recovered clock.
		LB_TX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Tx Driver.
		LB_TX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects PRBS generator output into the Tx Driver.
LOOPBK_REG3	9	PRBS_GENERATOR_DATA_ RATE_CONTROL	5:0	RW	0	0-63	PRBS Generator Frequency Tuning Control. The tuning range is 9.9GHz to 10.4GHz from minimum to maximum setting.
PWRDN_REG2	139	PD_PRBS_GEN	1:1	RW	1	0-1	When HIGH, power-down the PRBS generator and associated buffers.
		PD_PRBS_CHK	2:2	RW	1	0-1	When HIGH, power-down the PRBS checker and associated buffers.

To ensure proper operation of the PRBS7 generator, **PRBS_GEN_START** needs to be set HIGH and then LOW once after the generator is powered-up through **PD_PRBS_GEN**.

To ensure proper operation of the PRBS7 checker, **PRBS_CHK_CLEAR_ERR** needs to be set HIGH and then LOW after application of valid PRBS7 pattern to clear any spurious errors. **PRBS_CHK_STATUS**, may be polled to check for errors flagged by the checker.

The PRBS generator can be configured to apply a PRBS7 pattern to RxSDO or TxSDO.

Table 4-5: PRBS Generator/Checker Configuration

Loopback Mode	Description	PD_PRBS_GEN	PD_PRBS_CHK	PRBS_CHK_CLK_SEL	LB_TX_OUT_PRBS_GEN	LB_RX_OUT_PRBS_GEN	LB_TX_OUT_EN	LB_RX_OUT_EN
PRBS Disabled	Default Mission mode	1	1	X	0	0	0	0
PRBS GEN → Rx Driver → Tx Equalizer → Tx CDR → PRBS CHECKER	External Rx Loopback (tests TX CDR)	0	0	1	0	1	0	1

4.6.2 Loopback

The GN2044S allows four different loopback paths, and supports loopback on both the electrical side and the optical side. The loopback paths are shown in Table 4-6. The blocks referenced in the different loopback paths are shown in Figure 4-17.

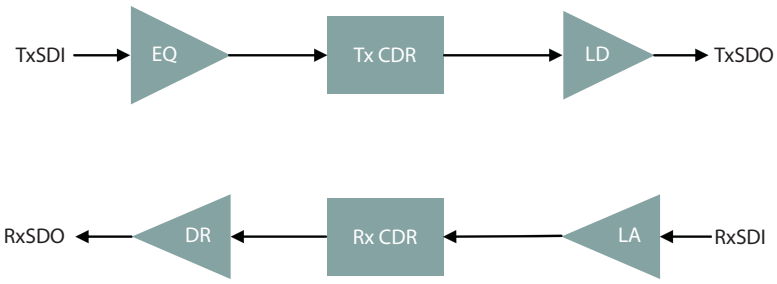


Figure 4-17: Simultaneous Loopback

Table 4-6: Loopback Paths

Mode #	Loopback Path
1	RxSDI → LA → LD → TxSDO
2	RxSDI → LA → RxCDR → LD → TxSDO
3	TxSDI → EQ → DR → RxSDO
4	TxSDI → EQ → TxCDR → DR → RxSDO

When loopback is enabled, the standard data path is not interrupted. For example: in Mode 1, the input to RXSDI will also be accessible at RXSDO. When using loopback modes, the automute feature for RxSDO or TxSDO may have to be disabled if the corresponding RxSDI or TxSDI inputs are unused.

The relevant parameters and their values required to enable each of the loopback options indicated above, are shown in Table 4-7.

The selection of a loopback path impacts the following features:

- Polarity inversion
- Phase adjust for jitter optimization for TxSDO (LD)

Table 4-7 also captures the impact on these features in each loopback mode.

Table 4-7: Loopback Options

Loop Back Mode (see Table 4-6)	LB_RX_OUT_EN	LB_RX_OUT_TX_DATA	LB_RX_OUT_PRBS_GEN	LB_RX_OUT_RX_CLK	RX_PLL_BYPASS	LB_TX_OUT_EN	LB_TX_OUT_RX_DATA	LB_TX_OUT_PRBS_GEN	LB_TX_OUT_TX_CLK	TX_PLL_BYPASS	TX_PLL_POLINV Effective	TX_SDO_PHADJ Available	RX_PLL_POLINV Effective
1	0	0	0	0	1	1	1	0	0	0	Y	N	N
2	0	0	0	0	0	1	1	0	0	0	Y	N	N
3	1	1	0	0	0	0	0	0	0	1	N	—	Y
4	1	1	0	0	0	0	0	0	0	0	N	—	Y
Control Register Address	7	7	7	7	24	8	8	8	8	14	—	—	—
Associated Bit Slice	4	5	6	7	2	4	5	6	7	2	—	—	—

4.7 Digital Diagnostics

The GN2044S has an on-chip ADC to provide diagnostic information through the digital interface. Refer to the GN204x Family ADC Application Note (PDS-060373) for more details.

4.8 Power-Down Options

The GN2044S provides a high-degree of flexibility in configuring the device for optimal power through power-down registers. Typical usage scenarios are shown. For further description on each of the individual control bits, see Table 5-1, registers **134** to **137**. This section describes the power-down controls for the following sub-systems:

1. Rx LA Power-Down
2. Rx CDR & SDO Power-Down
3. Tx CDR Power-Down
4. Tx SDO Power-Down

Table 4-8: Rx LA Power-Down

RX_PD_PATH	RX_PD_LA	RX_PD_LOS	RX_PD_SLICE_ADJ	Description
1	x	1	1	Completely powers-down the Rx LA.
x	1	1	1	Completely powers-down the Rx LA.
0	0	0	0	All features on. This is diagnostic mode.
0	0	0	1	Powers-down the slice adjust mode.
0	0	1	1	Powers down the SLA and LOS feature for lowest power mode.

Table 4-9: Rx CDR & SDO Power-Down

RX_PLL_BYPASS	RX_PD_PATH	RX_PD_RXCDR	RX_PD_SONET_IJT	RX_PD_RXSDO	RX_PD_RXSDO_EMPHASIS	Description
0	1	x	x	1	1	Completely powers-down the Rx CDR and Rx SDO.
0	x	1	x	1	1	Completely powers-down the Rx CDR and Rx SDO
1	0	x	x	0	1	Main data path through Rx CDR and RxSDO is powered-up for bypass mode. (RxLA has to be powered-up).
0	0	0	1	0	1	Standard operating mode, Rx CDR & SDO enabled in low-power mode. High IJT mode and emphasis are disabled.
0	0	0	0	0	0	Standard operating mode, Rx CDR & SDO enabled. High IJT mode and emphasis are enabled. IJT performance is set by RX_PLL_SELECT_HIGH_IJT registers.
0	0	0	1	0	0	Rx CDR & SDO are enabled. High IJT mode is powered-down. Emphasis is enabled.

Table 4-10: Tx CDR Power-Down

TX_PLL_BYPASS	TX_PD_TXPATH	TX_PD_TXCDR	TX_PD_JIT_FILT	TX_PD_TXSDO	PD_TXSDO_PHASE_ADJ	Description
0	1	1	x	1	x	Completely powers-down the Tx CDR and Tx path.
1	0	1	x	0	1	Main data path through Tx CDR is powered-up for bypass mode. (TxEq has to be powered-up).
0	0	0	1	0	1	Standard operating mode, Tx CDR is enabled in standard mode. Tx SDO jitter optimization through phase adjust is powered-down.
0	0	0	0	0	1	Standard operating mode, Tx CDR is enabled in jitter filter mode. (Requires appropriate configuration of jitter filter controls. See Section 4.3.3).
0	0	0	1	0	0	Standard operating mode, Tx SDO jitter optimization feature through phase adjust is enabled. (Requires appropriate configuration of Tx SDO controls).

Table 4-11: Tx SDO Power-Down

TX_PD_TXPATH	TX_PD_TXSDO	TX_PD_TXCDR	PD_TXSDO_PHASE_ADJ	PD_TXSDO_CPA	PD_APC	Description
1	x	x	x	x	x	Completely powers-down the Tx SDO.
x	1	x	x	x	x	Completely powers-down the Tx SDO.
0	0	0	0	x	x	Enables the Tx SDO jitter optimization through phase adjust feature.
0	0	x	x	1	x	Independently powers-down the Tx SDO cross point adjust feature.
0	0	x	x	x	1	Independently powers-down the Tx SDO Automatic Power Control loop.
0	0	0	0	0	0	Standard operating mode with Tx SDO jitter optimization, crossing point adjust and APC loop enabled.
0	0	0	0	0	0	Tx SDO with all features enabled.

4.9 Device Reset

$\overline{\text{RESET}}$ is an active-low signal with LVTTL/LVCMOS-compatible signalling levels. Due to the timing requirements of $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ to $\overline{\text{RESET}}$, it is recommended that $\overline{\text{RESET}}$ be driven by the Micro on the module. An external 10kΩ pull-down resistor is also recommended on the $\overline{\text{RESET}}$ line. $\overline{\text{RESET}}$ does not have a Schmitt trigger since reset negation is internally synchronized. See Figure 3-10.

4.9.1 Reset State During Power-up

The device requires $\overline{\text{RESET}}$ to be continuously pulled to GND during power ramp-up. $\overline{\text{RESET}}$ must continue to remain in that state for the minimum specified time after all of the power supplies have reached 90% of their final settling value. Following a $\overline{\text{RESET}}$ assertion at power-up, the device may be reset again at any time with the minimum specified pulse width on $\overline{\text{RESET}}$. Refer to Figure 4-18.

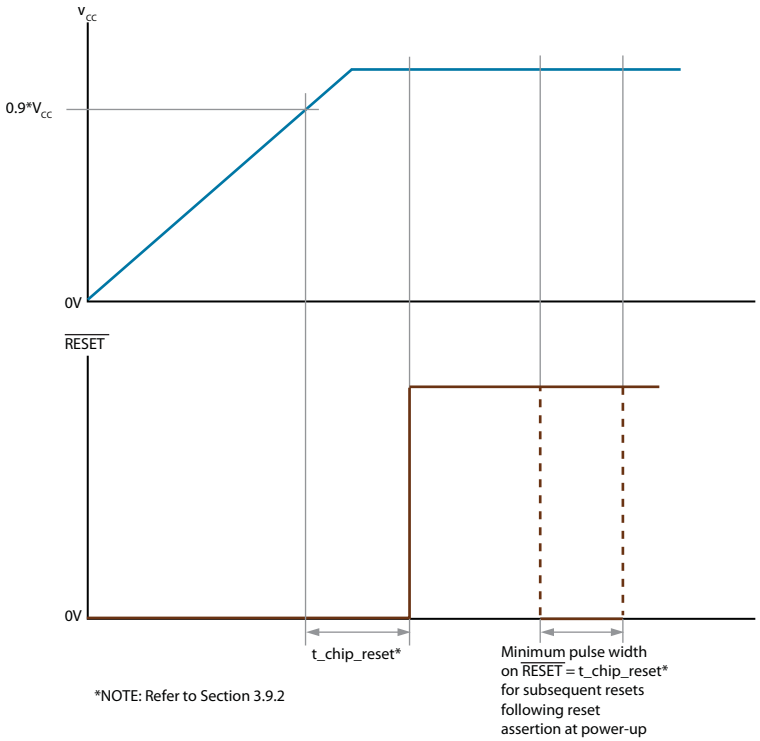


Figure 4-18: Reset State During Power-up

4.9.2 $\overline{\text{RESET}}$ Timing

The following $\overline{\text{RESET}}$ timing specifications apply:

- **t_chip_reset: 10µs**
  Defined as the minimum duration that $\overline{\text{RESET}}$ must be asserted after the supply has reached 90% of its final settling value
- **t_ISELb_setup: 500ns**
  Defined as the minimum duration that the $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ pin must be asserted HIGH to select the SPI mode before $\overline{\text{RESET}}$ is negated

- **t_SPI_ready: 500ns**

  Defined as the minimum duration before an SPI/I^{2}C operation may be initiated, after $\overline{\text{RESET}}$ negation

When I^{2}C mode is desired, the $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$ pin is recommended to be pulled to ground throughout operation of the device.

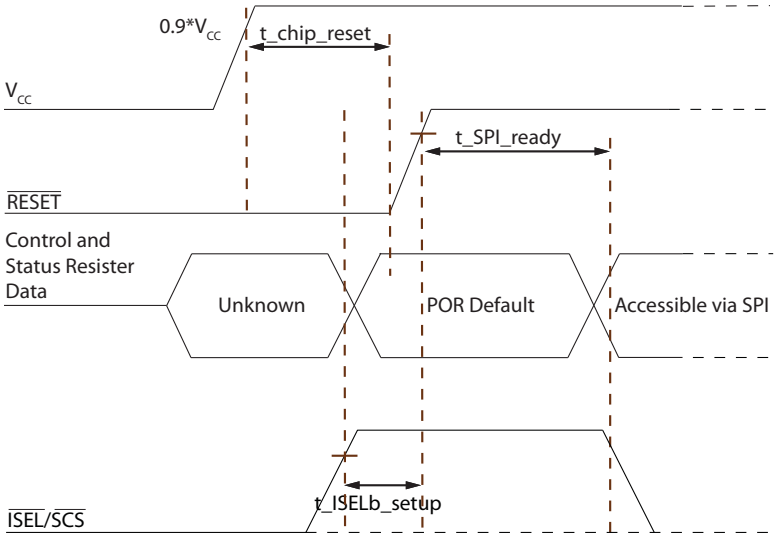


Figure 4-19: GN2044S Device Reset Timing Diagram

4.9.3 I/O and Register States During and After Reset

All configuration registers are set to their post-reset defaults state immediately following $\overline{\text{RESET}}$ assertion.

The following I/O states are applicable upon $\overline{\text{RESET}}$ assertion:

Table 4-12: I/O and Register States During and After Reset

Pin Name	I/O State upon $\overline{\text{RESET}}$ Assertion
SDA/SDIO/MISO	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance with a weak pull-down of 5µA.
SCL/SCLK and SSEL/MOSI	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted, and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance with a weak pull-down of 5µA.
MODNR	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. The loss of lock indicators will assert MODNR HIGH. This output will be high-impedance, and it's state will depend on the external pull-up.
LOSL	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. If a signal is present, the output will be pulled LOW. Otherwise, this output will be high-impedance and it's state will depend on the external pull-up.

Note: While the device is in reset, the SDA/SDI/MISO pin will output the state of the SSEL/MOSI pin. This can inhibit the ability for the master to communicate with other slave devices on the bus.

4.10 Digital Control Interface

The GN2044S has a tri-mode serial control interface to communicate with the part. Either an I^2C or SPI 3-wire, or SPI 4-wire protocol can be used. The protocol is selected using the $\overline{ISEL}/\overline{SCS}$ and SSEL pins at the time of reset de-assertion.

When pin $\overline{ISEL}/\overline{SCS}$ is held LOW, or left unconnected, and the $\overline{RESET}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in I^2C mode. After reset de-assertion, the state of the $\overline{ISEL}/\overline{SCS}$ pin is a 'don't care'. However, it is recommended that if the pin is not left unconnected, then it be driven LOW.

When the $\overline{ISEL}/\overline{SCS}$ pin is held HIGH, and the SSEL pin is held LOW or left unconnected, and the $\overline{RESET}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in a three-wire SPI mode. After reset de-assertion, the $\overline{ISEL}/\overline{SCS}$ pin functions as the $\overline{SCS}$ pin of a three-wire SPI interface.

When the $\overline{ISEL}/\overline{SCS}$ pin is held HIGH, and the SSEL pin is held HIGH, and the $\overline{RESET}$ pin is asserted to 0 for a valid reset interval and released to 1, the host interface is configured in a four-wire SPI mode. After reset de-assertion, the $\overline{ISEL}/\overline{SCS}$ pin functions as the $\overline{SCS}$ pin, and the SSEL/MOSI functions as the slave data input pin, and the SDA/SDIO/MISO functions as the slave data output of a four-wire SPI interface.

4.10.1 I^2C Host Interface Mode

The I^2C mode supports standard-mode (100kHz) and fast-mode (400kHz) signalling. The device only supports slave mode. The pins SDA/SDIO and SCL/SCLK are used for bi-directional serial data and clock respectively. Signalling rates lower than the standard-mode and fast-mode rates are also supported by the device.

The GN2044S device slave address is 24h.

The I^2C protocol is implemented as per the following description:

Each access begins with a 7-bit I^2C slave address word, an 8-bit register address word, followed by one 8-bit data word in a write command, or the device slave address with the read/write bit plus one 8-bit data word in the read command.

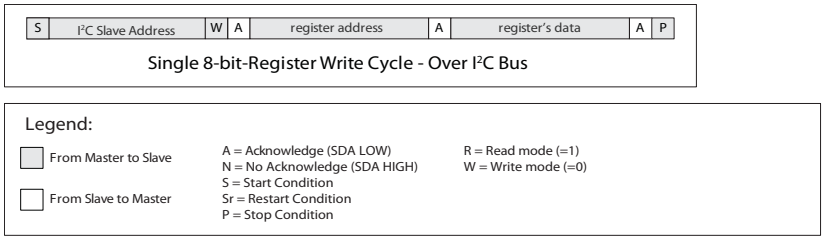


Figure 4-20: Single Register Write Cycle over I²C Bus

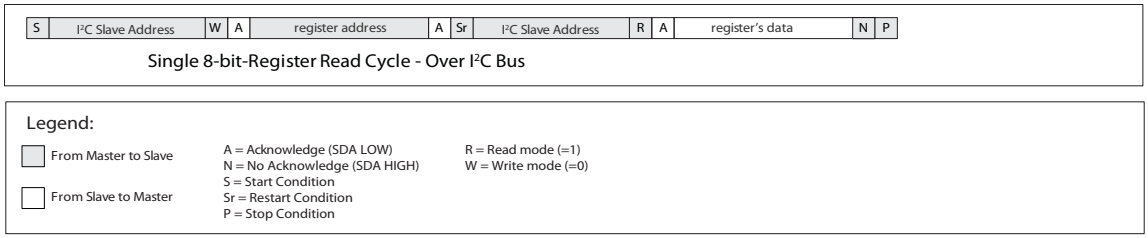


Figure 4-21: Single Register Read Cycle over I²C Bus

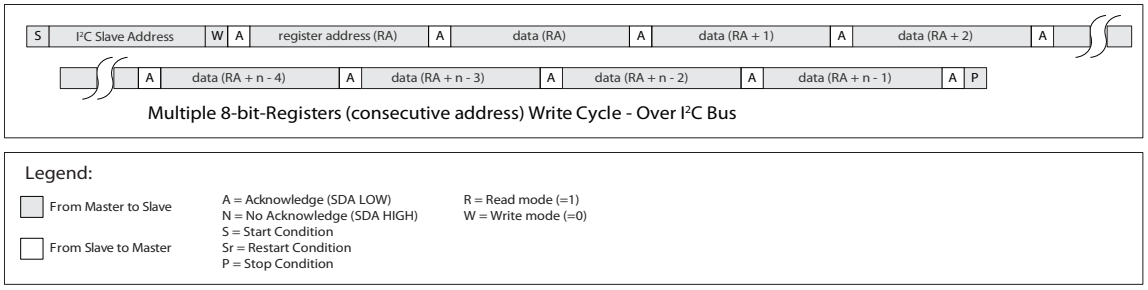


Figure 4-22: Bulk Register Write Cycle over I²C Bus

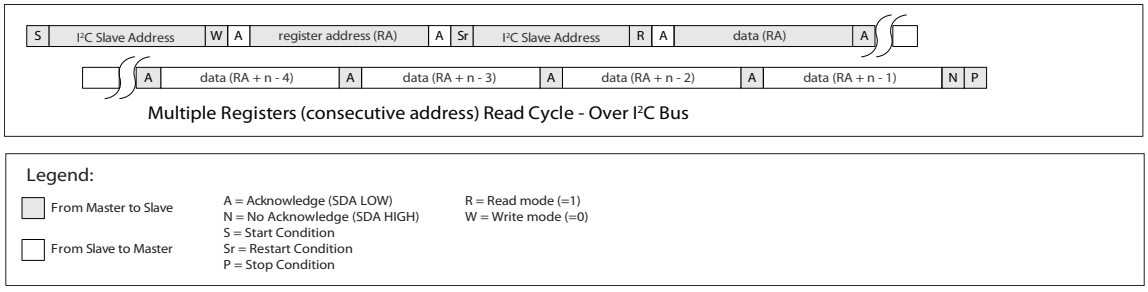


Figure 4-23: Bulk Register Read Cycle over I²C Bus

4.10.2 SPI Host Interface Mode

The GN2044S uses either a 3-wire or a 4-wire SPI protocol. The 3-wire SPI protocol's serial communication takes place via the bi-directional serial data signal (SDA/SDIO). The 4-wire SPI protocol's serial communication uses SSEL/MOSI as its data input and SDA/SDIO as its data output. In both modes, SCL/SCLK is the clock input and $\overline{ISEL}$/$\overline{SCS}$ is the chip select.

The signalling rate can be up to 10Mb/s. The interface uses 8-bit data and 16-bit address + control.

The 16-bit address + control is made up of an 8-bit address, 1-bit command, 1-bit for auto-increment and 6 unused bits. The 3-wire SPI protocol is implemented as per Figure 4-24 and Figure 4-25. The signal sdo_oen_o is an internal signal indicating the direction of the SDIN_SDOUT pin. When '1', the SDIN_SDOUT pin is configured as an input, when '0', its configured as an output. The 4-wire SPI protocol is implemented as per Figure 4-26.

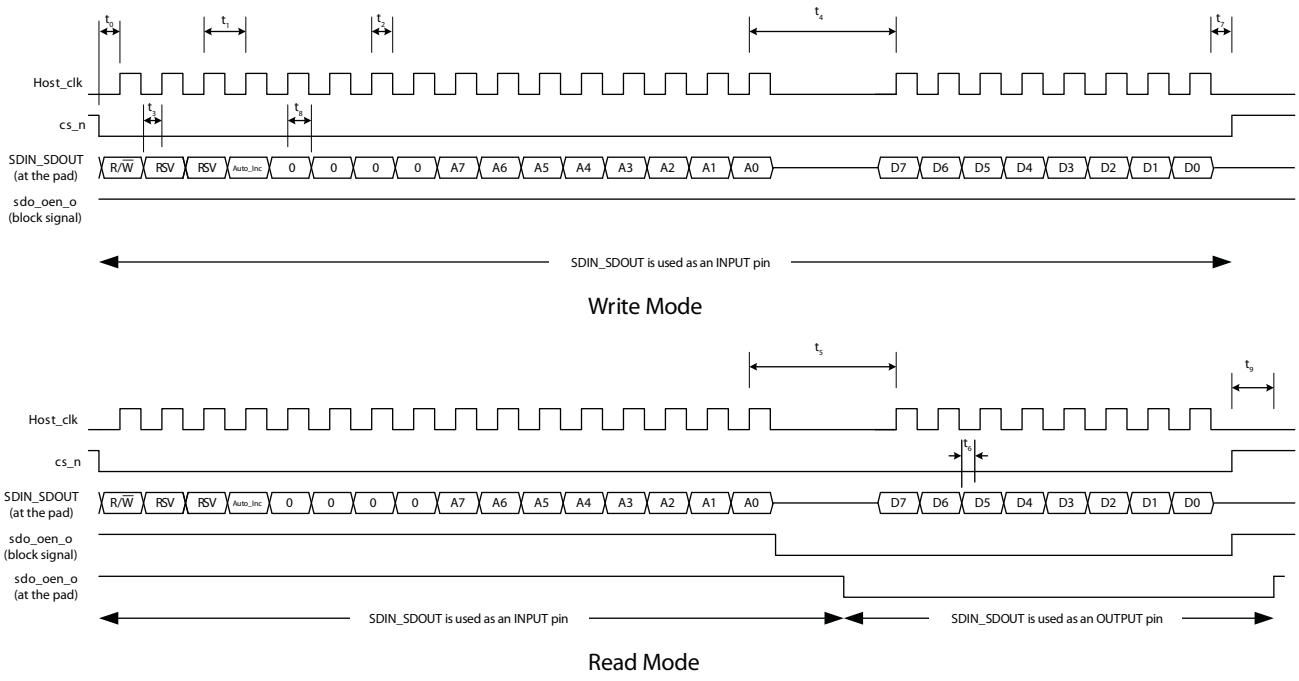


Figure 4-24: SPI Write and Read Timing Diagrams (Single Transaction)

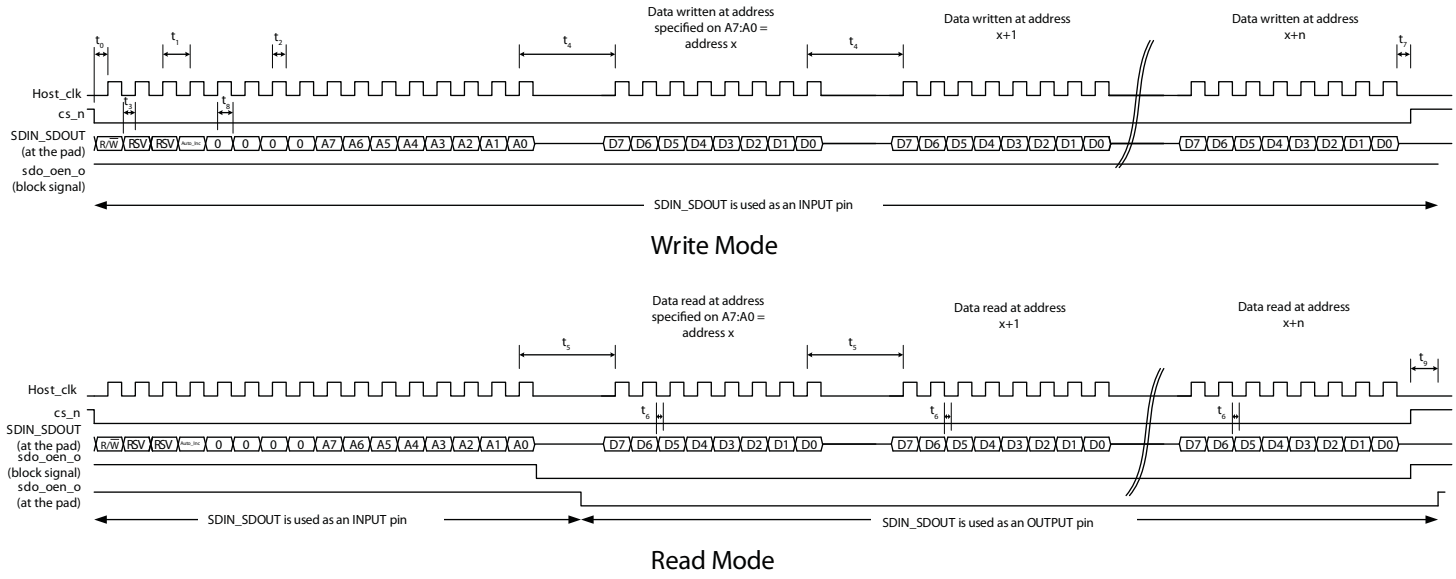


Figure 4-25: SPI Write and Read Timing Diagrams (Auto-Increment Transaction)

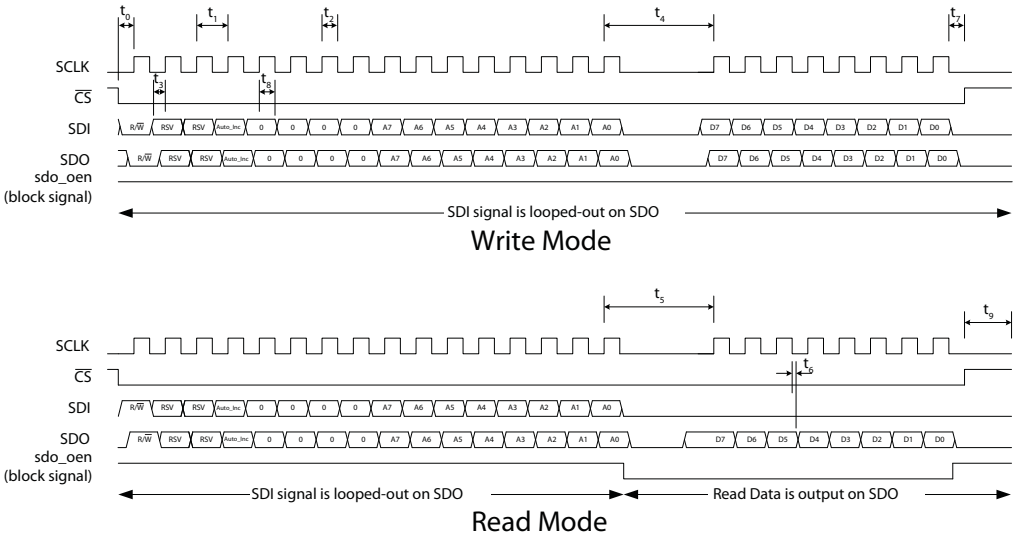


Figure 4-26: SPI Write and Read Timing Diagrams (4-wire)

Table 4-13: SPI Host Interface Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CS_N low before HOST_CLK rising edge	t_0	50% levels; 1.8V operation	1.5	—	—	ns
HOST_CLK period	t_1		100	—	—	ns
HOST_CLK duty cycle	t_2		40	50	60	%
Input data setup time	t_3		1.5	—	—	ns
Time between end of command word (or data in Auto Increment mode) and the first host_clk of the following data word write cycle	t_4		93.5	—	—	ns
Time between end of command word (or data in Auto Increment mode) and the first host_clk of the following data wordread cycle	t_5		420	—	—	ns
Output hold time (15pF load)	t_6		1.5	—	—	ns
CS_N high after last host_clk rising edge	t_7		93.5	—	—	ns
Input data hold time	t_8		1.5	—	—	ns
CS_N high time	t_9		233.6	—	—	ns
CS_N input rise/fall time*	—	20% to 80%	10	—	—	ns

In Figure 4-24, Figure 4-25, and Figure 4-26, CS_N = $\overline{\text{ISEL}}$/$\overline{\text{SCS}}$, HOST_CLK = SCL/SCLK, SDIN_SDOUT = SDA/SDIO, SDI = SSEL/MOSI, and SDO = SDA/SDIO.

There is an auto-increment bit in the command (bit 12) allowing for write burst and read burst transactions.

*The specified minimum rise/fall time must be met to avoid degrading receive sensitivity.

4.10.3 Digital I/O (Schmitt trigger)

A Schmitt trigger is available on the following signals:

- $\overline{ISEL}/\overline{SCS}$
- SDA/SDIO in input mode
- SCL/SCK in input mode SSEL/MOSI
- SSEL/MOSI

The transfer characteristics of the Schmitt Trigger buffer are shown in Figure 4-27 below:

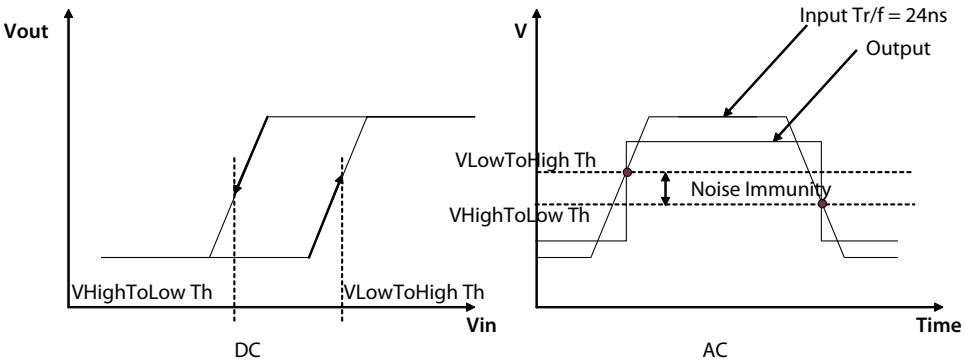


Figure 4-27: Schmitt Trigger Transfer Characteristics

The DC and AC thresholds are shown in Table 2-2: DC Electrical Characteristics.

5. Register Descriptions

Table 5-1: Register Descriptions

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
0	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
1	TOP_REG1	RSVD	7:6	—	0	0-3	Reserved – do not change.
		SPIOUT_OPEN_DRAIN	5:5	RW	0	0-1	0 = Normal SPI operation 1 = Enables SPI output driver open-drain configuration
		MODNR_MASK_TXFAULT	4:4	RW	0	0-1	When HIGH, masks-out TxFault from asserting MODNR.
		MODNR_MASK_TXLOL	3:3	RW	1	0-1	When HIGH, masks-out TxLOL from asserting MODNR.
		MODNR_MASK_TXLOS	2:2	RW	0	0-1	When HIGH, masks-out TxLOS from asserting MODNR.
		MODNR_MASK_RXLOL	1:1	RW	1	0-1	When HIGH, masks-out RxLOL from asserting MODNR.
		MODNR_MASK_RXLOS	0:0	RW	0	0-1	When HIGH, masks-out RxLOS from asserting MODNR.
2	TOP_REG2	LOSL_MASK_TXLOL	7:7	RW	1	0-1	When HIGH, masks-out TxLOL from asserting LOSL.
		LOSL_MASK_TXLOS	6:6	RW	1	0-1	When HIGH, masks-out TxLOS from asserting LOSL.
		LOSL_MASK_RXLOL	5:5	RW	1	0-1	When HIGH, masks-out RxLOL from asserting LOSL.
		LOSL_MASK_RXLOS	4:4	RW	0	0-1	When HIGH, masks-out RxLOS from asserting LOSL.
		OPEN_DRAIN_MODNR	3:3	RW	1	0-1	When HIGH, makes the MODNR output driver open-drain.
		OPEN_DRAIN_LOSL	2:2	RW	1	0-1	When HIGH, makes the LOSL output driver open-drain.
		POLINV_LOSL	1:1	RW	0	0-1	When HIGH, inverts the polarity of the LOSL output.
		POLINV_MODNR	0:0	RW	0	0-1	When HIGH, inverts the polarity of the MODNR output.
3	TOP_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		PRBS_CHK_CLEAR_ERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from the PRBS Checker.
		PRBS_GEN_START	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts the PRBS Generator.
4	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.
5	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
6	TOP_REG6	RSVD	7:1	—	0	0-127	Reserved – do not change.
		PRBS_CHK_STATUS	0:0	RO	0	0-1	When HIGH, the PRBS Checker has detected an error.
7	LOOPBK_REG1	LB_RX_OUT_RX_CLK	7:7	RW	0	0-1	Selects the Rx Clk into the Rx Driver.
		LB_RX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects the PRBS Generator O/P into the Rx Driver.
		LB_RX_OUT_TX_DATA	5:5	RW	0	0-1	Selects the Tx data into the Rx Driver.
		LB_RX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into the Rx Driver.
		RSVD	3:0	—	0	0-15	Reserved – do not change.
8	LOOPBK_REG2	LB_TX_OUT_TX_CLK	7:7	RW	0	0-1	Selects the Tx Clock into the Tx Driver.
		LB_TX_OUT_PRBS_GEN	6:6	RW	0	0-1	Selects the PRBS Generator O/P into the Tx Driver.
		LB_TX_OUT_RX_DATA	5:5	RW	0	0-1	Selects the Rx data into the Tx Driver.
		LB_TX_OUT_EN	4:4	RW	0	0-1	Selects the LB input into Tx Driver.
		RSVD	3:2	—	0	0-3	Reserved – do not change.
		PRBS_CHK_CLK_SEL	1:1	RW	0	0-1	When HIGH, selects the Tx recovered clock. When LOW, selects the Rx recovered clock.
		RSVD	0:0	—	0	0-1	Reserved – do not change.
9	LOOPBK_REG3	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PRBS_GENERATOR_DATA_RATE_CONTROL	5:0	RW	0	0-63	PRBS Generator frequency tuning control. See Section 4.6.1.
10	TXPLL_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TX_PLL_LBW_POS_ADJ	4:0	RW	1110	0-31	Adjusts LBW positive temperature coefficient control. See Section 4.3.2.
11	TXPLL_REG2	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TX_PLL_LBW_NEG_ADJ	4:0	RW	10	0-31	Adjusts LBW negative temperature coefficient control. See Section 4.3.2.
12	RSVD_REG	RSVD	7:0	—	00010010	0-255	Reserved – do not change.
13	RSVD_REG	RSVD	7:0	—	00000101	0-255	Reserved – do not change.
14	TXPLL_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		TX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the Tx CDR into bypass mode.
		RSVD	1:1	—	0	0-1	Reserved – do not change.
		TX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
15	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
16	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
17	TXPLL_REG8	TX_JIT_FILT_TRACK_ADJUST	7:3	RW	00010	0-31	Sets the tracking capability when Tx jitter filter mode is enabled. See Section 4.3.3.
		RSVD	2:0	—	101	0-7	Reserved – do not change.
18	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
19	TXPLL_REG10	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		TX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.
20	RXPLL_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		RX_PLL_LBW_POS_ADJ	4:0	RW	11101	0-31	Adjusts LBW positive temperature coefficient control. See Section 4.2.4.
21	RXPLL_REG2	RSVD	7:5	—	0	0-7	Reserved – do not change.
		RX_PLL_LBW_NEG_ADJ	4:0	RW	111	0-31	Adjusts LBW negative temperature coefficient control. See Section 4.2.4.
22	RSVD_REG	RSVD	7:0	—	00010010	0-255	Reserved – do not change.
23	RSVD_REG	RSVD	7:0	—	00000101	0-255	Reserved – do not change.
24	RXPLL_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_PLL_BYPASS	2:2	RW	0	0-1	When HIGH, forces the CDR into bypass mode.
		RSVD	1:1	—	0	0-1	Reserved – do not change.
		RX_PLL_POL_INV	0:0	RW	0	0-1	When HIGH, inverts the data path polarity.
25 to 26	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
27	RXPLL_REG8	RX_PLL_SONET_IJT_SETTING	7:3	RW	10	0-31	Control for Sonet IJT performance. Used in conjunction with Sonet IJT modes 2 and 3 to set IJT performance. Gradually increase setting for increased margins. See Section 4.2.5.
		RX_PLL_LOCK_DCD_TOL_DIS	2:2	RW	1	0-1	When LOW, enables tolerance of data duty cycle distortion for locking.
		RSVD	1:0	—	1	0-3	Reserved – do not change.
28	RXPLL_REG9	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_PLL_SELECT_HIGH_IJT	3:3	RW	1	0-1	When HIGH, selects high-margin Sonet IJT mode in conjunction with RX_PLL_SONET_IJT_SETTING. See Section 4.2.5.
		RSVD	2:0	—	0	0-7	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
29	RXPLL_REG10	RSVD	7:2	—	0	0-63	Reserved – do not change.
		RX_PLL_LOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		RX_PLL_LOS	0:0	RO	0	0-1	Loss of signal when HIGH.
30	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
31	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
32	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
33	TX_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TX_EQ_BOOST	1:0	RW	11	0-3	Controls the Tx path input equalization setting: 00 = 0dB 01 = 2dB 10 = 4dB 11 = 6dB
34	RSVD_REG	RSVD	7:0	—	111111	0-255	Reserved – do not change.
35	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
36	RSVD_REG	RSVD	7:0	—	101	0-255	Reserved – do not change.
37	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
38	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
39	TX_REG9	TXLOS_TH_NEG	7:0	RW	11011	0-255	Negative temperature coefficient LOS threshold setting. Refer to Section 4.5.2.
40	TX_REG10	TXLOS_TH_POS	7:0	RW	0	0-255	Positive temperature coefficient LOS threshold setting. Refer to Section 4.5.2.
41	TX_REG11	RSVD	7:4	—	0	0-15	Reserved – do not change.
		TXLOS_HYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB.
42	TX_REG12	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TXLOS_FORCE_ASSERT_EN	4:4	RW	0	0-1	When HIGH, LOS is controlled by TXLOS_FORCE_ASSERT.
		TXLOS_FORCE_ASSERT	3:3	RW	0	0-1	Directly sets the state of TXLOS accordingly if TXLOS_FORCE_ASSERT_EN is HIGH.
		RSVD	2:0	—	0	0-7	Reserved – do not change.
43	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
44	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
45	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
46	RSVD_REG	RSVD	7:0	—	1111	0-255	Reserved – do not change.
47	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
48	RX_REG1	RSVD	7:4	—	111	0-15	Reserved – do not change.
		RXLA_BOOST_MSB	3:0	RW	0	0-15	RXLA boost control bit MSBs. 0 = 0dB to 15 = 14dB
49	RX_REG2	RXLA_SLICE_ADJ	7:0	RW	0	0-255	Slice adjust magnitude control.
50	RX_REG3	RSVD	7:2	—	0	0-63	Reserved – do not change.
		RXLA_SLICE_ADJ_LO_RANGE	1:1	RW	0	0-1	Selects slice level adjust point. When LOW, slicing point is option 1. When HIGH, slicing point is option 2. See Section 4.2.2.
		RXLA_SLICE_ADJ_POL	0:0	RW	0	0-1	Slice adjust polarity. When HIGH, slice adjust is positive.
51	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
52	RX_REG5	RSVD	7:1	—	1000	0-127	Reserved – do not change.
		RXLA_MANUAL_SLICE_ADJ_EN	0:0	R/W	0	0-1	When HIGH, enables user to adjust slice level at Rx input. See Section 4.2.2.
53	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
54	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
56	RX_REG9	RXLOS_TH_NEG	7:0	RW	1001001	0-255	Negative tempco LOS threshold setting.
57	RX_REG10	RXLOS_TH_POS	7:0	RW	0	0-255	Positive tempco LOS threshold setting.
58	RX_REG11	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RXLOS_HYS	3:0	RW	1001	0-15	Hysteresis control 0-15 -> 0-6dB. Default 9 = 3dB.
59	RX_REG12	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RXLOS_FORCE_ASSERT_EN	3:3	RW	0	0-1	When HIGH, LOS is controlled by RXLOS_FORCE_ASSERT.
		RXLOS_FORCE_ASSERT	2:2	RW	0	0-1	Directly sets the state of RXLOS accordingly if RXLOS_FORCE_ASSERT_EN is HIGH.
		RXLOS_RANGE	1:0	RW	1	0-3	LOS range: 0 = highest 3 = lowest
60	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
61	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
62	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
63	RX_REG16	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RXLA_BOOST_LSB	2:0	RW	0	0-7	RXLA boost control bit LSBs for fine tuning gain with smaller step size. See Section 4.2.3.
64	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
65 to 74	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
75	RXSDO_REG1	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_SDO_SWING	3:0	RW	110	0-15	Driver swing: 100mV$_{ppd}$ to 850mV$_{ppd}$, Default = 6 = 400mV$_{ppd}$
76	RXSDO_REG2	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_SDO_EMPHASIS	3:0	RW	0	0-15	Driver emphasis control.
77	RXSDO_REG3	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_SDO_PWR_DN_ON_MUTE	2:2	RW	1	0-1	Enables power-down on mute for output stage.
		RX_SDO_AUTO_MUTE_EN	1:1	RW	1	0-1	Enables muting the driver upon LOS.
		RX_SDO_FORCE_MUTE	0:0	RW	0	0-1	Mutes driver to CM when not in auto mute mode.
78	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
79	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
80	RSVD_REG	RSVD	7:0	—	00100000	0-255	Reserved – do not change.
81	RSVD_REG	RSVD	7:0	—	11110001	0-255	Reserved – do not change.
82	TXSDO_REG5	RSVD	7:2	—	0	0-63	Reserved – do not change.
		IPH_RANGE_SEL	1:0	RW	10	0-3	IPHOTO range select: 00 = 0mA to 0.25mA 01 = 0.25mA to 0.75mA 10 = 0.75mA to 1.25mA 11 = 1.25mA to 2.14mA
83	RSVD_REG	RSVD	7:0	—	110	0-255	Reserved – do not change.
84	RSVD_REG	RSVD	7:0	—	110110	0-255	Reserved – do not change.
85	TXSDO_REG8	RSVD	7:4	—	0	0-15	Reserved – do not change.
		TXSDO_BIAS_MON_EN	3:3	RW	0	0-1	Enables the laser driver bias monitor circuitry.
		TXSDO_MOD_MON_EN	2:2	RW	0	0-1	Enables the laser driver modulation monitor circuitry.
		RSVD	1:0	—	11	0-3	Reserved – do not change.
86	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
87	TXSDO_REG10	TXSDO_IMOD_LO	7:0	RW	0	0-255	LD modulation current LSB.
88	TXSDO_REG11	RSVD	7:2	—	0	0-63	Reserved – do not change.
		TXSDO_IMOD_HI	1:0	RWC	0	0-3	LD modulation current MSB.
89	TXSDO_REG12	RSVD	7:6	—	0	0-3	Reserved – do not change.
		TXSDO_CPA	5:0	RW	11111	0-63	LD crossing point adjust: 0~ = > 80% 31 = 50% 63~ = < 20%

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
90	TXSDO_REG13	TXSDO_PHASE_ADJUST	7:0	RW	0	0-255	LD phase adjust—compensation for jitter generation due to Sonet header.
91	TxSDO_REG14	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TXDSO_PREEMPH_AMP	4:0	RW	00000	0-31	LD pre-emphasis amplitude control.
92	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
93	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
94	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
95	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
98	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
99	TXSDO_REG25	RSVD	7:6	—	0	0-255	Reserved – do not change.
		TXSDO_PWR_DN_ON_MUTE	5:5	RW	1	0-1	When HIGH, enables power-down on mute for output stage.
		TXSDO_AUTO_MUTE_EN	4:4	RW	1	0-1	When HIGH, enables muting the driver upon LOS.
		TXSDO_FORCE_MUTE	3:3	RW	0	0-1	When HIGH, mutes driver to CM when not in auto mute mode.
		TXSDO_FORCE_TXDSBL	2:2	RW	0	0-1	When HIGH, shuts down the LD mod, bias and APC.
		TXSDO_PHASEADJ_DIR	1:1	RW	0	0-1	LD phase adjust (Z0) compensation direction: Early = 0, Late = 1.
		TXSDO_MOD_SQUELCH	0:0	RW	0	0-1	When HIGH, LD modulation is squelched.
100	TXSDO_REG26	RSVD	7:5	—	0	0-7	Reserved – do not change.
		TXSDO_BIAS_SINK_EN	4:4	RW	0	0-1	LD bias sink is enabled when HIGH. TXSDO_BIAS_SOURCE_EN must be LOW.
		TXSDO_BIAS_SOURCE_EN	3:3	RW	1	0-1	LD bias source is enabled when HIGH. TXSDO_BIAS_SINK_EN must be LOW.
		RSVD	2:0	—	001	0-7	Reserved – do not change.
101	RSVD_REG	RSVD	7:0	—	00000110	0-255	Reserved – do not change.
102	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
103	RSVD_REG	RSVD	7:0	—	11000010	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
104	APC_REG1	RSVD	7:5	—	0	0-7	Reserved – do not change.
		APC_SEL_HIGH_REF	4:4	RW	0	0-1	When HIGH, IPHOTO is sourced from the GN2044S and is sunk in the TOSA. When LOW, IPHOTO is sourced from the TOSA and is sunk in the GN2044S.
		APC_RESET	3:3	RW	0	0-1	When HIGH, the APC control loop is reset.
		RSVD	2:1	—	0	0-3	Reserved – do not change.
		APC_EN	0:0	RW	1	0-1	When HIGH, enables the APC.
105	APC_REG2	RSVD	7:7	—	0	0-1	Reserved – do not change.
		APC_CLK_SLOW_DIV	6:4	RW	101	0-7	APC update rate3 divide ratio: 0 = 32 1 = 64 2 = 128 3 = 256 4 = 512 5 = 1024 (default) 6 = 2048 7 = 4096
		APC_CLK_FAST_DIV	3:2	RW	0	0-3	APC update rate2 divide ratio: 0 = 32 (default) 1 = 64 2 = 128 3 = 256
		RSVD	1:0	—	0	0-3	Reserved – do not change.
106	APC_REG4	APC_DAC_OVR_VAL_LO	7:0	RW	0	0-255	Override value for the APC DAC counter [7:0]. Sets the LD bias current manually when used with APC_DAC_OVR_VAL_HI, and when APC_OVR is HIGH. Step size is approximately 0.15mA.
107	APC_REG5	RSVD	7:3	—	0	0-31	Reserved – do not change.
		APC_OVR	2:2	RW	0	0-1	When HIGH, overrides the APC loop with the DAC override value to set the LD bias current manually.
		APC_DAC_OVR_VAL_HI	1:0	RWC	0	0-3	Override APC DAC [9:8]. A write triggers an update.
108	APC_REG6	APC_REF_DAC_CTRL	7:0	RW	0	0-255	Sets the APC final target reference threshold.
109	RSVD_REG	RSVD	7:0	—	01000110	0-255	Reserved – do not change.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
110	APC_REG8	RSVD	7:7	—	0	0-1	Reserved – do not change.
		APC_TH_HI_BYPASS	6:6	RW	0	0-1	When HIGH, bypasses Threshold Hi and associated APC clock rate.
		APC_TH_HI	5:0	RW	110110	0-63	APC Threshold Hi setting 110110 (default) - 0.9x of setpoint 1 LSB = 0.0167x of setpoint.
111	APC_REG9	RSVD	7:2	—	0	0-63	Reserved – do not change.
		APC_DAC_VAL_LO	1:0	RO	0	0-3	Read out value from the APC DAC counter [1:0].
112	APC_REG10	APC_DAC_VAL_HI	7:0	RO	0	0-255	Read out value from the APC DAC counter [9:3].
113	TXFLT_REG1	RSVD	7:7	—	0	0-1	Reserved – do not change.
		TXFAULT_CLEAR_STATUS	6:6	RW	0	0-1	When HIGH, clears the latched Tx fault status.
		TXFAULT_DISABLE_EN	5:5	RW	0	0-1	When HIGH, a TxDisable assertion triggers a fault.
		TXFAULT_LD_IPHOTO_EN	4:4	RW	1	0-1	Enables IPHOTO monitoring for Fault.
		TXFAULT_LDMOD_CUR_EN	3:3	RW	1	0-1	Enables LD Modulation monitoring for fault.
		TXFAULT_LDBIAS_CUR_EN	2:2	RW	1	0-1	Enables LD Bias Current monitoring for Fault.
		TXFAULT_LDBIAS_V_EN	1:1	RW	1	0-1	Enables LD Bias Voltage monitoring for Fault.
		TXFAULT_EN	0:0	RW	1	0-1	Enable all Tx Faults.
114	TXFLT_REG2	RSVD	7:3	—	0	0-31	Reserved – do not change.
		TXFAULT_LDBIAS_VTH	2:0	RW	0	0-7	Fault threshold for LD Bias minimum voltage. The fault threshold covers a range of 0 to 800mV on the LDBias pin, in steps of 100mV typical. If LDBias is set to source mode, the fault threshold covers V_{CC} to V_{CC}-800mV in 100mV steps.
115	TXFLT_REG3	TXFAULT_LDBIAS_CUR_TH	7:0	RW	11111111	0-255	Fault threshold for LD Bias maximum current. The fault threshold covers a range of 147mA of LD bias current in steps of 0.575mA typical.
116	TXFLT_REG4	TXFAULT_LDMOD_CUR_TH	7:0	RW	11111111	0-255	Fault threshold for LD Mod maximum current. The fault threshold covers a range of 0-100mA$_{pp}$ LD modulation current in steps of 0.4mA$_{pp}$ typical.
117	TXFLT_REG5	TXFAULT_LD_IPHOTO_TH	7:0	RW	11111111	0-255	Fault threshold for APC IPHOTO maximum voltage.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
118	TXFLT_REG6	RSVD	7:6	—	0	0-3	Reserved – do not change.
		TXFAULT_MUTE_EN	5:5	RW	0	0-1	When HIGH, mutes fault output, faults reported through register status only.
		TXDISABLE_TO_CLEAR_FAULT	4:4	RW	0	0-1	When HIGH, TxDSBL clears faults.
		RSVD	3:0	—	1111	0-15	Reserved – do not change.
119	TXFLT_REG7	RSVD	7:7	—	0	0-1	Reserved – do not change.
		TXFAULT_MODNR	6:6	RO	0	0-1	Reflects the status of the MODNR pin due to TxFault. It can be used to identify the source of the MODNR assertion.
		RSVD	5:5	—	0	0-1	Reserved – do not change.
		TXFAULT_DRV_DISABLE	4:4	RO	0	0-1	Fault status of TxDisable. When HIGH, there is a fault condition.
		TXFAULT_LD_IPHOTO	3:3	RO	0	0-1	Fault status of IPHOTO. When HIGH, there is a fault condition.
		TXFAULT_LDMOD_CUR	2:2	RO	0	0-1	Fault status of LD Mod Current. When HIGH, there is a fault condition.
		TXFAULT_LDBIAS_CUR	1:1	RO	0	0-1	Fault status of LD Bias Current. When HIGH, there is a fault condition.
		TXFAULT_LDBIAS_V	0:0	RO	0	0-1	Fault status of the LD Bias Voltage node. When HIGH, there is a fault condition.
120	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
121	ADC_REG0	RSVD	7:4	—	0	0-15	Reserved – do not change.
		ADC_AUTO_CALIBRATION_EN	3:3	RW	1	0-1	1 = Enables Auto ADC Calibration mode 0 = Disables Auto ADC Calibration mode
		ADC_JUST_LSB	2:2	RW	1	0-1	When HIGH, justify towards LSB. When LOW justify towards MSB.
		ADC_AUTO_CONV_EN	1:1	RW	1	0-1	When HIGH, enables auto conversion, set LOW for manual.
		ADC_RESET	0:0	RW	1	0-1	Reset for the ADC.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
		RSVD	7:4	—	0	0-15	Reserved – do not change.
122	ADC_REG1	ADC_SRC_SEL	3:0	RW	0	0-15	Selects ADC source used for measurement: 0000 = ADC reference voltage 0001 = Laser driver bias monitor 0010 = Photo diode voltage at IPHOTO 0011 = Laser driver modulation monitor 0100 = Temperature sensor (vbe@255µA) 0101 = Temperature sensor (vbe@2.55µA) 0110 = V3p3 supply (0.75*v3p3) 0111 = V1p8 supply (0.5*v1p8)
123	ADC_REG2	RSVD	7:7	—	0	0-1	Reserved – do not change.
		ADC_CLK_RATE	6:3	RW	11	0-15	ADC clock divide ratio.
		ADC_RESOLUTION	2:0	RWC	11	0-7	ADC resolution control: 0-6 -> 4,6,8,10,12,14,16 bits.
124	ADC_REG3	RSVD	7:1	—	0	0-127	Reserved – do not change.
		ADC_START_CONV	0:0	RWC	0	0-1	ADC start conversion.
125	ADC_REG4	RSVD	7:1	—	0	0-127	Reserved – do not change.
		ADC_DONE_CONV	0:0	RO	0	0-1	ADC conversion done flag.
126	ADC_REG5	ADC_OUT_LO	7:0	RO	0	0-255	ADC output low MSB.
127	ADC_REG6	ADC_OUT_HI	7:0	RO	0	0-255	ADC output high MSB.
128	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
129	RSVD_REG	RSVD	7:0	—	0	0-255	Reserved – do not change.
130	TXPWRDN_REG1	RSVD	7:3	—	00000	0-31	Reserved – do not change.
		TX_PD_TXSDO	2:2	RW	0	0-1	When HIGH, power-down for the entire laser driver.
		TX_PD_TXCDR	1:1	RW	0	0-1	When HIGH, power-down for the entire Tx CDR.
		TX_PD_TXPATH	0:0	RW	0	0-1	When HIGH, Power-down for the entire Tx path.
131	TXPWRDN_REG2	RSVD	7:2	—	100000	0-63	Reserved – do not change.
		TX_PD_LOS	1:1	RW	0	0-1	When HIGH, power-down for the Tx LOS.
		TX_PD_EQ	0:0	RW	0	0-1	When HIGH, power-down for the Tx input Equalizer.
132	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
133	TXPWRDN_REG4	RSVD	7:1	—	0000111	0-127	Reserved – do not change.
		TX_PD_JIT_FILT	0:0	RW	1	0-1	When HIGH, power-down for the Tx jitter filter.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
134	RXPWRDN_REG1	RSVD	7:4	—	0	0-15	Reserved – do not change.
		RX_PD_RXSDO_EMPHASIS	3:3	RW	1	0-1	When HIGH, power-down for the trace driver pre-emphasis.
		RX_PD_RXSDO	2:2	RW	0	0-1	When HIGH, power-down for the Rx path trace driver.
		RX_PD_RXCDR	1:1	RW	0	0-1	When HIGH, power-down for the entire Rx CDR.
		RX_PD_PATH	0:0	RW	0	0-1	When HIGH, power-down for the entire Rx path.
135	RXPWRDN_REG2	RSVD	7:3	—	0	0-31	Reserved – do not change.
		RX_PD_LOS	2:2	RW	0	0-1	When HIGH, power-down for the Rx path LOS.
		RX_PD_SLICE_ADJ	1:1	RW	1	0-1	When HIGH, power-down for the LA slice adjust.
		RX_PD_LA	0:0	RW	0	0-1	When HIGH, power-down for the Rx path LA.
136	RSVD_REG	RSVD	7:0	—	11111111	0-255	Reserved – do not change.
137	RXPWRDN_REG4	RSVD	7:1	—	111	0-127	Reserved – do not change.
		RX_PD_SONET_IJT	0:0	RW	0	0-1	When HIGH, powers-down the Rx path Sonet IJT feature to save power.
138	PWRDN_REG1	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PD_APC	5:5	RW	0	0-1	When HIGH, power-down for APC blocks.
		RSVD	4:4	—	1	0-1	Reserved – do not change.
		PD_TXSDO_CPA	3:3	RW	1	0-1	When HIGH, power-down for the LD crossing point adjust.
		PD_TXSDO_PHASE_ADJ	2:2	RW	1	0-1	When HIGH, power-down for the LD phase adjust (Z0) compensation.
		RSVD	1:1	—	1	0-1	Reserved – do not change.
		PD_TXSDO_PREEMPH	0:0	RW	1	0-1	When HIGH, power-down for the LD pre-emphasis.

Table 5-1: Register Descriptions (Continued)

Register Address$_d$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_b$	Valid Range$_d$	Description
139	PWRDN_REG2	RSVD	7:6	—	0	0-3	Reserved – do not change.
		PD_ADC	5:5	RW	1	0-1	When HIGH, power-down for the ADC.
		PD_SUPPLY_SENSOR	4:4	RW	1	0-1	When HIGH, power-down for the supply sensor.
		PD_TEMP_SENSOR	3:3	RW	1	0-1	When HIGH, power-down for the temperature sensor(s).
		PD_PRBS_CHK	2:2	RW	1	0-1	When HIGH, power-down for the PRBS Checker and associated buffers.
		PD_PRBS_GEN	1:1	RW	1	0-1	When HIGH, power-down for the PRBS Generator and associated buffers.
		RSVD	0:0	—	1	0-1	Reserved – do not change.
140 to 153	RSVD_REG	RSVD	All	—	0	0-255	Reserved – do not change.
154	TXLBW_REG1	RSVD	7:1	—	0	0-127	Reserved – do not change.
		TX_DYN_LBW_ENABLE	0:0	RW	1	0-1	Tx dynamic loop bandwidth block enable: 0 = disabled 1 = enabled
155	RSVD_REG	RSVD	7:0	—	00001111	0-255	Reserved – do not change.
156	RSVD_REG	RSVD	7:0	—	00000011	0-255	Reserved – do not change.
157	RSVD_REG	RSVD	7:0	—	00011111	0-255	Reserved – do not change.
158	RSVD_REG	RSVD	7:0	—	00000100	0-255	Reserved – do not change.
159	RXLBW_REG1	RSVD	7:1	—	0	0-127	Reserved – do not change.
		RX_DYN_LBW_ENABLE	0:0	RW	1	0-1	Rx dynamic loop bandwidth block enable: 0 = Disabled 1 = Enabled
160 to 221	RSVD_REG	RSVD	All	—	0	0-255	Reserved – do not change.

6. Applications Information

6.1 Typical Application Circuit

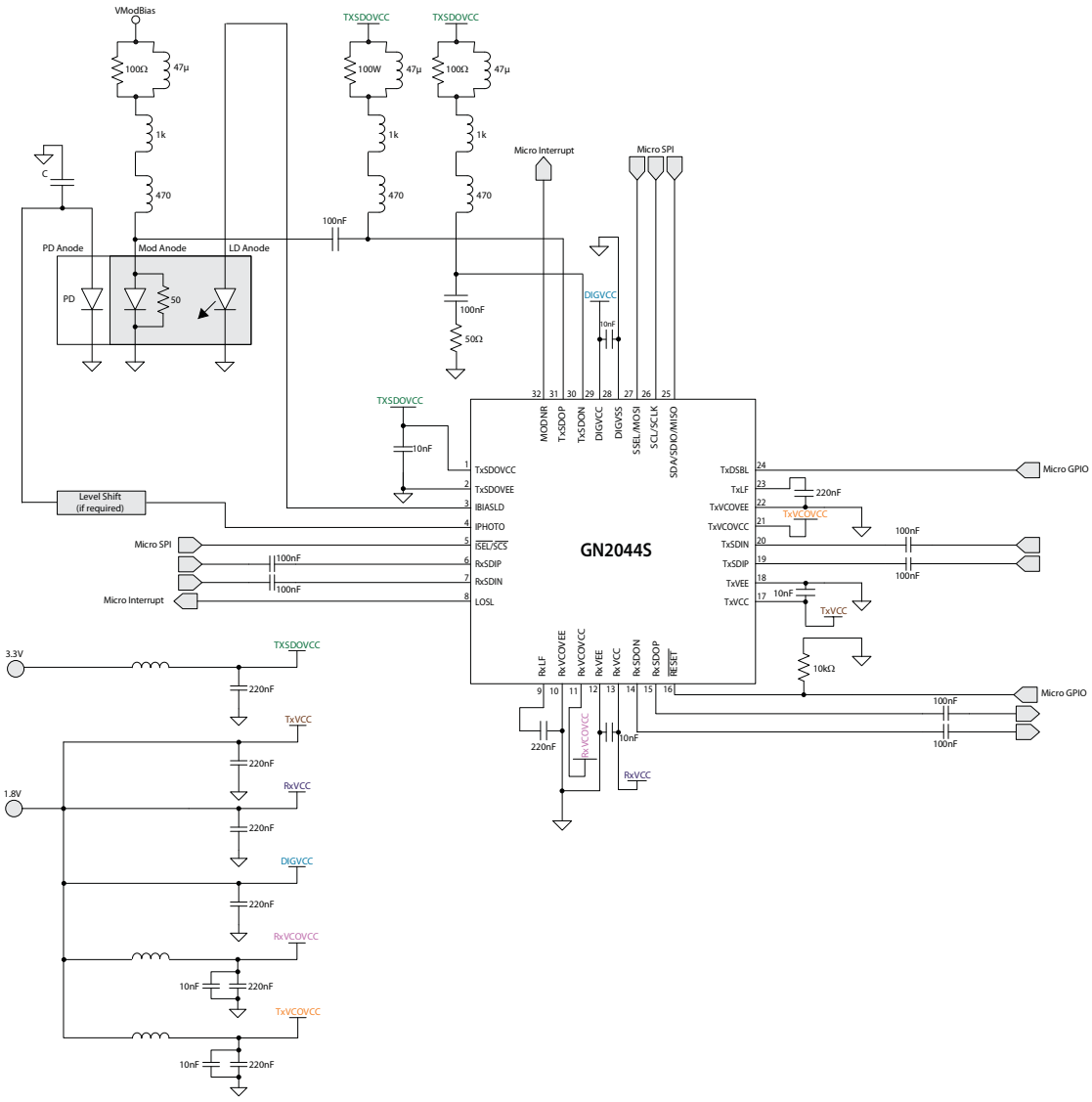


Figure 6-1: Typical Application Circuit

- Use high-quality, temperature-stable LF capacitors. For example, silicon, tantalum or C0G dielectric ceramic capacitors. Lower quality capacitors such as X7R are more sensitive to environmental conditions and may not perform adequately across conditions for this node. Silicone conformal coating can be used with such capacitors as an effective way to mitigate environmental sensitivity

  Note: Please refer to the document "Preventing Loop Filter Capacitor Leakage Current" (PDS-060519) for more information.

- Place lowest value decoupling capacitor closest to the device
- Component values for the TOSA interface must be optimized for the TOSA type
- Status indicator connections are shown for a LVCMOS/LVTTL compatible mode. These I/Os can be configured as open-drain with pull-up
- Host interface is shown configured for SPI mode. I^2C mode is also supported

6.2 Power Supply Filter Recommendations

RC filters for isolating supplies are not recommended due to the large currents drawn from each supply.

- The Tx and Rx VCOs do not have independent supplies; additional filtering for the VCOs is not required

For improved isolation between the Tx and Rx paths, and to achieve the best Rx sensitivity and Tx jitter generation, a supply filter such as the one shown in Figure 6-2 is recommended.

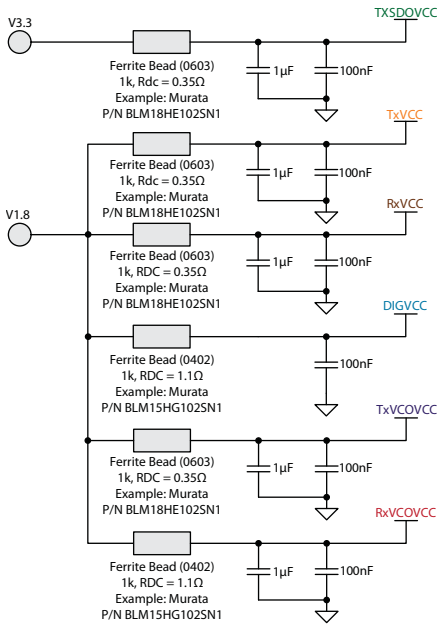


Figure 6-2: Power Supply Filter Recommendations

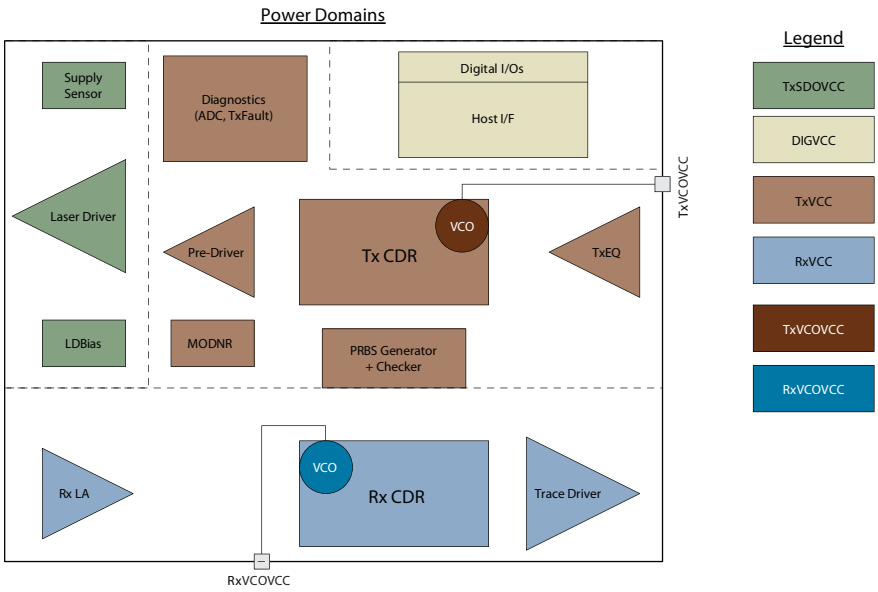


Figure 6-3: Power Supply Domains

6.3 Layout Considerations

The following high-frequency design rules should be considered to achieve optimum performance of the GN2044S:

- Use carefully designed controlled-impedance transmission lines with minimal local discontinuities for all high-speed data signals
- Place decoupling capacitors as close as possible to the supply pins
- For optimal electrical and thermal performance, the QFN's exposed pad should be soldered to the module ground plane
- It is recommended to have LF cap ground and VCO caps ground to be common with multiple stitching of vias to ground. Capacitors should be placed from smallest value to largest value away from chip. In addition, the connection from the LF pin to the capacitor should be as small as possible with no vias. Figure 6-4 below demonstrates this technique:

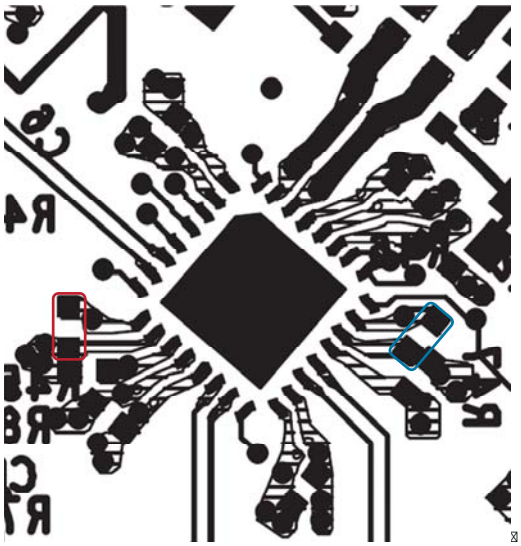


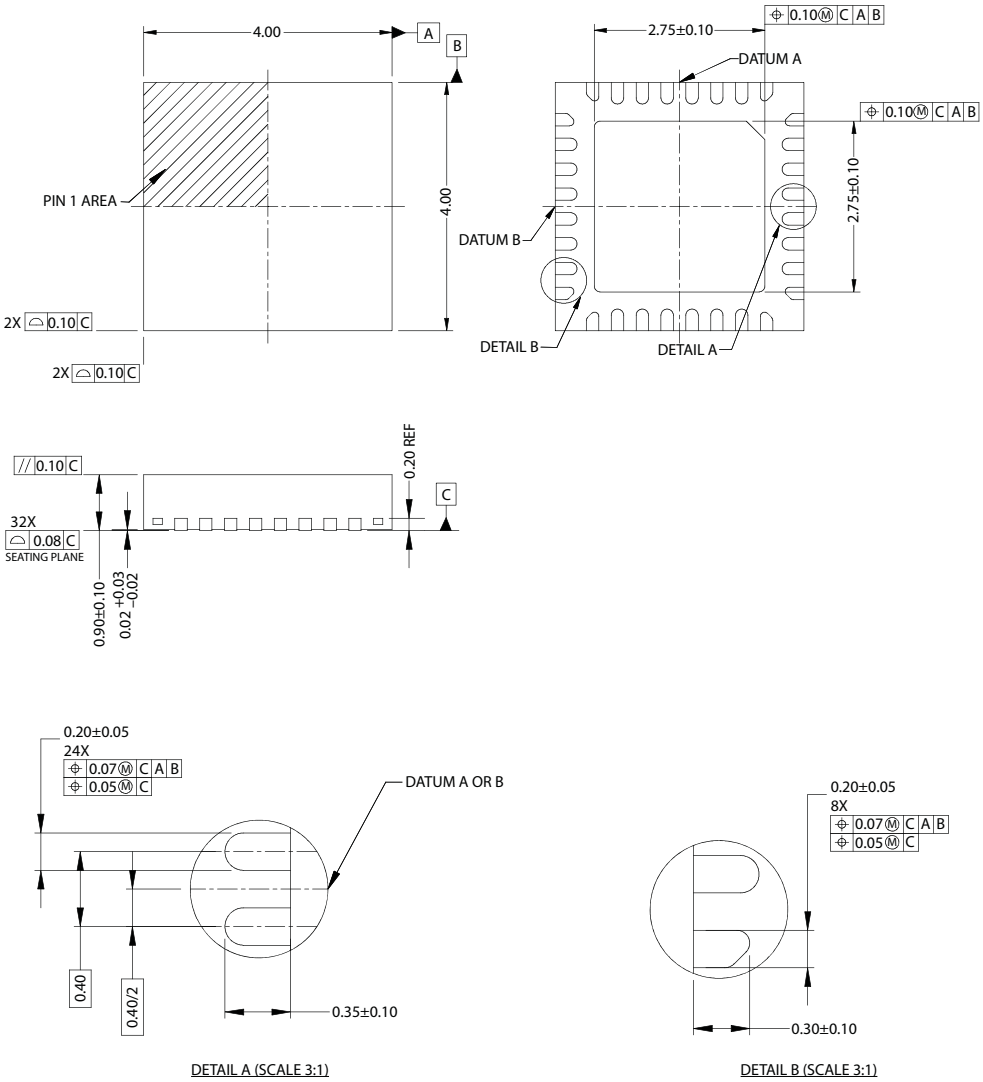
Figure 6-4: Loop Filter Capacitor PCB Layout

- All supply decoupling capacitors should have multiple vias to ground/power planes, and placed as close to chip as possible
- All supplies/grounds should be routed to corresponding decoupling capacitors pads, and never to the centre pad
- The recommended PCB layout for the GN2044S device is shown in Figure 7-2
- Use high-quality, temperature-stable LF capacitors (i.e. capacitors connected to pins 9 and 23). For example: X7R or C0G dielectrics for ceramic capacitors. Lower-quality capacitors with smaller package sizes (e.g. 0201) are more sensitive to environmental conditions and may not perform adequately across conditions for this node. Silicone conformal coating is also an effective way to mitigate environmental sensitivity

7. Package and Ordering Information

7.1 Package Dimensions

The GN2044S is a 4mm x 4mm, 32-pin QFN.



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994.
   ALL DIMENSIONS ARE IN MILLIMETERS, ° IN DEGREES.

2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint

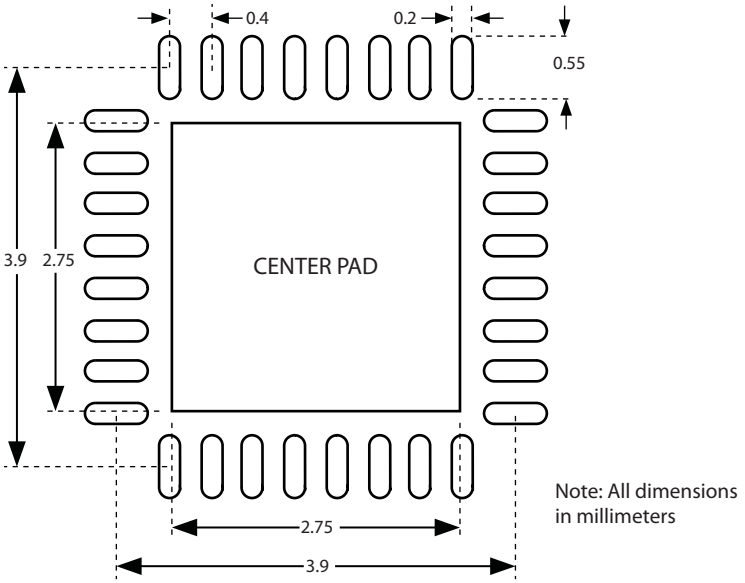


Figure 7-2: Recommended PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	32-pin QFN / 4mm x 4mm / 0.4mm pad pitch
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	29.8°C/W
Junction to Air Thermal Resistance (at zero airflow), θ_{j-a}	35.4°C/W
Psi = Junction-to-Top (of Package) Characterization Parameter, Ψ	0.3°C/W
Pb-free and RoHS compliant	Yes

7.4 Solder Reflow Profile

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 7-3.

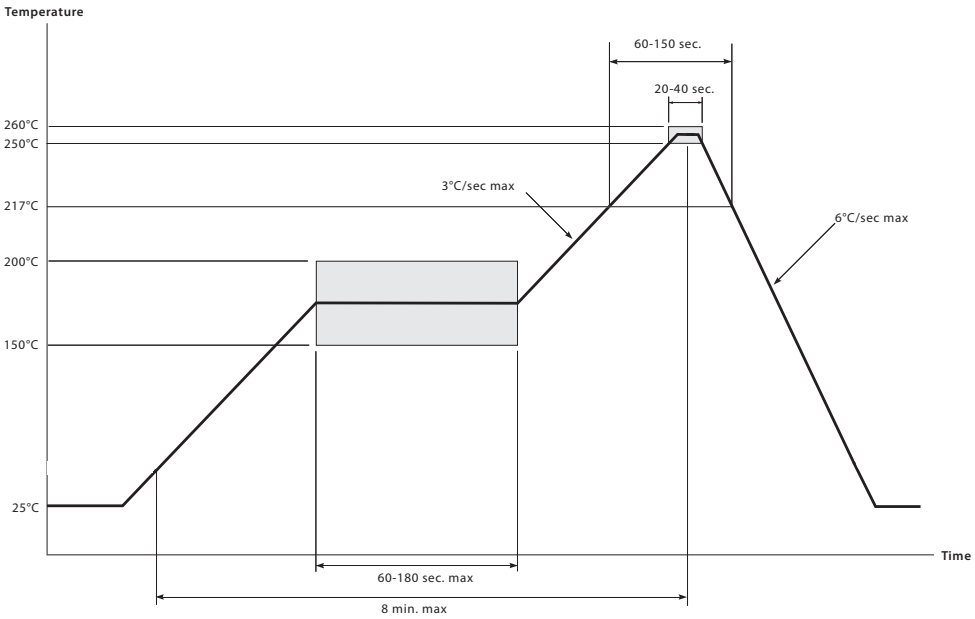


Figure 7-3: Maximum Pb-free Solder Reflow Profile

7.5 Marking Diagram

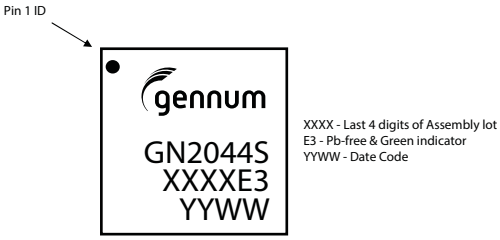


Figure 7-4: Marking Diagram

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Package	Case Temperature Range
GN2044SINE3	32-pin QFN	-40°C to +100°C
GN2044SINTE3D	32-pin QFN (500pc tape and reel)	-40°C to +100°C

DOCUMENT IDENTIFICATION
FINAL DATA SHEET
The product is in production. Semtech reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com