ON Semiconductor®

Product Bulletin

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Title of Change:	AR1820HS Datasheet Update.
Effective date:	27 December 2017
Contact information:	Contact your local ON Semiconductor Sales Office or <Sonya.Yip@onsemi.com>
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change category:	☐ Wafer Fab Change ☐ Assembly Change ☐ Test Change ☒ Other Documentation

Change Sub-Category(s):

☐ Manufacturing Site Change/Addition
☐ Manufacturing Process Change
☐ Material Change
☐ Product specific change
☒ Datasheet/Product Doc change
☐ Shipping/Packaging/Marking
☐ Other: _____

Sites Affected:	ON Semiconductor Sites: None	External Foundry/Subcon Sites: None

Description and Purpose:

AR1820HS Datasheet was updated to correct documentation errors. The changes will not impact die, package, or function of products.

AR1820HS Datasheet Changes

1. Updated "Table 2, Available Part Numbers" (Previously Table 4)

Old Table :

Table 4: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
AR1820HSSC00SHEA0-DR	RGB, 0deg CRA, IBGA Package	Drypack
AR1820HSSC12SHEA0-DR	RGB, 12deg CRA, IBGA Package	Drypack
AR1820HSSC00SHEA0	RGB, 0deg CRA, IBGA Package	Drypack and Protective Film
AR1820HSSC12SMD20	RGB, 12deg CRA, Recon Die	
AR1820HSSC31SMD20	RGB, 31deg CRA, Recon Die	
AR1820HSSC00SHQAD3-GEVK	0deg CRA	Demo Kit
AR1820HSSC00SHQAH3-GEVB	0deg CRA	Head Board
AR1820HSSC12SHQAD3-GEVK	12deg CRA	Demo Kit
AR1820HSSC12SHQAH3-GEVB	12deg CRA	Head Board
AR1820HSSC31SMEAD3-GEVK	31deg CRA	Demo Kit
AR1820HSSC31SMEAH3-GEVB	31deg CRA	Head Board

Note: Orderable iBGA options support both HiSPi and MIPI interface.
See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

New Table 2:

Table 2. ORDERING INFORMATION

Part Number	Product Description	Orderable Product Attribute Description
AR1820HSSC00SHEA0−DR	RGB, 0deg CRA, iBGA Package	Drypack without Protective Film
AR1820HSSC12SHEA0−DR	RGB, 12deg CRA, iBGA Package	Drypack without Protective Film
AR1820HSSC12SHEA0−DP	RGB, 12deg CRA, iBGA package	Drypack with protective film
AR1820HSSC00SHEA0−DP	RGB, 0deg CRA, iBGA Package	Drypack and Protective Film
AR1820HSSC12SMD20	RGB, 12deg CRA, Recon Die	
AR1820HSSC31SMD20	RGB, 31deg CRA, Recon Die	
AR1820HSSC00SHQAH3−GEVB	0deg CRA	Head Board
AR1820HSSC12SHQAH3−GEVB	12deg CRA	Head Board
AR1820HSSC31SMEAH3−GEVB	31deg CRA	Head Board

NOTE: Orderable iBGA options support both HiSPi and MIPI interface.
See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

2. In "Register Notation" section, changed "For example, R0x3024 is a 2-bit register… to "For example, R0x3024 is a 8-bit register…

Old Description:

are described by address, the size of the registers is explicit. For example, R0x3024 is a 2-bit register at address 0x3024, and R0x3000–1 is a 16-bit register at address 0x3000–0x3001. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that model_id is a 16-bit register.

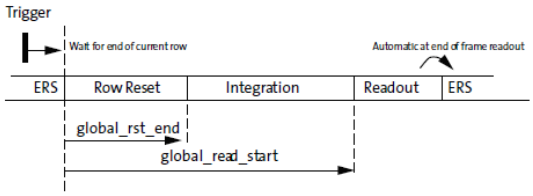
New Description:

size of the registers is explicit. For example, R0x3024 is a 8–bit register at address 0x3024, and R0x3000–1 is a 16–bit register at address 0x3000–0x3001. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that model_id is a 16–bit register.

3. Updated Figure 39 (Previously Figure 40). Global_read_start begins after global_rst_end.

Old Figure 40 :

Figure 40: Controlling the Reset and Integration Phases of the Global Reset Sequence



New Figure 39

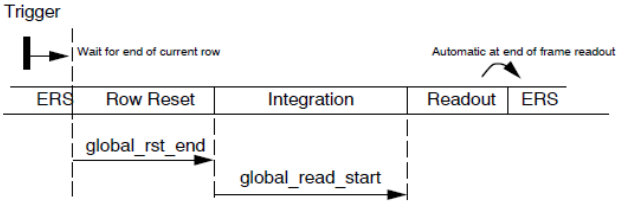
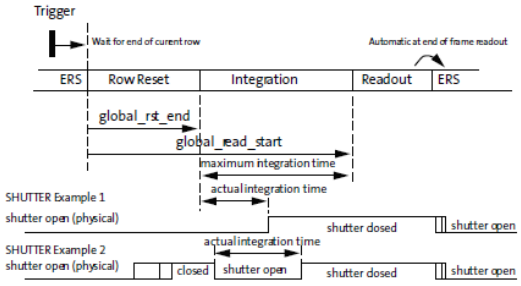


Figure 39. Controlling the Reset and Integration Phases of the Global Reset Sequence

4. Updated Figure 40 (Previous Figure 41) by shifting global_shutter_start to align with global_read_start.

Old Figure 41:

Figure 41: Control of the Electromechanical Shutter



New Figure 40:

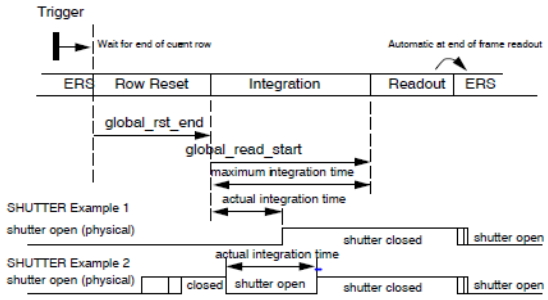
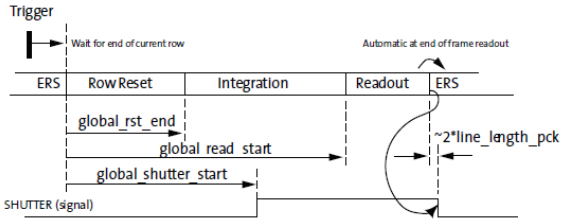


Figure 40. Control of the Electromechanical Shutter

5. Updated Figure 41 (Previously Figure 42)

Old Figure 42:

Figure 42: Controlling the SHUTTER Output



New Figure 41 :

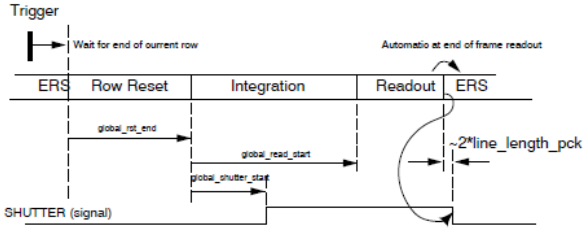
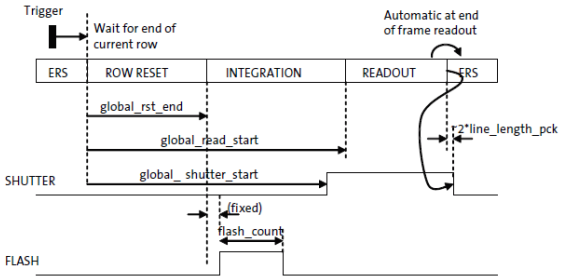


Figure 41. Controlling the SHUTTER Output

6. Updated Figure 42 (Previously Figure 43):

Old Figure 43:

Figure 43: Using FLASH with Global Reset



New Figure 42 :

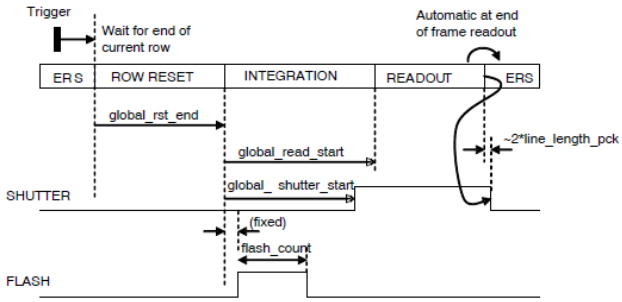
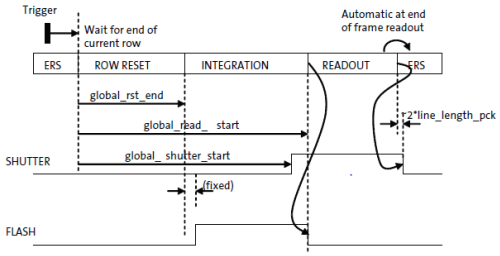


Figure 42. Using FLASH with Global Reset

7. Updated Figure 43 (Previously Figure 44):

Old Figure 44:

Figure 44: Extending FLASH Duration in Global Reset (Reference Readout Start)



New Figure 43:

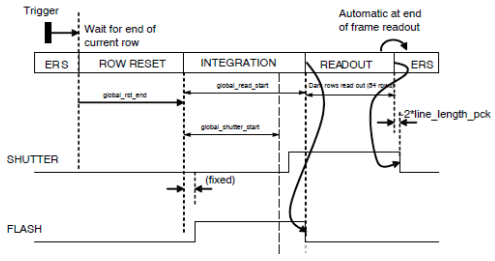


Figure 43. Extending FLASH Duration in Global Reset (Reference Readout Start)

8. Updated Equation 12

Old Equation 12:

The integration time of the GRR sequence is defined as:

$$integration\_time = \frac{global\_scale \times [global\_read\_start - global\_shutter\_start - global\_rst\_end]}{(vt\_pix\_clk\_freq\_mhz \times 10^6)} \quad \text{(EQ 12)}$$

New Equation 12:

The integration time of the GRR sequence when a mechanical shutter is in place is defined as:

$$Tint = Global\_Shutter\_Start \times Global\_Scale/clk\_pix \quad \text{(eq. 12)}$$

9. Added new equation 13

New Equation 13:

The integration time of the GRR sequence when no mechanical shutter is in place is defined as:

$$Tint\ (for\ row\ 0) = [(Global\_Read\_Start \times Global\_Scale)/(Global\_Scale)] + (N \times line\_length\_pck/4/clk\_pix) \quad \text{(eq. 13)}$$

Typically N is 54.
clk_pix is defined in Equation 2 on Page 78. The maximum allowed clk_pix frequency is 133.33 MHz.

10. Removed Continuous GRR section

Old Section:

Continuous GRR Mode

AR1820HS also features continuous GRR capturing.

- Unlike previous part (for example, A-14041), after GRR frame readout completed, sensor will automatically go back to ERS mode.
- AR1820HS has an option of keeping sensor staying at GRR mode operation.
- This feature is controlled by programming R0x3158[12]:
  - R0x3158[12] is frame sync controlled.
  - The sensor will remain at GRR mode if R0x3158[12] stays at high.
  - When R0x3158[12] being pulled down, sensor will go back to ERS mode after end of current GRR frame.

11. Added "In slave mode, R0x315E[0] needs to be set to 1 to operate in ERS mode" to "Slave Mode Section"

Old Section:

If the slave mode is disabled, the new frame will begin after the extra delay period is finished.

The slave mode will react to the rising edge of the input VD signal if it is in an active state. When the VD signal is received, the sensor will begin the frame readout and the slave mode will remain inactive for the period of one frame time minus 16 clock periods (T_{FRAME} - (16 / CLK_PIX)). After this period, the slave mode will re-enter the active state and will respond to the VD signal.

New Section:

If the slave mode is disabled, the new frame will begin after the extra delay period is finished.

The slave mode will react to the rising edge of the input VD signal if it is in an active state. When the VD signal is received, the sensor will begin the frame readout and the slave mode will remain inactive for the period of one frame time minus 16 clock periods (T_{FRAME} – (16 / CLK_PIX)). After this period, the slave mode will re–enter the active state and will respond to the VD signal. In slave mode, R0x315E[0] needs to be set to 1 to operate in ERS mode.

12. Removed Slave Mode GRR section

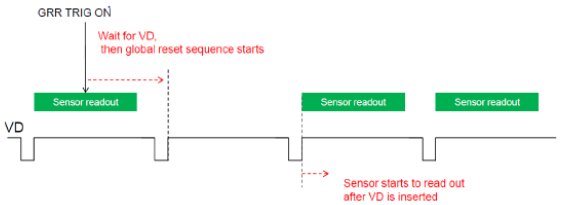
Old Section:

Slave Mode GRR

Global reset sequence is triggered by programming the global_seq_trigger bit. After this register bit is written the sensor will wait for rising edge of VD signal at the end of the current frame to go into GRR mode. The control bit needed to be set to enable this functionality is vd_trigger_grst. Once in the GRR integration phase, the sensor will wait for the next VD rising edge to begin the readout.

At the end of the readout phase, the sensor automatically resumes operation in ERS mode with readout of successive frames starting with rising edge of VD. Figure 48 and Figure 49 on page 63 are related timing diagrams:

Figure 47: Slave Mode ERS-GRR Transition



Slave Mode GRR Timing

For example, to switch between ERS and GRR (and back to ERS), see Figure 48:

Figure 48: Slave Mode GRR Timing

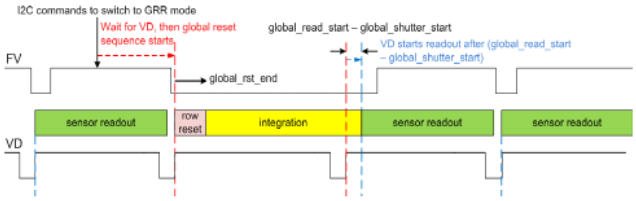
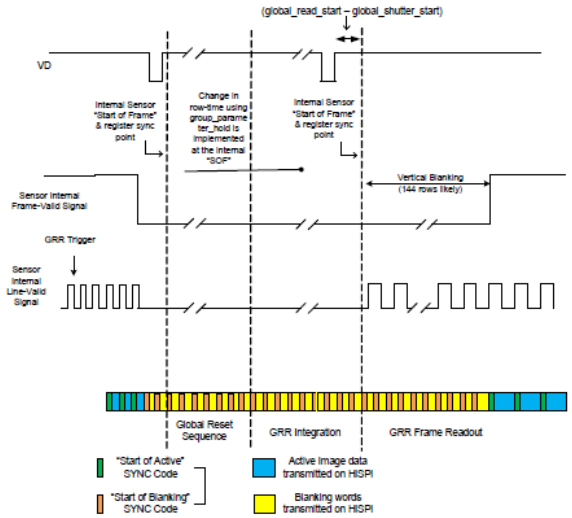


Figure 49: Slave Mode HISPI Output (ERS to GRR Transition)



When GRR is triggered (by the rising edge of VD signal), the AR1820HS sensor starts GRR sequence and also send a start-of-blanking (SOB) SYNC code at the end of current ERS frame. It continues to send SOB sync codes during the entire GRR sequence.

13. Removed all Three- Wire Serial Interface Information

Old Section:

Three-wire Serial Interface		
CS_BAR	Input	CS_BAR = 0 to enable 3-wire interface
CS_EN	Input	CSI_EN should be "1" to enable 3-wire interface.

Three-Wire Serial Interface

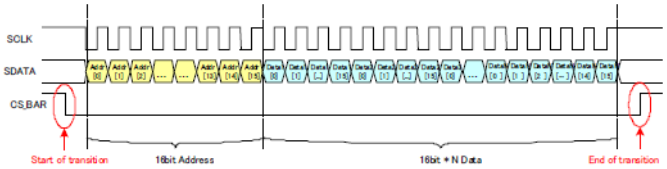
The three-wire interface is designed to allow higher speed host register writes. The maximum operation frequency for the three-wire interface is 10 MHz.

CS_BAR is used to enable the three-wire interface when CS_BAR = 0.

CSI_EN should be "1" to enable full speed for the three-wire interface.

The three-wire interface supports register writes only, no register reads; register read is supported by I^2C.

Figure 16: Timing Diagram for Three-Wire Serial Interface



The CS_BAR signal is the indicator that the three-wire interface is being used, so, during CS_BAR = 0, SDATA and SCLK input for I^2C logic is disabled

1080p120 fps. The AR1820HS sensor is programmabl through a simple two−wire serial (or new 3−wire) interfac and has very low power consumption.

14. Replaced Table 21 with new gain table

Old Table 21:

Table 21: Total Gain Setting Summary for Native Mode

Target Gain	R0x305E				R0x3ED2	R0x3040		R0x3EE0				R0x3EC8	R0x3EDC	R0x3ED8	R0x3ECC	R0x3F1A	R0x3F44
	Fine Gain		Digital Gain														
	[6:3]	Gain Value	[15:7]	Gain Value	[15:12]	[13]	[11]	[0]	[1]	[15]	[6]	[7:4]	[0]	[4]	[11:8]	[15:0]	[15:0]
1	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
1.03	1	1.0322581	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
...	...	...	...	...	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
1.88	15	1.8823529	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
2	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
2.06	1	1.0322581	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
...	...	...	...	...	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
3.94	15	1.8823529	67	1.046875	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
4	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
4.13	1	1.0322581	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
...	...	...	...	...	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
7.88	15	1.8823529	67	1.046875	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
8	0	1	64	1	4	0	0	0	0	0	1	7	1	0	5	0x1E1E	0x0708
8.13	0	1	65	1.015625	4	0	0	0	0	0	1	7	1	0	5	0x1E1E	0x0708
...	0	1	...	...	4	0	0	0	0	0	1	7	1	0	5	0x1E1E	0x0708
15.5	0	1	124	1.9375	4	0	0	0	0	0	1	7	1	0	5	0x1E1E	0x0708
16	0	1	128	2	4	0	0	0	0	0	1	7	1	0	5	0x1919	0x0708

Note: R0x3040 will be changed during Mode switch.

New Table 21:

Table 21. TOTAL GAIN SETTING SUMMARY FOR NATIVE MODE

Target Gain	R0x305E				R0x3ED2	R0x3040		R0x3EE0				R0x3EC8	R0x3EDC	R0x3ED8	R0x3ECC	R0x3F1A	R0x3F44	0x3ED0	0x3EE6
	Fine Gain		Digital Gain																
	[6:3]	Gain Value	[15:7]	Gain Value	[15:12]	[13]	[11]	[0]	[1]	[15]	[6]	[7:4]	[0]	[4]	[11:8]	[15:0]	15:0]		
1	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x00FF	0xF87A
1.03	1	1.0322581	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x00FF	0xF87A
...	...	...	...	...	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x00FF	0xF87A
1.88	15	1.8823529	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x00FF	0xF87A
2	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x005F	0xF87A
2.06	1	1.0322581	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x005F	0xF87A
...	...	...	...	...	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x005F	0xF87A
3.94	15	1.8823529	67	1.046875	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x005F	0xF87A
4	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x005F	0xB87A
4.13	1	1.0322581	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x005F	0xB87A
...	...	...	...	...	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x005F	0xB87A
7.88	15	1.8823529	67	1.046875	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C	0x005F	0xB87A
8	0	1	64	1	4	0	0	0	0	0	1	7	1	0	5	0x1E1E	0x0708	0x005F	0xB87A
8.13	0	1	65	1.015625	4	0	0	0	0	0	1	7	1	0	5	0x1E1E	0x0708	0x005F	0xB87A
...	0	1	...	...	4	0	0	0	0	0	1	7	1	0	5	0x1E1E	0x0708	0x005F	0xB87A
15.5	0	1	124	1.9375	4	0	0	0	0	0	1	7	1	0	5	0x1E1E	0x0708	0x005F	0xB87A
16	0	1	128	2	4	0	0	0	0	0	1	7	1	0	5	0x1919	0x0708		

15. Replaced Table 22 with new gain table

Old Table 22:

Table 22: Total Gain Setting Summary for Subsampling

		R305E						R0x3ED2	R0x3040		R0x3EE0				R0x 3EC8	R0x 3EDC	R0x 3ED8	R0x 3ECC	R0x 3F1A	R0x 3F44
		Coarse Gain		Fine Gain		Digital Gain														
Target Gain	Hex	305E [2:0]	Gain Value	305E [6:3]	Gain Value	305E [15:7]	Gain Value	[15:12]	[13]	[14]	[0]	[1]	[15]	[6]	[7:4]	[0]	[4]	[11:8]	[15:0]	[15:0]
2	2081	1	0.705	0	1	91	1.421875	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0C0C
2.07	2F01	1	0.705	0	1	94	1.46875	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0C0C
...	...	1	1	...	...	...	...	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0C0C
3.75	5501	1	0.705	0	1	100	170	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0C0C
4	2002	2	2	0	1	64	1	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
4.13	200A	2	2	1	1.0322581	64	1	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
...	...	2	2	...	...	...	...	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
7.88	21FA	2	2	15	1.8823529	67	1.046875	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
8	2003	3	4	0	1	64	1	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
8.13	2183	3	4	0	1	67	1.046875	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x1010
...	...	3	4	...	...	...	...	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x1010
15.5	3E03	3	4	0	1	124	1.9375	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x1010
16	2004	4	8	0	1	64	1	4	1	1	0	0	0	1	7	0	0	3	0x0504	0x0101
16.75	2184	4	8	0	1	67	1.04687	4	1	1	0	0	0	1	7	0	0	3	0x0504	0x0101
...	...	4	8	0	1	...	...	4	1	1	0	0	0	1	7	0	0	3	0x0504	0x0101
31	3E04	4	8	0	1	124	1.9375	4	1	1	0	0	0	1	7	0	0	3	0x0504	0x0101
32	4004	4	8	0	1	128	2	4	1	1	0	0	0	1	7	0	0	3	0x0609	0x0101

Note: R0x3040 will be changed during Mode switch.

New Table 22:

Table 22. TOTAL GAIN SETTING SUMMARY FOR SUBSAMPLING

		R305E						R0x 3ED2	R0x3040		R0x3EE0				R0x 3EC8	R0x 3EDC	R0x 3ED8	R0x 3ECC	R0x 3F1A	R0x3F44	0x 3ED0	0x3EE6
		Coarse Gain		Fine Gain		Digital Gain																
Target Gain	Hex	305E [2:0]	Gain Value	305E [6:3]	Gain Value	305E [15:7]	Gain Value	[15:12]	[13]	[11]	[0]	[1]	[15]	[6]	[7:4]	[0]	[4]	[11:8]	[15:0]	[15:0]	[15:0]	[15:0]
2	2081	1	0.705	0	1	91	1.421875	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0101	0x00FF	0xF87A
2.07	2F01	1	0.705	0	1	94	1.46875	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0101	0x00FF	0xF87A
...	...	1	1	...	...	...	...	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0101	0x00FF	0xF87A
3.75	5501	1	0.705	0	1	170	2.65625	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0101	0x00FF	0xF87A
4	2002	2	2	0	1	64	1	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0101	0x005F	0xF87A
4.13	200A	2	2	1	1.0322581	64	1	4	1	1	0	0	0	1	7	1	0	7	0x0404	0x0101	0x005F	0xF87A
...	...	2	2	...	...	...	...	4	1	1	0	0	0	1	7	1	0	7	0x0404	0x0101	0x005F	0xF87A
7.88	21FA	2	2	15	1.8823529	67	1.046875	4	1	1	0	0	0	1	7	1	0	7	0x0404	0x0101	0x005F	0xF87A
8	2003	3	4	0	1	64	1	4	1	1	0	0	0	1	7	1	0	7	0x0404	0x0101	0x005F	0xB87A
8.13	2183	3	4	0	1	67	1.046875	4	1	1	0	0	0	1	7	1	0	7	0x0404	0x0101	0x005F	0xB87A
...	...	3	4	...	...	...	...	4	1	1	0	0	0	1	7	1	0	7	0x0404	0x0101	0x005F	0xB87A
15.53	217B	3	4	15	1.8823529	67	1.046875	4	1	1	0	0	0	1	7	1	0	7	0x0404	0x0101	0x005F	0xB87A
16	2004	4	8	0	1	64	1	4	1	1	0	0	0	1	7	0	0	7	0x0504	0x0101	0x005F	0xB87A
16.75	2184	4	8	0	1	67	1.04687	4	1	1	0	0	0	1	7	0	0	7	0x0504	0x0101	0x005F	0xB87A
...	...	4	8	0	1	...	...	4	1	1	0	0	0	1	7	0	0	7	0x0504	0x0101	0x005F	0xB87A
31	3E04	4	8	0	1	124	1.9375	4	1	1	0	0	0	1	7	0	0	7	0x0504	0x0101	0x005F	0xB87A
32	4004	4	8	0	1	128	2	4	1	1	0	0	0	1	7	0	0	7	0x0607	0x0101	0x005F	0xB87A

NOTE: R0x3040 will be changed during Mode switch.

16. Replaced Table 23 with new gain table

Old Table 23:

Table 23: Summary Native Gain

Gain Name for Native Mode	R0x305E	R0x3ED2	R0x3EE0	R 0x3EDC	R 0x3EC8	R0X3ED8	R0X3ECC	R0x3F1A	R0x3F44
1	2001	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.07	2011	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.14	2021	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.23	2031	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.33	2041	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.45	2051	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.6	2061	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.78	2071	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.88	2079	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2	2002	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.06	200A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.13	2012	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.21	201A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.29	2022	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.37	202A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.46	2032	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.56	203A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.67	2042	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.78	204A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.91	2052	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3	2152	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.1	20DA	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.2	2062	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.37	206A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.56	2072	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.76	207A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.82	20FA	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.94	21FA	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
4	2003	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C

New Table 23:

Table 23. SUMMARY NATIVE GAIN

Gain Name for Native Mode	R0x305E	R0x3ED2	R0x3EE0	R0x3EDC	R0x3EC8	R0X3ED8	R0X3ECC	R0x3F1A	R0x3F44	0x3ED0	0x3EE6
1	2001	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x00FF	0xF87A
1.07	2011	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x00FF	0xF87A
1.14	2021	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x00FF	0xF87A
1.23	2031	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x00FF	0xF87A
1.33	2041	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x00FF	0xF87A
1.45	2051	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x00FF	0xF87A
1.6	2061	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x00FF	0xF87A
1.78	2071	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x00FF	0xF87A
1.88	2079	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x00FF	0xF87A
2	2002	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.06	200A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.13	2012	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.21	201A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.29	2022	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.37	202A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.46	2032	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.56	203A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.67	2042	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.78	204A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
2.91	2052	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
3	2152	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
3.1	20DA	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
3.2	2062	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
3.37	206A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
3.56	2072	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
3.76	207A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
3.82	20FA	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
3.94	21FA	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xF87A
4	2003	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C	0x005F	0xB87A

17. Replaced Table 24 with new gain table

Old Table 24:

Table 24: Summary Subsampling Gain

Gain Name for Subsampling Mode	R0x305E	R0X3ED2	R 0x3EE0	R0x3EDC	R 0x3EC8	R0X3ED8	R0X3ECC	R0x3F1A	R0x3F44
2	2D81	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
2.07	2F01	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
2.45	3781	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
2.71	3D81	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
3.00	4401	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
3.24	4981	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
3.48	4F01	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
3.75	5501	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
4	2002	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.13	200A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.27	2012	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.41	201A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.57	2022	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.74	202A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
5	20B2	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101

New Table 24:

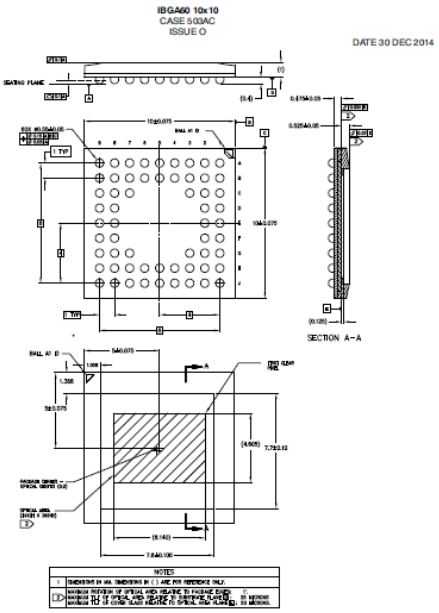
Table 24. SUMMARY SUBSAMPLING GAIN

Gain Name for Subsampling Mode	R0x305E	R0X3ED2	R0x3EE0	R0x3EDC	R0x3EC8	R0X3ED8	R0X3ECC	R0x3F1A	R0x3F44	0x3ED0	0x3EE6
2	2D81	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101	0x00FF	0xF87A
2.07	2F01	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101	0x00FF	0xF87A
2.45	3781	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101	0x00FF	0xF87A
2.71	3D81	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101	0x00FF	0xF87A
3.00	4401	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101	0x00FF	0xF87A
3.24	4981	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101	0x00FF	0xF87A
3.48	4F01	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101	0x00FF	0xF87A
3.75	5501	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101	0x00FF	0xF87A
4	2002	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101	0x005F	0xF87A
4.13	200A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101	0x005F	0xF87A
4.27	2012	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101	0x005F	0xF87A
4.41	201A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101	0x005F	0xF87A
4.57	2022	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101	0x005F	0xF87A
4.74	202A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101	0x005F	0xF87A
5	20B2	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101	0x005F	0xF87A

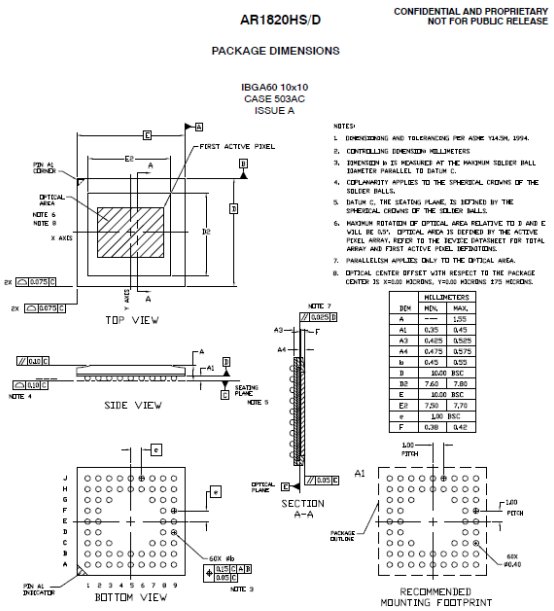
18. Changed package drawing to official ON Semiconductor Case outline

Old Package Drawing:

Figure 67: Package Diagram



New Package Drawing:



List of Affected Parts:
AR1820HSSC00SHEA0-DP1
AR1820HSSC00SHEA0-DR
AR1820HSSC12SHEA0-DP
AR1820HSSC12SHEA0-DR
AR1820HSSC12SHEA0-DR1
AR1820HSSC12SMD20
AR1820HSSC31SMD20

Appendix A: Changed Products

Product	Customer Part Number
AR1820HSSC00SHEA0-DP1	
AR1820HSSC00SHEA0-DR	
AR1820HSSC12SHEA0-DP	
AR1820HSSC12SHEA0-DR	
AR1820HSSC12SHEA0-DR1	