ES_LPC11U1x

Errata sheet LPC11U1x

Rev. 3.1 — 30 September 2013 **Errata sheet**

Document information

Info	Content
Keywords	LPC11U12FHN33, LPC11U12FBD48, LPC11U13FBD48, LPC11U14FHN33, LPC11U14FHI33, LPC11U14FBD48, LPC11U14FET48, LPC11U1x errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
3.1	20130930	• Added Note.2.
3	20130117	• Added I2C.1.
2.1	20121002	• Added Rev A to Note.1.
2	20120112	• Added Rev B. • Added ADC.1.
1.2	20110901	• Added Note.1.
1.1	20110622	• Section 3.4: Corrected device name.
1	20110601	• Initial version.

Contact information

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1. Product identification

The LPC11U1x devices typically have the following top-side marking:

LPC11U1x

/xxx

xxxxxxx

xxYYWWxR[x]

The last letter in the last line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC11U1x:

Table 1. Device revision table

Revision identifier (R)	Revision description
‘A’	Initial device revision
‘B’	Second device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

2. Errata overview

Table 2. Errata summary table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	A/D Global Data register should not be used with burst mode or hardware triggering.	‘A’, ‘B’	Section 3.1
I2C.1	In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register.	‘A’, ‘B’	Section 3.2
IRC.1	Accuracy of the Internal RC oscillator (IRC) frequency may be outside of the 12 MHz ± 1 % specification.	‘A’	Section 3.3
USART.1	‘False positive’ break indicator events may occur.	‘A’	Section 3.4
USART.2	SCI Transmit retry error interrupt not working.	‘A’	Section 3.5
USB.1	The VBUSDEBOUNCED status bit is not updated correctly.	‘A’	Section 3.6

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
Note.1	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.	'A', 'B'	Section 5.1
Note.2	Depending on bootloader version, pin(s) PIO0_1 or PIO0_1 and PIO0_3 must be pulled LOW to enter UART ISP mode.	'A', 'B'	Section 5.2

3. Functional problems detail

3.1 ADC.1: A/D Global Data register should not be used with burst mode or hardware triggering

Introduction:

On the LPC11U1x, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

3.2 I2C.1: In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register

Introduction:

The I2C monitor allows the device to monitor the I2C traffic on the I2C bus in a non-intrusive way.

Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I2C bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1); //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:     // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:     // data byte in DAT transmitted, ACK received
case 0xC0:     // (last) data byte transmitted, NACK received
case 0xC8:     // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER;//Save data. Data can be process in Main loop
    LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

3.3 IRC.1: Accuracy of the IRC frequency may be outside of the 12 MHz ± 1 % specification

Introduction:

The LPC11U1x has three independent oscillators: the system oscillator, the Internal RC oscillator (IRC), and the Watchdog oscillator. The IRC can be optionally used as a clock source for the CPU, the system PLL, and the peripherals blocks. The IRC frequency spec is 12 MHz ± 1 % accuracy over the entire voltage and temperature range. During In-System Programming (ISP), the auto-baud routine is expecting the IRC frequency to be 12 MHz ± 1 % and is used to synchronize with the host via serial port 0.

Problem:

On the LPC11U1x Rev A device(s) only, the IRC frequency could be outside the nominal frequency of 12 MHz ± 1 %. The IRC is hence not recommended to be used as a clock source. This behavior could also affect the auto-baud routine's ability to synchronize with the host via serial port 0 during ISP.

Work-around:

None. This errata was fixed on the LPC11U1x Rev B device.

3.4 USART.1: ‘False positive’ break interrupt events may occur

Introduction:

The LPC11U1x device family features an option to operate the UART in synchronous mode.

Problem:

When using synchronous UART mode (USART) under the following conditions:

- CSCEN = 0 (SCK active only during transmission)
- CSRC = 0 (Synchronous Slave Mode)
- FES = 1 (Falling Edge Sampling)
- SSDIS = 0 (Use Start and Stop Bit)
- The external transmitting device (Master) sends start and stop bits
- The external device transmits 0x00

The Break Interrupt (BI) flag can become set, despite the fact that no break condition on the bus has occurred. This problem does not manifest when the external master device uses two stop bits.

Work-around:

None, however in some cases system designers have control over the protocol being used between devices and can avoid the error condition outlined above in their system design and/or communication protocol.

3.5 USART.2: SCI Transmit retry error interrupt not working

Introduction:

The USART can be used as a ISO 7816-3 compliant asynchronous smart card interface (SCI). When used in this mode, data transmissions are automatically retried if a NACK is received. If the number of retries exceeds the maximum allowed value (set via the TXRETRY field in the (SCICTRL register) the USART is locked and a transmit error interrupt is generated.

Problem:

When a transmission error occurs, and the interface does not initiate a deactivation sequence (e.g. when the TXRETRY register has been set to 0x0) a lock state is entered.

Work-around:

Recovery from this locked state can be achieved as follows:

When the USART external smartcard clock is used:

1. After a transmission error occurs, wait for at minimum half a smartcard clock period
2. Reset the Tx FIFO

When The USART external smartcard clock is not used:

1. Reset the Tx FIFO
2. Toggle the SCIEN bit

3.6 USB.1: The VBUSDEBOUNCED status bit is not updated correctly

Introduction:

The VBUSDEBOUNCED status bit (bit 28 in DEVCMDSTAT register) indicates if Vbus is detected or not. The bit is set when Vbus becomes high. It gets set to zero if Vbus is low for at least 3 ms. If this bit is high and the DCon bit (bit 16 in DEVCMDSTAT register) is set, the pull-up resistor on USB_DP pin will be enabled to signal a connect.

Problem:

When the LPC11U1x USB interface is configured as a self-powered device, occasionally, the VBUSDEBOUNCED status (bit 28) is not updated correctly in the DEVCMDSTAT register when the USB connector is disconnected from the host while the USB_NeedClk is not set to "PLL Always ON" (bit 9 in DEVCMDSTAT register). When the VBUSDEBOUNCED bit doesn't reflect correct status, the USB_CONNECT signal pin will drive the pull-up resistor on the USB_DP pin all the time. In turn, the LPC11U1x will fail the back voltage test which is part of the USB compliance test (USB-IF).

Work-around:

1. Turn "PLL always ON" (bit 9) off by setting the bit to zero in the DEVCMDSTAT register.
2. Enable the clock to the GPIO Pin interrupts register interface (PINT, bit 19) in the SYSAHBCLKCTRL register.
3. Configure the PIO0_3 pin as USB_VBUS function (PIO0_3 register) and the PIO0_6 pin as USB_CONNECT function (PIO0_6 register)
4. Select the USB_VBUS (PIO0_3 pin) to be one of the GPIO pin interrupt sources by setting the PINTSELx register, and configure the interrupt to trigger as a falling edge sensitive.
5. When the GPIO pin interrupt occurs (VBUS is falling when USB cable is disconnected), check the VBUSDEBOUNCED status (bit 28) in the DEVCMDSTAT register. If it is still set, then configure the USB_CONNECT pin as PIO0_6 function, drive it output high, wait for VBUSDEBOUNCED bit to go low, and then configure the PIO0_6 function back to USB_CONNECT function.

4. AC/DC deviations detail

4.1 n/a

5. Errata notes detail

5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the VDD level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the VDD supply ramps up.

5.2 Note.2

For LPC11U1x parts with bootloader version 7.0, pins PIO0_1 and PIO0_3 must be pulled LOW to enter UART ISP mode.

For LPC11U1x parts with bootloader version 7.1, pin PIO0_1 must be pulled LOW to enter UART ISP mode.

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