I_O = 1 A, V_{IN} = 27 V Linear Regulator IC

NR301E, NR302A

Data Sheet

Description

NR301E and NR302A are linear regulator ICs whose maximum output current is 1 A. Output voltage is adjusted by external resistors. The IC uses the 8 pin surface mount package with exposed thermal pad.

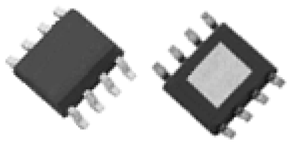
The IC has various functions including the Output On/Off Function, the Overcurrent Protection and the Thermal Shutdown, and achieves a linear regulator circuit with few external components. In addition, stable output voltage with ceramic capacitor reduces the mounting area compared to using electrolytic capacitors.

Features

- Reducing Mounting Area
  Stable with a Ceramic Output Capacitor
- Adjustable Output Voltage (V_{OUT} = 1.1 V to 16 V)
- Output On/Off Function
- Protections:
  Overcurrent Protection (OCP): Fold-back
  Thermal Shutdown (TSD) with Hysteresis: Auto-restart

Packages

NR301E: eSOIC8
NR302A: HSOP8



Not to scale

Specifications

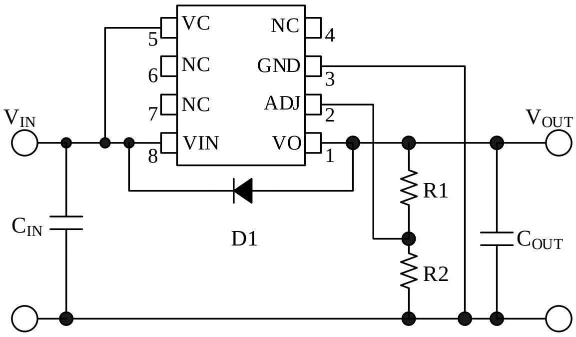
- Recomended Input Voltage, V_{IN}: 2.7 V to 27 V
- Voltage Reference, V_{ADJ}: 1.0 V ± 1.5%
- Output Current, I_O: 1.0 A
- Typical Dropout Voltage, V_{DIF}: 0.6 V

Applications

- Audio Visual Equipment
- Office Automation Equipment
- White Goods

Typical Application

NR301E
NR302A



Contents

1. Absolute Maximum Ratings

Unless otherwise specified, $T_A = 25$ °C.

Parameter	Symbol	Conditions	Rating	Unit
VIN Pin Voltage	V_{IN}		−0.3 to 30	V
VC Pin Voltage	V_C	$V_C \leq V_{IN}$	−0.3 to 30	V
ADJ Pin Voltage	V_{ADJ}		−0.3 to 5.0	V
Power Dissipation	P_D	The IC is mounted on the glass-epoxy board. See Figure 15-1.	2.27	W
Junction Temperature	T_J		−40 to 125	°C
Storage Temperature	T_{stg}		−40 to 125	°C

2. Recommended Operating Range

Parameter	Symbol	Min.	Max.	Unit
VIN Pin Voltage*	V_{IN}	2.7	27	V
Output Current*	I_{OUT}	0	1.0	A
Output Voltage*	V_{OUT}	1.1	16	V
Operating Ambient Temperature	$T_{OP(A)}$	−30	85	°C
Operating Junction Temperature	$T_{OP(J)}$	−30	100	°C

*Following equation shows the relationship between V_{IN}, V_{OUT}, and I_{OUT}. Thus, Dropout Voltage ($V_{IN} - V_{OUT}$) or I_{OUT} may be limited in some conditions.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C, V_{IN} = 6 V and V_{OUT} = 5 V (R1 = 40 kΩ and R2 = 10 kΩ).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference Voltage	V_{ADJ}	I_{OUT} = 10 mA	0.985	1.00	1.015	V
Line Regulation	ΔV_{LINE}	V_{IN} = 6 V to 15 V, I_{OUT} = 10 mA	—	25	50	mV
Load Regulation	ΔV_{LOAD}	I_{OUT} = 0 A to 1 A	—	30	60	mV
Dropout Voltage	ΔV_{DIF}	I_{OUT} = 0.5 A	—	0.3	0.4	V
		I_{OUT} = 1 A	—	0.6	0.8	V
Quiescent Current	I_Q	I_{OUT} = 0 mA, V_C = 2 V	0.5	0.9	1.6	mA
Circuit Current during Regulator Output Off	$I_{Q(OFF)}$	V_C = 0 V	—	0	1	µA
Output Voltage Temperature Coefficient	$\Delta V_{OUT}/\Delta T_A$	T_J = 0 °C to 100 °C	—	±0.5	—	mV/°C
Ripple Rejection Ratio	R.REJ	V_{OUT} = 5 V, I_{OUT} = 0.1 A, f = 100 Hz to 120 Hz	—	55	—	dB
VC Pin Voltage (Output On)	$V_{C(H)}$	I_{OUT} = 10 mA	2.0	—	—	V
VC Pin Voltage (Output Off)	$V_{C(L)}$	I_{OUT} = 10 mA	—	—	0.6	V
VC Pin Current (Output On)	$I_{C(H)}$	V_C = 2.0 V	—	4	40	µA
VC Pin Current (Output Off)	$I_{C(L)}$	V_C = 0 V	−2	0	0.1	µA
Overcurrent Protection Operating Current	I_{S1}	*	1.1	—	—	A
Thermal Shutdown Operating Temperature	T_{SD}		135	155	—	°C
Thermal Shutdown Temperature Hysteresis	$T_{SD(HYS)}$		—	50	—	°C

* After the Overcurrent Protection is activated, I_{S1} is measured when the output voltage decreases by 5% from the reference output voltage (I_{OUT} = 10 mA).

4. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance between Junction and Ambient	θ_{J-A}	The IC is mounted on the glass-epoxy board. See Figure 15-1.	—	—	44	°C/W
Thermal Resistance between Junction and Lead*	θ_{J-L}		—	20	—	°C/W

* The lead temperature is measured at 3 pin (GND).

5. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.08	—	g

6. Performance Curves

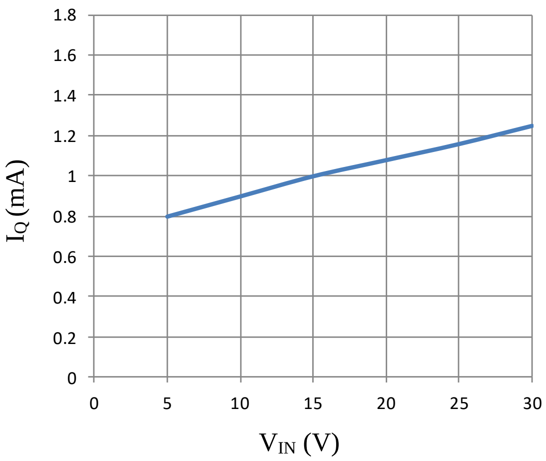


Figure 6-1. Quiescent Current, I_Q vs. Input Voltage, V_{IN}

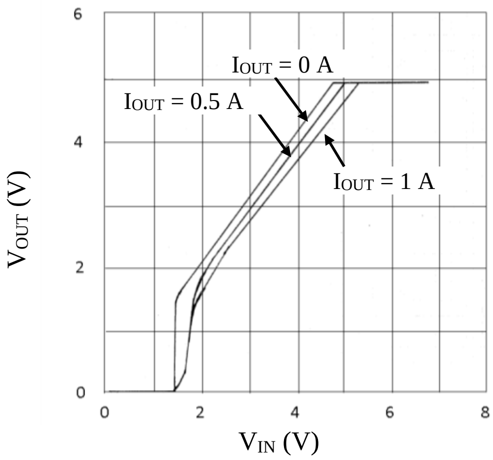


Figure 6-2. Output Voltage, V_{OUT} vs. Input Voltage, V_{IN}

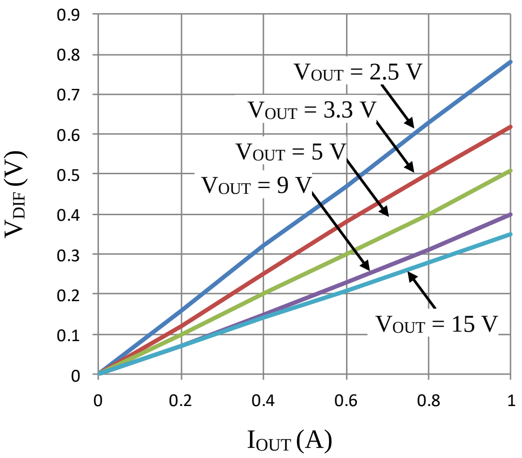


Figure 6-3. Dropout Voltage, V_{DIF} vs. Output Current, I_{OUT}

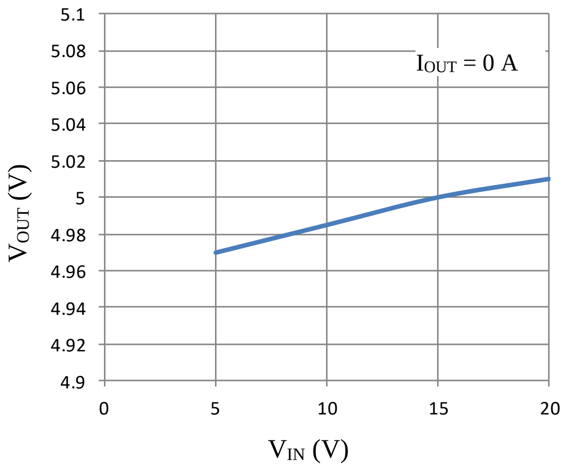


Figure 6-4. Line Regulation

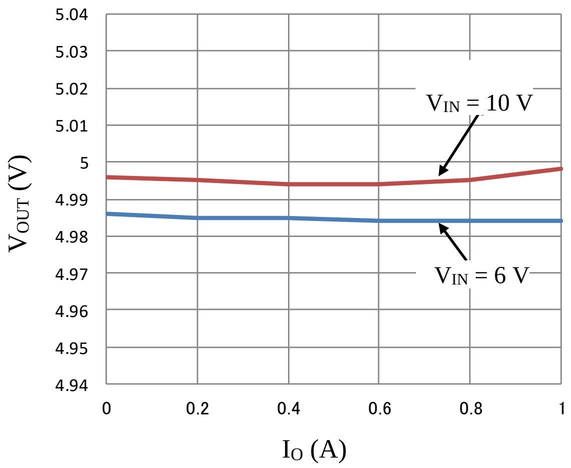


Figure 6-5. Load Regulation

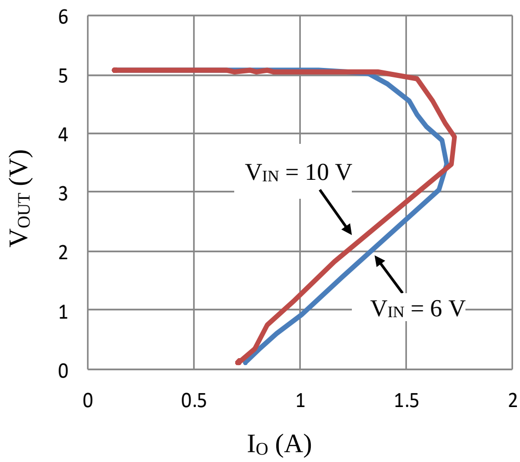


Figure 6-6. Overcurrent Protection Characteristics

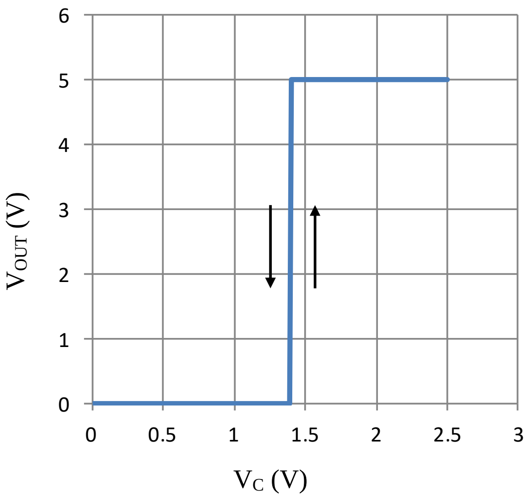


Figure 6-7. VC Pin Output On/Off Characteristics

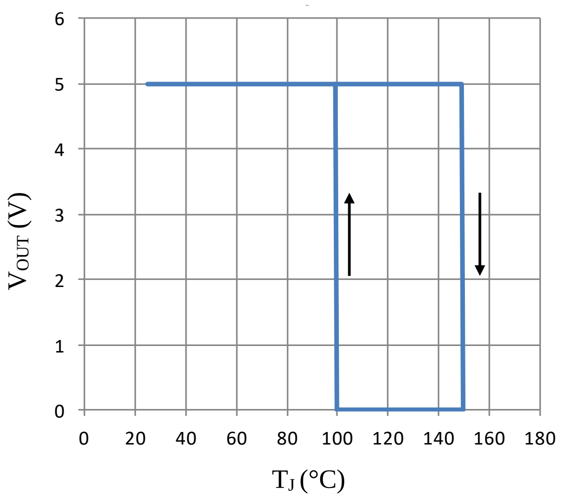


Figure 6-8. Thermal Shutdown Characteristics

7. Derating Curve

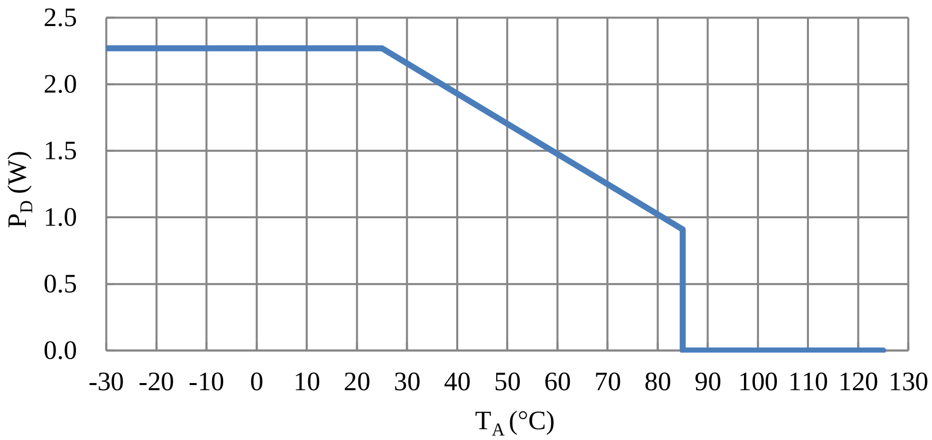
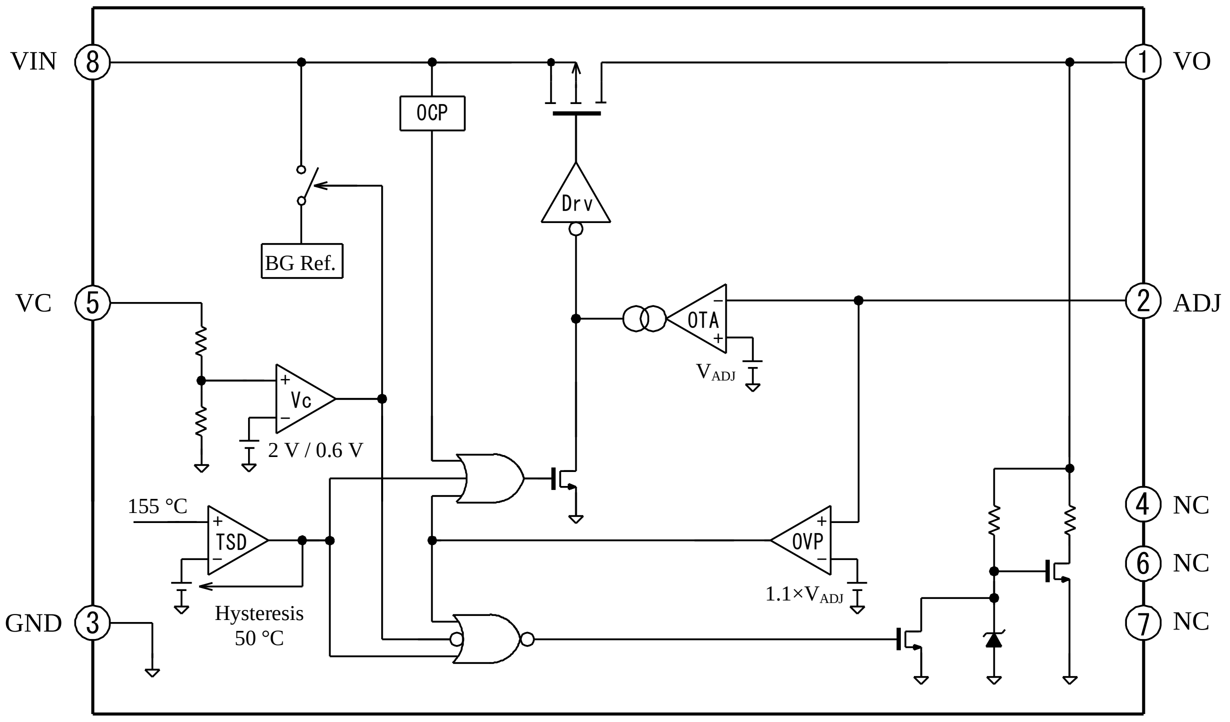
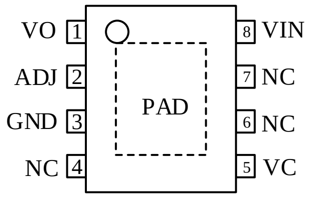


Figure 7-1. Allowable Power Dissipation, P_D vs. Ambient Temperature, T_A

8. Block Diagram



9. Pin Configuration Definitions



Pin Number	Pin Name	Function
1	VO	Voltage output
2	ADJ	Output voltage setting resistor connection
3	GND	Ground
4	NC	(No connection)
5	VC	Output on/off signal input (When the Output On/Off Function is disabled, VC pin must be connected to stable potential.)
6	NC	(No connection)
7	NC	(No connection)
8	VIN	Supply input
(Back Side)	PAD	Exposed pad for heat release (The thermal pad must be soldered to copper trace on PCB, and be connected to the GND pin.)

10. Typical Application

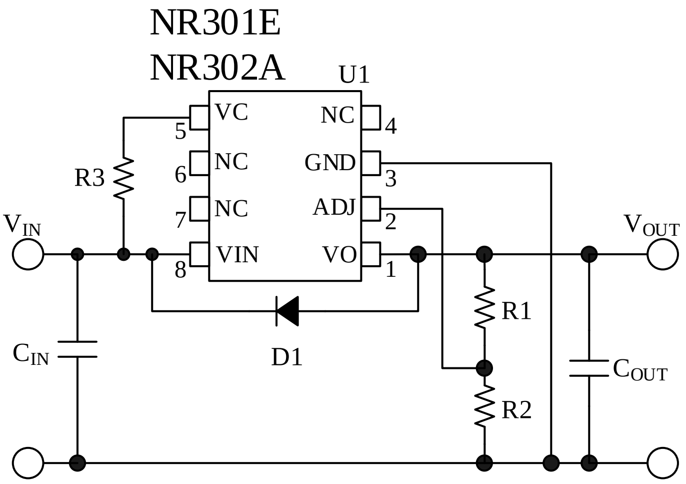


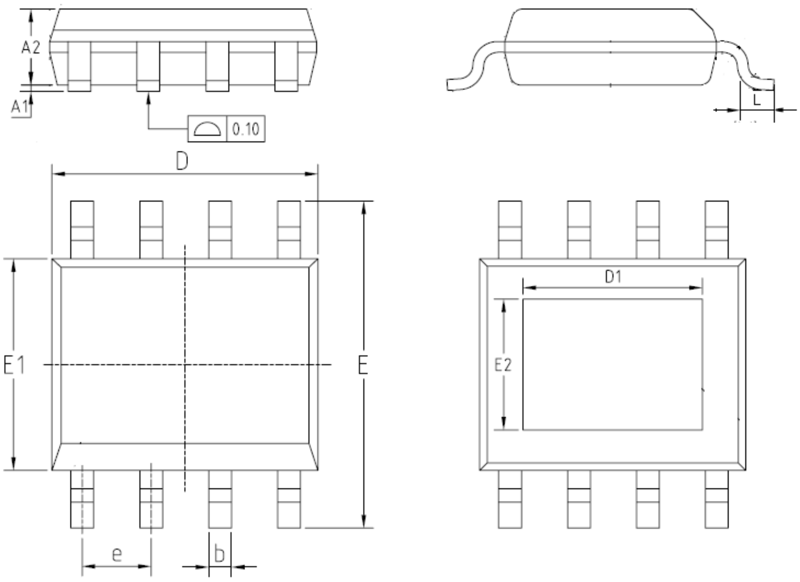
Figure 10-1. Typical Application (Output On/Off Function Disabled)

Table 10-1. Reference Value of External Components (When V_{IN} = 6 V and V_{OUT} = 5 V.)

Symbol	Part Type	Reference Value	Remarks
C_{IN}	Ceramic capacitor	1 µF	Place C_{IN} close to the IC. C_{IN} should be connected to the VIN and GND pins with short traces.
C_{OUT}	Ceramic capacitor	1 µF	Place C_{OUT} close to the IC. C_{OUT} should be connected to the VO and GND pins with short traces.
R1	Resistor	40 kΩ	Adjust resistance based on the output voltage.
R2	Resistor	10 kΩ	For the resistance setting, see Section 13.2.
R3	Resistor	0 Ω	For the resistance setting, see Section 13.5.
D1	Diode	Option	If the condition of VIN < VO is included in the power supply application, it is required to add D1.

11. Physical Dimensions

- **eSOIC8 Package (NR301E)**

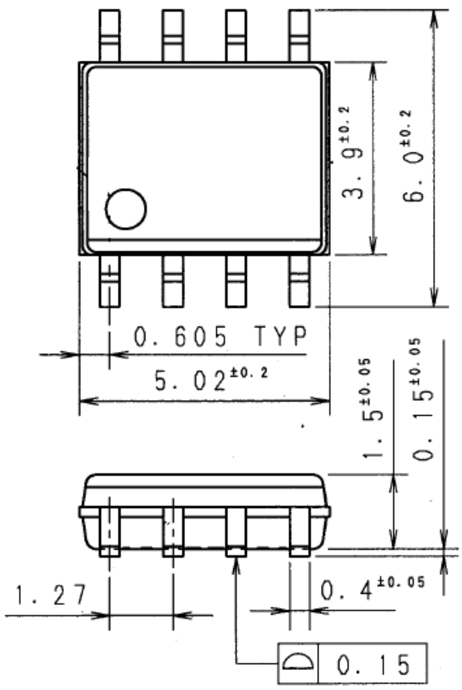


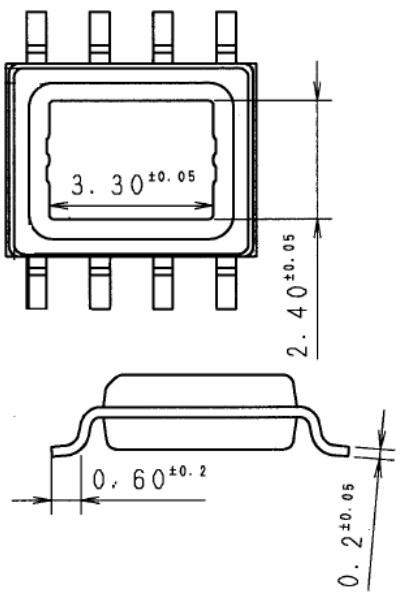
Symbol	Min.	Typ.	Max.
A1	0	0.10	0.15
A2	1.25	1.40	1.65
b	0.38	—	0.51
D	4.80	4.90	5.00
D1	3.10	3.30	3.50
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.20	2.40	2.60
e	—	1.27	—
L	0.45	0.60	0.80

NOTES:

- Dimensions in millimeters
- Bare lead frame and pad: Pb-free (RoHS compliant)
- Dimensions do not include mold burrs.

- **HSOP8 Pakage (NR302A)**

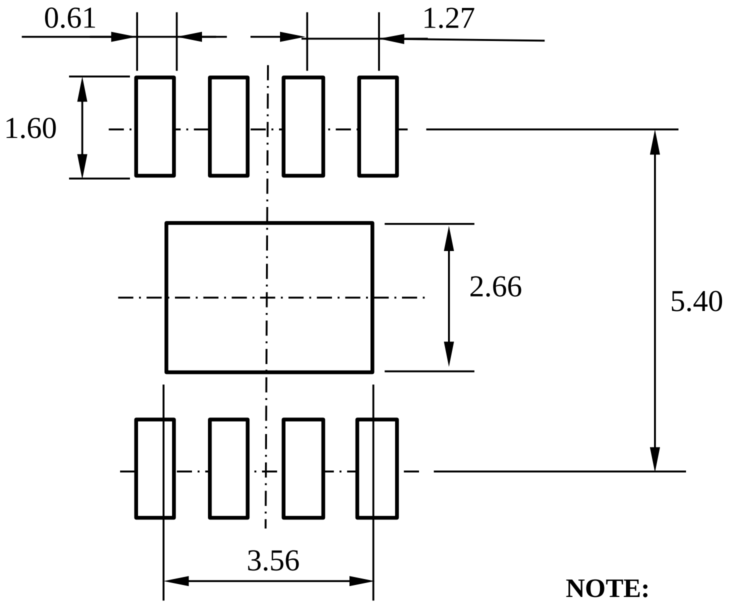




NOTES:

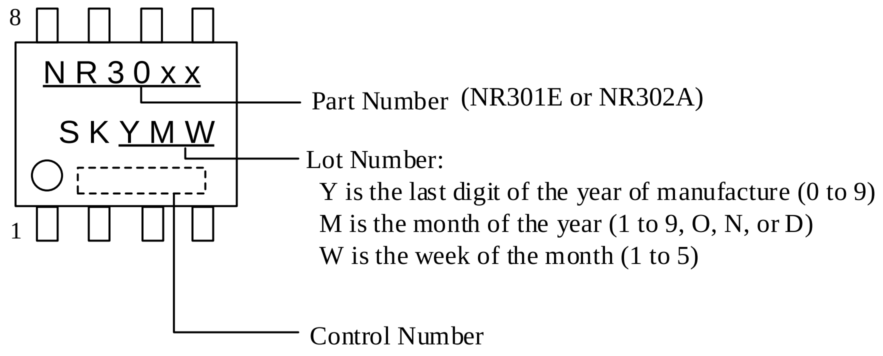
- Dimensions in millimeters
- Bare lead frame and pad: Pb-free (RoHS compliant)

11.1. Land Pattern Example



NOTE:
Dimensions in millimeters

12. Marking Diagram



13. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

13.1. Constant Voltage Control

The IC is with the circuit including the reference voltage, the error amplifier, and P channel power MOSFET. The drain-to-source voltage of the P channel MOSFET is under linear control so that the ADJ pin voltage becomes equal to the reference voltage by the internal error amplifier. As a result, the constant output voltage is provided.

The power loss of the IC is obtained from the product of the drain-to-source voltage (Dropout Voltage) by the output voltage. Note that the thermal design must be taken into account.

13.2. Output Voltage Setting

Output Voltage is adjusted by external resistors, R1 and R2. The setting resisters are connected to the ADJ pin as shown in Figure 13-1.

The feedback signal for the output voltage setting inputs to the ADJ pin. Other signal must not input to the ADJ pin.

The feedback current through R1 and R2 should be set about 100 µA. The reference voltage of the ADJ pin, V_{ADJ}, is 1.00 V. R2 value is calculated by Equation (1).

$$R2 = \frac{V_{ADJ}}{100\ \mu A} = \frac{1.00\ V}{100\ \mu A} = 10\ k\Omega \quad (1)$$

Output voltage, V_{OUT}, is calculated by the following equation.

$$V_{OUT} = \frac{R1 + R2}{R2} \times V_{ADJ} \quad . \quad (2)$$

Thus, R1 is calculated by using Equation (3).

$$R1 = \frac{R2 \times (V_{OUT} - V_{ADJ})}{V_{ADJ}}$$

$$= \frac{10\ k\Omega \times (V_{OUT} - 1.00\ V)}{1.00\ V} \quad (3)$$

If the calculation result does not match the E series, adjustment resistors should be added in series or parallel to R1.

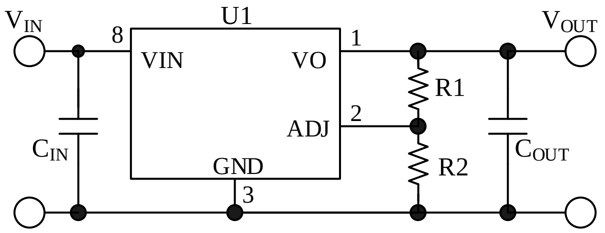


Figure 13-1. ADJ Pin Peripheral Circuit

13.3. Overcurrent Protection (OCP)

The IC has Overcurrent Protection (OCP) with the fold-back characteristic that the output current at the short circuit load (V_{OUT} = 0 V) is smaller than it at OCP activation (see Figure 6-6). The IC loss at the short circuit load ($V_{IN} \times I_O$) is less than constant current or fold-forward characteristic.

When the IC starts at the output capacitor voltage of 0 V, the output current is limited by OCP; and output voltage gradually increases.

13.4. TSD (Thermal Shutdown Protection)

The IC has the Thermal Shutdown (TSD) with hysteresis. When the junction temperature of the IC increase to T_{SD} = 155 °C or more, TSD is activated, and turns off the internal p channel power MOSFET to shutdown the load current.

The temperature hysteresis of TSD is about 50 °C. When the junction temperature decreases to about 100 °C after the load current shutdown, the IC restarts the constant voltage control.

Since the TSD may be activated at the junction temperature of 135 °C that is the minimum characteristics for T_{SD}, it is required to design the heat release so that TSD is not activated in normal operation (junction temperature must be below 125 °C).

The TSD protects the IC against the heat generation when the loss of the IC increases due to the instantaneous short-circuit of the load. This does not guarantee the operation including the reliability in the short-circuit state for long period or the state where the heat generation continues.

13.5. Output On/Off Function

The output is turned on/off by the input signal to the VC pin.

When $V_C \geq V_{C(H)}$, the output is supplied. When $V_C \leq V_{C(L)}$, the output is shutdown. Where, V_C is the VC pin voltage, $V_{C(H)}$ = 2 V (min.), and $V_{C(L)}$ = 0.6 V (max.).

The VC pin is pulled down by internal high impedance resistor for the power dissipation reduction. If the VC pin is open, its input status may be unstable; and the malfunction may be caused.

To disable the Output On/Off Function, the VC pin must be connected to the VIN pin.

As shown in Figure 13-2 and Figure 13-3, the on/off signal is generated by a general-purpose logic IC or a transistor, and inputs to the VC pin. When the general-purpose logic IC is used, pull-up resistor, R3, is unnecessary.

In the case of Figure 13-3, the R3 value should satisfy Equation (4) that the maximum sink current of the VC pin is taken into account. The minimum value of R3 should be set taking into account the loss of the transistor.

$$R3 < \frac{V_{IN} - V_{C(H)}(\mathrm{min.})}{I_{C(H)}(\mathrm{max.})} \qquad (4)$$

Where V_{IN} is input voltage, $V_{C(H)}$(min.) is minimum specification of $V_{C(H)}$ (= 2 V), and $I_{C(H)}$(max.) is minimum specification of $I_{C(H)}$ (= 40 µA).

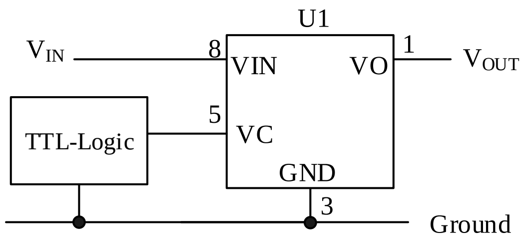


Figure 13-2. Output On/Off Function
(In the Case of General-purpose Logic IC)

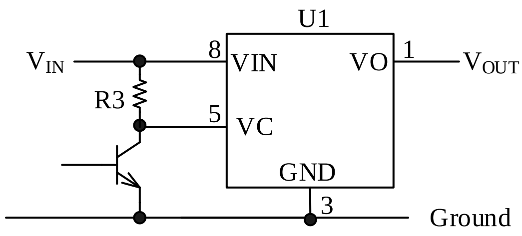


Figure 13-3. Output On/Off Function
(In the Case of Transistor)

14. Design Notes

14.1. Input and Output Capacitor

Input capacitor, C_{IN}, and output capacitor, C_{OUT}, must be used low ESR and high DC bias characteristics. Since the capacitance has variation and temperature characteristics, it should be set taking into account enough margins.

If the traces between C_{IN} and the VIN pin, and between C_{OUT} and the VO pin are long, the power supply impedance is high. For stable operation, C_{IN} and C_{OUT} must be placed close to the VIN pin and VO pin respectively, and be connected to each pin with short trace.

- **C_{IN} Setting:**

Use ceramic capacitor of ≥1 µF or electrolytic capacitor of about 22 µF. Be sure to confirm the actual operation and set the capacitance.

When electrolytic capacitor is used, it is required to connect a ceramic capacitor between the VIN and GND pins. The ceramic capacitor should be connected close to these pins (The power supply including electrolytic capacitor operates stable in normal temperature, but it may operate unstable in low temperature due to the effect of the temperature characteristic of ESR).

- **C_{OUT} Setting:**

Use ceramic capacitor of ≥1 µF.

The output voltage can be stable with ceramic capacitor whose mounting area is small, because the phase compensation circuit is built in the IC.

14.2. Protection Diode for Reverse Biasing

If the condition of VIN < VO is included in the power supply application (ex. the dynamic changing in input voltage), a protection diode, D1, must be connected between the VIN pin and the VO pin (see Figure 10-1).

14.3. Considerations in Circuit Configuration

The overcurrent protection of the IC has the fold-back characteristic. To avoid startup failure, do not use the circuit configurations as follows:

- Constant current circuit is connected to the IC.
- CV/CC circuit is connected to the IC.
- Load 2 is stacked on Load 1 (see in Figure 14-1).
- The output voltage setting resistor is connected between the GND pin and Ground (see Figure 14-2).

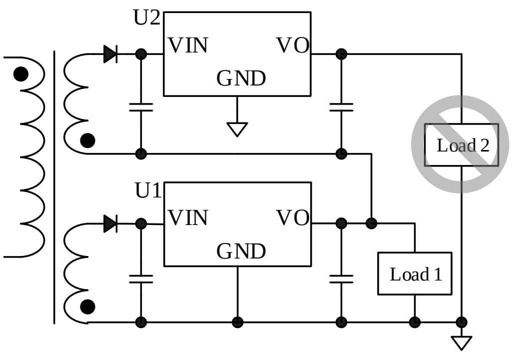


Figure 14-1. Stacked on Loads
(Do not connect Load 2.)

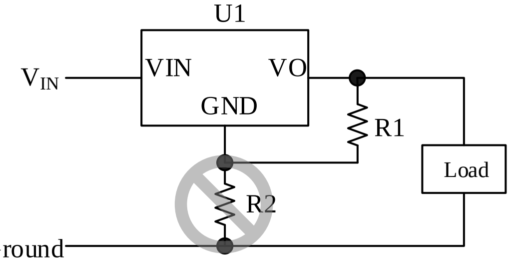
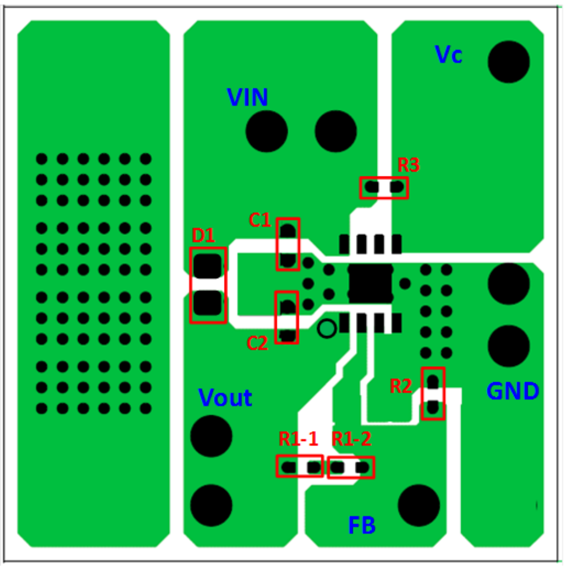


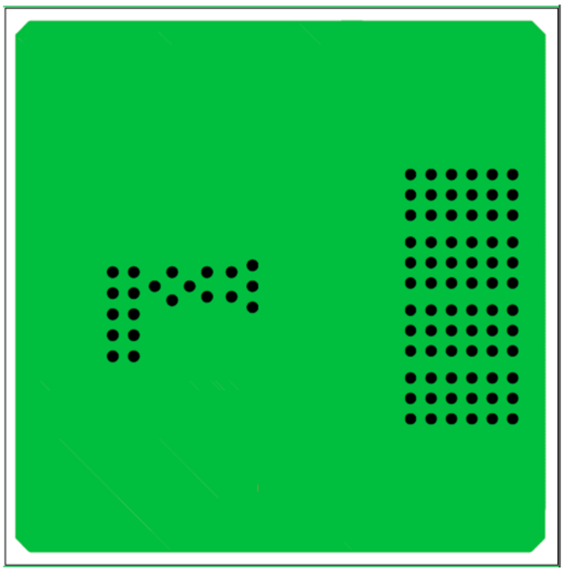
Figure 14-2. Output Voltage Setting
(Do not connect R2.)

15. Pattern Layout Example

The IC has an exposed pad to improve its heat releasing capability. The exposed pad must be soldered to copper trace on PCB.



(Top View)



(Bottom View)

Remarks:

- Double-sided PCBs with through-hole: FR4
- Thickness of the glass-epoxy board: 1.6 mm
- Area: 40 mm × 40 mm
- Copper thickness: 35 μm

Figure 15-1. PCB Pattern Layout Example

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DSGN-CEZ-16003