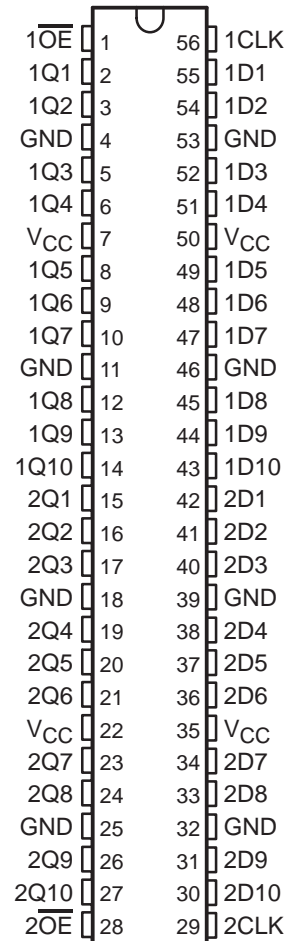


# SN54ALVTH16821, SN74ALVTH16821 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCES078E – JULY 1996 – REVISED JANUARY 1999

- State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V  $V_{CC}$ )
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- High-Drive (–24/24 mA at 2.5-V and –32/64 mA at 3.3-V  $V_{CC}$ )
- Power Off Disables Outputs, Permitting Live Insertion
- High-Impedance State During Power Up and Power Down Prevents Driver Conflict
- Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Auto3-State Eliminates Bus Current Loading When Output Exceeds  $V_{CC} + 0.5$  V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model; and Exceeds 1000 V Using Charged-Device Model, Robotic Method
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package

SN54ALVTH16821 . . . WD PACKAGE  
SN74ALVTH16821 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description

The 'ALVTH16821 devices are 20-bit bus-interface flip-flops with 3-state outputs designed for 2.5-V or 3.3-V  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20-bit flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK), the flip-flops store the logic levels set up at the D inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

# SN54ALVTH16821, SN74ALVTH16821

## 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCES078E – JULY 1996 – REVISED JANUARY 1999

---

#### description (continued)

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH16821 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALVTH16821 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

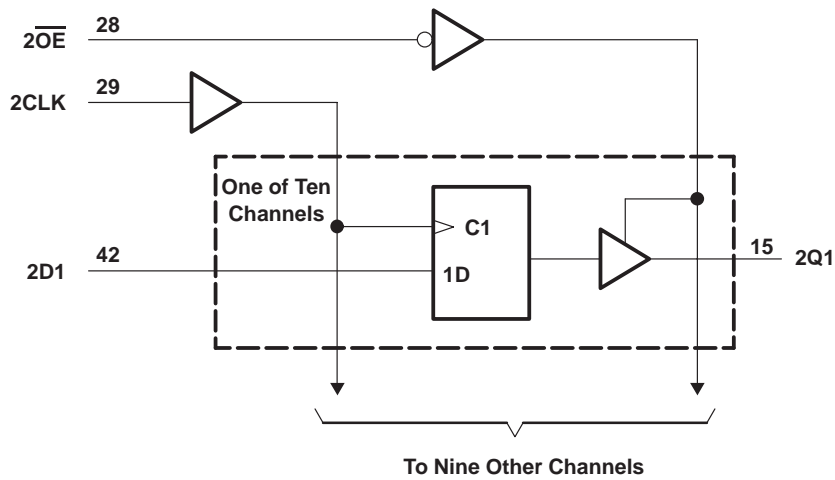
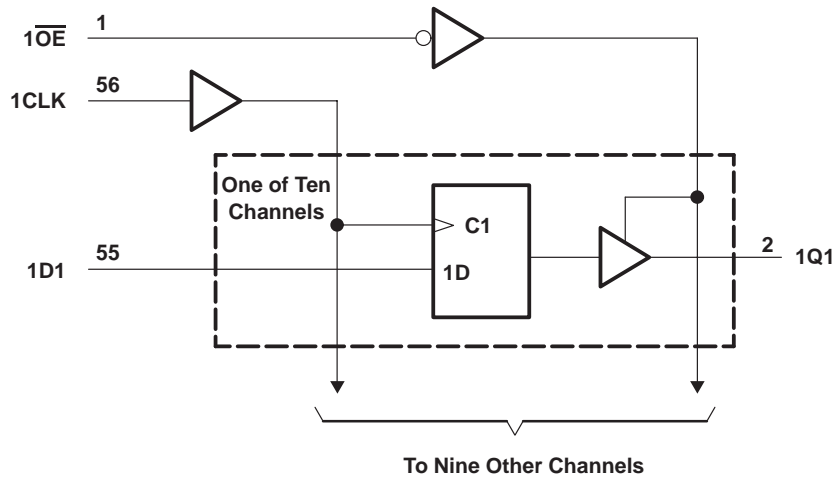
FUNCTION TABLE  
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

SN54ALVTH16821, SN74ALVTH16821  
 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS  
 WITH 3-STATE OUTPUTS

SCES078E – JULY 1996 – REVISED JANUARY 1999

logic diagram (positive logic)



# SN54ALVTH16821, SN74ALVTH16821

## 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCES078E – JULY 1996 – REVISED JANUARY 1999

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1)	–0.5 V to 7 V
Output current in the low state, $I_O$ : SN54ALVTH16821	96 mA
SN74ALVTH16821	128 mA
Output current in the high state, $I_O$ : SN54ALVTH16821	–48 mA
SN74ALVTH16821	–64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 3)

		SN54ALVTH16821			SN74ALVTH16821			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	2.3		2.7	2.3		2.7	V
$V_{IH}$	High-level input voltage	1.7			1.7			V
$V_{IL}$	Low-level input voltage			0.7			0.7	V
$V_I$	Input voltage	0	$V_{CC}$	5.5	0	$V_{CC}$	5.5	V
$I_{OH}$	High-level output current			–6			–8	mA
$I_{OL}$	Low-level output current			6			8	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$			18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
$T_A$	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN54ALVTH16821, SN74ALVTH16821**  
**2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SCES078E – JULY 1996 – REVISED JANUARY 1999

**recommended operating conditions,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (see Note 3)**

		SN54ALVTH16821			SN74ALVTH16821			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	3		3.6	3		3.6	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_I$	Input voltage	0	$V_{CC}$	5.5	0	$V_{CC}$	5.5	V
$I_{OH}$	High-level output current			-24			-32	mA
$I_{OL}$	Low-level output current			24			32	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$			48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
	Outputs enabled							
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
$T_A$	Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54ALVTH16821, SN74ALVTH16821

## 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCES078E – JULY 1996 – REVISED JANUARY 1999

electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS		SN54ALVTH16821		SN74ALVTH16821		UNIT
			MIN	TYP†	MAX	MIN	
$V_{IK}$	$V_{CC} = 2.3\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V
$V_{OH}$	$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V
	$V_{CC} = 2.3\text{ V}$	$I_{OH} = -6\text{ mA}$	1.8		1.8		
$V_{OL}$	$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2		V
	$V_{CC} = 2.3\text{ V}$	$I_{OL} = 6\text{ mA}$	0.4				
		$I_{OL} = 8\text{ mA}$			0.4		
		$I_{OL} = 18\text{ mA}$	0.5				
$I_I$	Control inputs	$V_{CC} = 2.7\text{ V}$ , $V_I = V_{CC}$ or GND	$\pm 1$		$\pm 1$		$\mu\text{A}$
		$V_{CC} = 0$ or $2.7\text{ V}$ , $V_I = 5.5\text{ V}$	10		10		
	Data inputs	$V_{CC} = 2.7\text{ V}$ , $V_I = 5.5\text{ V}$	10		10		
		$V_{CC} = 2.7\text{ V}$ , $V_I = V_{CC}$	1		1		
		$V_I = 0$	-5		-5		
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$				$\pm 100$		$\mu\text{A}$
$I_{BHL}^\ddagger$	$V_{CC} = 2.3\text{ V}$ , $V_I = 0.7\text{ V}$		115		115		$\mu\text{A}$
$I_{BHH}^\S$	$V_{CC} = 2.3\text{ V}$ , $V_I = 1.7\text{ V}$		-10		-10		$\mu\text{A}$
$I_{BHLO}^\P$	$V_{CC} = 2.7\text{ V}$ , $V_I = 0$ to $V_{CC}$		300		300		$\mu\text{A}$
$I_{BHHO}^\#$	$V_{CC} = 2.7\text{ V}$ , $V_I = 0$ to $V_{CC}$		-300		-300		$\mu\text{A}$
$I_{EX}^\parallel$	$V_{CC} = 2.3\text{ V}$ , $V_O = 5.5\text{ V}$		125		125		$\mu\text{A}$
$I_{OZ(PU/PD)}^\star$	$V_{CC} \leq 1.2\text{ V}$ , $V_O = 0.5\text{ V to } V_{CC}$ , $V_I = \text{GND or } V_{CC}$ , $\overline{OE} = \text{don't care}$		$\pm 100$		$\pm 100$		$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 2.7\text{ V}$	$V_O = 2.3\text{ V}$ , $V_I = 0.7\text{ V or } 1.7\text{ V}$	5		5		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 2.7\text{ V}$	$V_O = 0.5\text{ V}$ , $V_I = 0.7\text{ V or } 1.7\text{ V}$	-5		-5		$\mu\text{A}$
$I_{CC}$	$V_{CC} = 2.7\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high	0.04	0.1	0.04	0.1	mA
		Outputs low	2.3	4.5	2.3	4.5	
		Outputs disabled	0.04	0.1	0.04	0.1	
$C_i$	$V_{CC} = 2.5\text{ V}$ , $V_I = 2.5\text{ V or } 0$		3.5		3.5		pF
$C_o$	$V_{CC} = 2.5\text{ V}$ , $V_O = 2.5\text{ V or } 0$		6.5		6.5		pF

† All typical values are at  $V_{CC} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

\* High-impedance state during power up or power down

**SN54ALVTH16821, SN74ALVTH16821**  
**2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SCES078E – JULY 1996 – REVISED JANUARY 1999

**electrical characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54ALVTH16821		SN74ALVTH16821		UNIT		
				MIN	TYP†	MAX	MIN		TYP†	MAX
$V_{IK}$		$V_{CC} = 3\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V		
$V_{OH}$		$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V		
		$V_{CC} = 3\text{ V}$		2		2				
$V_{OL}$		$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2		V		
		$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$		0.4				
				$I_{OL} = 24\text{ mA}$		0.5				
				$I_{OL} = 32\text{ mA}$		0.5				
				$I_{OL} = 48\text{ mA}$		0.55				
		$I_{OL} = 64\text{ mA}$		0.55						
$I_I$		Control inputs $V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND		$\pm 1$		$\pm 1$		$\mu\text{A}$		
				$V_{CC} = 0$ or $3.6\text{ V}$ , $V_I = 5.5\text{ V}$		10			10	
		Data inputs $V_{CC} = 3.6\text{ V}$		$V_I = 5.5\text{ V}$		10			10	
				$V_I = V_{CC}$		1			1	
		$V_I = 0$		-5		-5				
$I_{off}$		$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$				$\pm 100$		$\mu\text{A}$		
$I_{BHL}^\ddagger$		$V_{CC} = 3\text{ V}$ , $V_I = 0.8\text{ V}$		75		75		$\mu\text{A}$		
$I_{BHH}^\S$		$V_{CC} = 3\text{ V}$ , $V_I = 2\text{ V}$		-75		-75		$\mu\text{A}$		
$I_{BHLO}^\P$		$V_{CC} = 3.6\text{ V}$ , $V_I = 0$ to $V_{CC}$		500		500		$\mu\text{A}$		
$I_{BHHO}^\#$		$V_{CC} = 3.6\text{ V}$ , $V_I = 0$ to $V_{CC}$		-500		-500		$\mu\text{A}$		
$I_{EX}^\parallel$		$V_{CC} = 3\text{ V}$ , $V_O = 5.5\text{ V}$		125		125		$\mu\text{A}$		
$I_{OZ(PU/PD)}^\star$		$V_{CC} \leq 1.2\text{ V}$ , $V_O = 0.5\text{ V to } V_{CC}$ , $V_I = \text{GND or } V_{CC}$ , $\overline{OE} = \text{don't care}$		$\pm 100$		$\pm 100$		$\mu\text{A}$		
$I_{OZH}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$ , $V_I = 0.8\text{ V or } 2\text{ V}$		5		5		$\mu\text{A}$		
$I_{OZL}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$ , $V_I = 0.8\text{ V or } 2\text{ V}$		-5		-5		$\mu\text{A}$		
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND		Outputs high		0.07 0.1		mA		
				Outputs low		3.2 5.5				
				Outputs disabled		0.07 0.1				
$\Delta I_{CC}^\square$		$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND		0.4		0.4		mA		
$C_i$		$V_{CC} = 3.3\text{ V}$ , $V_I = 3.3\text{ V or } 0$		3.5		3.5		pF		
$C_o$		$V_{CC} = 3.3\text{ V}$ , $V_O = 3.3\text{ V or } 0$		6		6		pF		

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

☆ High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN54ALVTH16821, SN74ALVTH16821**  
**2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SCES078E – JULY 1996 – REVISED JANUARY 1999

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

		SN54ALVTH16821		SN74ALVTH16821		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	150		150		MHz
$t_w$	Pulse duration, CLK high or low	1.6		1.5		ns
$t_{\text{su}}$	Setup time, data before CLK $\uparrow$	Data high	1.6	1.5		ns
		Data low	2.1	2		
$t_h$	Hold time, data after CLK $\uparrow$	Data high	0.4	0.3		ns
		Data low	1.1	1		

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 2)**

		SN54ALVTH16821		SN74ALVTH16821		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	150		150		MHz
$t_w$	Pulse duration, CLK high or low	1.6		1.5		ns
$t_{\text{su}}$	Setup time, data before CLK $\uparrow$	Data high	1.6	1.5		ns
		Data low	1.6	1.5		
$t_h$	Hold time, data after CLK $\uparrow$	Data high	1.1	1		ns
		Data low	1.1	1		

**switching characteristics over recommended operating free-air temperature range,  $C_L = 30\text{ pF}$ ,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16821		SN74ALVTH16821		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			150		150		MHz
$t_{\text{PLH}}$	CLK	Q	1	4.2	1	4.1	ns
$t_{\text{PHL}}$			1	4.5	1	4.4	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	1.5	4.7	1.5	4.6	ns
$t_{\text{PZL}}$			1	4.2	1	4.1	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	1.5	4.6	1.5	4.5	ns
$t_{\text{PLZ}}$			1	5	1	4.9	

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16821		SN74ALVTH16821		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			150		150		MHz
$t_{\text{PLH}}$	CLK	Q	1	3.6	1	3.5	ns
$t_{\text{PHL}}$			1	3.6	1	3.5	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	1	4.2	1	4.1	ns
$t_{\text{PZL}}$			1	3.7	1	3.6	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	1	4.9	1	4.8	ns
$t_{\text{PLZ}}$			1	4.8	1	4.6	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



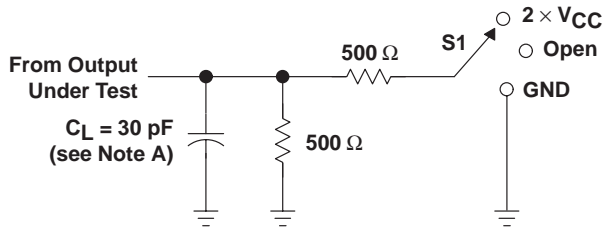


SN54ALVTH16821, SN74ALVTH16821  
2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS  
WITH 3-STATE OUTPUTS

SCES078E – JULY 1996 – REVISED JANUARY 1999

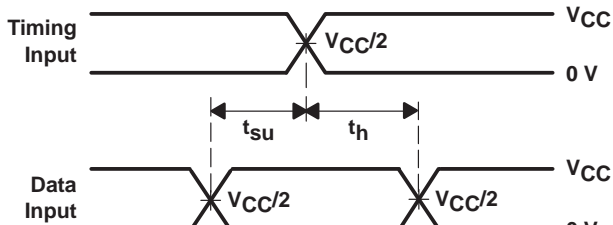
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

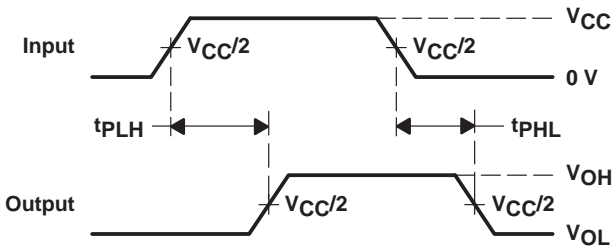


LOAD CIRCUIT

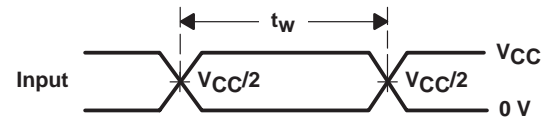
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



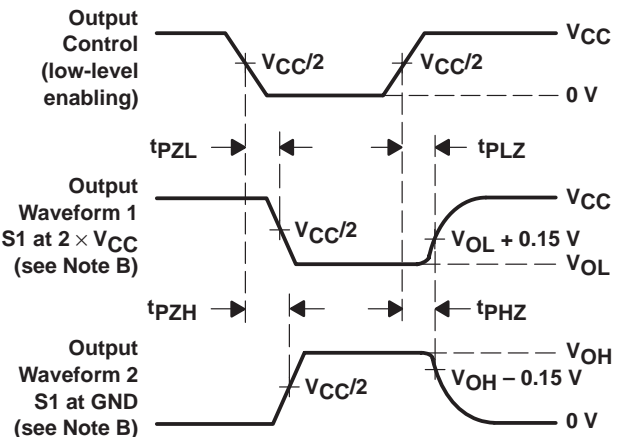
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

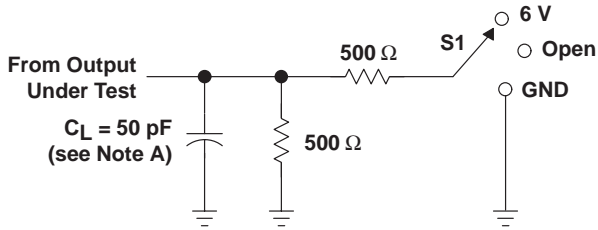
Figure 1. Load Circuit and Voltage Waveforms

**SN54ALVTH16821, SN74ALVTH16821**  
**2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SCES078E – JULY 1996 – REVISED JANUARY 1999

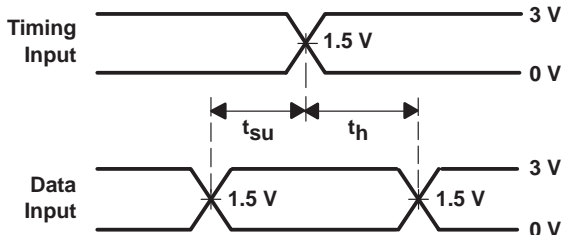
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

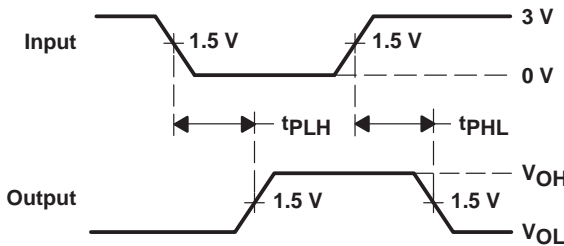


**LOAD CIRCUIT**

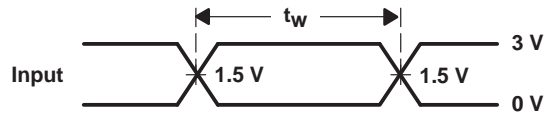
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



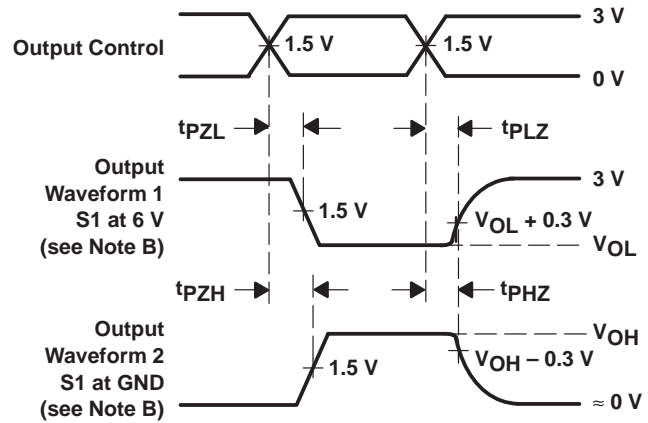
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVTH16821DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH16821	<a href="#">Samples</a>
SN74ALVTH16821DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH16821	<a href="#">Samples</a>
SN74ALVTH16821GR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH16821	<a href="#">Samples</a>
SN74ALVTH16821VR	ACTIVE	TVSOP	DGV	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VT821	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

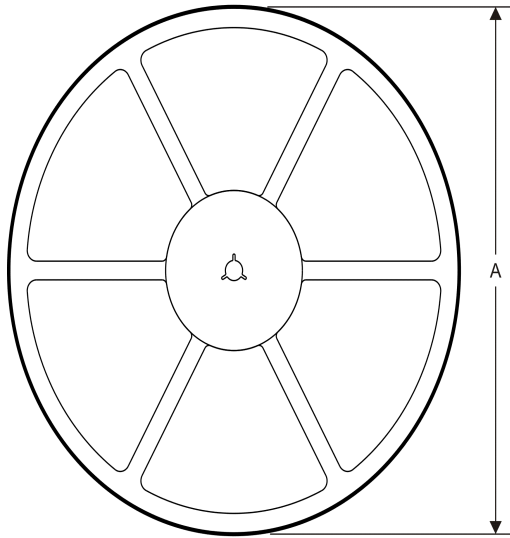
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVTH16821DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74ALVTH16821GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVTH16821VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVTH16821DLR	SSOP	DL	56	1000	367.0	367.0	55.0
SN74ALVTH16821GR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74ALVTH16821VR	TVSOP	DGV	56	2000	367.0	367.0	45.0

DGV (R-PDSO-G\*\*)

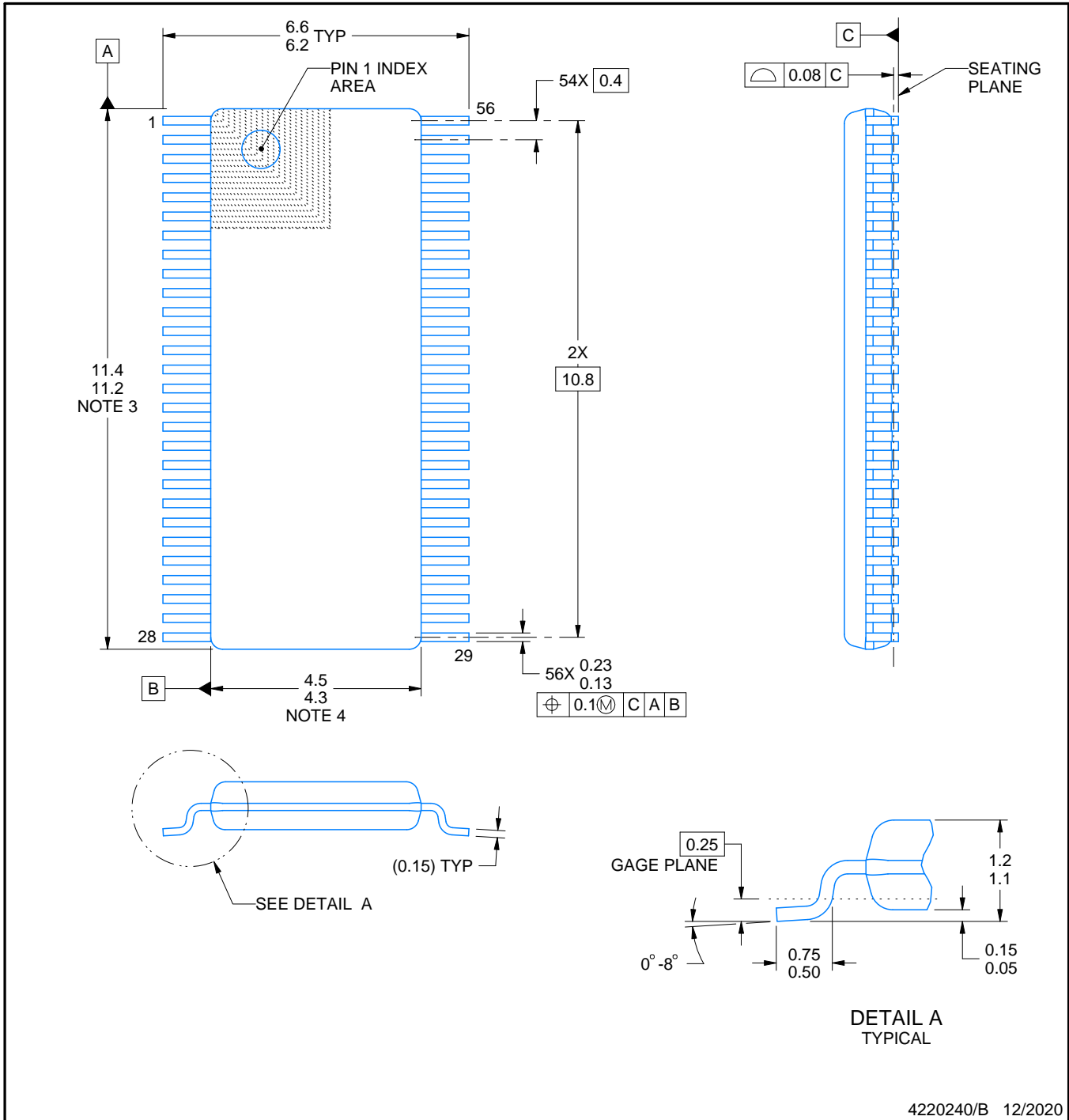
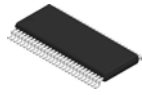
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



4220240/B 12/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.

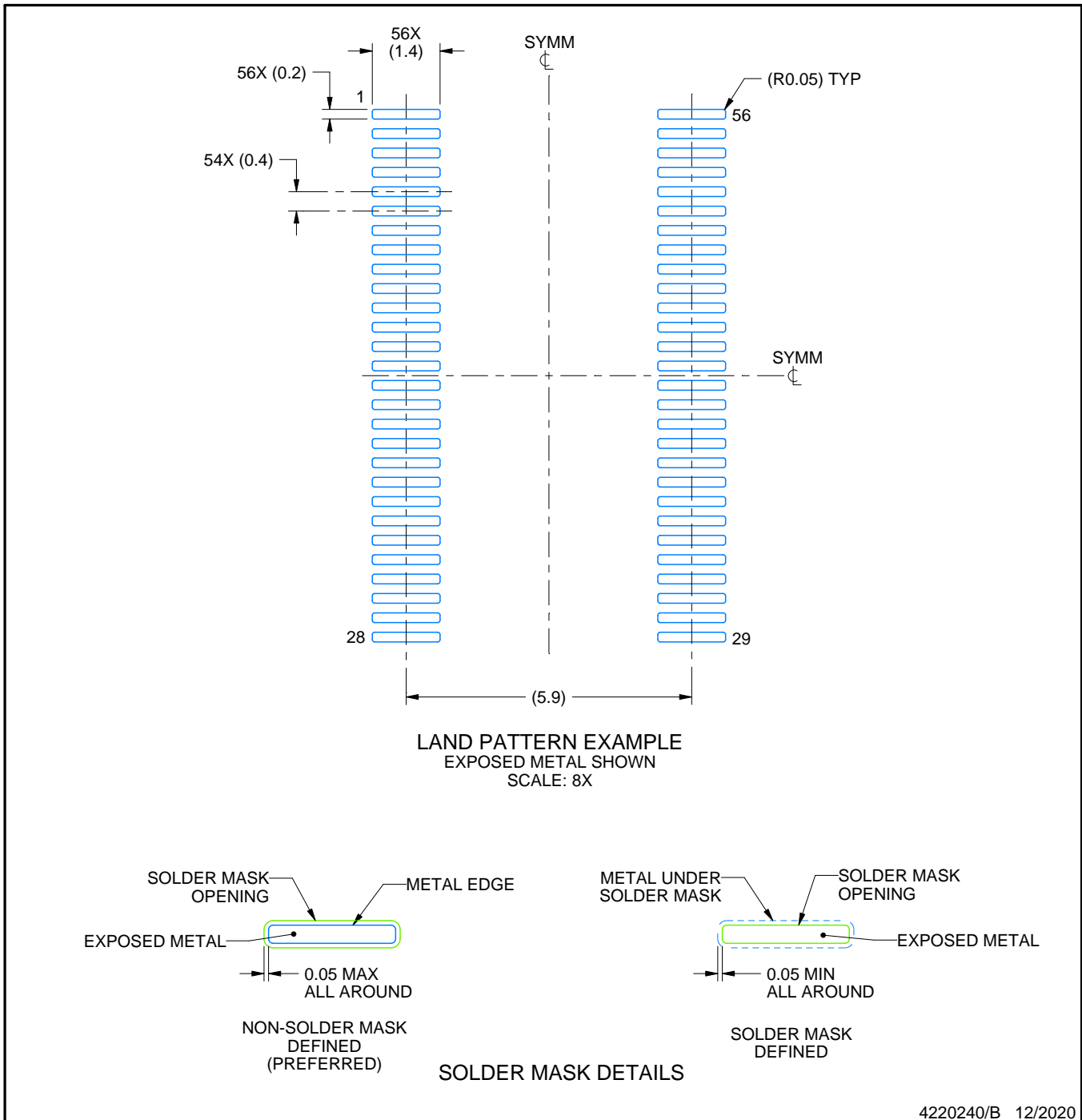


# EXAMPLE BOARD LAYOUT

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220240/B 12/2020

NOTES: (continued)

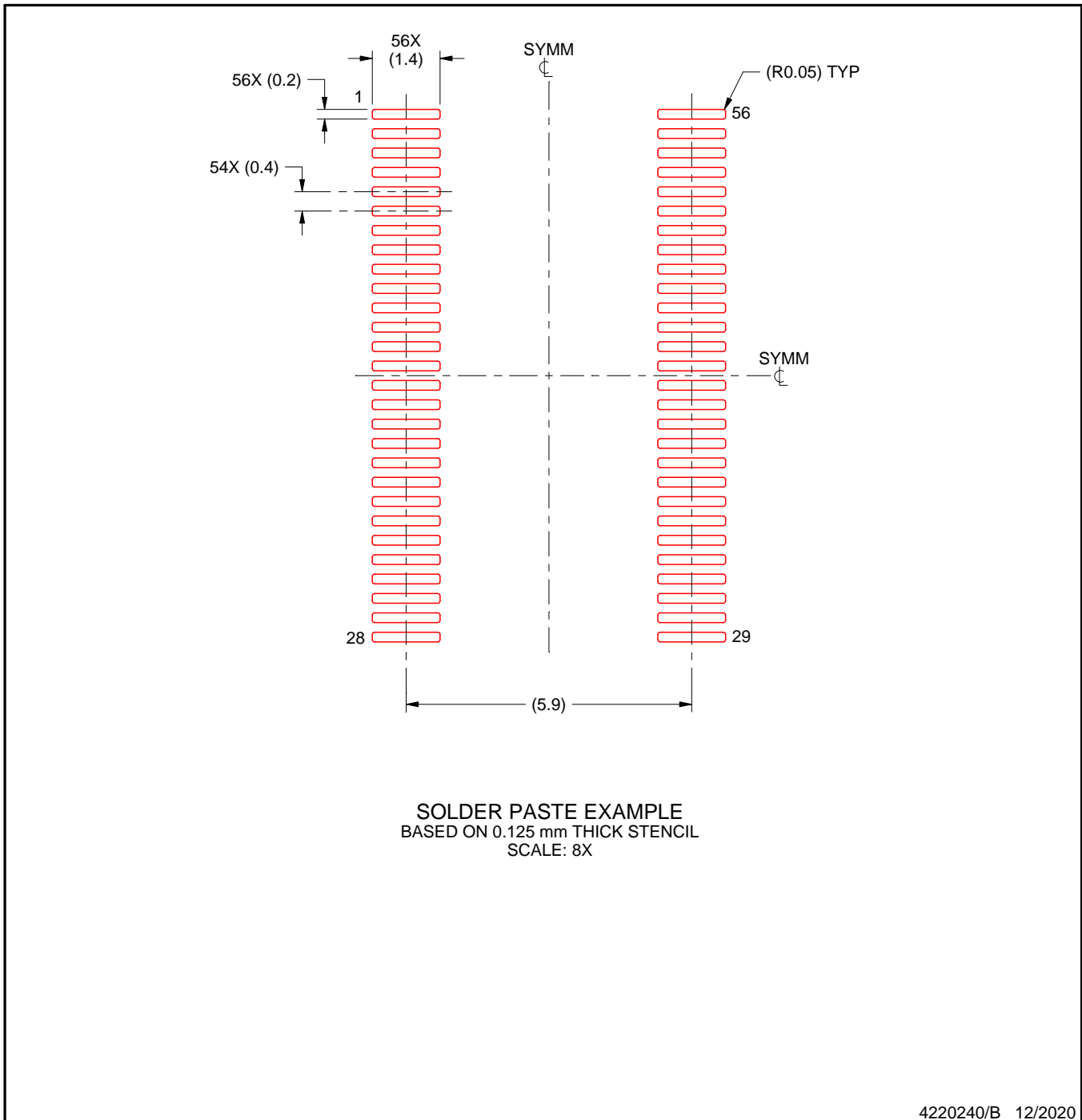
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



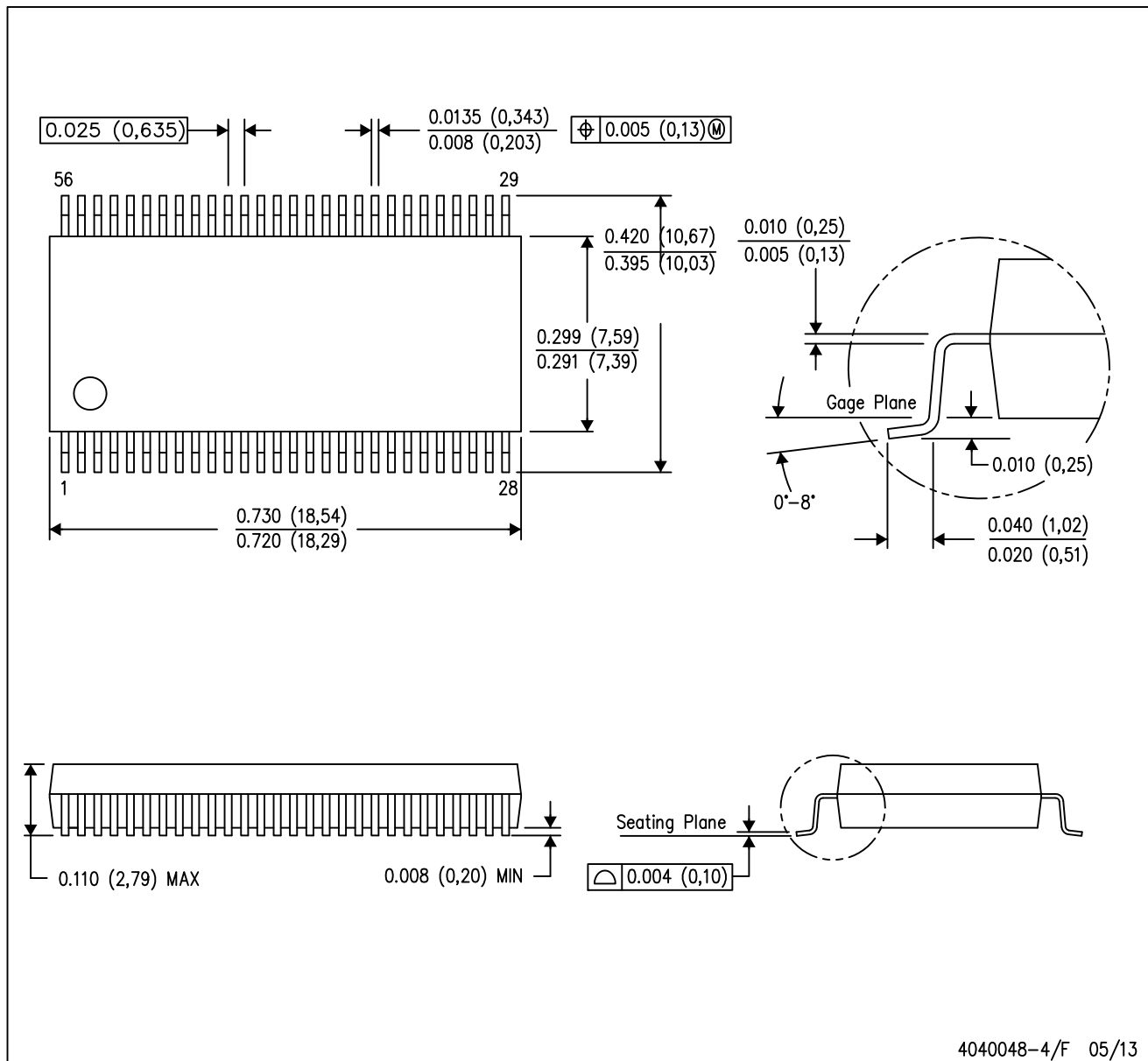
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

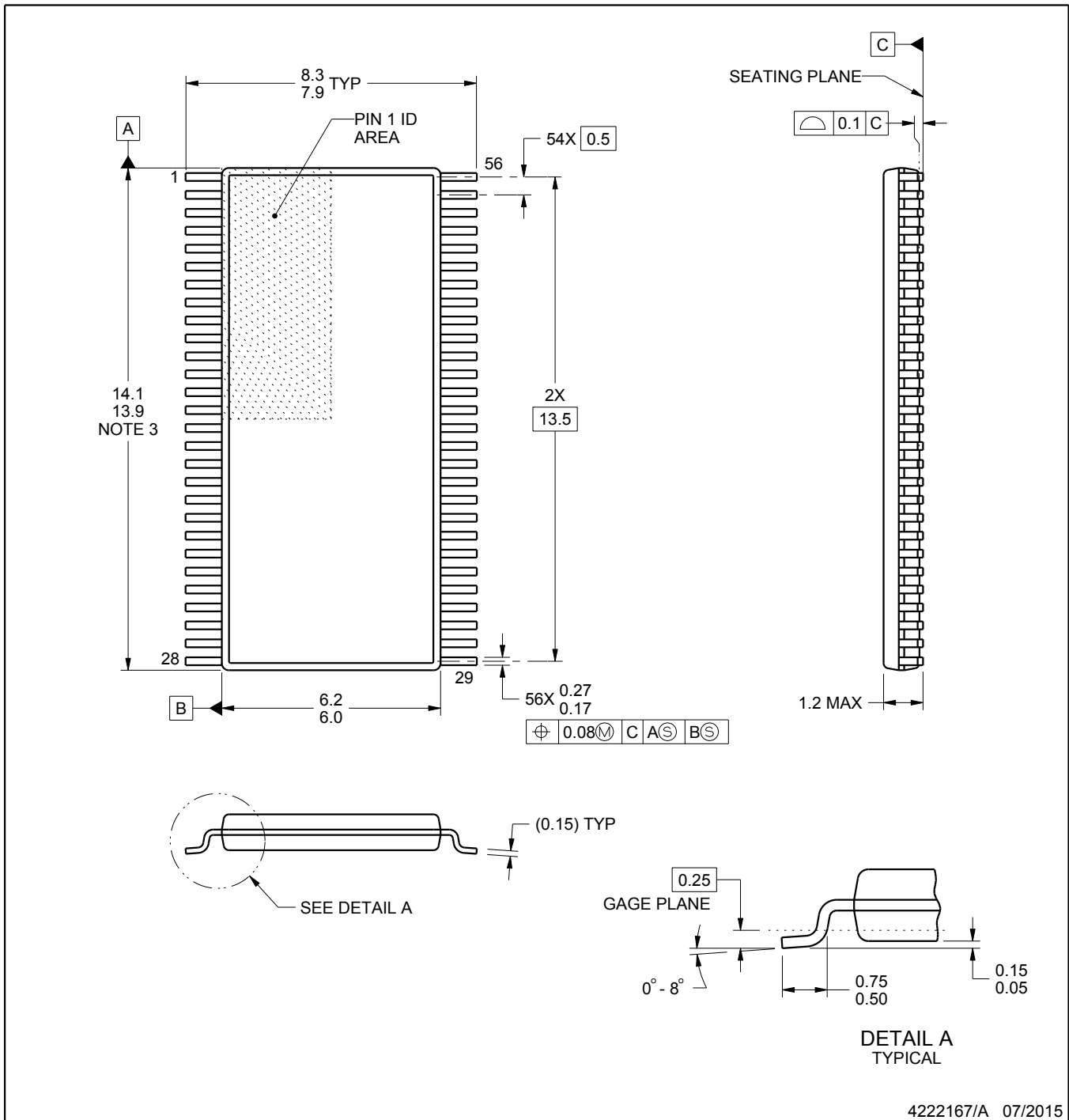
# DGG0056A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4222167/A 07/2015

### NOTES:

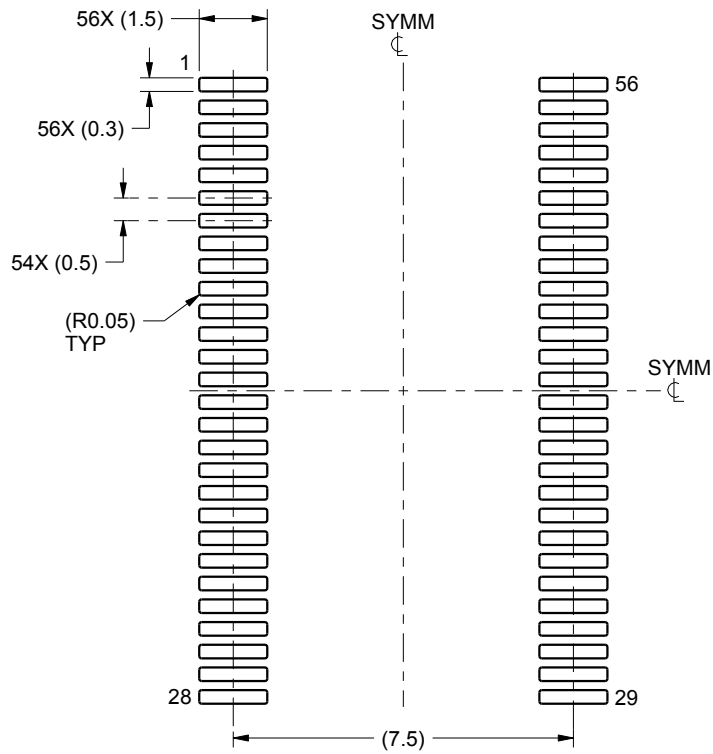
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

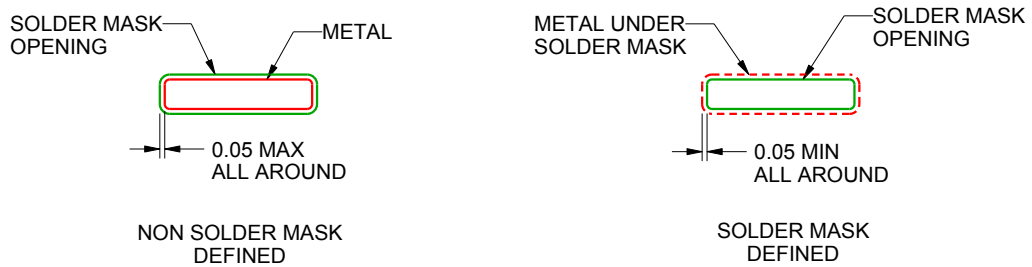
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

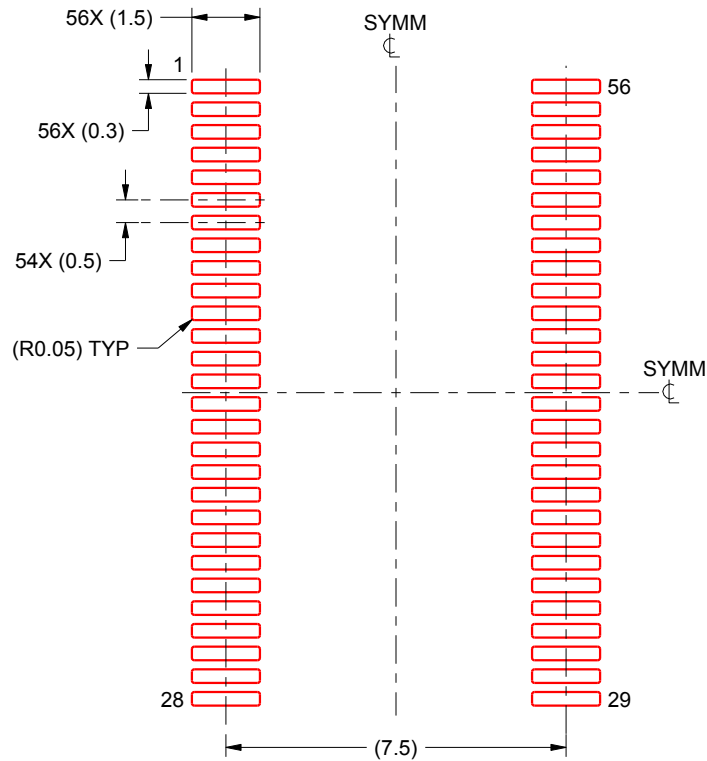
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated