Reference Board User's Manual
High Voltage Synchronous Buck Regulators: 3 V to 24 V
SiC431 (24 A)

DESCRIPTION

The SiC431 is family of synchronous buck regulators with integrated high side and low side power MOSFETs. Its power stage is capable of supplying up to 24 A continuous current at 1 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 3 V to 24 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial. SiC43x series employs a constant on time control architecture that supports ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device is internally compensated and no external ESR network is required for loop stability purposes. The device also incorporates a power saving scheme that significantly increases light load efficiency. The regulator integrates a full protection feature set, including output over voltage protection (OVP), cycle by cycle over current protection (OCP) short circuit protection (SCP) and thermal shutdown (OTP). It also has UVLO and a user programmable soft start. The SiC43x series is available in lead (Pb)-free power enhanced MLP44-24L package in 4 mm x 4 mm dimension.

ORDERING TABLE		
PART NUMBER	**MODE**	**OUTPUT CURRENT**
SiC431AEVB-A	Ultrasonic	24 A
SiC431BEVB-A	Power safe	24 A

FEATURES

- Versatile
  - Single supply operation from 3 V to 24 V input voltage
  - Adjustable output voltage down to 0.6 V
  - Scalable solution: 24 A (SiC431)
  - Support start-up with pre-bias output voltage
  - ± 1 % output voltage accuracy at -40 °C to +125 °C
- Highly efficient
  - 97 % peak efficiency
  - 1 µA supply current at shutdown
  - 50 µA operating current not switching
- Highly configurable
  - Four programmable switching frequencies available: 300 kHz, 500 kHz, 750 kHz, and 1 MHz
  - Adjustable soft start and adjustable current limit (OCP)
  - 3 modes of operation: forced continuous conduction (FCCM), power save (PSM) (for SiC43xB), or ultrasonic (UTR) (for SiC43xA)
- Robust and reliable
  - Cycle-by-cycle current limit
  - Output overvoltage protection
  - Output undervoltage / short circuit protection with auto retry
  - Power good flag and over temperature protection
- Design tools
  - Supported by Vishay PowerCAD Online Design Simulation (https://vishay.transim.com/landing.aspx)
  - Design support kit (www.vishay.com/ppg?74589)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Industrial and automation
- Home automation
- Industrial and server computing
- Networking, telecom, and base station power supplies
- Wall transformer regulation
- Robotics
- High end hobby electronics: remote control cars, planes, and drones
- Battery management systems
- Power tools
- Vending, ATM, and slot machines

SPECIFICATIONS

This reference board allows the end user to evaluate the SiC43x series microBUCK® regulators for their features and functionalities. The user may also change the operating range by making changes to the jumper connections. See section “Selection Jumpers” below in the document.

CONNECTION AND SIGNAL / TEST POINTS

Power Terminals (J10)

- +V_{IN} (pin 1), V_{IN} GND (pin 2)

Connect to a voltage source to this pin. The minimum input voltage will be 3 V. For input voltages (V_{IN}) below 4.5 V an external V_{DD} and V_{DRD} is required.

- +V_{OUT} (pin 5 and pin 6), V_{OUT} GND (pin 3 and pin 4)

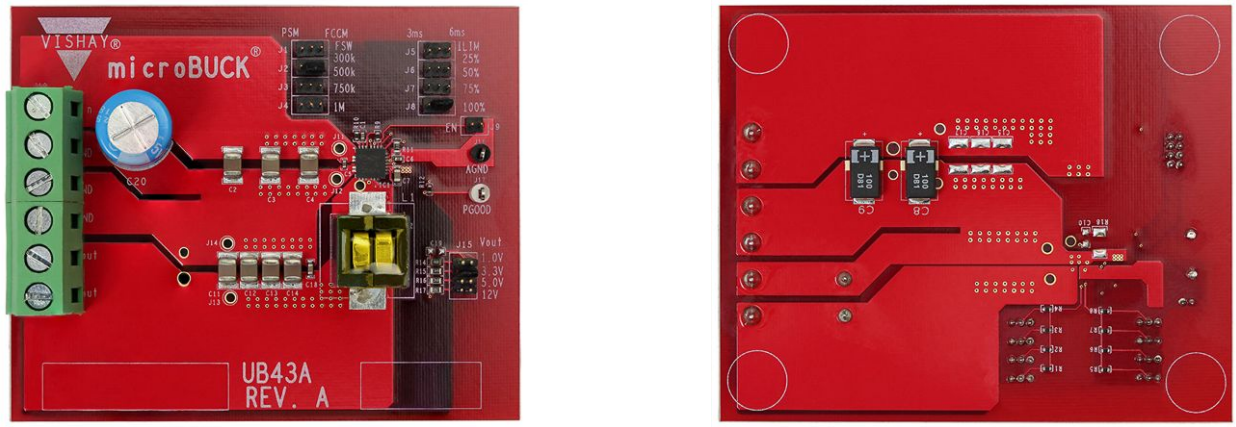


Fig. 1 - SiC431 EVB

BOARD CONFIGURATION TABLE

SiC431 EVB TYPICAL PRE-DEFINED OPERATING CONFIGURATIONS [a]				
V_{IN} (V)	V_{OUT} (V)	f_{sw} (kHz)	L (µH)	MAXIMUM I_{OUT} (A)
12.0	1.0	750	0.22	20
12.0	3.3	500	1.00	20
12.0	5.0	500	1.00	20
19.0	12.0	300	4.70	12

Note

a. Output voltage V_{OUT} is set by J15 jumper; switching frequency f_{sw} and switching mode is set by J1, J2, J3, J4 specified in table “Mode 1 options from setting J1, J2, J3, J4”; soft start time and OCP percentage is set by J5, J6, J7, J8 specified in table “Mode 2 options from setting J5, J6, J7, J8

SELECTION JUMPERS

Enable of Device

J9: this is the jumper that enables/disables the part.

With J9 two pins left open, the device is enabled.
With J9 two pins shorted, the device is disabled.

Output Voltage V_{out} Setting

J15: this is the jumper that select output voltage

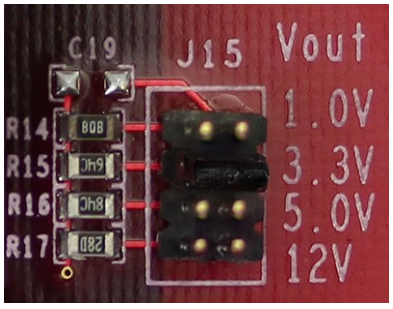


Fig. 2 - J15 Jumper on EVB for Output Setting

J15 is a 4 x 2 eight-pin header illustrated in Fig. 2. Shorting two pins in a row, from top to bottom as indicated in Fig. 2, output voltage V_{OUT} can be set to 1.0 V, 3.3 V, 5.0 V, or 12 V. An example setup illustrated in Fig. 2 is 3.3 V. The default setup is 5.0 V.

MODE 1 Select

J1, J2, J3, and J4: are four 1 x 3 three-pin header which allow user to select one option out of sixteen choices of switching frequency f_{sw} and mode of operation. Table “Mode 1 options from setting J1, J2, J3, J4” specifies all options to achieve by setting **J1, J2, J3, and J4**. The left pin is defined as the left most pin of the 1 x 3 header closer to Vishay logo on EVB. The right pin is defined as the right most pin of the 1 x 3 header far from the Vishay logo on EVB. The middle pin is defined as the pin of the 1 x 3 header sitting between the left pin and the right pin.

MODE 1 OPTIONS FROM SETTING J1, J2, J3, J4			
NO	f_{sw} (kHz)	MODE OF OPERATION	JUMPER SET UP ON J1, J2, J3, AND J4
1	300	FCCM	The **right** pin of **J1** shorted to the middle pin of **J1**; all other pins keep open
2	300	PSM (for SiC43xB) or UTR (for SiC43xA)	The **left** pin of **J1** shorted to the middle pin of **J1**; all other pins keep open
3 [a]	500	FCCM	The **right** pin of **J2** shorted to the middle pin of **J2**; all other pins keep open
4	500	PSM (for SiC43xB) or UTR (for SiC43xA)	The **left** pin of **J2** shorted to the middle pin of **J2**; all other pins keep open
5	750	FCCM	The **right** pin of **J3** shorted to the middle pin of **J3**; all other pins keep open
6	750	PSM (for SiC43xB) or UTR (for SiC43xA)	The **left** pin of **J3** shorted to the middle pin of **J3**; all other pins keep open
7	1000	FCCM	The **right** pin of **J4** shorted to the middle pin of **J4**; all other pins keep open
8	1000	PSM (for SiC43xB) or UTR (for SiC43xA)	The **left** pin of **J4** shorted to the middle pin of **J4**; all other pins keep open

Note

a. Default setup on EVB

MODE 2 Select

J5, J6, J7, and J8 are four 1 x 3 three-pin headers which allow user to select one option out of sixteen choices of soft start time and OCP's percent over its maximum value. Table "Mode 2 options from setting J5, J6, J7, J8" specifies all options to achieve by setting J5, J6, J7, and J8. The left pin is defined as the left most pin of the 1 x 3 header closer to Vishay logo on EVB. The right pin is defined as the right most pin of the 1 x 3 header far from the Vishay logo on EVB. The middle pin is defined as the pin of the 1 x 3 header sitting between the left pin and the right pin.

MODE 2 OPTIONS FROM SETTING J5, J6, J7, J8			
NO	SOFT START (ms)	OCP (%)	JUMPER SET UP ON J5, J6, J7, AND J8
1	6	25	The **right** pin of **J5** shorted to the middle pin of **J5**; all other pins keep open
2	3	25	The **left** pin of **J5** shorted to the middle pin of **J5**; all other pins keep open
3	6	50	The **right** pin of **J6** shorted to the middle pin of **J6**; all other pins keep open
4	3	50	The **left** pin of **J6** shorted to the middle pin of **J6**; all other pins keep open
5	6	75	The **right** pin of **J7** shorted to the middle pin of **J7**; all other pins keep open
6	3	75	The **left** pin of **J7** shorted to the middle pin of **J7**; all other pins keep open
7 [a]	6	100	The **right** pin of **J8** shorted to the middle pin of **J8**; all other pins keep open
8	3	100	The **left** pin of **J8** shorted to the middle pin of **J8**; all other pins keep open

Note

a. Default setup on EVB

PV_{IN} Enhanced UVLO Option

SiC431 uses LDO circuit to generate internal V_{DD} from PV_{IN}, so its V_{DD} UVLO feature may be used to implement PV_{IN} UVLO like the EVB did. In cases that an enhanced PV_{IN} UVLO feature may be required in those applications where either the level of PV_{IN} UVLO is higher than 4 V or avoiding SiC431 falsely turn on during extreme PV_{IN} crashing is required, the user has an option to modify the EVB and use EN hysteresis to realize an enhanced PV_{IN} UVLO feature. The user needs to change R9 from 100 kΩ to 20 kΩ, then add a resistor and a capacitor 0.1 µF (50 V rating) in the schematic and BOM, where two components are connected from EN to ground. For the EVB, the user may populate the two components on the bottom side of EVB crossing two pins of J9. Equation (1) lists an equation for the user to calculate the resistance of the added resistor.

$$R99 = \frac{R9}{(PVIN_{EN_H} - 1)} \quad (1)$$

where $PVIN_{ENH}$ is the expected level of PV_{IN}, in volts, enabling SiC431, R9 is resistance of the resistor R9, R99 is resistance of the resistor to be added between EN and ground.

For example, provided that $PVIN_{ENH}$ is chosen as 7.6 V and R9 is 20 kΩ, the calculated resistance of R99 is 3.03 kΩ and a 3.01 kΩ resistor shall be selected following E96 table.

SIGNALS AND TEST LEADS

Input Voltage Sense

V_{IN_SENSE} (TP11), GND_{IN_SENSE} (TP12): this allows the user to measure the voltage directly at the input of the regulator bypassing any losses generated by connections to the board. These test points can also be as a remote sense port of a power source with remote sense capability.

Output Voltage Sense

V_{OUT_SENSE} (TP13), GND_{OUT_SENSE} (TP14): this allows the user to measure the output voltage directly at the sense point of the regulator bypassing any losses generated by connections to the board. These test points can also be as a remote sense port of an external load with remote sense capability.

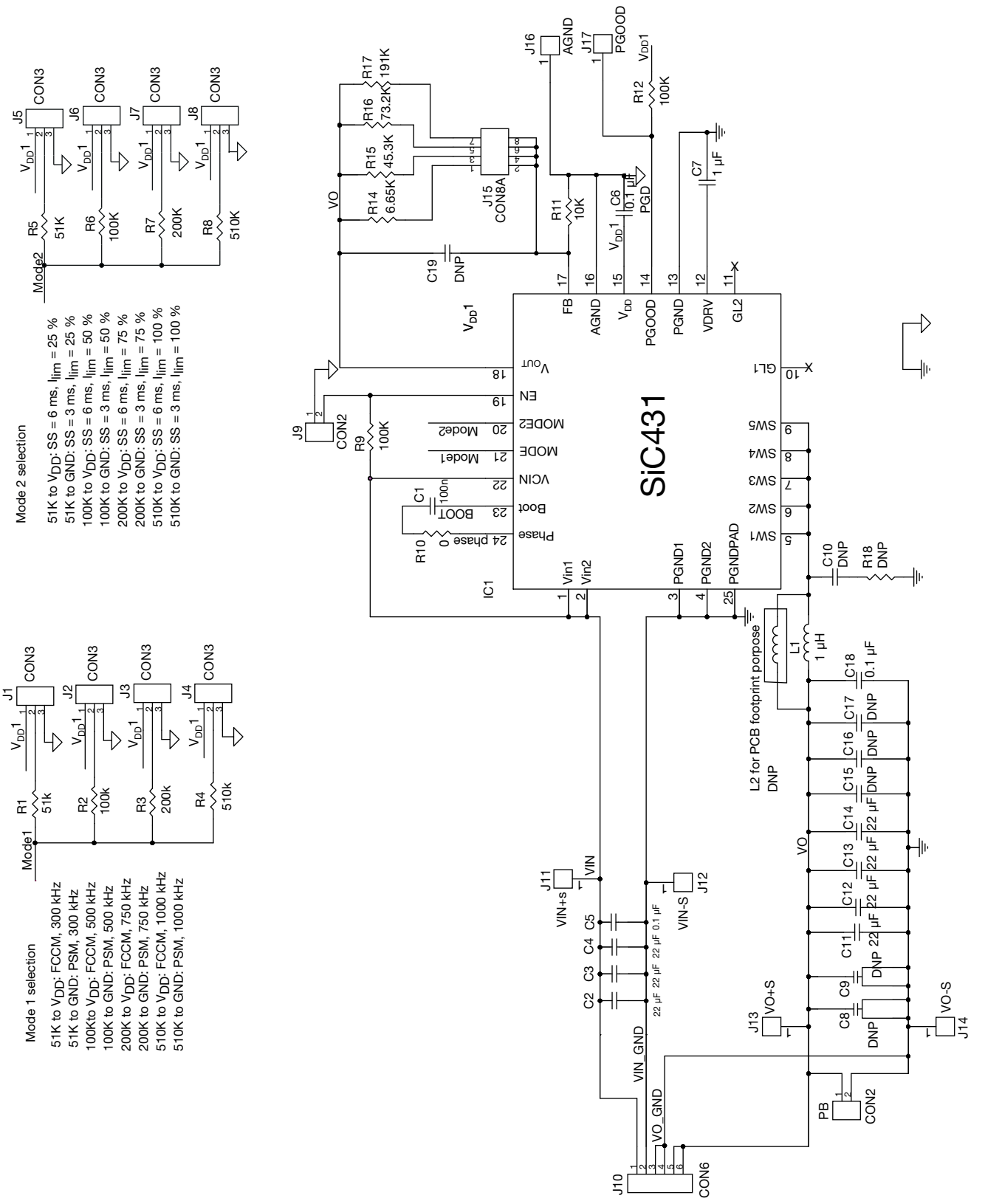
Power Good Indicator

PGD (J17): is an open drain output and is pulled up with a 100 kΩ resistor, R12, to V_{DD1} (≈ 5 V). When FB or V_{OUT} are within -10 % to +20 % of the set voltage this pin will go HI to indicate the output is okay. To prevent false triggering during transient events, the P_{GOOD} has a 25 µs blanking time.

Power Up Procedure

Before turning on the reference board, the user needs to finish jumper setup or use the default one (see section on mode selection). It is required to disable the SiC431 before making any changes to the jumpers.

SCHEMATIC FOR SiC431



SCHEMATIC, DESIGN, BILL OF MATERIALS, AND GERBER FILES FOR PCB FABRICATION

These files are as follows and available for download at www.vishay.com/power-ics/list/product-74589/tab/designtools-ppg/

- "*.DSN" for schematic design file
- "*.DBK" for data backup file for Orcad
- ".opj" Orcad project file. Any schematic work should always be opened with the opj file. Use of a DSN file for this purpose is not advised
- "*.xlsx" is the bill of materials (BOM) derived from the schematic
- "*.PDF" is the PDF version of the schematic from the "*.DSN" file

PCB LAYOUT FOR SiC431

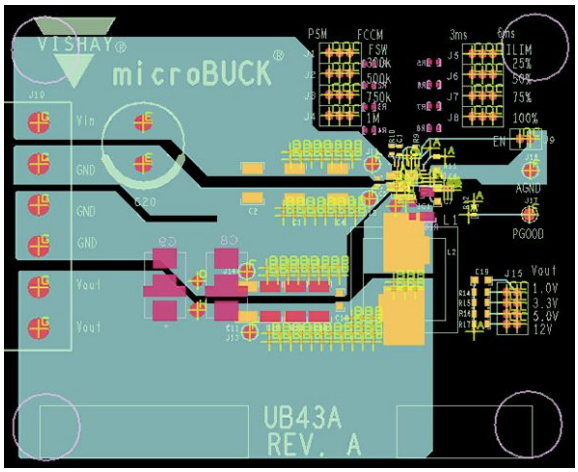


Fig. 3 - Top Layer

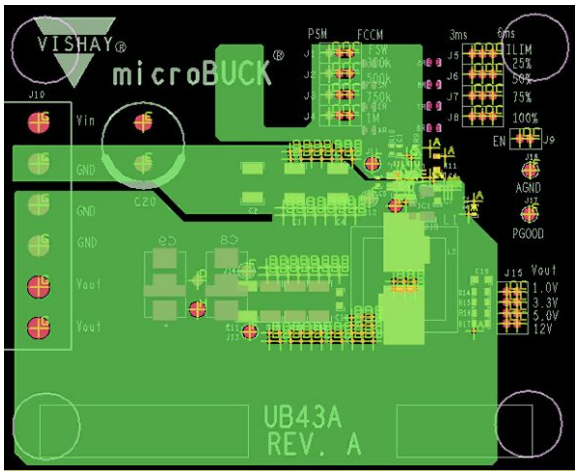


Fig. 6 - Inner Layer 4

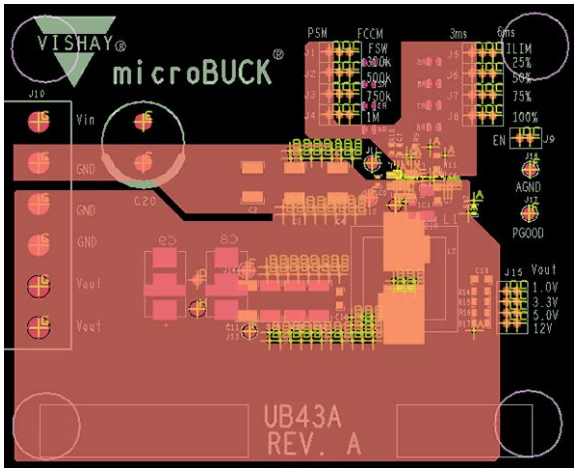


Fig. 4 - Inner Layer 2

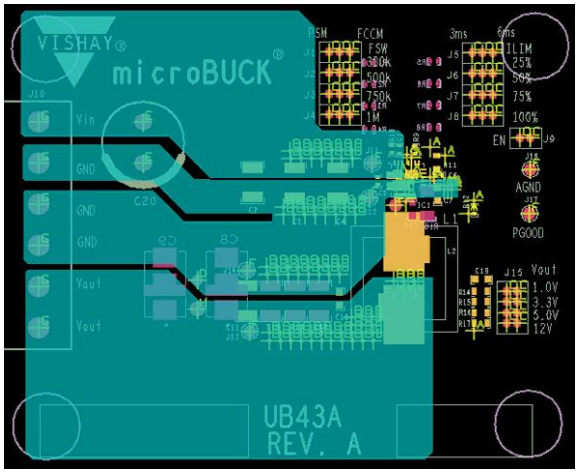


Fig. 7 - Inner Layer 5

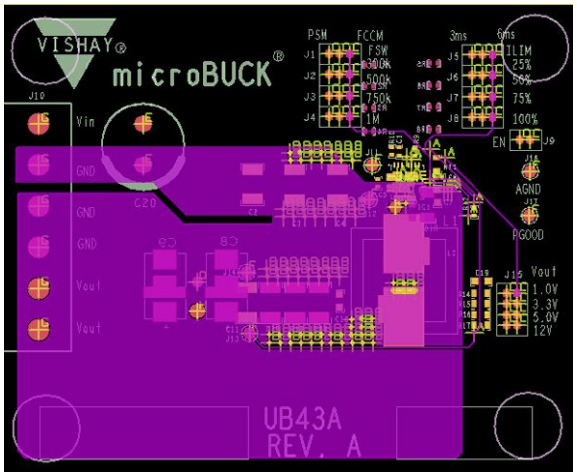


Fig. 5 - Inner Layer 3

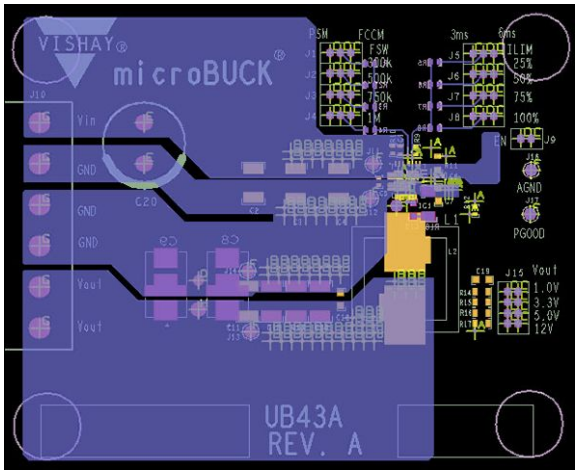


Fig. 8 - Bottom Layer

BILL OF MATERIAL REPORT, SiC431				
SYM_NAME	**COMP_VALUE**	**REFDES**	**PART NUMBER**	**PART RATING**
0402	0.1 µF	C1, C5, C6	GRM155R71H104ME14D	CAP CER 50 V X7R
1210	22 µF	C2, C3, C4	CL32B226KAJNFNE	CAP CER 25 V X7R
0603	1 µF	C7	GCM188R71E105KA64D	CAP CER 25 V X7R
POSCAP	100 µF	C8, C9	20TQC100MYF	CAP TANT POLY 20 V
0603	DNP	C10	-	CAP CER 50 V X7R
1210	22 µF	C11, C12, C13, C14	CL32B226KAJNFNE	CAP CER 25 V X7R
1210	DNP	C15, C16, C17	-	CAP CER 25 V X7R
0603	0.1 µF	C18	GCM188R71E104KA57D	CAP CER 2 5V X7R
0603	DNP	C19	-	CAP CER 25 V X7R
CAP10P2x5	220 µF	C20	UBT1E221M	CAP ALUM 25 V RADIAL
SiC431	SiC431	IC1	-	-
MINIJUMPER3	CON3	J1, J2, J3, J4, J5, J6, J7, J8	M50-3530342	-
CON2	CON2	J9	M50-3530242	-
CON6	CON6	J10	277-1581-ND	-
TP30	VIN+S	J11	36-5000-ND	-
TP30	VO-S	J12	36-5001-ND	-
TP30	VO+S	J13	36-5000-ND	-
TP30	VO-S	J14	36-5001-ND	-
MINIJUMPER 2x4	CON8A	J15	S9015E-04-ND	-
TP30	A_{GND}	J16	36-5001-ND	-
TP30	P_{GOOD}	J17	36-5002-ND	-
ZenithTek	1 µH	L1	ZPWE-101014NA-1R0K (recommended for V_{OUT} = 3.3, or 5 V)	1 µH, 10 %, 0.81 mΩ DCR, 30 A I_{RMS}, 37 A $I_{SAT\ 1}$ at 25 °C (20 % roll off), 30 A $I_{SAT\ 1}$ at 100 °C (20 % roll off)
-	DNP	L1	ZPWE-108075-R22 (recommended for V_{OUT} = 1.0 V)	215 nH, 10 %, 0.29 mΩ DCR, 61 A I_{RMS}, 50 A $I_{SAT\ 1}$ at 25 °C (20 % roll off), 43 A $I_{SAT\ 1}$ at 100 °C (20 % roll off)
			IHLP5050FDER4R7M01 (recommended for V_{OUT} = 12.0 V)	4.7 µH, 20 %, 8.0 mΩ DCR, 13.5 A I_{RMS}, 32 A $I_{SAT\ 1}$ at 25 °C (20 % roll off)
0402	51 kΩ	R1, R5	CRCW040251K0FKED	-
0402	100 kΩ	R2, R6, R9, R12	CRCW0402100KFKED	-
0402	200 kΩ	R3, R7	CRCW0402200KFKED	-
0402	510 kΩ	R4, R8	CRCW0402510KFKED	-
0402	0 Ω	R10	CRCW04020000Z0ED	-
0603	10 kΩ	R11	TNPW060310K0BXEN	-
0603	6.65 kΩ	R14	TNPW06036K65BEEA	-
0603	45.3 kΩ	R15	TNPW060345K3BEEA	-
0603	73.2 kΩ	R16	TNPW060373K2BEEA	-
0603	191 kΩ	R17	TNPW0603191KBEEA	-
1206	DNP	R18	-	-
JUMPER	-	OFF BOARD x3	NPB02SVFN-RC	-