NTMFS4849N

Power MOSFET
30 V, 71 A, Single N−Channel, SO−8FL

Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Thermally Enhanced SO8 Package
- These are Pb−Free Devices

Applications
- Refer to Application Note AND8195/D
- CPU Power Delivery
- DC−DC Converters
- High Side Switching

ON Semiconductor®

http://onsemi.com

V$_{(BR)DSS}$	R$_{DS(ON)}$ MAX	I$_D$ MAX
30 V	5.1 mΩ @ 10 V	71 A
	7.9 mΩ @ 4.5 V	

N−CHANNEL MOSFET

D (5,6)

G (4)

S (1,2,3)

MAXIMUM RATINGS (T$_J$ = 25°C unless otherwise stated)

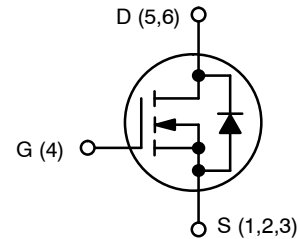| Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V$_{DSS}$	30	V
Gate−to−Source Voltage			V$_{GS}$	±16	V
Continuous Drain Current R$_{\theta JA}$ (Note 1)	Steady State	T$_A$ = 25°C	I$_D$	16.1	A
		T$_A$ = 85°C		11.6	
Power Dissipation R$_{\theta JA}$ (Note 1)		T$_A$ = 25°C	P$_D$	2.17	W
Continuous Drain Current R$_{\theta JA}$ ≤ 10 sec		T$_A$ = 25°C	I$_D$	26.0	A
		T$_A$ = 85°C		18.8	
Power Dissipation R$_{\theta JA}$, t ≤ 10 sec		T$_A$ = 25°C	P$_D$	5.7	W
Continuous Drain Current R$_{\theta JA}$ (Note 2)		T$_A$ = 25°C	I$_D$	10.2	A
		T$_A$ = 85°C		7.3	
Power Dissipation R$_{\theta JA}$ (Note 2)		T$_A$ = 25°C	P$_D$	0.87	W
Continuous Drain Current R$_{\theta JC}$ (Note 1)		T$_C$ = 25°C	I$_D$	71	A
		T$_C$ = 85°C		51	
Power Dissipation R$_{\theta JC}$ (Note 1)		T$_C$ = 25°C	P$_D$	42.4	W
Pulsed Drain Current	t$_p$=10μs	T$_A$ = 25°C	I$_{DM}$	142	A
Current limited by package		T$_A$ = 25°C	I$_{Dmaxpkg}$	100	A
Operating Junction and Storage Temperature			T$_J$, T$_{STG}$	−55 to +150	°C
Source Current (Body Diode)			I$_S$	42	A
Drain to Source dV/dt			dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (V$_{DD}$ = 50 V, V$_{GS}$ = 10 V, I$_L$ = 27 A$_{pk}$, L = 0.3 mH, R$_G$ = 25 Ω)			EAS	109	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T$_L$	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
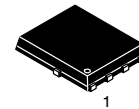

SO−8 FLAT LEAD CASE 488AA STYLE 1

MARKING DIAGRAM

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4849N
AYWZZ
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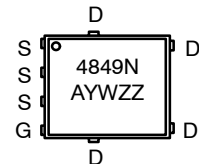
A	= Assembly Location
Y	= Year
W	= Work Week
ZZ	= Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4849NT1G	SO−8FL (Pb−Free)	1500 / Tape & Reel
NTMFS4849NT3G	SO−8FL (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMFS4849N

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	2.95	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	57.6	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	143.3	
Junction−to−Ambient − t $\leq$ 10 sec	$R_{\theta JA}$	21.95	

1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				25.2		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25 °C			1	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = $\pm$16 V				$\pm$100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.45	1.9	2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V to 11.5 V	I_D = 30 A		3.9	5.1	mΩ
			I_D = 15 A		3.9		
		V_{GS} = 4.5 V	I_D = 30 A		6.2	7.9	
			I_D = 15 A		6.1		
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 30 A			62		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 12 V			2040		pF
Output Capacitance	C_{OSS}				361		
Reverse Transfer Capacitance	C_{RSS}				181		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A			15	22	nC
Threshold Gate Charge	$Q_{G(TH)}$				2.2		
Gate−to−Source Charge	Q_{GS}				5.7		
Gate−to−Drain Charge	Q_{GD}				5.1		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 11.5 V, V_{DS} = 15 V, I_D = 30 A			34.6		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			15.6		ns
Rise Time	t_r				45.1		
Turn−Off Delay Time	$t_{d(OFF)}$				18.2		
Fall Time	t_f				5.7		

3. Pulse Test: pulse width $\leq$ 300 μs, duty cycle $\leq$ 2%.
4. Switching characteristics are independent of operating junction temperatures.

NTMFS4849N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 11.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			9.4		ns
Rise Time	t_r				19.4		
Turn−Off Delay Time	$t_{d(OFF)}$				25.3		
Fall Time	t_f				4.4		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 30 A	T_J = 25°C		0.84	1.0	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 30 A			12.5		ns
Charge Time	t_a				8.3		
Discharge Time	t_b				4.2		
Reverse Recovery Charge	Q_{RR}				3.0		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			0.93		nH
Drain Inductance	L_D				0.005		
Gate Inductance	L_G				1.84		
Gate Resistance	R_G				0.9		Ω

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS
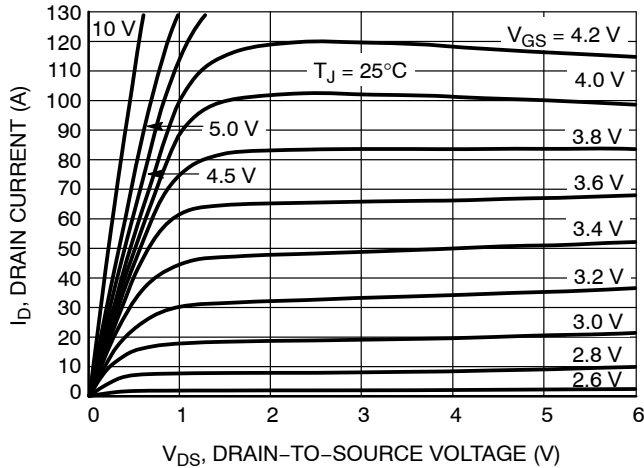
Figure 1. On−Region Characteristics
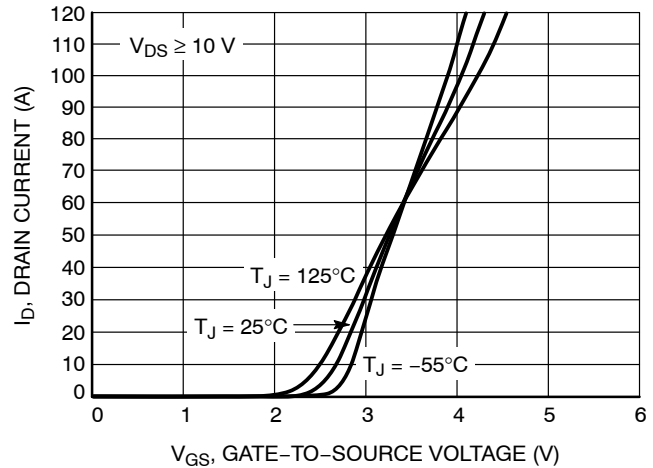
Figure 2. Transfer Characteristics

TYPICAL CHARACTERISTICS
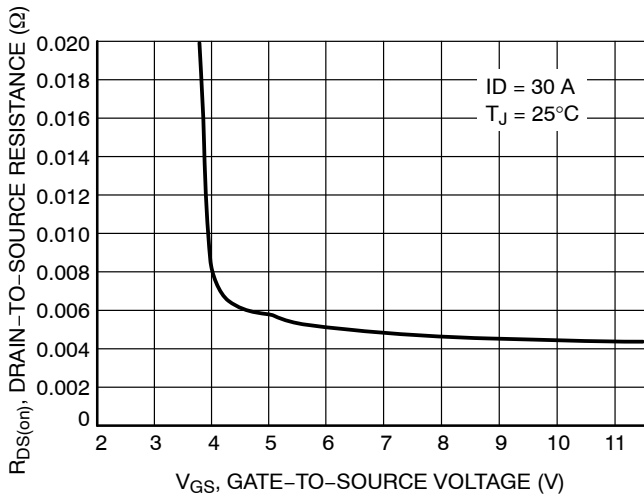
Figure 3. On−Resistance vs. Gate-to-Source Voltage
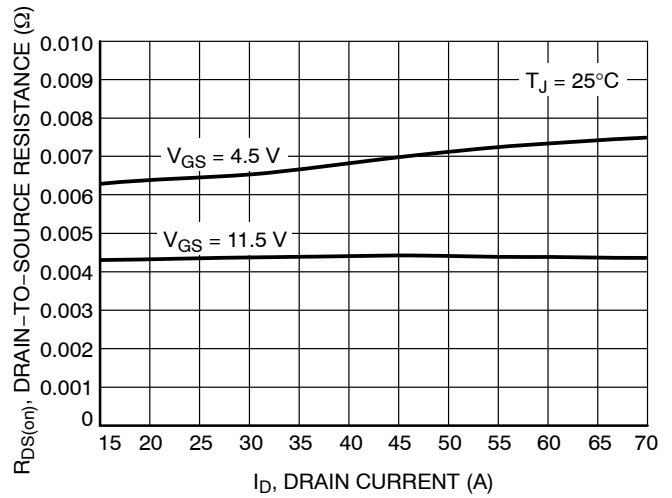
Figure 4. On−Resistance vs. Drain Current and Gate Voltage
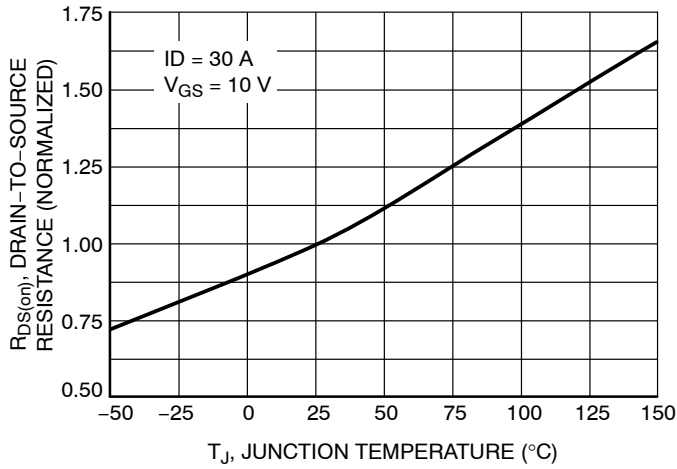
Figure 5. On−Resistance Variation with Temperature
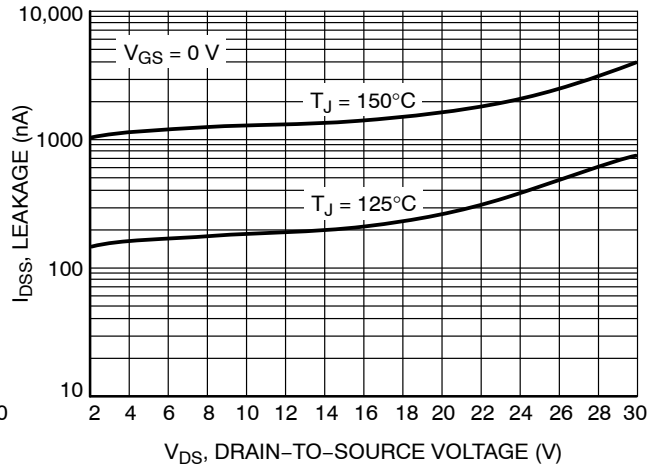
Figure 6. Drain−to−Source Leakage Current vs. Voltage
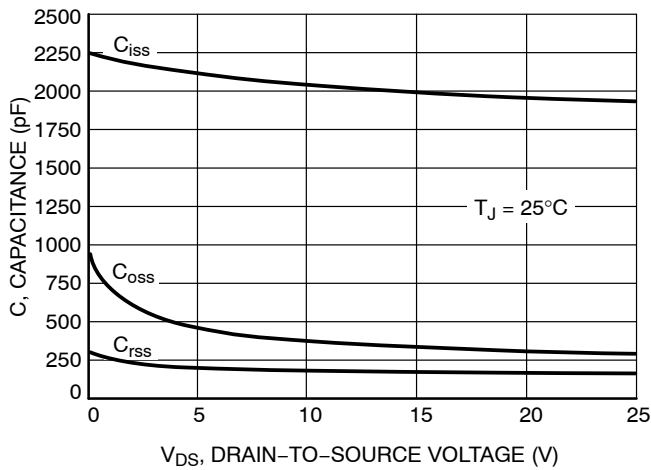
Figure 7. Capacitance Variation
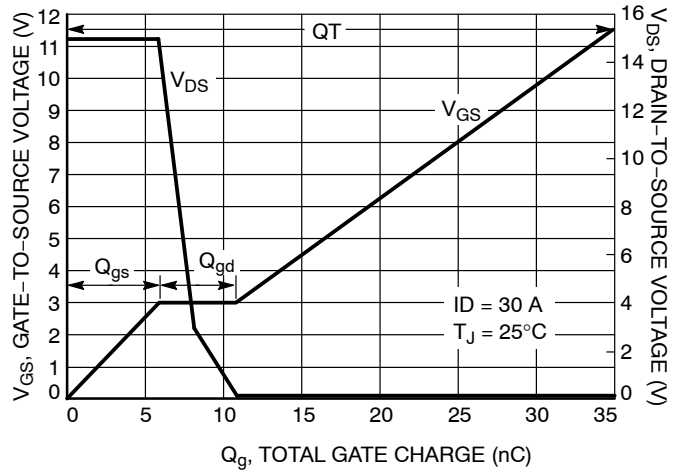
Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge
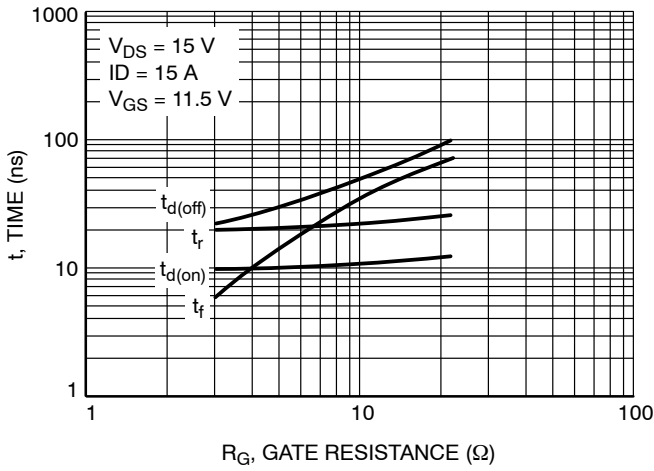
TYPICAL CHARACTERISTICS

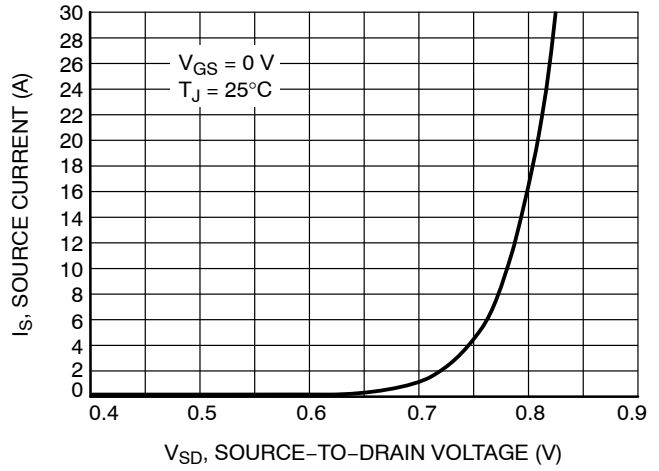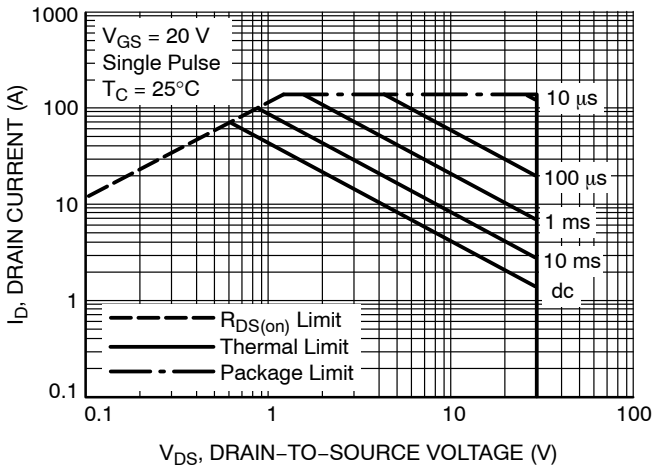**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

Figure 10. Diode Forward Voltage vs. Current

Figure 11. Maximum Rated Forward Biased Safe Operating Area
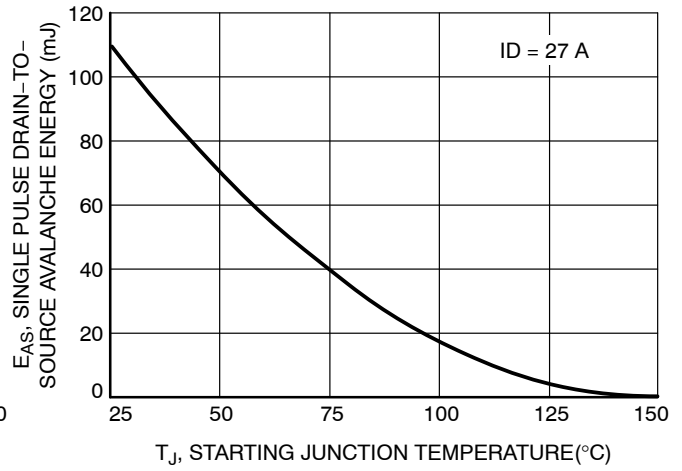
Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature
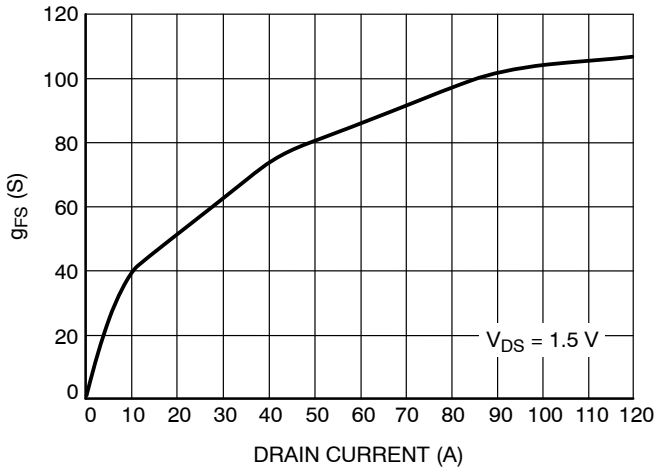
Figure 13. g_{FS} vs. Drain Current
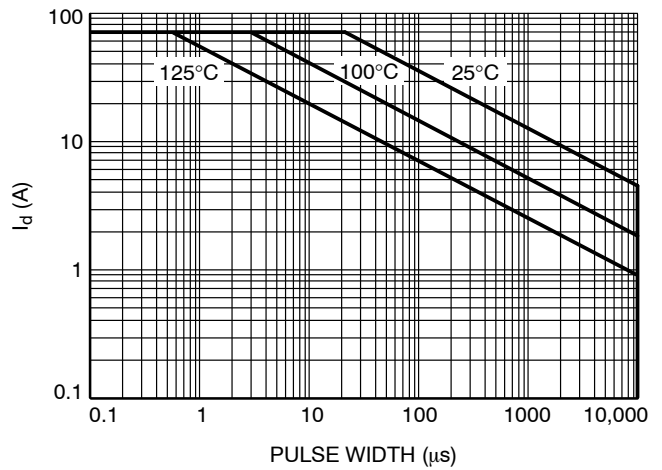
Figure 14. Avalanche Characteristics

onsemi

**DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N**

SCALE 2:1

DATE 25 JUN 2018

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

2 X | 0.20 | C

D
▶ | A |
2
D1
| B | 2 X
| 0.20 | C
E1
E
2

TOP VIEW

4 X
θ
c
A1
| C |
SEATING PLANE

DETAIL A

| | 0.10 | C |
| | 0.10 | C |
A

SIDE VIEW — DETAIL A

8X **b**
| ⊕ | 0.10 | C | A | B |
| | 0.05 | c |
e/2
e
L
1 | 4
K
E2
PIN 5
(EXPOSED PAD)
L1 | M
G
D2

BOTTOM VIEW

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	---	12 °

**GENERIC
MARKING DIAGRAM***

1
XXXXXX
AYWZZ

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

**RECOMMENDED
SOLDERING FOOTPRINT***

2X
0.495
2X
1.530
4.560
2X
1.530
3.200
4.530
2X
0.475
1.330
2X
0.905
1
0.965
4X
1.000
1.270
PITCH
4X 0.750

DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| DESCRIPTION: | DFN5 5x6, 1.27P (SO−8FL) | | PAGE 1 OF 1 |

ADDITIONAL INFORMATION

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