

# 74AHC1G02; 74AHCT1G02

## 2-input NOR gate

Rev. 8 — 11 January 2022

Product data sheet

## 1. General description

The 74AHC1G02; 74AHCT1G02 is a single 2-input NOR gate. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

## 2. Features and benefits

- Wide supply voltage range from 2.0 to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Symmetrical output impedance
- Balanced propagation delays
- Input levels:
  - For 74AHC1G02: CMOS level
  - For 74AHCT1G02: TTL level
- ESD protection:
  - HBM JESD22-A114E: exceeds 2000 V
  - MM JESD22-A115-A: exceeds 200 V
  - CDM JESD22-C101C: exceeds 1000 V
- Specified from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G02GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHCT1G02GW				
74AHC1G02GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74AHCT1G02GV				

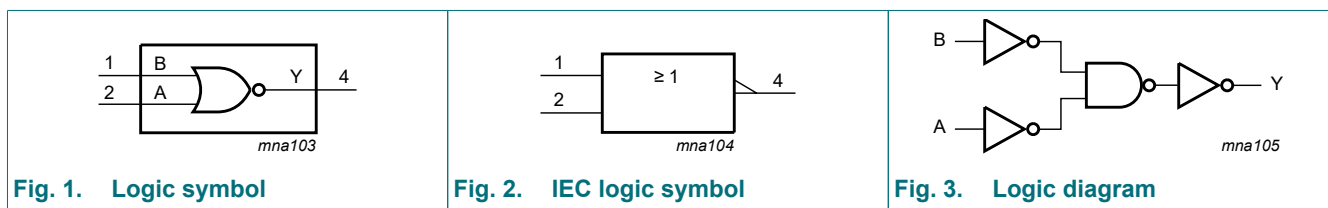
## 4. Marking

Table 2. Marking codes

Type number	Marking <sup>[1]</sup>
74AHC1G02GW	AB
74AHC1G02GV	A02
74AHCT1G02GW	CB
74AHCT1G02GV	C02

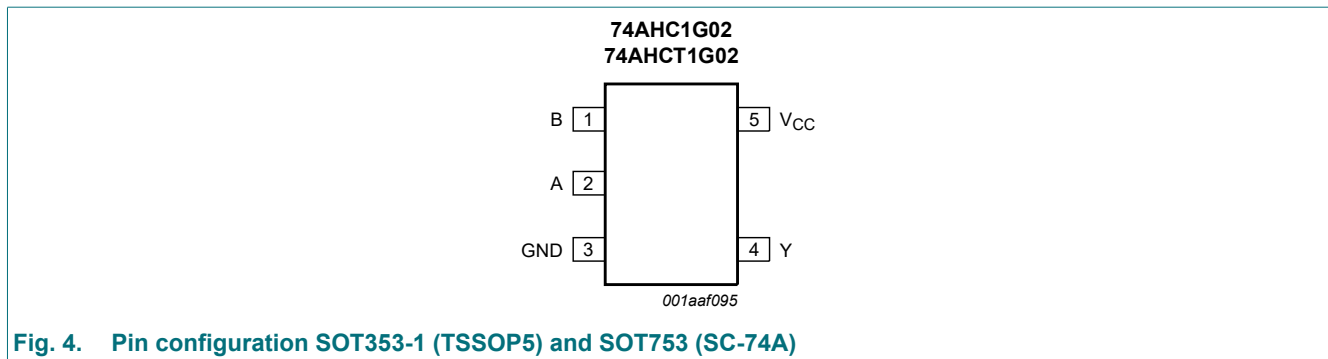
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram



## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input B
A	2	data input A
GND	3	ground (0 V)
Y	4	data output Y
V <sub>CC</sub>	5	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level.*

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
$I_O$	output current	$-0.5$ V < $V_O$ < $V_{CC} + 0.5$ V	-	±25	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.  
For SOT753 (SC-74A) package:  $P_{tot}$  derates linearly with 3.8 mW/K above 85 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	74AHC1G02			74AHCT1G02			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC1G02</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	µA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF
<b>74AHCT1G02</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	µA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = 3.4$ V; other inputs at $V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance		-	1.5	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

$GND = 0$  V;  $t_r = t_f = \leq 3.0$  ns. For test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC1G02</b>										
$t_{pd}$	propagation delay	A and B to Y; see Fig. 5 [1]								
		$V_{CC} = 3.0$ V to 3.6 V [2]								
		$C_L = 15$ pF	-	4.4	7.9	1.0	9.5	1.0	10.5	ns
		$C_L = 50$ pF	-	6.3	11.4	1.0	13	1.0	14.5	ns
		$V_{CC} = 4.5$ V to 5.5 V [3]								
		$C_L = 15$ pF	-	3.2	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50$ pF	-	4.6	7.5	1.0	8.5	1.0	9.5	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = GND$ to $V_{CC}$ [4]	-	18	-	-	-	-	-	pF
<b>74AHCT1G02</b>										
$t_{pd}$	propagation delay	A and B to Y; see Fig. 5 [1]								
		$V_{CC} = 4.5$ V to 5.5 V [3]								
		$C_L = 15$ pF	-	3.5	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50$ pF	-	4.9	7.5	1.0	8.5	1.0	9.5	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = GND$ to $V_{CC}$ [4]	-	19	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2] Typical values are measured at  $V_{CC} = 3.3$  V.

[3] Typical values are measured at  $V_{CC} = 5.0$  V.

[4]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu$ W).

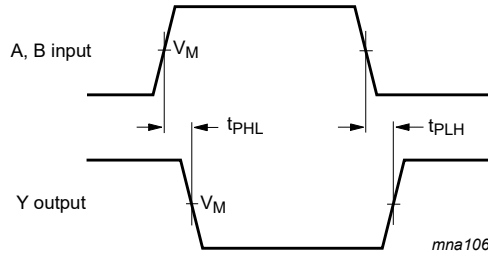
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volt.

11.1. Waveform and test circuit

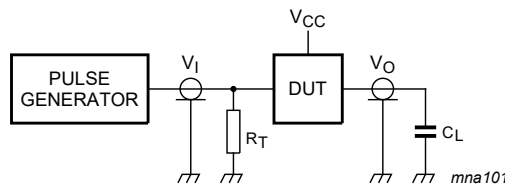


Measurement points are given in [Table 9](#).

Fig. 5. The inputs (A and B) to output (Y) propagation delays

Table 9. Measurement point

Type	Input		Output
	V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>
74AHC1G02	GND to V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>
74AHCT1G02	GND to 3.0 V	1.5 V	0.5 × V <sub>CC</sub>



Test data is given in [Table 8](#).

Definitions for test circuit:

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

Fig. 6. Test circuit for measuring switching times

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig. 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

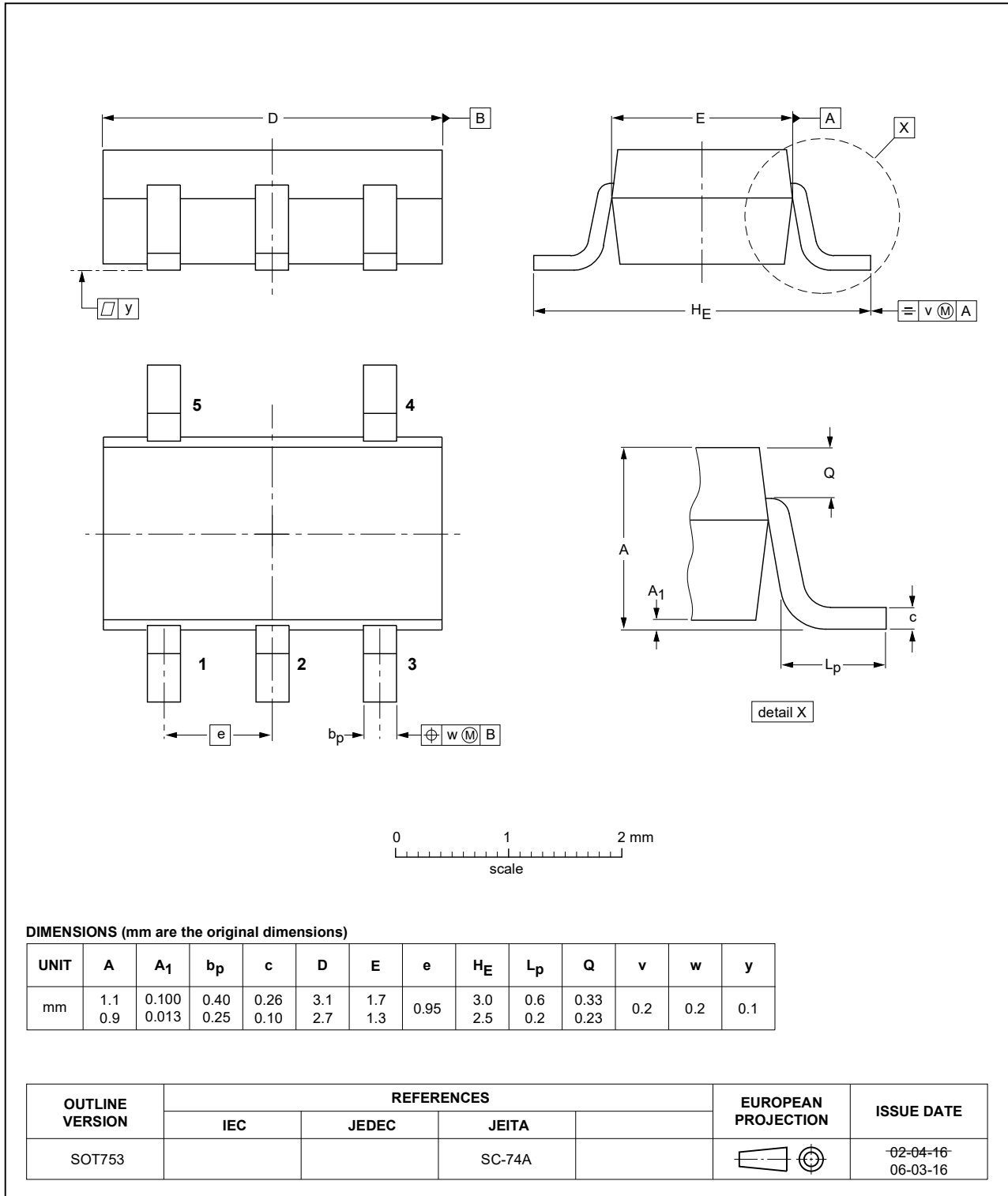


Fig. 8. Package outline SOT753 (SC-74A)



## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G02 v.8	20220111	Product data sheet	-	74AHC_AHCT1G02 v.7
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Fig. 7SOT353-1</a> (TSSOP5) package outline drawing has changed.</li> <li><a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74AHC_AHCT1G02 v.7	20141106	Product data sheet	-	74AHC_AHCT1G02 v.6
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 4</a>: table note added.</li> </ul>			
74AHC_AHCT1G02 v.6	20070530	Product data sheet	-	74AHC_AHCT1G02 v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Package SOT353 changed to SOT353-1 in <a href="#">Section 3</a> and <a href="#">Section 12</a>.</li> <li>Quick reference data and Soldering sections removed.</li> </ul>			
74AHC_AHCT1G02 v.5	20020527	Product specification	-	74AHC_AHCT1G02 v.4
74AHC_AHCT1G02 v.4	20020215	Product specification	-	74AHC_AHCT1G02 v.3
74AHC_AHCT1G02 v.3	20010131	Product specification	-	74AHC_AHCT1G02 v.2
74AHC_AHCT1G02 v.2	19990127	Product specification	-	74AHC_AHCT1G02_N v.1
74AHC_AHCT1G02_N v.1	19981125	Preliminary specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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