SEC1100/SEC1200

Smart Card Bridge to Full-Speed USB, SPI, and UART Interfaces

PRODUCT FEATURES

Data Brief

General Description

The SEC1100 and SEC1200 provide a single-chip solution for a Smart Card bridge to USB, SPI, and UART interfaces. These bridges are controlled by an enhanced 8051 micro controller and all chip peripherals are accessed and controlled through the SFR or XDATA register space. SMSC's TrustSpan™ Technology enables digital systems to securely communicate, process, move and store information on system boards, across networks and through the cloud.

General Features

- Smart Card
  - The SEC1100 provides one Smart Card interface and the SEC1200 provides two
  - Fully compliant with ISO/IEC 7816, EMV, and PC/SC standards
  - Versatile ETU rate generation, supporting current and proposed rates (up to 826 Kbps)
  - Full support of both T=0 and T=1 protocols
  - Full-packet FIFO (259 bytes), for transmit and receive
  - Half-duplex operation (no software intervention required between transmit and receive phases of exchange)
  - Loose real-time response required of software (approximately 180 ms)
  - Dynamically programmable FIFO threshold with byte granularity
  - Time-out FIFO flush interrupt, independent of threshold
  - Programmable Smart Card clock frequency
  - UART-like register file structure, expanded to 4 banks of 16 registers
  - Supports Class A, Class B, Class C, or Class AB Smart Cards (1.8 V, 3.0 V and 5.0 V cards)
  - Automatic character repetition for T=0 protocol parity error recovery
  - Automatic card deactivation on card removal and on other system events, including persistent parity errors
  - Internal procedure byte filtering for T=0 protocol
  - Protocol timers (Guard, Timeout, and CWT) for EMV-defined timing parameters
    - Detection of an unresponsive card
    - Activation/deactivation sequences
    - Cold/warm resets
    - Monitoring for all EMV timing constraints
    - 16-bit general purpose down counter for software timing use
  - Fully compliant ESD protection on card pins
- USB
  - Full-speed (12 Mbps) USB operation compliant to the USB 2.0 Specification
  - Integrated USB 1.5 K pull-up resistor
  - Integrated USB devices controller with:
    - 8/16/32/64 byte control buffer
    - Five 8/16/32/64 byte programmable (bulk/interrupt) endpoint buffers
- 8051 Processor
  - Reduced instruction cycle time (approximately 9 times 80C51)
  - 16 MHz max clock speed
  - Enhanced peripherals; three 16-bit timers, watchdog timer, interrupt controller, JTAG
  - OTP (One Time Programmable) ROM
    - 16 KB
  - RAM
    - 1.5 KB
- UART (SEC1200 only)
  - Standard PC baud rates supported
  - 1 M baud high-speed rate (not PC standard)
- SPI (SEC1200 only)
  - Master and Slave capability with 12 MHz max performance
- General
  - 5.0 V tolerance on user accessible IO pins
  - Self-clocking internal oscillator, no external crystal required
  - 3.0 V - 5.5 V supply input
    - Internal 4.8 V comparator disables Class A card support if the input voltage is too low

Applications

- USB Smart Card reader
- SPI-based Smart Card reader
- UART-based Smart Card reader
- Dual Smart Card reader

PRODUCT PREVIEW

Order Numbers:

ORDER NUMBERS	LEAD-FREE ROHS COMPLIANT PACKAGE	PACKAGE/ REEL SIZE	TEMPERATURE RANGE
SEC1100-A5-xx	16QFN	5x5 mm	0ºC to 70ºC
SEC1200-CN-xx	24QFN		
SEC1202-HZE-xx	48QFN		

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI

Overview

The SEC1100 and SEC1200 provide a single-chip solution for a Smart Card bridge to USB, SPI, and UART interfaces. These bridges are controlled by an enhanced 8051 micro controller and all chip peripherals are accessed and controlled through the SFR or XDATA register space.

Feature Highlights

- Smart Card
  - Fully compliant with standards: ISO/IEC 7816, EMV 4.2 (May 2008), and PC/SC
  - Versatile ETU rate generation, supporting current and proposed rates (to 826 Kbps and beyond)
  - Full support of both T=0 and T=1 protocols
  - Full-packet FIFO (259 bytes), for transmit and receive
  - Half-duplex operation, with no software intervention required between Transmit and Receive phases of an exchange
  - Very loose real-time response required of software: approximately 180 ms worst case
  - Dynamically programmable FIFO threshold, with byte granularity
  - Time-out FIFO flush interrupt, independent of threshold
  - Programmable Smart Card clock frequency
  - UART-like register file structure
  - Supports Class A, Class B, Class C, or Class AB Smart Cards (all 1.8 V, 3.0 V and 5.0 V cards)
  - Automatic character repetition for T=0 protocol parity error recovery
  - Automatic card deactivation on card removal and on other system events, including persistent parity errors
  - Internal procedure byte filtering for T=0 protocol
  - Protocol timers (guard, time-out and CWT) for EMV-defined timing parameters
    - Detection of an unresponsive card
    - Activation/deactivation sequences
    - Cold/warm resets
    - Monitoring for all EMV timing constraints
    - 16-bit general purpose down counter for software timing use
  - Fully compliant ESD protection on card pins per JESD22-A114D (March 2006) and JESD22-A115A “Machine Model” from AN1181
  - Fully EMV compliant, internal signal current limits
  - 3.3 V internal operation with 5.0 V tolerant buffers where required
  - Self-contained management of Smart Card power:
    - $SC1_{VCC}$ and $SC2_{VCC}$, supply output
    - Regulator for 3.0 V, and 5.0 V from supply input
    - Current limiter with over-current sense interrupt (short circuit detect)
    - Hardware-guaranteed, compliant deactivation sequence on card removal
    - Synchronous card support
- USB
  - Full-Speed (12 Mbps) USB operation compliant with the *USB 2.0 Specification*
  - Integrated USB 1.5 K pull-up resistor
  - Integrated USB devices controller with:
    - 8/16/32/64 byte control endpoint 0 buffer
    - Five 8/16/32/64 byte programmable (bulk/interrupt) endpoint buffers
- 8051
  - Reduced instruction cycle time (approximately 9 times 80C51)
  - 16 MHz max clock speed
  - Enhanced peripherals: three 16-bit timers, watch dog timer, interrupt controller, JTAG
  - 16 KB One Time Programmable (OTP) ROM

  - 1.5 KB RAM
- UART
  - Standard PC (9600, 19200, 38400 and 115200) baud rates supported
  - 1 M baud high-speed rate (non-PC standard)
- SPI
  - Master and Slave capability with 12 MHz max performance
- General
  - 5.0 V tolerance on user accessible IO pins
  - Self-clocking internal oscillator, no external crystal required
  - 3.0 V-5.5 V supply input
  - Internal 4.8 V comparator disables Class A card support if the input voltage is too low

PRODUCT PREVIEW

Block Diagrams

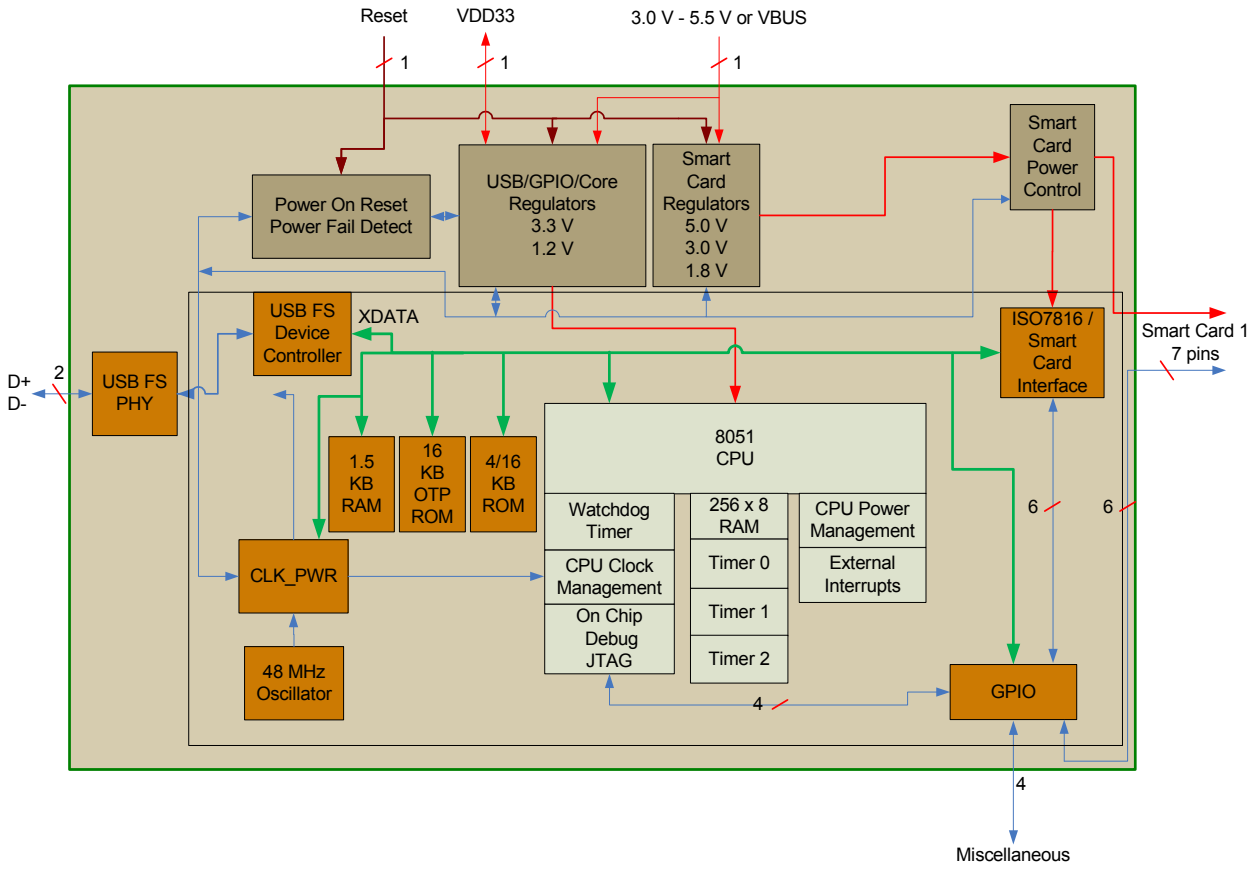


Figure 1 SEC1100 Block Diagram

PRODUCT PREVIEW

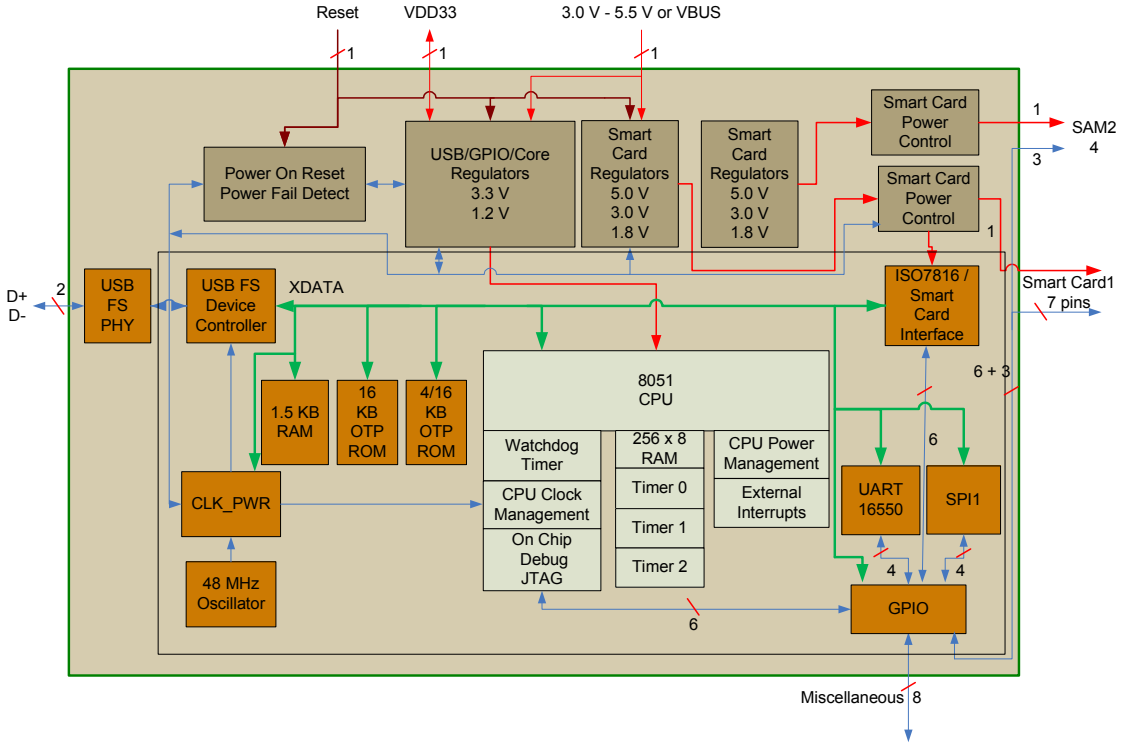


Figure 2 SEC1200 Block Diagram

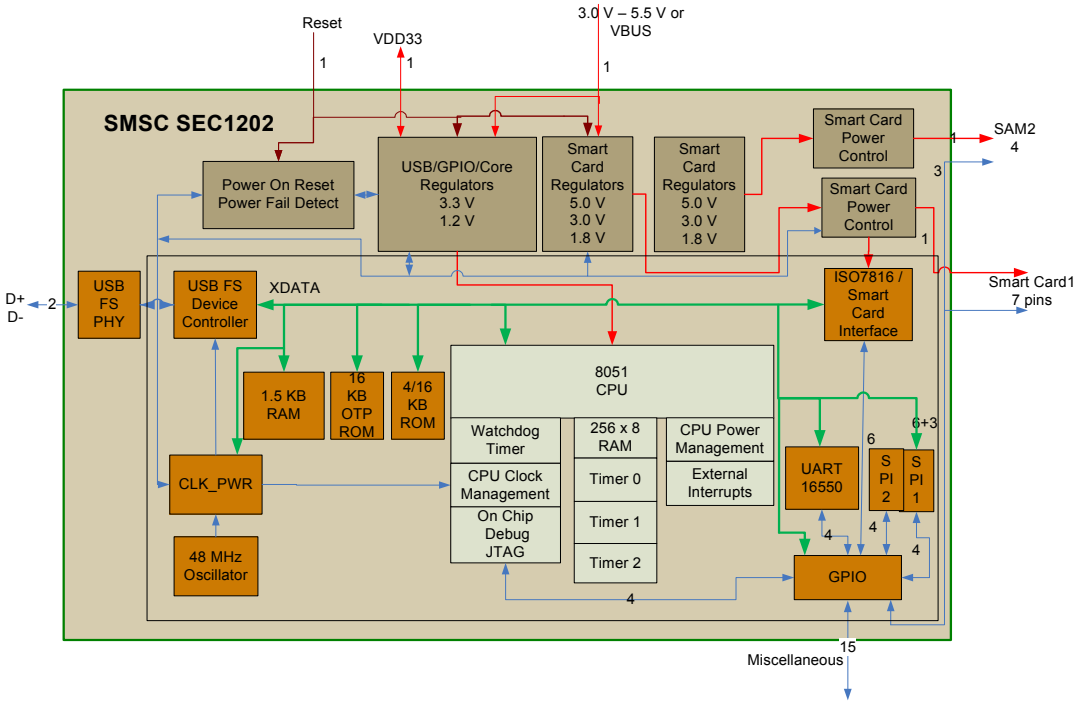
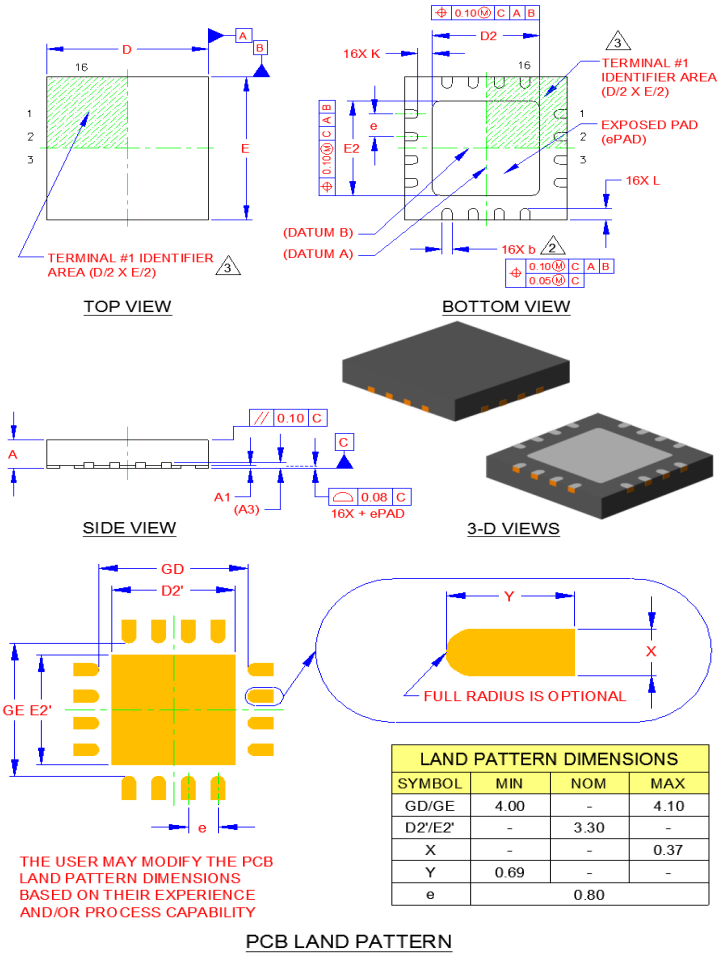


Figure 3 SEC1202 Block Diagram

PRODUCT PREVIEW

Package Outlines



LAND PATTERN DIMENSIONS

SYMBOL	MIN	NOM	MAX
GD/GE	4.00	-	4.10
D2'/E2'	-	3.30	-
X	-	-	0.37
Y	0.69	-	-
e		0.80	

Figure 4 SEC1100 16-Pin QFN Package Outline

Table 1 Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	0.80	0.90	1.00	Overall Package Height
A1	0	0.02	0.05	Standoff
A3		0.20 REF		Lead-Frame Thickness
D/E	4.90	5.00	5.10	X/Y Body Size
D2/E2	3.20	3.30	3.40	X/Y Exposed Pad Size
L	0.35	0.40	0.45	Terminal Length
b	0.25	0.30	0.35	Terminal Width (Note 2)
K	0.35	0.45	-	Terminal to Pad Distance
e		0.80 BSC		Terminal Pitch

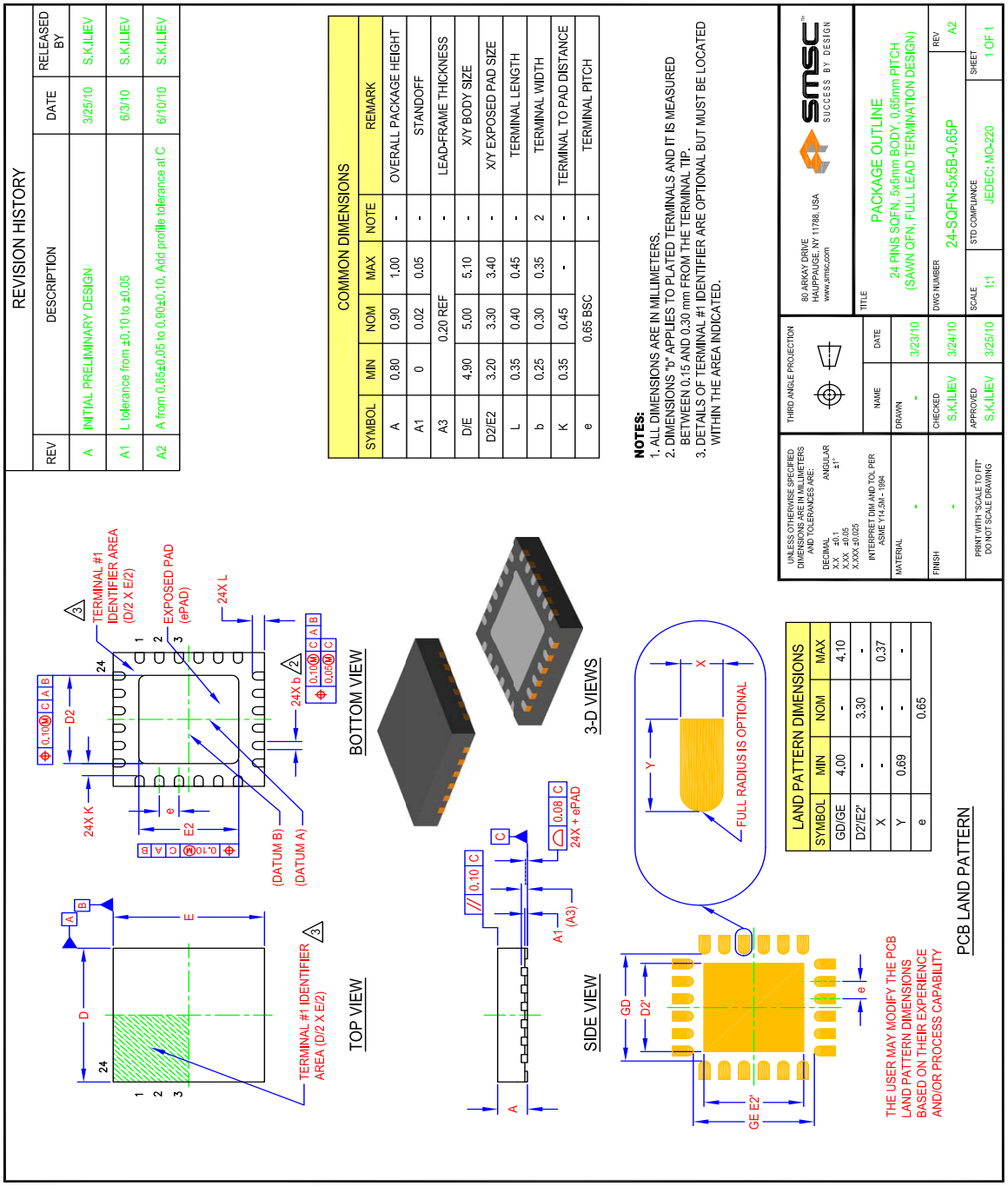


Figure 5 SEC1200 24-Pin QFN Package Outline

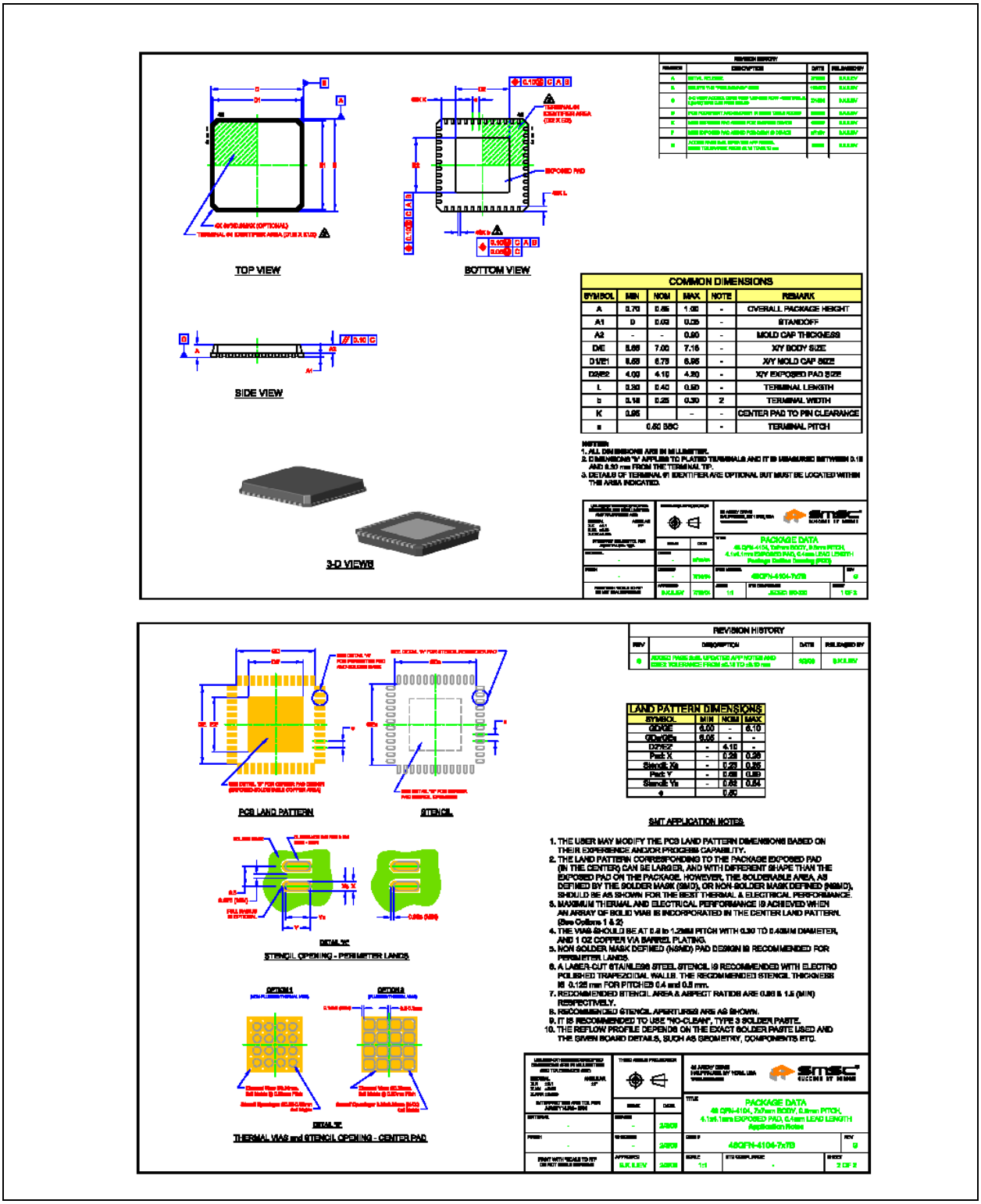


Figure 6 SEC1202 48-pin QFN Package Outline