

Preliminary

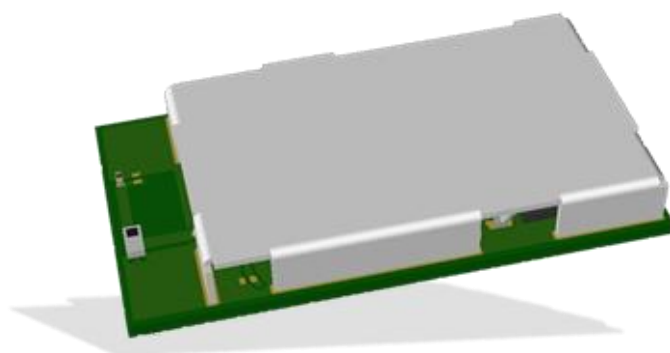
**Panasonic**  
INDUSTRY

# PAN9520

Embedded Wi-Fi Module

## Product Specification

Rev. 0.1



## Overview

The PAN9520 is a 2.4 GHz ISM band Wi-Fi embedded module based on Espressif ESP32-S2, which includes a wireless radio and a MCU for easy integration of Wi-Fi connectivity into various electronic devices.

## Features

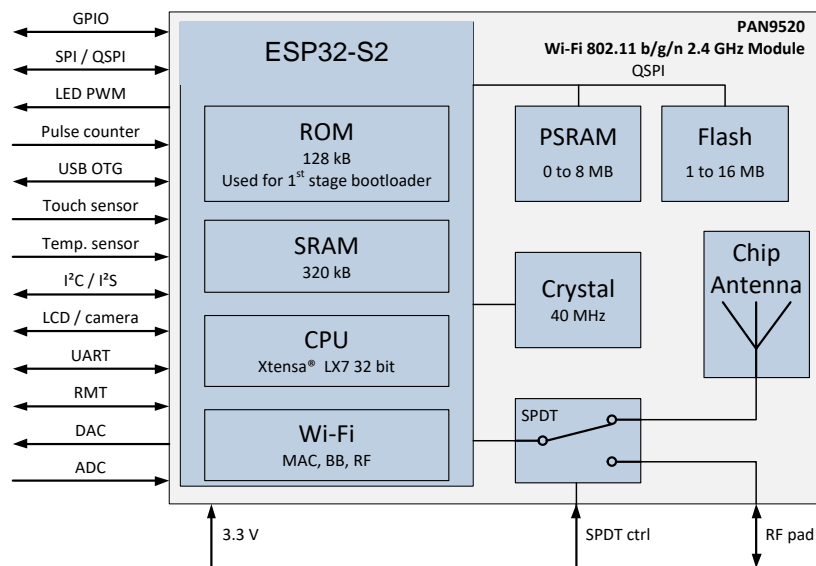
- Embedded 2.4 GHz Wi-Fi 802.11 b/g/n module
- Xtensa® single-core 32-bit LX7 microprocessor, up to 240 MHz
- Chip internal 128 kB ROM, 320 kB SRAM, and 16 kB low power SRAM
- Integrated QSPI Flash and PSRAM (density depends on product version)
- Ultra-Low Power (ULP) co-processor usable in deep sleep mode
- All security features required for WPA2 and WPA3 personal
- Espressif Integrated Development Framework (ESP-IDF) with a multitude of examples available for software development
- Supports 20 MHz and 40 MHz bandwidths in 2.4 GHz band with data rates up to 150 Mbps
- Simultaneous support for Infrastructure Station, SoftAP, and promiscuous modes
- 802.11mc Fine Time Measurement (FTM)

- 43x programmable GPIOs with a rich set of alternative functionalities:
  - 2x 12-bit SAR ADCs, up to 20 channels
  - 2x 8-bit DAC
  - 14x touch sensing IOs
  - 4x SPI (2x available for general purpose)
  - 1x I<sup>2</sup>S
  - 2x I<sup>2</sup>C
  - 2x UART
  - RMT (Tx/Rx)
  - LED PWM, up to 8 channels
  - 1x full-speed USB OTG
  - 1x DVP 8/16 camera interface (I<sup>2</sup>S resources used)
  - 1x LCD interface (SPI2 resources used)
  - 1x LCD interface (I<sup>2</sup>S resources used)

## Characteristics

- Surface Mount Type (SMT):  
24 mm × 13 mm × 3.1 mm
- Tx power up to 19.5 dBm at IEEE 802.11b 1 Mbps
- Rx sensitivity of -97 dBm at IEEE 802.11b 1 Mbps
- Power supply 3 V to 3.6 V
- Current consumption 190 mA Tx (average at 11b, 1 Mbps), 68 mA Rx (40 MHz channel), 310 mA Tx peak
- Deep sleep mode <100 µA typical power consumption (RTC timer only and VDD\_SPI disconnected)
- Wide temperature range from -40 °C to 85 °C

## Block Diagram



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## 1 About This Document



### 1.1 Purpose and Audience

This Product Specification provides details on the functional, operational, and electrical characteristics of the Panasonic PAN9520 module. It is intended for hardware design, application, and Original Equipment Manufacturers (OEM) engineers. The product is referred to as “the PAN9520” or “the module” within this document.

### 1.2 Revision History

Revision	Date	Modifications/Remarks
0.1	2020-08-12	First preliminary version

### 1.3 Use of Symbols

Symbol	Description
	<p><b>Note</b></p> <p>Indicates important information for the proper use of the product. Non-observance can lead to errors.</p>
	<p><b>Attention</b></p> <p>Indicates important notes that, if not observed, can put the product's functionality at risk.</p>
⇒ [chapter number] [chapter title]	<p><b>Cross reference</b></p> <p>Indicates cross references within the document.</p> <p><b>Example:</b></p> <p>Description of the symbols used in this document ⇒ 1.3 Use of Symbols.</p>

### 1.4 Related Documents

For related documents please refer to the Panasonic website ⇒ [7.2.2 Product Information](#).

## 2 Overview

The PAN9520 is a 2.4 GHz 802.11 b/g/n embedded Wi-Fi module based on Espressif ESP32-S2 that includes the powerful Xtensa 32-bit LX7 CPU. An integrated chip antenna, and QSPI memory enable the module to be used in a variety of stand-alone or host-controlled applications. The integrated crystal ensures connection performance over full temperature range and lifetime. Besides, the module offers a rich set of peripherals like full-speed USB OTG, SPI, UART, I<sup>2</sup>C, and many more.

The PAN9520 combines a high-performance CPU, high-sensitivity wireless radio, baseband (BB) processor, Medium Access Controller (MAC), encryption unit, ROM bootloader, chip-internal SRAM, and module-internal QSPI flash and PSRAM. Features as CCMP, TKIP, WAPI, WEP, BIP, and an AES<sup>1</sup> accelerator enable the usage of secure data connections.

Parallel support of access point and station mode allows easy setup of simultaneous Wi-Fi connections from the module to smart devices and home network routers.

With the Espressif Integrated Development Framework (ESP-IDF), software can be developed for a wide range of applications. At the same time, a huge number of software examples can be used as starting point for the development.



Please note that the ESP-IDF is provided by Espressif Systems. Always use the latest updates <https://github.com/espressif/esp-idf>.

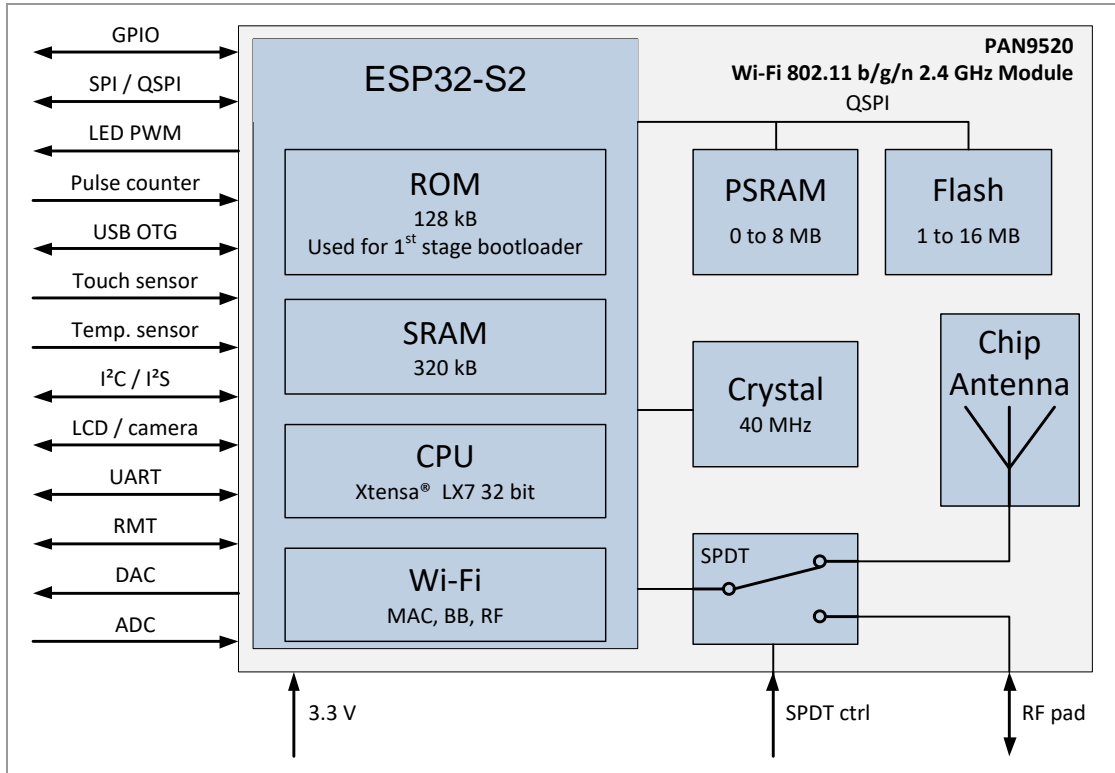
For related documents please refer to ⇒ [7.2.2 Product Information](#).

For further information on the variants and versions please refer to ⇒ [7.1 Ordering Information](#).

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<sup>1</sup> Counter Mode with CBC-MAC Protocol (CCMP); Temporary Key Integrity Protocol (TKIP); WLAN Authentication and Privacy Infrastructure (WAPI); Wired Equivalent Privacy (WEP); Broadcast/Multitask Integrity Protocol (BIP); Advanced Encryption Standard (AES)

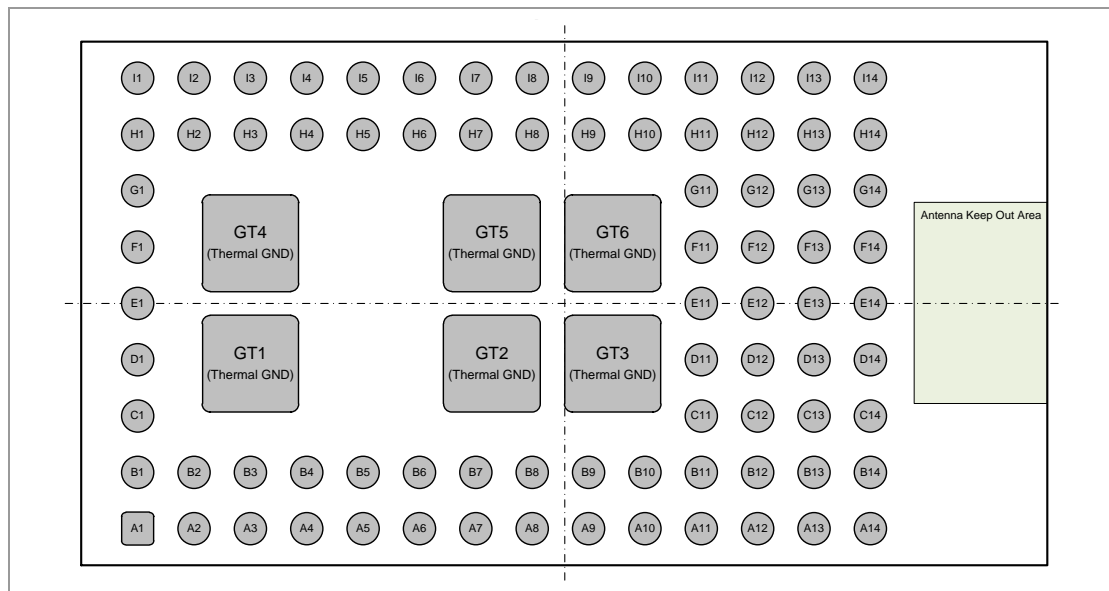
## 2.1 Block Diagram



## 2.2 Pin Configuration

### Pin Assignment

#### Top View



### Pin Functions

No.	Pin Name	Pin Type	Description
A1	GND	Ground Pin	Connect to ground
A2	GPIO35	Digital I/O	SPIIO6, GPIO35, FSPID
A3	GPIO36	Digital I/O	SPIIO7, GPIO36, FSPICLK
A4	GPIO37	Digital I/O	SPIDQS, GPIO37, FSPIQ
A5	GPIO38	Digital I/O	GPIO38, FSPIWP
A6	GND	GND	Connect to ground
A7	U0TXD	Digital I/O	U0TXD (can be used for programming), GPIO43, CLK_OUT1
A8	U0RXD	Digital I/O	U0RXD (can be used for programming), GPIO44, CLK_OUT2
A9	GND	GND	Connect to ground
A10	GPIO45	Digital I/O	GPIO45 (strapping pin to control VDD_SPI) <b>Note:</b> Do not connect or pull down at boot up ⇒ <a href="#">4.3.6 Strapping Pins</a> .
A11	GPIO46	Digital I/O	GPIO46 (strapping pin for print control) <b>Note:</b> For details please refer to ⇒ <a href="#">4.3.6 Strapping Pins</a> .



No.	Pin Name	Pin Type	Description
A12	CHIP PU	Chip enable	High: Enables the ESP32-S2 Wi-Fi chip Low: Disables the ESP32-S2 Wi-Fi chip <b>Note:</b> Do not leave the CHIP_PU pin floating and please refer to ⇒ <a href="#">4.3.5 Power up Sequence and Reset</a> .
A13	V <sub>DD</sub>	PWR Pin	Connect to 3.3 V
A14	GND	Ground Pin	Connect to ground
B1	GPIO34	Digital I/O	SPIIO5, GPIO34, FSPICS0
B2	GND	Ground Pin	Connect to ground
B3	NC	NC	Do not connect
B4	GND	Ground Pin	Connect to ground
B5	NC	NC	Do not connect
B6	NC	NC	Do not connect
B7	V <sub>DD</sub>	Supply Pin	Connect to 3.3 V
B8	V <sub>DD</sub>	Supply Pin	Connect to 3.3 V
B9	NC	NC	Do not connect
B10	NC	NC	Do not connect
B11	GPIO1	Digital I/O	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
B12	SPDT2	Digital Input	SPDT control pin: Configures if the antenna or RF pad is fed <b>Note:</b> Do not connect or pull up to connect the internal antenna ⇒ <a href="#">4.3.2 Module Selectable RF In/Output</a> .
B13	SPDT1	Digital Input	SPDT control pin: Configures if the antenna or RF pad is fed <b>Note:</b> Do not connect or pull down to connect the internal antenna ⇒ <a href="#">4.3.2 Module Selectable RF In/Output</a> .
B14	GND	Ground Pin	Connect to ground
C1	GPIO33	Digital I/O	SPIIO4, GPIO33, FSPIH0
C11	GPIO2	Digital I/O Analog	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
C12	GPIO3	Digital I/O Analog	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
C13	GPIO4	Digital I/O Analog	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
C14	GND	Ground Pin	Connect to ground
D1	GND	Ground Pin	Connect to ground
D11	GPIO5	Digital I/O Analog	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
D12	GND	Ground Pin	Connect to ground

No.	Pin Name	Pin Type	Description
D13	GPIO6	Digital I/O Analog	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
D14	GND	Ground Pin	Connect to ground
E1	MTCK	Digital I/O	MTCK, GPIO39, CLK_OUT3
E11	GPIO7	Digital I/O Analog	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
E12	GPIO8	Digital I/O Analog	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7
E13	GPIO9	Digital I/O Analog	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPiHD
E14	GND	Ground Pin	Connect to ground
F1	MTDO	Digital I/O	MTDO, GPIO40, CLK_OUT2
F11	GPIO11	Digital I/O Analog	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPiD, FSPiIO5
F12	GND	Ground Pin	Connect to ground
F13	GPIO10	Digital I/O Analog	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPiCS0, FSPiIO4
F14	GND	Ground Pin	Connect to ground
G1	MTDI	Digital I/O	MTDI, GPIO41, CLK_OUT1
G11	GPIO14	Digital I/O	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPiWP, FSPiDQS
G12	GPIO13	Digital I/O Analog	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPiQ, FSPiIO7
G13	GPIO12	Digital I/O Analog	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPiCLK, FSPiIO6
G14	GND	Ground Pin	Connect to ground
H1	MTMS	NC	MTMS, GPIO42
H2	NC	NC	Do not connect
H3	NC	NC	Do not connect
H4	NC	NC	Do not connect
H5	NC	NC	Do not connect
H6	GPIO20	Digital I/O Analog	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
H7	GPIO19	Digital I/O Analog	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-

No.	Pin Name	Pin Type	Description
H8	GND	Ground Pin	Connect to ground
H9	GND	Ground Pin	Connect to ground
H10	GND	Ground Pin	Connect to ground
H11	GPIO21	Digital I/O	RTC_GPIO21, GPIO21
H12	GND	Ground Pin	Connect to ground
H13	GND	Ground Pin	Connect to ground
H14	GND	Ground Pin	Connect to ground
I1	GND	Ground Pin	Connect to ground
I2	NC	NC	Do not connect
I3	GND	Ground Pin	Connect to ground
I4	V <sub>DD</sub>	Supply Pin	Connect to 3.3 V
I5	V <sub>DD</sub>	Supply Pin	Connect to 3.3 V
I6	GND	Ground Pin	Connect to ground
I7	DAC 2	Digital I/O Analog	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3
I8	DAC 1	Digital I/O Analog	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1
I9	XTAL_32K_N	Digital I/O Analog	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
I10	XTAL_32K_P	Digital I/O Analog	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
I11	GPIO0	Digital I/O	RTC_GPIO0, GPIO0 (strapping pin to configure boot or download mode) <b>Note:</b> Do not connect or pull high for boot mode ⇒ <a href="#">4.3.6 Strapping Pins</a> .
I12	GND	Ground Pin	Connect to ground
I13	RF pad	RF I/O	The RF signal can be routed to this pin by setting SPDT1 to a low and SPDT2 to a high level.
I14	GND	Ground Pin	Connect to ground
GT1	Thermal GND	Ground Pin	Connect to ground for heat dissipation
GT2	Thermal GND	Ground Pin	Connect to ground for heat dissipation
GT3	Thermal GND	Ground Pin	Connect to ground for heat dissipation
GT4	Thermal GND	Ground Pin	Connect to ground for heat dissipation
GT5	Thermal GND	Ground Pin	Connect to ground for heat dissipation
GT6	Thermal GND	Ground Pin	Connect to ground for heat dissipation

## 2.3 WLAN Features

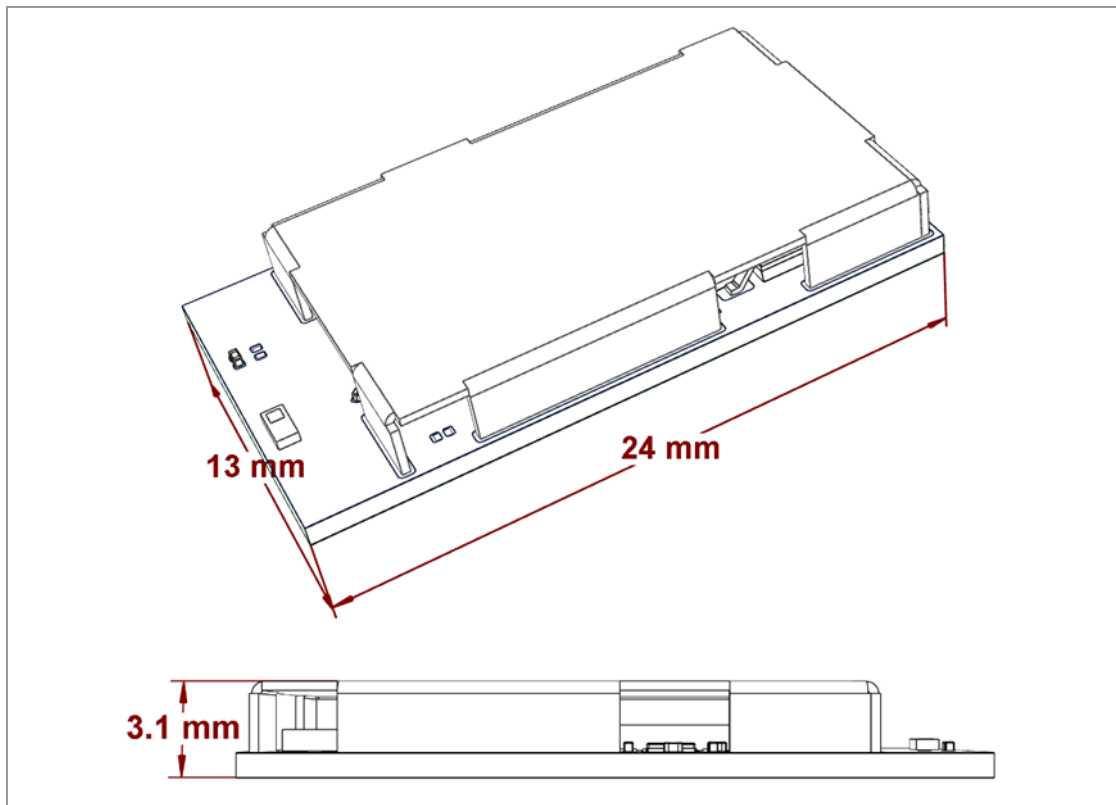
Type	Features
IEEE 802.11/Standards	<ul style="list-style-type: none"> <li>• 802.11 data rates: 1 Mbps and 2 Mbps (DSSS)</li> <li>• 802.11b data rates: 5.5 Mbps and 11 Mbps (CCK)</li> <li>• 802.11g data rates: 6, 9, 12, 18, 24, 36, 48, and 54 Mbps (OFDM)</li> <li>• 802.11n compliant with maximum data rates: up to 72 Mbps (20 MHz channel) and 150 Mbps (40 MHz channel)</li> <li>• 802.11n MCS32 (HT duplicate)</li> <li>• 802.11mc Fine Time Measurement (FTM)</li> <li>• Supports clients (stations) implementing IEEE Power Save mode</li> <li>• Wi-Fi direct connectivity</li> </ul>
WLAN MAC	<ul style="list-style-type: none"> <li>• Simultaneous Soft-AP and Infrastructure Station modes</li> <li>• Distributed Control Function (DCF)</li> <li>• Request to Send (RTS) and Clear to Send (CTS) and immediate Block Acknowledgement (BA or Block ACK)</li> <li>• 4x virtual Wi-Fi interfaces</li> <li>• Fragmentation and defragmentation</li> <li>• Aggregated Mac Protocol Data Unit (A-MPDU) for Rx and Tx</li> <li>• Aggregated Mac Service Data Unit (A-MSDU) for Rx</li> <li>• Transmission Opportunity (TXOP)</li> <li>• Wi-Fi Multimedia (WMM)</li> <li>• CCMP, TKIP, WAPI, WEP, BIP</li> <li>• Automatic beacon monitoring/hardware Time Synchronization Function (TSF)</li> </ul>
WLAN Baseband and Radio	<ul style="list-style-type: none"> <li>• 802.11n 1x1 SISO (WLAN SoC with SISO RF radio)</li> <li>• PHY data rates: up to 150 Mbps</li> <li>• Short guard interval (0.4 <math>\mu</math>s)</li> <li>• 20 MHz and 40 MHz bandwidth/channel</li> <li>• Modulation and Coding Scheme MCS 0-7</li> <li>• Radio resource measurement</li> <li>• Space Time Block Coding (STBC) with one spatial stream reception</li> <li>• MCS32 (HT duplicate)</li> <li>• Automatic Gain Control (AGC)</li> <li>• Direct conversion radio (no need for external SAW filter)</li> </ul>
WLAN Encryption	<ul style="list-style-type: none"> <li>• Embedded WLAN Radio SoC with the following features:</li> <li>• Advanced Encryption Standard (AES) – 128/192/256 bit (hardware accelerated)</li> <li>• Counter Mode with CBC-MAC Protocol (CCMP)</li> <li>• Temporary Key Integrity Protocol (TKIP)</li> <li>• WLAN Authentication and Privacy Infrastructure (WAPI)</li> <li>• Wired Equivalent Privacy (WEP)</li> <li>• Broadcast/Multitask Integrity Protocol (BIP)</li> </ul>

### 3 Detailed Description

#### 3.1 Dimensions



All dimensions are in millimeters.

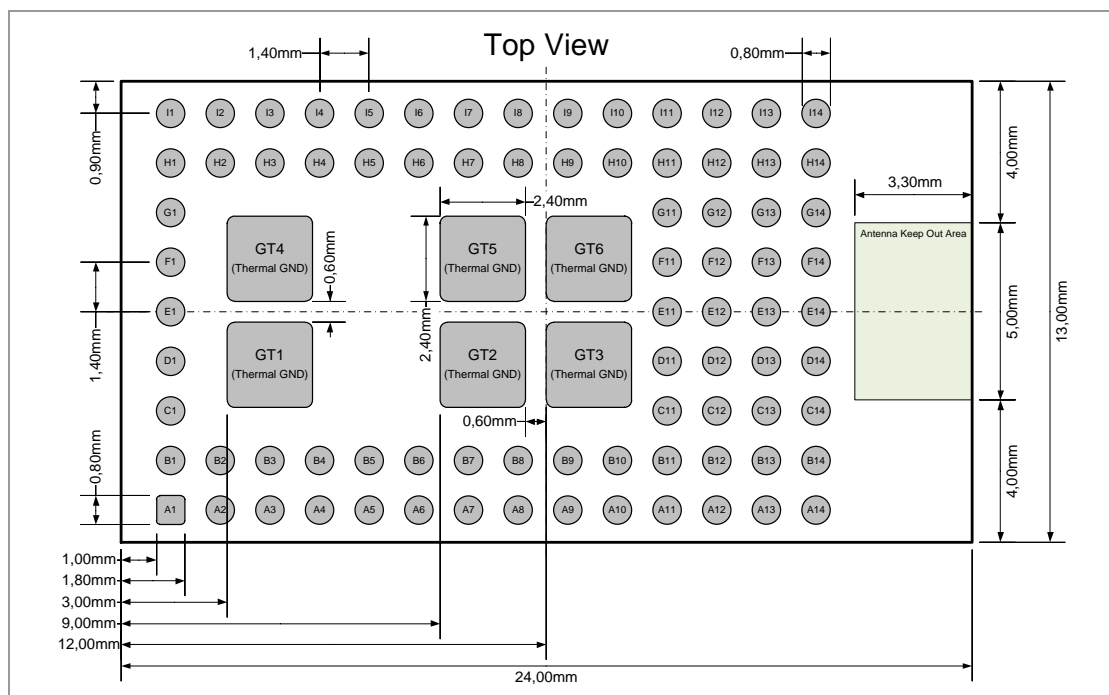


No.	Item	Dimension (mm)	Tolerance (mm)	Remark
1	Width	13.00	TBD	
2	Length	24.00	TBD	
3	Height	3.10	TBD	With case

## 3.2 Footprint



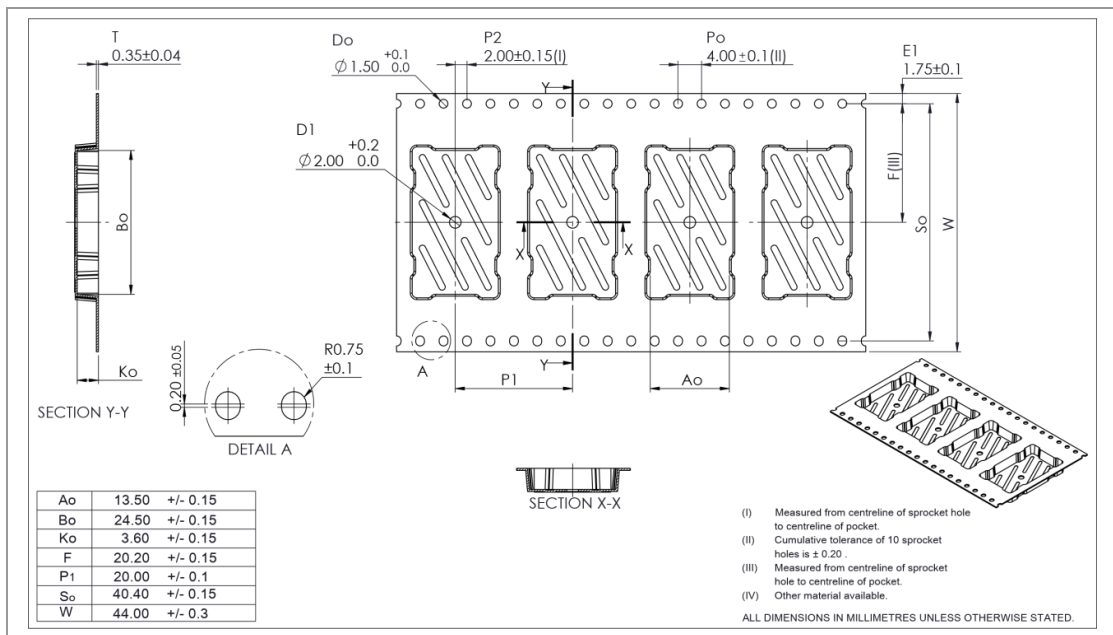
The outer dimensions have a tolerance of (TBD).



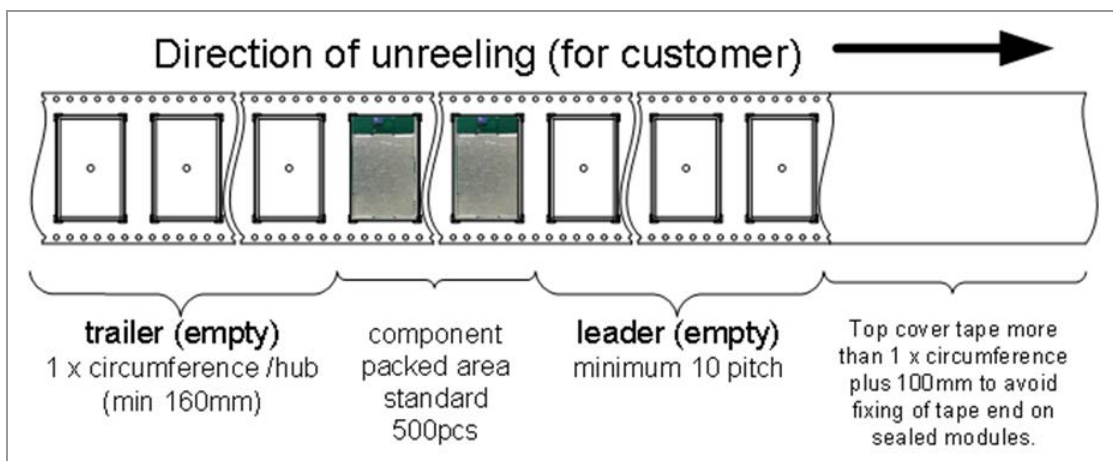
### 3.3 Packaging

The module is a mass production status product and will be delivered in the package described below.

#### 3.3.1 Tape Dimensions



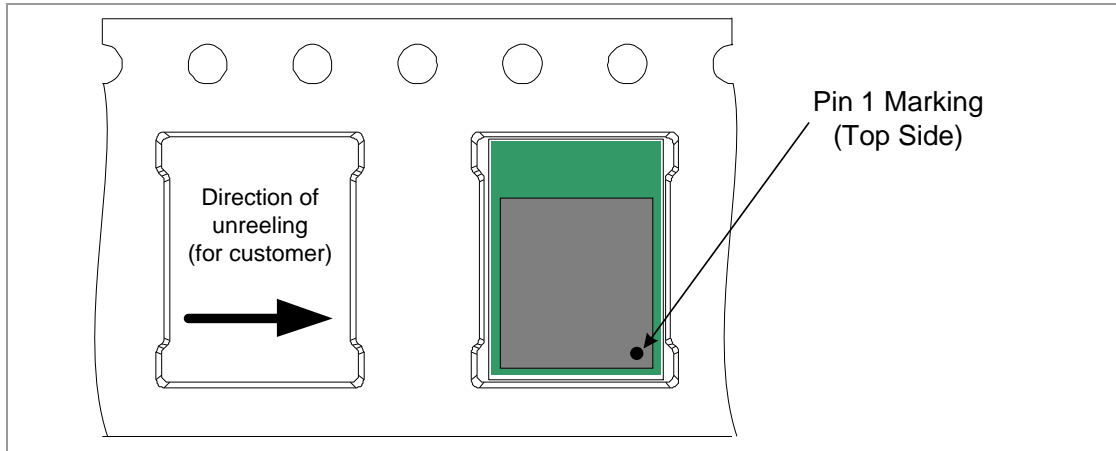
#### 3.3.2 Packing in Tape



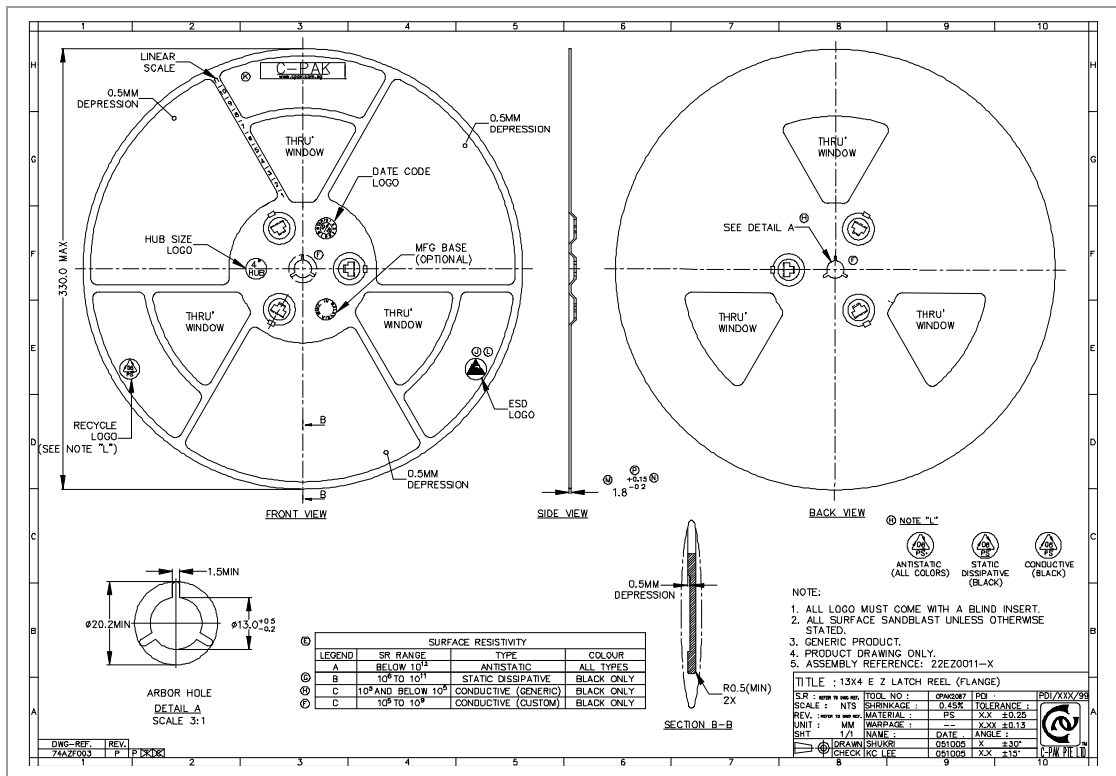
Empty spaces in the component packed area shall be less than two per reel and those spaces shall not be consecutive.

The top cover tape shall not be found on reel holes and it shall not stick out from the reel.

### 3.3.3 Component Direction



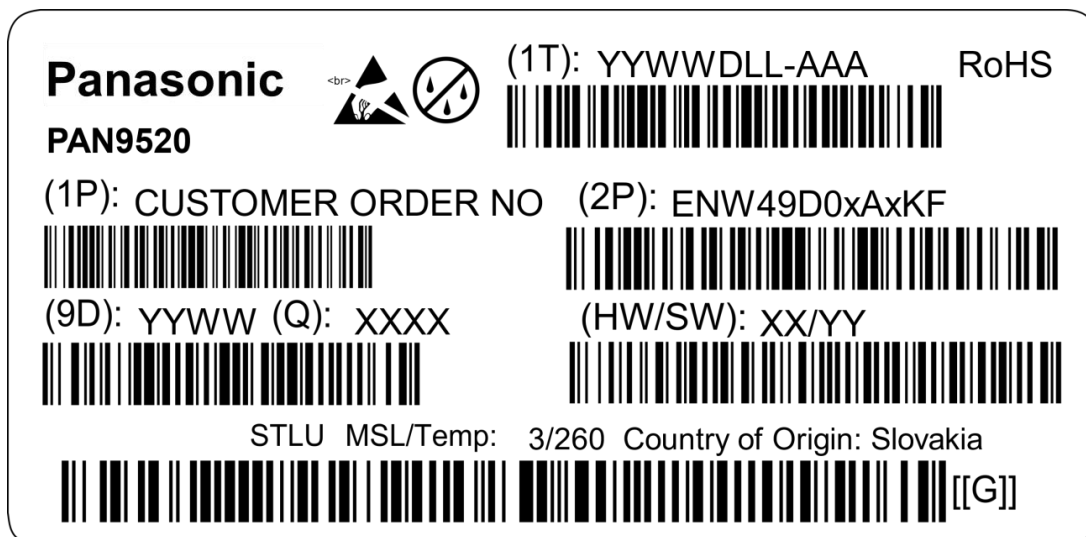
### 3.3.4 Reel Dimension





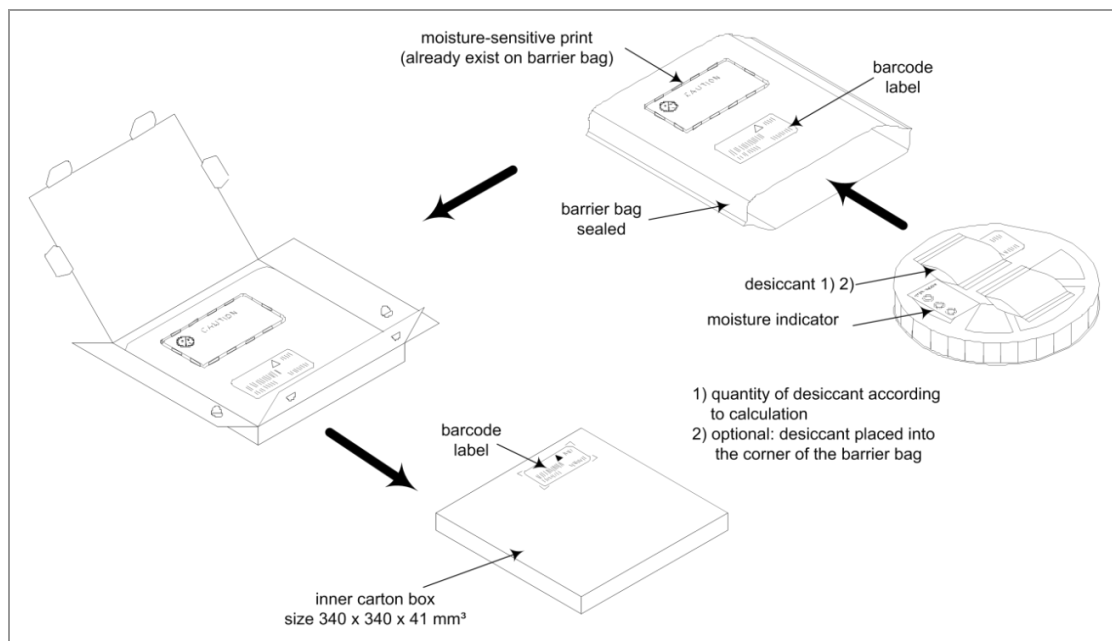
### 3.3.5 Package Label

Example:



(1T)	Lot code
(1P)	Customer order number, if applicable
(2P)	Order number
(9D)	Date code
(Q)	Quantity
(HW/SW)	Hardware/software version

### 3.3.6 Total Package



## 3.4 Case Marking

Example:



- 1 Brand name
- 2 Hardware/software version
- 3 Engineering Sample (optional)
- 4 Model Name/ENW number
- 5 Lot code
- 6 Serial number
- 7 WLAN MAC address
- 8 FCC ID
- 9 IC Canada
- 10 Marking for Pin 1
- 11 2D barcode, for internal usage only

## 4 Specification



All specifications are over temperature and process, unless indicated otherwise.

### 4.1 Default Test Conditions



Temperature: 25 °C ± 10 °C  
 Humidity: 40 % to 85 % RH  
 Supply Voltage: 3.3 V

### 4.2 Absolute Maximum Ratings



The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T <sub>STOR</sub>	Storage Temperature		-40		85	°C
V <sub>ESD</sub>	ESD Robustness	TBD				
PRF	RF Input Level	11b, 1 Mbps			5	dBm
		11b, 11 Mbps			5	dBm
		11g, 6 Mbps			5	dBm
		11g, 54 Mbps			0	dBm
		11n, HT20, MCS0			5	dBm
		11n, HT20, MCS7			0	dBm
		11n, HT40, MCS0			5	dBm
		11n, HT40, MCS7			0	dBm
V <sub>DD MAX</sub>	Maximum Voltage	Maximum power supply voltage from any pin with respect to VSS (GND)	-0.3		3.6	V
V <sub>DIG</sub>	Voltage on any Digital Pins	Not Specified				

### 4.3 Recommended Operating Conditions



The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$T_A$	Ambient Operating Temperature Range	Industrial grade	-40		85	°C
$V_{DD}$			3.0	3.3	3.6	V

#### 4.3.1 Digital Pin Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IH}$	High Level Input Voltage	3.3 V operation ( $V_{IO}=V_{DD}$ )	$0.75 V_{DD}$		$V_{DD} + 0.3$	V
$V_{IL}$	Low Level Input Voltage	3.3 V operation ( $V_{IO}=V_{DD}$ )	-0.3		$0.25 V_{DD}$	V
$I_{IH}$	High Level Input Current				50	nA
$I_{IL}$	Low Level Input Current				50	nA
$V_{OH}$	High Level Output Voltage	Measured on high-impedance load	$0.8 V_{DD}$			V
$V_{OL}$	Low Level Output Voltage	Measured on high-impedance load			$0.1 V_{DD}$	
$I_{OH}$ at $V_{OH} \geq 2.64$ V	High Level Output Current	3.3 V operation ( $V_{IO}=V_{DD}$ ), Pin is current source		40		mA
$I_{OL}$ at 0.495 V	Low Level Output Current	3.3 V operation ( $V_{IO}=V_{DD}$ ); Pin is current sink		28		mA
RPU	Internal Pull-Up Resistance	Except pins SPDT1 and SPDT2		45		k $\Omega$
RPD	Internal Pull-Down Resistance	Except pins SPDT1 and SPDT2		45		k $\Omega$
$V_{IH\_nRST}$	Chip Reset Release Voltage	CHIP_PU (pin A12)=nRST pin	$0.75 V_{DD}$		$V_{DD} + 0.3$	V
$V_{IL\_nRST}$	Chip Reset Voltage	CHIP_PU (pin A12)=nRST pin	-0.3		$0.25 V_{DD}$	V

## 4.3.2 Module Selectable RF In/Output

Module RF-Output can be switched between the on-board ceramic chip antenna and the 50 Ω RF-pad (pin I13) output by adjusting the voltage level on pin B12 (SPDT2) and pin B13 (SPDT1). If pin B12 and pin B13 are not connected (NC), output state will be on-board ceramic chip antenna. This default configuration is applied by internal 100 kΩ pull-resistors.

RF In/Output	Pin B12 (SPDT2)	Pin B13 (SPDT1)
On-board ceramic chip antenna output	NC or GND (0 V)	NC or 3 V to 3.6 V (typ. 3.3 V)
Module 50 Ω RF-pad (pin I13)	3 V to 3.6 V (typ. 3.3 V)	GND (0 V)

## 4.3.3 Current Consumption



The current consumption depends on the user scenario and on the setup and timing in the power modes.

Assume  $V_{DD}=3.3\text{ V}$ ,  $T_{amb}=25\text{ °C}$ , if nothing else stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
TBD					

## 4.3.4 Internal Operating Frequencies

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fSYSCLK1	CPU/System/ Encryption Clock Speed				240	MHz
fREFCLK1	WLAN/MCU Crystal Fundamental Frequency	Frequency tolerance < ±25 ppm over operating temperature and process		40		MHz

## 4.3.5 Power up Sequence and Reset



Please follow the described power up sequence, when powering the device.

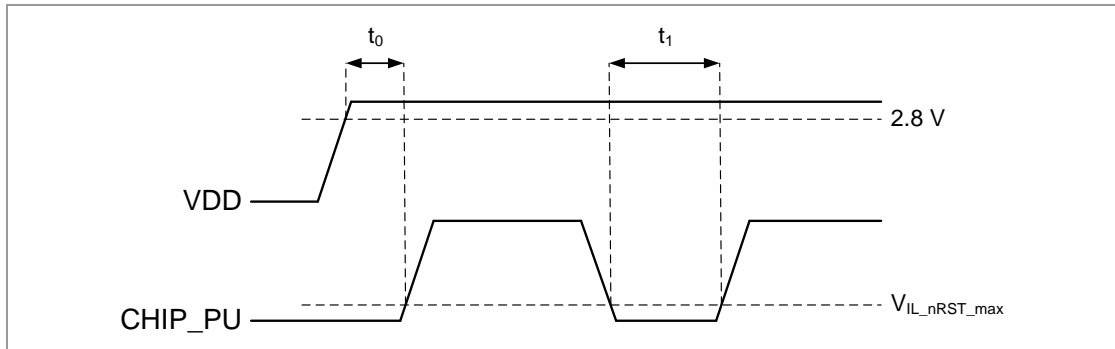
Make sure that the reset signal is active (CHIP\_PU=low), when the module is powered. After the supply voltage  $V_{DD}$  has risen to a level of 2.8 V and the time  $t_0$  has passed, the reset signal can be activated (voltage on CHIP\_PU  $\geq V_{IL\_nRST\_max}=0.25 V_{DD}$ ).

If the device is active, this can be reset by activating the reset signal (CHIP\_PU=low).



Please note that CHIP\_PU must be low (voltage below  $V_{IL\_nRST\_max}$ ) for at least  $t_1$  to reset the chip.

For specifications of  $V_{IL\_nRST}$  please refer to ⇒ 4.3.1 Digital Pin Characteristics.



Parameter	Condition	Min.	Typ.	Max.	Unit
$t_0$	Time period from power up until CHIP_PU activated	0.5			ms
$t_1$	Time period, in which the reset signal must be active (CHIP_PU low) to reset the device.	0.5			ms

### 4.3.6 Strapping Pins

Three pins of the PAN9520 are evaluated at boot-up to set up the module’s mode and behavior. These pins are called “strapping pins”. This section explains their function in more detail.

The three mentioned strapping pins are GPIO0, GPIO45, and GPIO46. Their voltage level is captured during each reset and boot-up caused by one of the following sources: power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset. The detected level of each strapping pin is written to the register GPIO\_STRAPPING as zero (low level) or one (high level). The captured values are kept until the next reset. After boot-up, all strapping bits are available in the register GPIO\_STRAPPING (read only) and thus the strapping pins can be used as usual pins.

Each strapping pin level can be set-up by applying an external voltage from a different I/O or a pull-resistor. Besides, weak chip-internal pull-resistors determine the default level of the pins at boot-up.

In the following, the strapping functionality and default level is described for each of the three pins.

## GPIO0

GPIO0 determines, if the device does a normal boot and runs an application or if it enters the download mode, in which data can be written to the QSPI flash. Per default, the pin is set to “1” by a weak chip-internal pull-up resistor. This makes the device entering the usual boot mode. Applying a zero (low level) to the pin at boot-up makes the device entering the download mode.

## GPIO45



Be aware that GPIO45 must be left open or pulled down at boot-up. Applying a high-level voltage causes malfunction of the PAN9520 device.

GPIO45 determines the voltage of the QSPI Flash and PSRAM. The mounted QSPI memories expect a voltage of 3.3 V. This is applied, if GPIO45 is set to a low level at boot-up. This is done by a chip-internal weak pull-down resistor. Therefore, the pin must be left floating or pulled to ground at boot-up. A high level on GPIO45 at boot-up causes malfunction of the PAN9520 module.



Please note that the functionality of GPIO45 can be disabled by setting the eFuse bit VDD\_SPI\_FORCE (OTP) to “1”. In this case, the voltage is defined by the eFuse bit VDD\_SPI\_TIEH (OTP).

## GPIO46



Be aware that applying a high level to GPIO46 will trigger unexpected behavior, if GPIO0 is set to a low level (download mode).

The pre-installed first stage bootloader of the ESP32-S2 can print several information, when running. The values of the eFuse UART\_PRINT\_CONTROL (OTP) and GPIO46 determine if this functionality is enabled. The different configurations are explained in the following:

Value of UART_PRINT_CONTROL	Value of GPIO46	Print Setting
0		Printing during boot-up is enabled.
1	0	Printing during boot-up is enabled.
	1	Printing during boot-up is disabled.
2	0	Printing during boot-up is disabled.
	1	Printing during boot-up is enabled.
3		Printing during boot-up is disabled.

The value of UART\_PRINT\_CONTROL is zero at delivery of the module. Therefore, the level on GPIO46 at boot-up has not any effect, if the device is in boot mode (GPIO0=low). Anyway, if the device is started in download mode (GPIO=high), the level on GPIO46 must be a low level.



Please note that the chip-internal weak pull-down resistor makes the strapping bit to be low, if the pin is left open.

## Summary

The following table summarizes the description that has been made previously:

Pin	Default	Level during boot	Description
GPIO0	Pull-up (one)	Low (zero)	Download mode (Flash memory can be written)
		High (one)	Boot mode (device continues booting an application)
GPIO45	Pull-down (zero)	Low (zero)	QSPI memory is powered by 3.3 V
		High (one)	QSPI memory is powered by 1.8 V (not allowed)
GPIO46	Pull-down (zero)	Low (zero)	Please see the previous table (GPIO46).
		High (one)	Please see the previous table (GPIO46) (not allowed in download mode).

## 4.4 RF Electrical Characteristics

### 4.4.1 WLAN Radio Specification

Parameter	Operation Mode				Specification
Standard Conformance	IEEE 802.11/IEEE 802.11b				
	IEEE 802.11g				
	IEEE 802.11n				
Modulation	IEEE 802.11b				DSSS/CCK
	IEEE 802.11g				OFDM
	IEEE 802.11n				OFDM at MCS0~7
Physical Layer Data Rates	IEEE 802.11				1 and 2 Mbps at DSSS
	IEEE 802.11b				5.5 and 11 Mbps at DSSS/CCK
Supported Data Rates	IEEE 802.11g				6, 9, 12, 18, 24, 36, 48, 54 Mbps
	IEEE 802.11n	MCS0~7	HT20	LGI	6.5, 13, 19.5, 26, 39, 52, 58.5, and 65 Mbps
				SIGI	7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, and 72.2 Mbps
			HT40	LGI	13.5, 27, 40.5, 54, 81, 108, 121.5, and 135 Mbps
SIGI				15, 30, 45, 60, 90, 120, 135, and 150 Mbps	
Supported Bandwidth (BW)	IEEE 802.11n				20 MHz (HT20), 40 MHz (HT40)



Parameter	Operation Mode		Specification
Supported Guard Interval	IEEE 802.11n		400 ns (SGI), 800 ns (LGI)
Supported Channel 2.4 GHz <sup>2</sup>	IEEE 802.11 b/g/n	North America (US)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
		Canada (CA)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
		Europe (EU)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13

## 4.4.2 WLAN RF Characteristics

### 4.4.2.1 IEEE 802.11b (RF Characteristics)



Assume  $V_{DD}=3.3\text{ V}$ ,  $T_{amb}=25\text{ }^{\circ}\text{C}$ , if nothing else stated.

50  $\Omega$  terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Unit
RF Frequency Range			2 400		2 483.5	MHz
Carrier Frequency Tolerance			-25		+25	ppm
Transmit Output Power				TBD	+18	dBm
Spectrum Mask	fC $\pm$ 11 MHz				-30	dBr
	fC $\pm$ 22 MHz				-50	
Power-on/Power-Down Ramp					2	$\mu$ s
RF Carrier Suppression					-15	dB
Error Vector Magnitude (EVM)	Peak				35	%
Minimum Receive Sensitivity	1 Mbps (DSSS)	FER $\leq$ 8 %		TBD	-86	dBm
	2 Mbps (DSSS)	FER $\leq$ 8 %		TBD	-83	dBm
	5.5 Mbps (CCK)	FER $\leq$ 8 %		TBD	-79	dBm
	11 Mbps (CCK)	FER $\leq$ 8 %		TBD	-76	dBm
Maximum Input Level		FER $\leq$ 8 %	-10			dBm
Adjacent Channel Rejection		FER $\leq$ 8 %	35			dB

<sup>2</sup> In order to comply with the relevant regulatory requirements, please refer to the model's supported channels  
 ⇒ 7.1 Ordering Information.

## 4.4.2.2 IEEE 802.11g (RF Characteristics)



Assume  $V_{DD}=3.3\text{ V}$ ,  $T_{amb}=25\text{ }^{\circ}\text{C}$ , if nothing else stated.

50  $\Omega$  terminal load connected to the RF connector.

Parameter	Condition	Min.	Typ.	Max.	Unit
RF Frequency Range		2 400		2 483.5	MHz
Carrier Frequency Tolerance		-25		+25	ppm
Transmit Output Power	6 Mbps~54 Mbps		TBD	+16	dBm
Spectrum Mask	fC±11 MHz			-20	dBr
	fC±20 MHz			-28	dBr
	fC±30 MHz			-40	dBr
Transmitter Center Frequency Leakage				-15	dB
Transmitter Spectral Flatness		-2		+2	dB
Constellation Error (EVM)	BPSK, CR 1/2 (6 Mbps)			-5	dB
	BPSK, CR 3/4 (9 Mbps)			-8	dB
	QPSK, CR 1/2 (12 Mbps)			-10	dB
	QPSK, CR 3/4 (18 Mbps)			-13	dB
	16-QAM, CR 1/2 (24 Mbps)			-16	dB
	16-QAM, CR 3/4 (36 Mbps)			-19	dB
	64-QAM, CR 2/3 (48 Mbps)			-22	dB
	64-QAM, CR 3/4 (54 Mbps)			-25	dB
Minimum Receive Sensitivity	BPSK, CR 1/2 (6 Mbps)	PER ≤ 10 %	TBD	-82	dBm
	BPSK, CR 3/4 (9 Mbps)	PER ≤ 10 %	TBD	-81	dBm
	QPSK, CR 1/2 (12 Mbps)	PER ≤ 10 %	TBD	-79	dBm
	QPSK, CR 3/4 (18 Mbps)	PER ≤ 10 %	TBD	-77	dBm
	16-QAM, CR 1/2 (24 Mbps)	PER ≤ 10 %	TBD	-74	dBm
	16-QAM, CR 3/4 (36 Mbps)	PER ≤ 10 %	TBD	-70	dBm
	64-QAM, CR 2/3 (48 Mbps)	PER ≤ 10 %	TBD	-66	dBm
	64-QAM, CR 3/4 (54 Mbps)	PER ≤ 10 %	TBD	-65	dBm
Maximum Input Level	PER ≤ 10 %			-20	dBm
Adjacent Channel Rejection	BPSK, CR 1/2 (6 Mbps)	PER ≤ 10 %	16		dB
	64-QAM, CR 3/4 (54 Mbps)	PER ≤ 10 %	-1		dB

### 4.4.2.3 IEEE 802.11n: BW 20 MHz (RF Characteristics)



Assume  $V_{DD}=3.3\text{ V}$ ,  $T_{amb}=25\text{ }^{\circ}\text{C}$ , if nothing else stated.

50  $\Omega$  terminal load connected to the RF connector.

Parameter	Condition	Min.	Typ.	Max.	Unit	
RF Frequency Range		2 400		2 483.5	MHz	
Carrier Frequency Tolerance		-25		+25	ppm	
Transmit Output Power	MCS0-MCS4		TBD	+16	dBm	
	MCS5-MCS7		TBD	+15	dBm	
Spectrum Mask	$f_C \pm 11\text{ MHz}$			-20	dBr	
	$f_C \pm 20\text{ MHz}$			-28	dBr	
	$f_C \pm 30\text{ MHz}$			-45	dBr	
Transmitter Center Frequency Leakage				-15	dB	
Transmitter Spectral Flatness		-2		+2	dB	
Constellation Error (EVM)	BPSK, CR 1/2 (MCS0)			-5	dB	
	QPSK, CR 1/2 (MCS1)			-10	dB	
	QPSK, CR 3/4 (MCS2)			-13	dB	
	16-QAM, CR 1/2 (MCS3)			-16	dB	
	16-QAM, CR 3/4 (MCS4)			-19	dB	
	64-QAM, CR 2/3 (MCS5)			-22	dB	
	64-QAM, CR 3/4 (MCS6)			-25	dB	
	64-QAM, CR 5/6 (MCS7)			-27	dB	
Minimum Receive Sensitivity <sup>3</sup>	6.5 Mbps (MCS0)	PER $\leq 10\%$		TBD	-82	dBm
	13 Mbps (MCS1)	PER $\leq 10\%$		TBD	-79	dBm
	19.5 Mbps (MCS2)	PER $\leq 10\%$		TBD	-77	dBm
	26 Mbps (MCS3)	PER $\leq 10\%$		TBD	-74	dBm
	39 Mbps (MCS4)	PER $\leq 10\%$		TBD	-70	dBm
	52 Mbps (MCS5)	PER $\leq 10\%$		TBD	-66	dBm
	58.5 Mbps (MCS6)	PER $\leq 10\%$		TBD	-65	dBm
	65 Mbps (MCS7)	PER $\leq 10\%$		TBD	-64	dBm
Maximum Input Level		PER $\leq 10\%$		-20	dBm	
Adjacent Channel Rejection <sup>4</sup>	65 Mbps (MCS7)	PER $\leq 10\%$	-2		dB	

<sup>3</sup> The Minimum Sensitivity levels apply only to non-STBC modes, MCS 0-7, 800 ns LGI and BCC.

<sup>4</sup> The Adjacent Channel Rejection levels apply only to non-STBC modes, MCS 0-7, 800 ns LGI and BCC.

## 4.4.2.4 IEEE 802.11n: BW 40 MHz (RF Characteristics)



Assume  $V_{DD}=3.3\text{ V}$ ,  $T_{amb}=25\text{ °C}$ , if nothing else stated.

50  $\Omega$  terminal load connected to the RF connector.

## 4.5 Reliability Tests

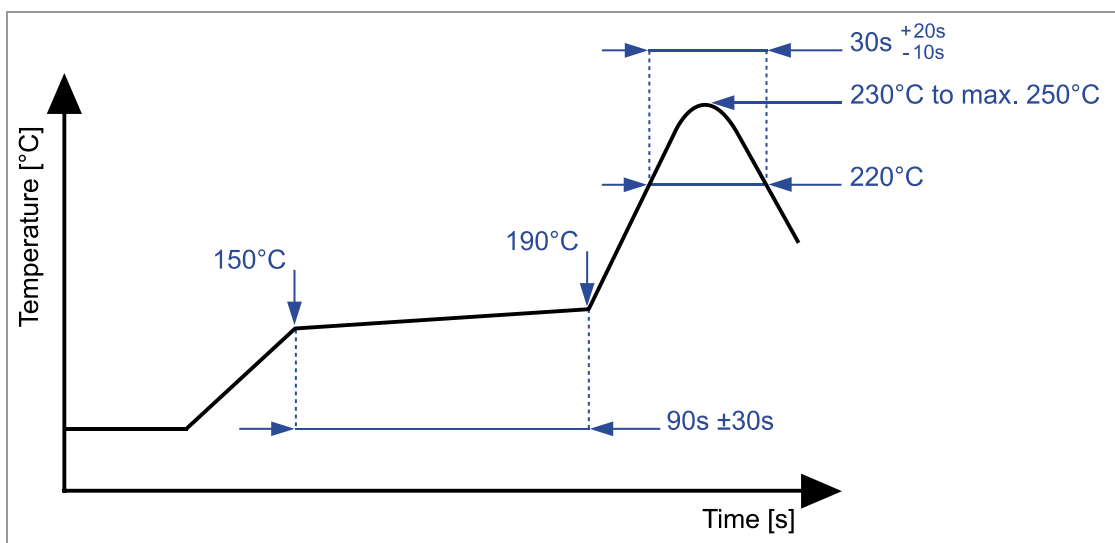
The measurement should be done after the test device has been exposed to room temperature and humidity for one hour.

No.	Item	Limit	Condition
1	Vibration test	Electrical parameter are in specification	Freq.: 20~2 000 Hz; 17g~50g /cycle, 2 h each of XYZ axis
2	Shock test		Dropped onto concrete from a height of 1 m for 3 times
3	Heat shock cycle test		-50 °C for 30 min. and +125 °C for 300 cycles each 15 min.
4	Temperature humidity bias test (THB)		+85 °C, 85 % RH, 500 h
5	Low temperature storage test (LTST)		-40 °C, 300 h
6	High temperature storage test (HTST)		+85 °C, 300 h

## 4.6 Recommended Soldering Profile



- Reflow permissible cycles: 2
- Opposite side reflow is prohibited due to module weight
- More than 75 percent of the soldering area shall be coated by solder
- The soldering profiles should be adhered to in order to prevent electrical or mechanical damage
- Soldering profile assumes lead-free soldering



## 5 Cautions



Failure to follow the guidelines set forth in this document may result in degrading of the module functions and damage to the module.

### 5.1 Design Notes

1. Follow the conditions written in this specification, especially the control signals of this module.
2. The supply voltage should abide by the maximum ratings (⇒ [4.2 Absolute Maximum Ratings](#)).
3. The supply voltage must be free of AC ripple voltage (for example from a battery or a low noise regulator output). For noisy supply voltages, provide a decoupling circuit (for example a ferrite in series connection and a bypass capacitor to ground of at least 47  $\mu$ F directly at the module).
4. This module should not be mechanically stressed when installed.
5. Keep this module away from heat. Heat is the major cause of decreasing the life time of these modules.
6. Avoid assembly and use of the target equipment in conditions where the module temperature may exceed the maximum tolerance.
7. Keep this module away from other high frequency circuits.
8. Refer to the recommended pattern when designing a board.

### 5.2 Installation Notes

1. Reflow soldering is possible twice based on the conditions set forth in ⇒ [4.6 Recommended Soldering Profile](#). Set up the temperature at the soldering portion of this module according to this reflow profile.
2. Carefully position the module so that the heat will not burn into printed circuit boards or affect other components that are susceptible to heat.
3. Carefully locate the module, to avoid an increased temperature caused by heat generated by neighboring components.
4. If a vinyl-covered wire comes into contact with the module, the wire cover will melt and generate toxic gas, damaging the insulation. Never allow contact between a vinyl cover and these modules to occur.
5. This module should not be mechanically stressed or vibrated when reflowed.
6. To repair the board by hand soldering, follow the conditions set forth in this chapter.
7. Do not wash this product.
8. Pressing on parts of the metal cover or fastening objects to the metal will cause damage to the module.

### 5.3 Usage Condition Notes

1. Take measures to protect the module against static electricity.  
If pulses or transient loads (a large load, which is suddenly applied) are applied to the modules, check and evaluate their operation before assembly of the final products.
2. Do not use dropped modules.
3. Do not touch, damage, or soil the pins.
4. Follow the recommended condition ratings about the power supply applied to this module.
5. Electrode peeling strength: Do not apply a force of more than 4.9 N in any direction on the soldered module.
6. Pressing on parts of the metal cover or fastening objects to the metal cover will cause damage.
7. These modules are intended for general purpose and standard use in general electronic equipment, such as home appliances, office equipment, information, and communication equipment.

### 5.4 Storage Notes

1. The module should not be stressed mechanically during storage.
2. Do not store these modules in the following conditions or the performance characteristics of the module, such as RF performance will be adversely affected:
  - Storage in salty air or in an environment with a high concentration of corrosive gas, such as Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, or NO<sub>x</sub>,
  - Storage in direct sunlight,
  - Storage in an environment where the temperature may be outside the range of 5 °C to 35 °C, or where the humidity may be outside the 45 % to 85 % range,
  - Storage of the modules for more than one year after the date of delivery storage period: Please check the adhesive strength of the embossed tape and soldering after 6 months of storage.
3. Keep this module away from water, poisonous gas, and corrosive gas.
4. This module should not be stressed or shocked when transported.
5. Follow the specification when stacking packed crates (max. 10).

### 5.5 Safety Cautions

These specifications are intended to preserve the quality assurance of products and individual components.

Before use, check and evaluate the operation when mounted on your products. Abide by these specifications without deviation when using the products. These products may short-circuit. If electrical shocks, smoke, fire, and/or accidents involving human life are anticipated when a short circuit occurs, provide the following failsafe functions as a minimum:

1. Ensure the safety of the whole system by installing a protection circuit and a protection device.
2. Ensure the safety of the whole system by installing a redundant circuit or another system to prevent a single fault causing an unsafe status.

## 5.6 Other Cautions

1. Do not use the module for other purposes than those listed in section ⇒ [5.3 Usage Condition Notes](#).
2. Be sure to provide an appropriate fail-safe function on your product to prevent any additional damage that may be caused by the abnormal function or the failure of the module.
3. This module has been manufactured without any ozone chemical controlled under the Montreal Protocol.
4. These modules are not intended for use under the special conditions shown below. Before using these modules under such special conditions, carefully check their performance and reliability under the said special conditions to determine whether or not they can be used in such a manner:
  - In liquid, such as water, salt water, oil, alkali, or organic solvent, or in places where liquid may splash,
  - In direct sunlight, outdoors, or in a dusty environment,
  - In an environment where condensation occurs,
  - In an environment with a high concentration of harmful gas (e. g. salty air, HCl, Cl<sub>2</sub>, SO<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, and NO<sub>X</sub>).
5. If an abnormal voltage is applied due to a problem occurring in other components or circuits, replace these modules with new modules, because they may not be able to provide normal performance even if their electronic characteristics and appearances appear satisfactory.



For further information please refer to the Panasonic website ⇒ [7.2.2 Product Information](#).



## **5.7 Restricted Use**

### **5.7.1 Life Support Policy**

This Panasonic Industrial Devices Europe GmbH product is not designed for use in life support appliances, devices, or systems where malfunction can reasonably be expected to result in a significant personal injury to the user, or as a critical component in any life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Panasonic customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Panasonic Industrial Devices Europe GmbH for any damages resulting.

### **5.7.2 Restricted End Use**

This Panasonic Industrial Devices Europe GmbH product is not designed for any restricted activity that supports the development, production, handling usage, maintenance, storage, inventory or proliferation of any weapons or military use.

Transfer, export, re-export, usage or reselling of this product to any destination, end user or any end use prohibited by the European Union, United States or any other applicable law is strictly prohibited.

## **6 Regulatory and Certification Information**

### **6.1 General Certification Information**

TBD

### **6.2 Federal Communications Commission (FCC) for US**

TBD

### **6.3 Innovation, Science, and Economic Development (ISED) for Canada**

TBD

### **6.4 European Conformity According to RED (2014/53/EU)**

TBD

### **6.5 RoHS and REACH Declaration**

The latest declaration of environmental compatibility (Restriction of Hazardous Substances, RoHS and Registration, Evaluation, Authorisation and Restriction of Chemicals, REACH) for supplied products can be found on the Panasonic website in the “Downloads” section of the respective product ⇒ [7.2.2 Product Information](#).

## 7 Appendix

### 7.1 Ordering Information

#### Variants and Versions

Order Number	Brand Name	Description	MOQ <sup>5</sup>
ENW49D0xAxKF	PAN9520 <sup>6</sup>	Embedded Wi-Fi Module	500

The PAN9520 is delivered with a pre-installed firmware. For further information please refer to our product documentation ⇒ [7.2.2 Product Information](#).

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<sup>5</sup> Abbreviation for Minimum Order Quantity (MOQ). The default MOQ for mass production is 500 pieces, fewer only on customer demand. Samples for evaluation can be delivered at any quantity via the distribution channels.

<sup>6</sup> The Grant IDs marked on the module labelling are referenced and only valid if the ceramic on-board chip antenna on module is used.

## 7.2 Contact Details

### 7.2.1 Contact Us

Please contact your local Panasonic Sales office for details on additional product options and services:

For Panasonic Sales assistance in the **EU**, visit

<https://eu.industrial.panasonic.com/about-us/contact-us>

Email: [wireless@eu.panasonic.com](mailto:wireless@eu.panasonic.com)

For Panasonic Sales assistance in **North America**, visit the Panasonic website “Sales & Support” to find assistance near you at

<https://na.industrial.panasonic.com/distributors>

Please visit the **Panasonic Wireless Technical Forum** to submit a question at

<https://forum.na.industrial.panasonic.com>

### 7.2.2 Product Information

Please refer to the Panasonic Wireless Connectivity website for further information on our products and related documents:

For complete Panasonic product details in the **EU**, visit

<http://pideu.panasonic.de/products/wireless-modules.html>

For complete Panasonic product details in **North America**, visit

<http://www.panasonic.com/rfmodules>