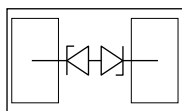
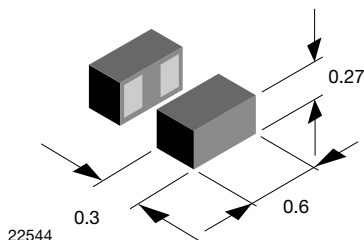




# Bidirectional Symmetrical (BiSy) Single Line ESD-Protection Diode in Silicon Package



22543



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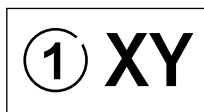
## FEATURES

- Ultra compact CLP0603 package
- Low package height < 0.3 mm
- 1-line ESD-protection
- Working range  $\pm 15$  V
- Low leakage current < 0.1  $\mu$ A
- Low load capacitance  $C_D = 5.5$  pF (typ.)
- ESD-protection acc. IEC 61000-4-2  
 $\pm 15$  kV contact discharge  
 $\pm 15$  kV air discharge
- Lead plating: Au (e4)
- Lead material: Ni
- Topside coating
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
**GREEN**  
(5-2008)

## MARKING (example only)



22545

1 = year code

Open circle = month code and pin 1

XY = type code

## LINKS TO ADDITIONAL RESOURCES



3D Models

ORDERING INFORMATION				
PART NUMBER (EXAMPLE)	ENVIRONMENTAL AND QUALITY CODE		PACKAGING CODE	ORDERING CODE (EXAMPLE)
	RoHS-COMPLIANT + LEAD (Pb)-FREE TERMINATIONS		GOLD PLATED	
	GREEN			
VCUT15A1-SD0-	G		15K PER 7" REEL (8 mm TAPE) 15K/BOX = MOQ	VCUT15A1-SD0-G4-08

PACKAGE DATA				
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	SOLDERING CONDITIONS
VCUT15A1-SD0	CLP0603-2L	15	0.12 mg	Peak temperature max. 260 °C Reflow soldering according JEDEC® STD-020

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot	$I_{PPM}$	2.5	A
Peak pulse power	Pin 1 to pin 2 acc. IEC 61000-4-5; $t_p = 8/20$ $\mu$ s; single shot	$P_{PP}$	65	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	$V_{ESD}$	$\pm 15$	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		$\pm 15$	
Operating temperature	Junction temperature	$T_J$	-55 to +150	°C
Storage temperature		$T_{stg}$	-55 to +150	°C

**CUT THE SPIKES WITH VCUT15A1-SD0**

The VCUT15A1-SD0 is a Bidirectional and Symmetrical (BiSy) ESD-protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VCUT15A1-SD0 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny CLP0603 package the line inductance is very low, so that fast transients like and ESD-strike can be clamped with minimal over- or undershoots.

<b>ELECTRICAL CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	15	V
Reverse voltage	At $I_R = 0.05\text{ }\mu\text{A}$	$V_R$	15	-	-	V
Reverse current	At $V_{RWM} = 15\text{ V}$	$I_R$	-	-	50	nA
Reverse breakdown voltage	At $I_R = 1\text{ mA}$	$V_{BR}$	15.8	16.8	17.8	V
Reverse clamping voltage	At $I_{PP} = 1\text{ A}$ ; $t_p = 8/20\text{ }\mu\text{s}$	$V_C$	-	18	20	V
	At $I_{PP} = I_{PPM} = 2.5\text{ A}$ ; $t_p = 8/20\text{ }\mu\text{s}$	$V_C$	-	21	26	V
Capacitance	At $V_R = 0\text{ V}$ ; $f = 1\text{ MHz}$	$C_D$	-	5.5	6.5	pF
	At $V_R = 5\text{ V}$ ; $f = 1\text{ MHz}$	$C_D$	-	4	-	pF
Clamping voltage	Transmission Line Pulse (TLP); $t_p = 100\text{ ns}$ $I_{TLP} = 8\text{ A}$	$V_{C-TLP}$	-	22	-	V
Clamping voltage	Transmission Line Pulse (TLP); $t_p = 100\text{ ns}$ $I_{TLP} = 16\text{ A}$	$V_{C-TLP}$	-	26	-	V
Dynamic resistance	Transmission Line Pulse (TLP); $t_p = 100\text{ ns}$	$R_{DYN}$	-	0.52	-	$\Omega$



**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

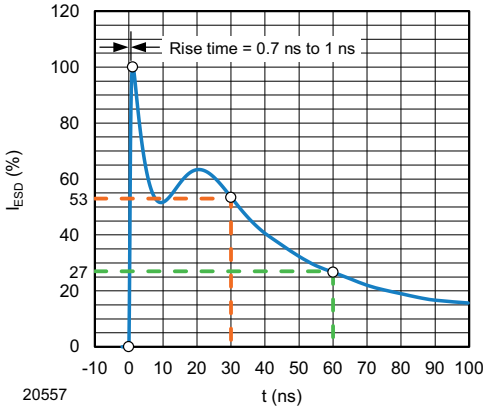


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

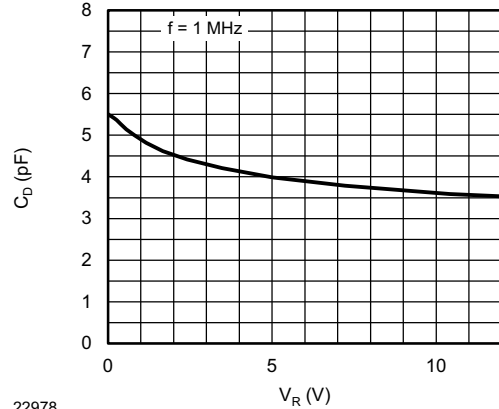


Fig. 4 - Typical Capacitance vs. Reverse Voltage

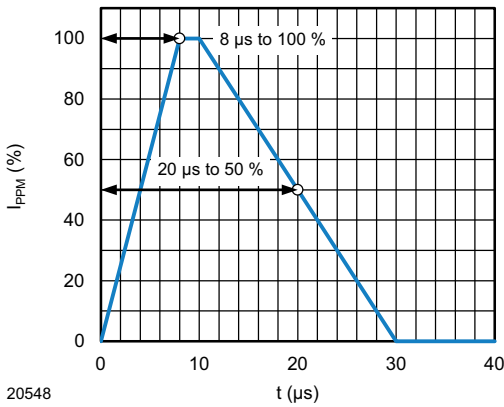


Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form acc. IEC 61000-4-5

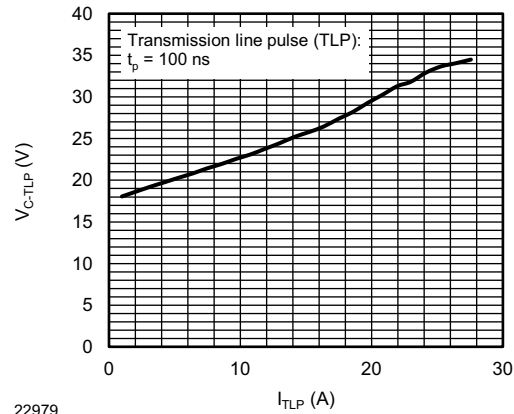


Fig. 5 - Typical Clamping Voltage vs. Peak Pulse Current

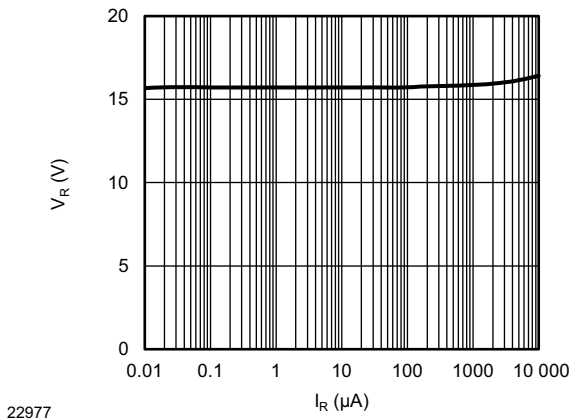


Fig. 3 - Typical Reverse Voltage vs. Reverse Current

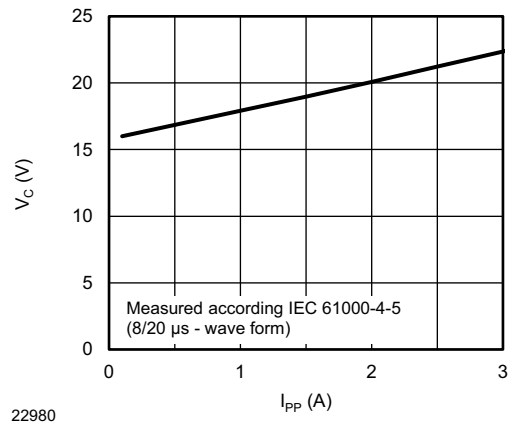
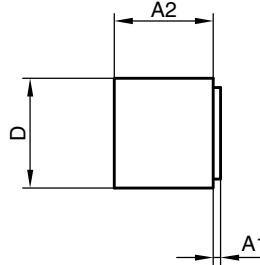
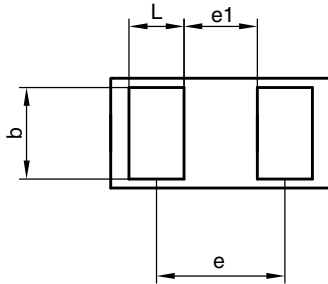


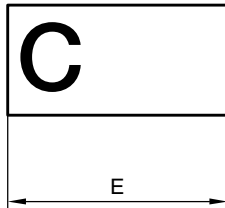
Fig. 6 - Typical Peak Clamping Voltage vs. Peak Pulse Current



**PACKAGE DIMENSIONS** in millimeters (mils): **CLP0603-2L**



Package = chip dimensions in mm [mils]



	Millimeters			mils		
	min.	nom.	max.	min.	nom.	max.
A	0.25	0.28	0.30	9.84	11.02	11.81
A1	0.01	0.01	0.02	0.39	0.39	0.79
A2	0.24	0.27	0.28	9.45	10.63	11.02
b	0.22	0.25	0.28	8.66	9.84	11.02
D	0.27	0.30	0.33	10.62	11.81	12.99
E	0.57	0.60	0.63	22.44	23.62	24.80
e		0.40			15.75	
e1		0.25			9.84	
L	0.12	0.15	0.18	4.72	5.91	7.09

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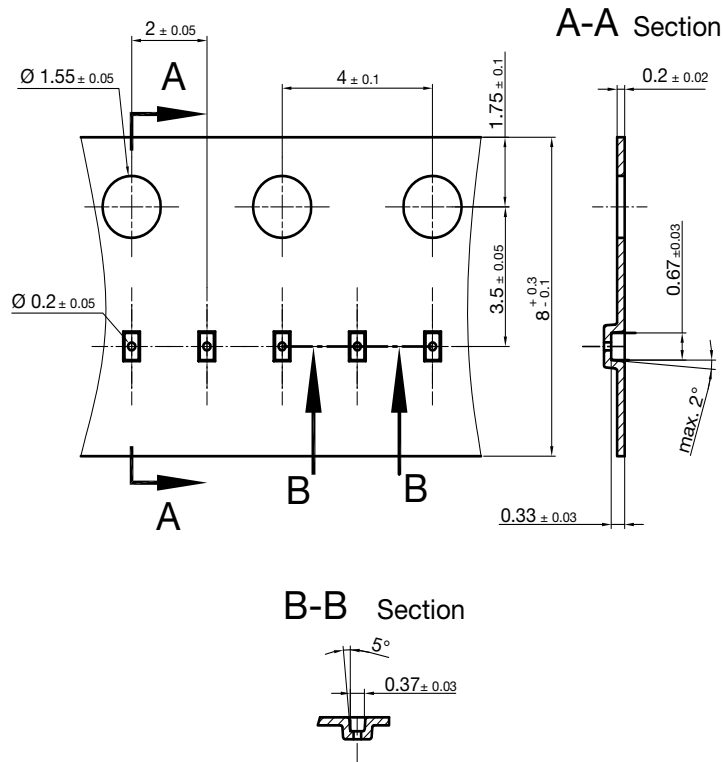
2 terminal leadless package (CLP)  
 Document no.: S8-V-3906.04-023 (4)  
 Created - Date: 22. Nov. 2010  
 Rev.8 - Date: 11. Nov. 2016

**Footprint and soldering recommendation:**

please see Application Note: [www.vishay.com/doc?85917](http://www.vishay.com/doc?85917)



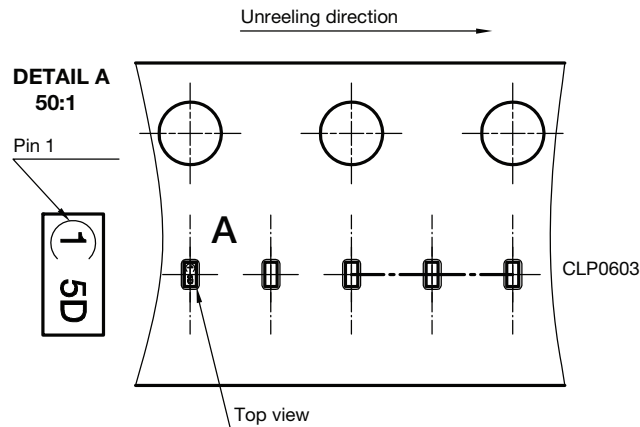
**CARRIER TAPE** in millimeters: **CLP0603-2L**



Cummulative tolerances of 10 sprocket holes is  $\pm 0.2$  mm

22591  
Document no. S8-V-3906.04-0025 (4)  
Created - Date: 22. Nov. 2010

**ORIENTATION IN CARRIER CLP0603-2L**



22936

Orientation in Carrier Tape (CLP0603)  
S8-V-3906.04-026 (4)  
22.10.2010



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