Errata for SmartLEWIS RX+ family (TDA5240/35/25) v1.5

Note: This Errata is valid for the current Data Sheets of TDA5240_v4.0, TDA5235_v1.0 and TDA5225_v1.0.

Status: April/03/2012

#	release version	release date	entry date	item group	a more detailed description	where to find	Note
1	1.0	17.05.2010	13.04.2010	TDA5240 / 35 - Data Slicer Mode	Information: The Data Slicer Configuration value **0x95** is wrong and needs to be replaced by a value of **0xD5** (register x_SLCCFG).	See Data Sheet of TDA5240 v4.0 on page 49 and 233. See Data Sheet of TDA5235 v1.0 on page 49 and 216.	
2	1.0	17.05.2010	17.05.2010	TDA5240 / 35 - Data Slicer Bit Mode and Wake-up Mode	Information: Description of "Data Slicer Bit Mode" can be relaxed from "**On using Data Slicer Bit Mode, the Wake-up criteria Equal Bits Detection and Pattern Detection cannot be applied.**" to "**On using Data Slicer Bit Mode, the Wake-up criteria Random Bits and Pattern Detection cannot be applied.** **When using Data Slicer Bit Mode, the Wake-up criterion Equal Bits Detection cannot be applied in case the transmitted Manchester/Bi-phase coded bit stream used for the Wake-up decision contains a sequence of at least two equal chips.** "	See Data Sheet of TDA5240 v4.0 on page 49. See Data Sheet of TDA5235 v1.0 on page 49.	
3	1.0	17.05.2010	17.05.2010	TDA5240 / 35 - Data Slicer Bit Mode and Wake-up Mode	Information: Description of "Data Slicer Bit Mode" can be relaxed from "**On using Data Slicer Bit Mode, the Wake-up criteria Equal Bits Detection and Pattern Detection ~~cannot be applied~~. Further details can be seen at the end of Chapter 2.4.8.4.**" to "**On using Data Slicer Bit Mode, the Wake-up criteria Equal Bits Detection, Random Bits and Pattern Detection have limitations. Further details can be seen at the end of Chapter 2.4.8.4.** "	See Data Sheet of TDA5240 v4.0 on page 53. See Data Sheet of TDA5235 v1.0 on page 53.	
4	1.0	17.05.2010	19.04.2010	TDA5240 / 35 / 25 - AGC calculation	Information: AGC calculation has a slight limitation: **Note: Following conditions always have to be fulfilled: AGCTHOFFS + 1.6 * AGCTLO < 102.4 and AGCTHOFFS + 25.6 + 1.6 * AGCTUP < 102.4**	See Data Sheet of TDA5240 v4.0 on page 31, 218 + 219. See Data Sheet of TDA5235 v1.0 on page 31, 202. See Data Sheet of TDA5225 v1.0 on page 30, 133 + 134.	
5	1.0	17.05.2010	30.04.2010	TDA5240 / 35 / 25 - ADC source selection	Information: **Measuring temperature (or VDDD) is recommended in Sleep Mode only and is fully functional in this mode.** **It is not recommended to measure Temperature or VDDD during Run Mode Slave or Self Polling Mode, as the RF input signal cannot be processed in that case and other side effects will occur.** Temperature or VDDD measurement itself would be working OK in the operating modes Run Mode Slave or Self Polling Mode, but changing the ADC input source to Temperature (or VDDD) does not open the connection to the subsequent Peak Memory filter in the signal chain in these modes. So during a temperature measurement the PMF gets loaded and the unloading is performed with the selected PMF Decay time, which is several bits usually. After 2 tau (2 * Decay time) the signal went down by 87% (this seems to be OK as first proposal). This additional "wait" time needs to be kept in mind, before being able to receive data again in Run Mode Slave or Self Polling Mode.	See Data Sheet of TDA5240 v4.0 on page 34 See Data Sheet of TDA5235 v1.0 on page 34 See Data Sheet of TDA5225 v1.0 on page 33	
6	1.1	23.11.2010	23.11.2010	TDA5240 / 35 / 25 - RSSI calibration procedure	Information: Calculation of RSSIOFFS needs to be slightly adapted from RSSIOFFS=(RSSIR2-RSSIM2)+(SLOPEM-SLOPER)*P_{IN2} to RSSIM2_corr = (RSSIM2*4 - 512)*Round(RSSISLOPE*2^7)*2^-7 + 512 Info: Round is applied due to discrete register values RSSIOFFS = RSSIR2 * 4 - RSSIM2_corr Info: Factor 4 is applied due to 8bit / 10bit values	See Data Sheet of TDA5240 v4.0 on page 37 See Data Sheet of TDA5235 v1.0 on page 37 See Data Sheet of TDA5225 v1.0 on page 35	
7	1.2	14.04.2011	14.04.2011	TDA5240 / 35 - External data processing using chip data output CH_DATA	On using "External Data Processing" mode for "**Chip Data (RX Mode: TMCDS)**" the Framer unit needs to be set to a special condition. Although Framer cannot be used in this mode: * the TSI length must be set to maximum of 32 chips * TSI pattern needs to be set to default value (all ZERO chips) and * no EOM criterion is allowed to be activated	This is relevant for TDA5240 and TDA5235 only. See Data Sheet of TDA5240 v4.0 on page 81 See Data Sheet of TDA5235 v1.0 on page 81	

8	1.3	20.04.2011	20.04.2011	TDA5240 / 35 - Data Slicer Bit Mode usage	On using Data Slicer Bit Mode (Note: no Manchester Code Violations CV allowed in this mode) a register-configured TSI is not completely unique, therefore undesired FSYNCs can be generated. 2 cases need to be considered for Data Slicer Bit Mode: * C1: If 2 consecutive chips are equal in a configured TSI pattern, then the 2nd equal chip will be interpreted as wildcard (means can be 0 or 1, see **X** in example). * C2: In case 2 equal chips are transmitted, then the 2nd chip may not be clearly detected by the Data Slicer in Bit mode (missing zero-tube in Bit mode generates 0 or 1 chip due to noise). Note: * Several sequences of 2 consecutive equal chips in a TSI increase the number of ambiguities. * A few chips before and after the configured TSI may be considered as well for this ambiguity. Remedy: * Data Slicer Chip Mode is working OK, therefore a change from Data Slicer Bit Mode to Data Slicer Chip Mode may be a good alternative. * A longer TSI pattern reduces the probability of occurence of an undesired FSYNC in Data Slicer Bit Mode. * In case MID is used in the application, this could slightly help in Data Slicer Bit Mode, as after detecting a undesired TSI and after an unsuccessful MID search (e.g.: 4 byte) a new TSI search will take place.	This is relevant for TDA5240 and TDA5235 only. See Data Sheet of TDA5240 v4.0 on page 49 See Data Sheet of TDA5235 v1.0 on page 49	Example: * Data Slicer Bit Mode (no CV allowed) * Manchester Encoding * TSI pattern configuration at RX: 010101010110 ==> in Bit mode interpreted as 0101010101**X**0 A RUNIN is transmitted before the TSI, where RUNIN looks like the beginning of the TSI (This is anyway a pre-condition for Data Slicer Bit Mode). Also **first chips of payload** can lead to accidentially FSYNC detection. * Transmitted TSI: 010101010110 generates FSYNC ==> **OK** as expected * Transmitted TSI: 010101010100 intepreted as 0101010101**X**0 generates FSYNC ==> **not OK**, but CV transmitted (C1) * Transmitted TSI: 010101010111 **10** interpreted as 0101010101X1 10 generates FSYNC ==> **not OK**, but CV transmitted (C2) * Transmitted TSI: 010101010101 **10** interpreted as 010101010101 10 generates FSYNC ==> **not OK**, but this is a general topic => make RX TSI more unique * Transmitted TSI: 010101010010 interpreted as 0101010100**X**10 generates FSYNC ==> **not OK**, but CV transmitted (C2) Note: This behavior in Data Slicer Bit Mode can occur both in Manchester and Bi-phase Decoding mode.
9	1.4	30.6..2011	30.06.2011	TDA5240 / 35 - Data Slicer Mode	Information: The Data Slicer Configuration gets additional explanation. x_SLCCFG = 0x94: Chip Mode EOM-Datalength: For patterns with code violations in data packet and optimized for activated EOM data length criterion only. **This mode can also be used for Manchester or Bi-phaseSpace/Bi-phaseMark encoded data at CH_DATA / CH_STR data output.** x_SLCCFG = 0xD5: Chip Mode Transparent: When Framer is not used, but CH_DATA / CH_STR are used for data processing. **This mode can be used, when baseband coding is a 2-phase coding, but neither Manchester, nor Bi-phaseSpace/Bi-phaseMark.**	See Data Sheet of TDA5240 v4.0 on page 49 and 233. See Data Sheet of TDA5235 v1.0 on page 49 and 216.	
10	1.5	03.04.2012	03.04.2012	TDA5240 / 35 / 25 - RSSIRX readout, RSSIPRX readout, RSSIPPL readout	Readout value of register RSSIRX, RSSIPRX and RSSIPPL can show premature saturation with following AGC settings (AGC is deactivated): * „AGC Start Configuration = **OFF**" (AGCSTART=0b00) * „AGC Gain Control = **automatic**" (AGCGAIN=0b11) (Info: Saturation of digital RSSI takes place at register readout value (AGCTHOFFS+AGCTHLO*1.6dB)*2.5digit/dB) Therefore AGC settings should be changed to the following (AGC is deactivated as well; no premature RSSIRX/RSSIPRX/RSSIPPL saturation will take place): * „AGC Start Configuration = **Direct ON**" (AGCSTART=0b01) * „AGC Gain Control = **0dB**" (AGCGAIN=0b00) This effect is anyway not observable, when AGC is activated („AGC Start Configuration = Direct ON" and „AGC Gain Control = automatic").	See also Data Sheet of TDA5240 v4.0 on page 37 See also Data Sheet of TDA5235 v1.0 on page 37 See also Data Sheet of TDA5225 v1.0 on page 35	