CML Microcircuits

COMMUNICATION SEMICONDUCTORS

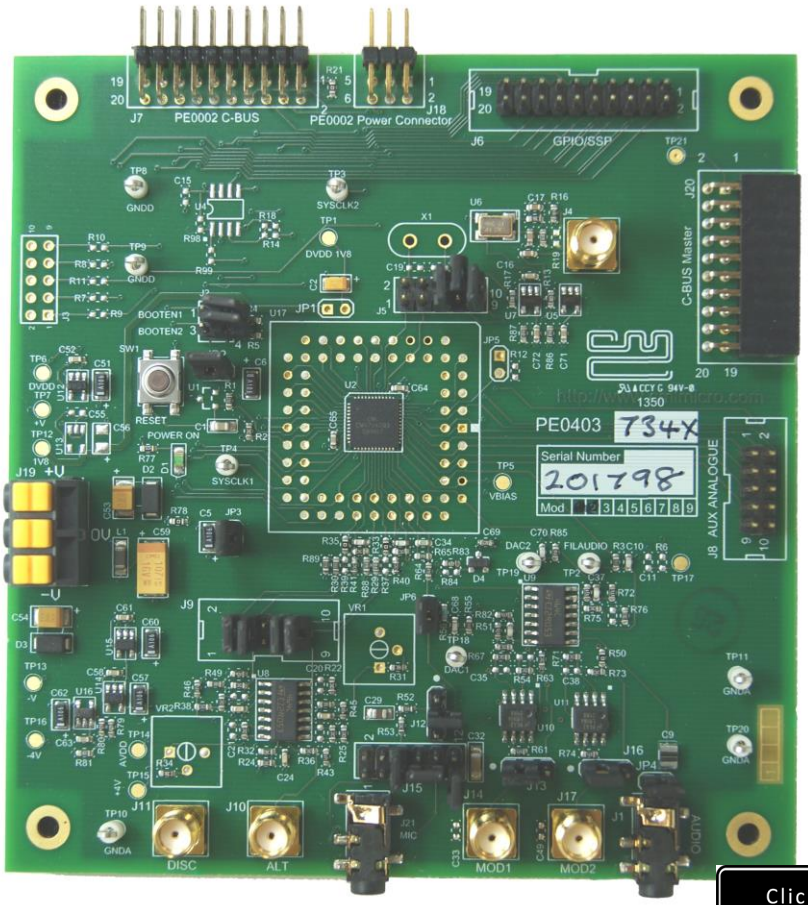
PE0403 Evaluation Kit User Manual

um0403/1 July 2014

Provisional Issue

Features

- **PE0403 - 724x for CMX724x family *FirmASIC*® product range evaluation; fitted with CMX7240 to emulate CMX724x device performance**
- **PE0403 - 734x for CMX734x family *FirmASIC*® product range evaluation; fitted with CMX7340 to emulate CMX734x device performance**
- **Instrumentation interface (requires an additional –5 volt supply):**
  - **50Ω Output signal drivers**
  - **Instrumentation interface to CMX7240 single-ended input signals (PE0403 - 724x only)**
  - **Instrumentation interface to CMX7340 differential input signals (PE0403 - 734x only)**
- **On-board supply regulators operate from a single 5 volt supply**
- **19.2MHz oscillator or external clock input to the on-board reference device**
- **Command and control by PC via the PE0002 Interface Card or via the user's microcontroller emulator or development application**
- **On-board access to all CMX7240/CMX7340 signals, commands and data**
- **C-BUS Master for CMX7240/CMX7340 control of other CML Evaluation Kits**



Click here for:
- Latest Datasheet
- Product Data Resource

1. Brief Description

The PE0403 Platform Evaluation Kit is designed to assist in the evaluation and application development of the CMX724x and CMX734x ranges of *FirmASIC*® products. The kit is in the form of a populated PCB comprising a generic CMX7240 or CMX7340 IC and the appropriate supporting components and circuitry. The PE0403 - 724x is fitted with a CMX7240 and the PE0403 - 734x is fitted with a CMX7340.

The board also incorporates all of the necessary power-supply regulation facilities for operation from a single 5 volt supply, or a dual +/-5 volt supply if the instrumentation interface is required.

The board is fitted with a C-BUS connector allowing the PE0403 to be operated by connection to either of the two C-BUS ports on a CML PE0002 Interface Card, and used with the associated PC GUI software, or by direct connection between the CMX7240/CMX7340 C-BUS and the user's µC development application or emulation system.

The common CMX724x/CMX734x Function Image™ (FI) can be loaded, on power-up, directly into the on-board target IC (CMX7240/CMX7340) using the PE0002 interface or the user's system.

Function images suitable for the CMX724x/CMX734x range of products can be downloaded from the CML Technical Portal.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
1	Initial release	1st July 2014

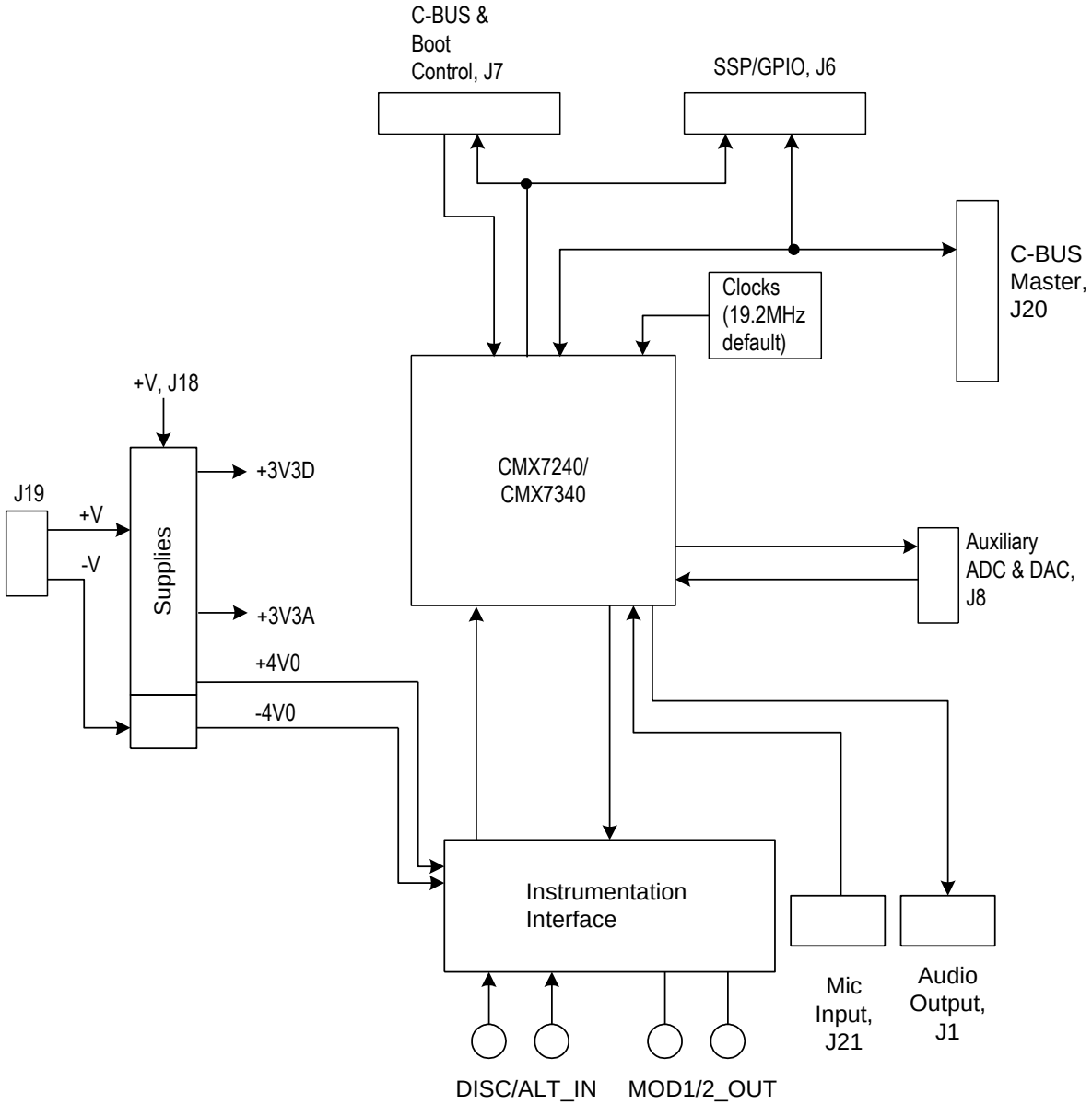


Figure 1 Block Diagram

2. Preliminary Information

2.1. Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

A 5 volt dc regulated power supply (or +/- 5 volt supply when using the instrumentation interface).

If the PE0403 is being used with the PE0002 Interface Card, the following items will also be required:

An IBM compatible PC with the following requirements:

- One of the following Windows operating systems installed: 2000sp4, XPsp2, Vista or Win7
- USB port
- Minimum screen resolution 800 x 600. Recommended resolution 1024 x 768.

A USB type A male to mini B male cable.

Software application **`ES000243.exe`**, or later version, installed on the PC.

2.2. Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

2.2.1. Static Protection

This product uses low-power CMOS circuits that can be damaged by electrostatic discharge. Partially-damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

2.2.2. Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EK0403) and notify CML within seven working days if the delivery is incomplete.

2.3. Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product.

3. Quick Start

This section is divided into two sub-sections. The first is for those users who are using the PE0403 with a PE0002 controller card and its Windows PC GUI software. The second is for users who are using the PE0403 by itself, without a PE0002.

3.1. With PE0002

Note that the C-BUS connector, J7, and the power connector J18 are both right angle headers and are designed to plug directly into sockets J5 (C-BUS 1 port) and J9 respectively, or sockets J3 (C-BUS 2 port) and J7 respectively, of a PE0002.

3.1.1. Setting-Up

Refer to the PE0002 user manual and follow the instructions given in the quick start section. Ensure the jumpers on J2 are open circuit. The CMX7240/CMX7340 BOOTEN1 and BOOTEN2 pins are driven from the PE0002.

The basic arrangement, when used with the PE0002, is shown below:

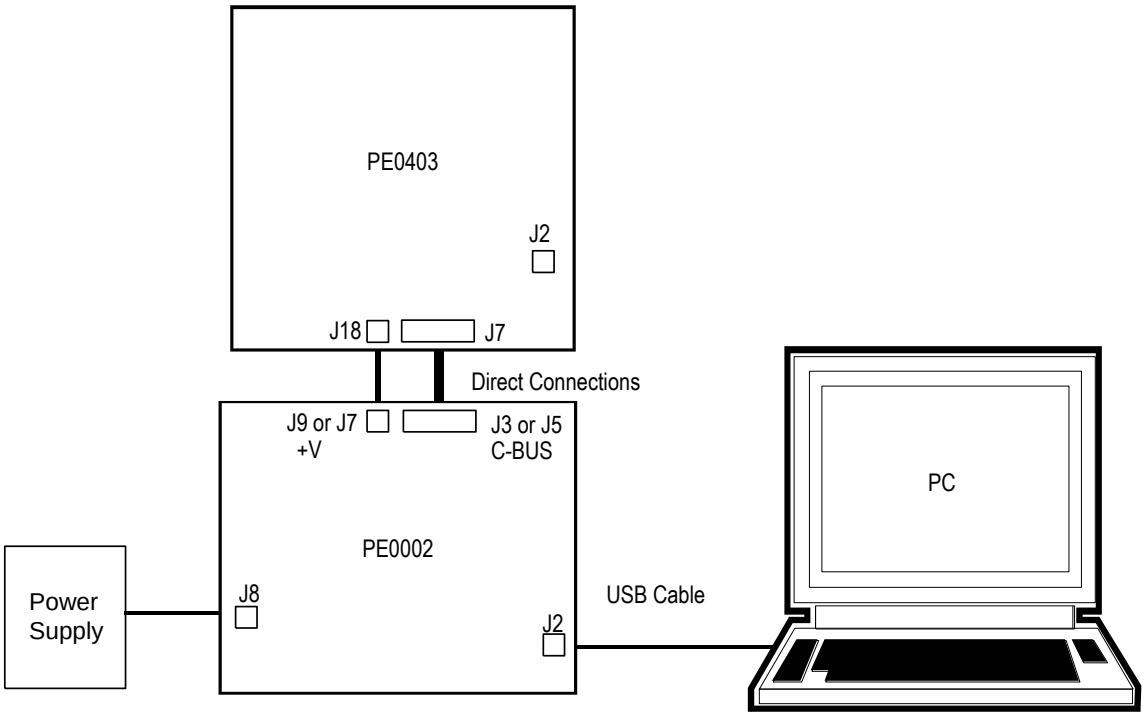


Figure 2 PE0403 used with PE0002

3.1.2. Operation

The Function Image™ (FI) must now be loaded into the CMX7240/CMX7340 device. A FI is provided as a 'C' type header file and must be obtained from the CML Project Resource Portal. This can be loaded directly from a file on the PE0002 host PC to the CMX7240/CMX7340.

The PE0403 should now be ready for evaluation of the CMX7240/CMX7340 with the chosen FI.

3.2. Without PE0002

As an alternative to using the PE0002 controller kit, users may control the CMX7240/CMX7340 target device with a user-supplied host controller card. The C-BUS connections are made via connector J7.

The power-up, or boot state of the CMX7240/CMX7340 BOOTEN1 and BOOTEN2 pins may be set using jumpers on header, J2. Consult the relevant CMX734x documentation for valid modes. A jumper in-circuit on header, J2, corresponds to a '0' state on the boot pins. Alternatively the state of these pins may be set via the connector, J7, pins 13 and 14. By default, 47kΩ pullup resistors on the PE0403 board provide a '1' state on each of the two BOOTEN pins.

A FI for the CMX7240/CMX7340 device must be included in the customer's host system and loaded into the CMX7240/CMX7340 device on power-up.

4. Signal Lists

Table 1 Signal List

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1	TIP	SPKR	O/P	AUDIO
	RING	-	(O/P)	*(dependent on the setting of JP4, see 6.1.6)*
	SLEEVE	GNDA	PWR	Analogue ground.
J4	-	CLK EXT	I/P	External input option for CMX7240/CMX7340 clock.
J6	1,4,5,6, 9,10,18	-	N/C	Do not make any connection to these pins
	2	GPIO1	BI	General purpose I/O pin.
	3	GPIO2	BI	General purpose I/O pin.
	7	GPIOA	BI	General purpose I/O pin.
	8	GPIOB	BI	General purpose I/O pin.
	11	SYSCLK2	O/P	CMX7240/CMX7340 system clock 2 output.
	12	SYSCLK1	O/P	CMX7240/CMX7340 system clock 1 output.
	13	MOSI	O/P	SSP Master output, slave input.
	14	SSOUT/ FSO	BI	SSP Frame sync.
	15	MISO	I/P	SSP Master input, slave output.
	16	EPSCSN	O/P	EEPROM Chip Select
	17	SSPCLK	BI	SSP Clock.
	19, 20	GNDD	PWR	Digital supply ground.
J7	3, 5, 7, 9, 15 to 20	-	N/C	Do not make any connection to these pins
	1	RESET	I/P	CMX7240/CMX7340 Hardware Reset Pin
	2	CSN	I/P	Chip select. Connects to host μC.
	4	CDATA	I/P	Serial Data input. Connects to host μC.
	6	SCLK	I/P	Serial clock input. Connects to host μC.
	8	RDATA	O/P	Serial data output. Connects to host μC.

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
	10	IRQN	O/P	Interrupt request. Connects to host μC.
	11, 12	GNDD	PWR	Digital supply ground.
J7	13	BOOTEN1	I/P	CMX7240/CMX7340 Hardware Boot Control.
	14	BOOTEN2	I/P	CMX7240/CMX7340 Hardware Boot Control.
J8	1	AUXADC4	I/P	Auxiliary ADC input.
	2	AUXDAC1	O/P	Auxiliary DAC output.
	3	AUXADC3	I/P	Auxiliary ADC input.
	4	AUXDAC2	O/P	Auxiliary DAC output.
	5	AUXADC2	I/P	Auxiliary ADC input.
	6	AUXDAC3	O/P	Auxiliary DAC output.
	7	AUXADC1	I/P	Auxiliary ADC input.
	8	AUXDAC4	O/P	Auxiliary DAC output.
	9, 10	GNDA	PWR	Analogue supply ground.
J9	1 #	IP1P	O/P	Channel 1(DISC) input positive, instrumentation output.
	2 #		I/P	Channel 1(DISC) input positive.
	3	IP1N	O/P	Channel 1(DISC) input negative, instrumentation output.
	4		I/P	Channel 1(DISC) input negative.
	5, 6	GNDA	PWR	Analogue ground.
	7	IP2N	O/P	Channel 2(ALT) input negative, instrumentation output.
	8		I/P	Channel 2(ALT) input negative.
	9 #	IP2P	O/P	Channel 2(ALT) input positive, instrumentation output.
	10 #		I/P	Channel 2(ALT) input positive.
J10	1	ALT	I/P	Channel 2(ALT) instrument input, single ended.
J11	1	DISC	I/P	Channel 1(DISC) instrument input, single ended.

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J14	1	MOD1	O/P	MOD1 output
J17	1	MOD2	O/P	MOD2 output.
J18	1, 2	GNDD	PWR	Digital supply ground.
	3 to 6	+V	PWR	External supply voltage – Daisy chained from PE0002.
J19	3	+V	PWR	External supply voltage, nominally +5 volt.
	2	0V	PWR	External supply ground.
	1	-V	PWR	Optional external negative supply voltage, nominally -5 volt.
J20	1,3,5,7, 9, 10 and 13 to 20	-	N/C	Do not make any connection to these pins
	2	SSOUT	BI	C-BUS master, chip select, FI dependent.
	4	MOSI	BI	C-BUS master, command data, FI dependent.
	6	CLK	BI	C-BUS master, serial clock, FI dependent.
	8	MISO	BI	C-BUS master, reply data, FI dependent.
	11, 12	GNDD	PWR	Digital ground.
J21	TIP	T	I/P	Optional Mic In (tip) – see 6.1.6 and J15
	RING	R	I/P	Optional Mic In (ring) – see 6.1.6 and J15
	SLEEVE	G	PWR	Analogue ground.(if J15 pin 9-7 shorted)

Notes:
BI = Bidirectional
HiZ = High impedance
I/P = Input
N/C = Not connected
O/P = Output
PWR = Power supply connection

For PE0403 - 724x boards, connector J9: pins 1, 2, 9 and 10 are N/C. Do not connect to these pins.

Table 2 Test Points

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP2	HiZ	Loop – Non-buffered Audio output
TP3	0V	Loop – CMX7240/CMX7340 system clock 2 output.
TP4	19.2MHz	Loop – CMX7240/CMX7340 system clock 1 output.
TP5	+1.65V	Pad – CMX7240/CMX7340 VBIAS.
TP6	+3.3V	Pad – DVDD, digital supply.
TP7	+5V	Pad – External supply voltage.
TP8	0V	Loop – GNDD, digital ground.
TP9	0V	Loop – GNDD, digital ground.
TP10	0V	Loop – GNDA, analogue ground.
TP11	0V	Loop – GNDA, analogue ground.
TP12	-	Pad – Output from on-board regulator (not fitted). Optional external DC supply voltage for CMX7240/CMX7340 core.
TP13	-5V	Pad – Optional external negative supply voltage, nominally -5 volt.
TP14	+3.3V	Pad – AVDD, analogue supply.
TP15	+4.0V	Pad – Output from on-board regulator. Positive supply voltage for instrumentation interface, +4.0V – if required.
TP16	-4.0V	Pad – Output from on-board regulator. Negative supply voltage for instrumentation interface, -4.0V – if required.
TP18	HiZ	Loop – MOD1 - Channel 1 output.
TP19	HiZ	Loop – MOD2 - Channel 2 output.
TP20	0V	Loop – GNDA, analogue ground.

Table 3 Jumpers

JUMPERS			
Link Ref.	**Positions**	**Default Position**	**Description**
JP2	1-2	Short	Isolates digital supply rail from CMX7240/CMX7340.
JP3	1-2	Short	Isolates analogue supply rail from CMX7240/CMX7340.
JP4	1-2	Open	Connects Audio(J1) connector Ring to Tip.
JP6	1-2	Short	Select Mic or Line level for Mic input (Short for Mic level)
J2	1-2	Open	Manual BootEn1 control (short = LO).
	3-4	Open	Manual BootEn2 control (short = LO).
J5	1-2	Open	Crystal clock source – if components fitted by customer.
	3-4	Open	Crystal clock source – if components fitted by customer.
	5-6	Short	19.2MHz oscillator clock source.
	7-8	Open	External clock source.
	9-10	Short	Ground external clock input.
J9	1-2	Short	Isolates channel 1(DISC) input +ve from instrumentation interface.
	3-4	Short	Isolates channel 1(DISC) input -ve from instrumentation interface.
	7-8	Short	Isolates channel 2(ALT) input -ve from instrumentation interface.
	9-10	Short	Isolates channel 2(ALT) input +ve from instrumentation interface.
J13	1-2/2-3	1-2	Connect the 50 Ohm driver to J14 if (1-2), or bypass the 50 Ohm driver if (2-3)
J12	1-2/2-3	Open	Set Mic bias level, 1-2 for 3V3, 2-3 for +V input, or open for bias disabled. See 6.1.6.
J15	3-4,5-6,7-9	-	See 6.1.6 Audio Interfaces.
	11-12	Open	Select coupling on Mic input. Short to DC couple.
J16	1-2	1-2/2-3	Connect the 50 Ohm driver to J17 if (1-2) or bypass the 50 Ohm driver if (2-3)

Table 4 LEDs

LEDs	
LED Ref.	**Description**
D1	Indicates that the digital supply voltage is present.

5. Circuit Schematics and Board Layouts

For clarity, circuit schematics are available as separate high-resolution files. These can be obtained via the CML website.

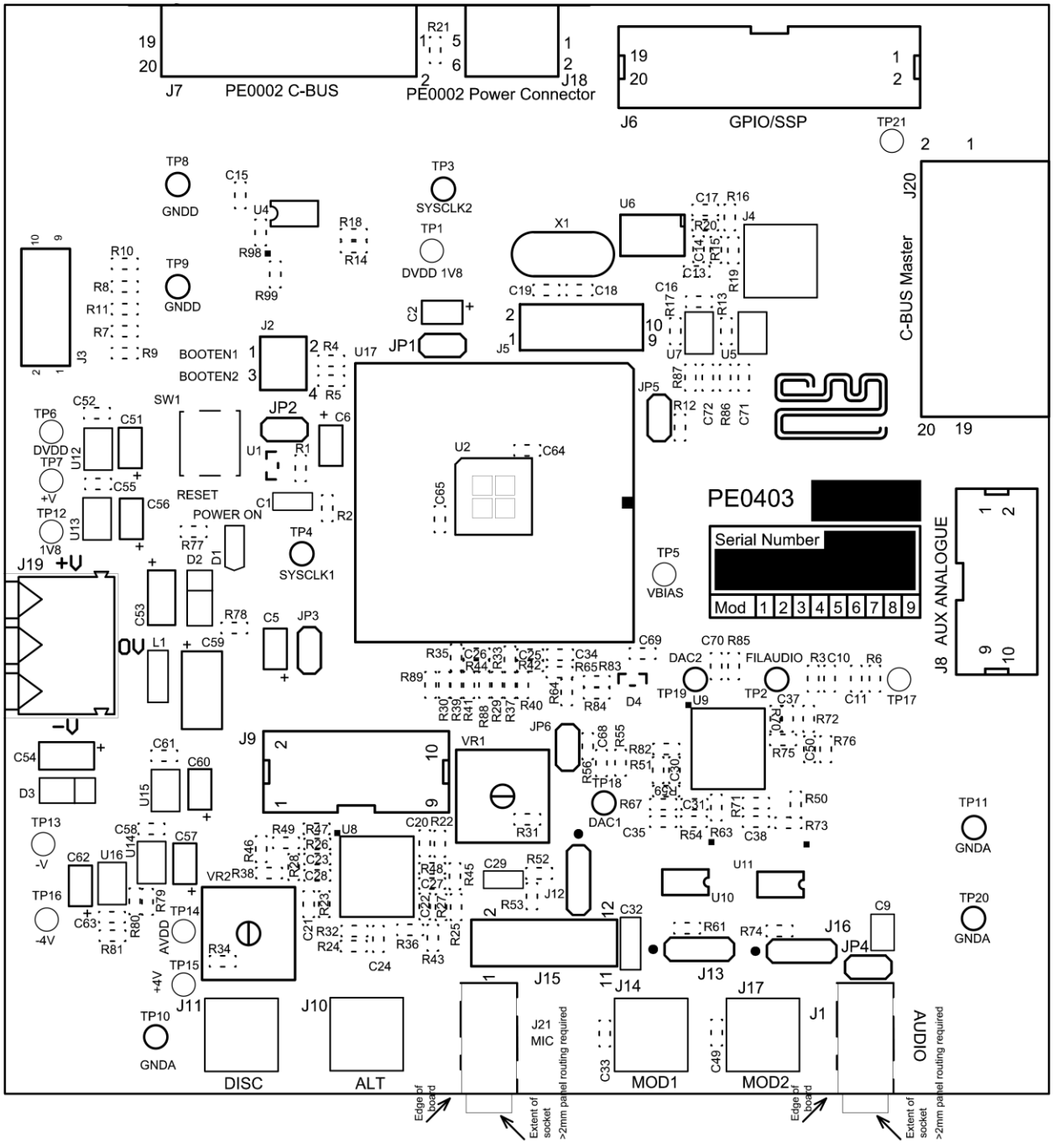


Figure 3 PCB Layout: Top

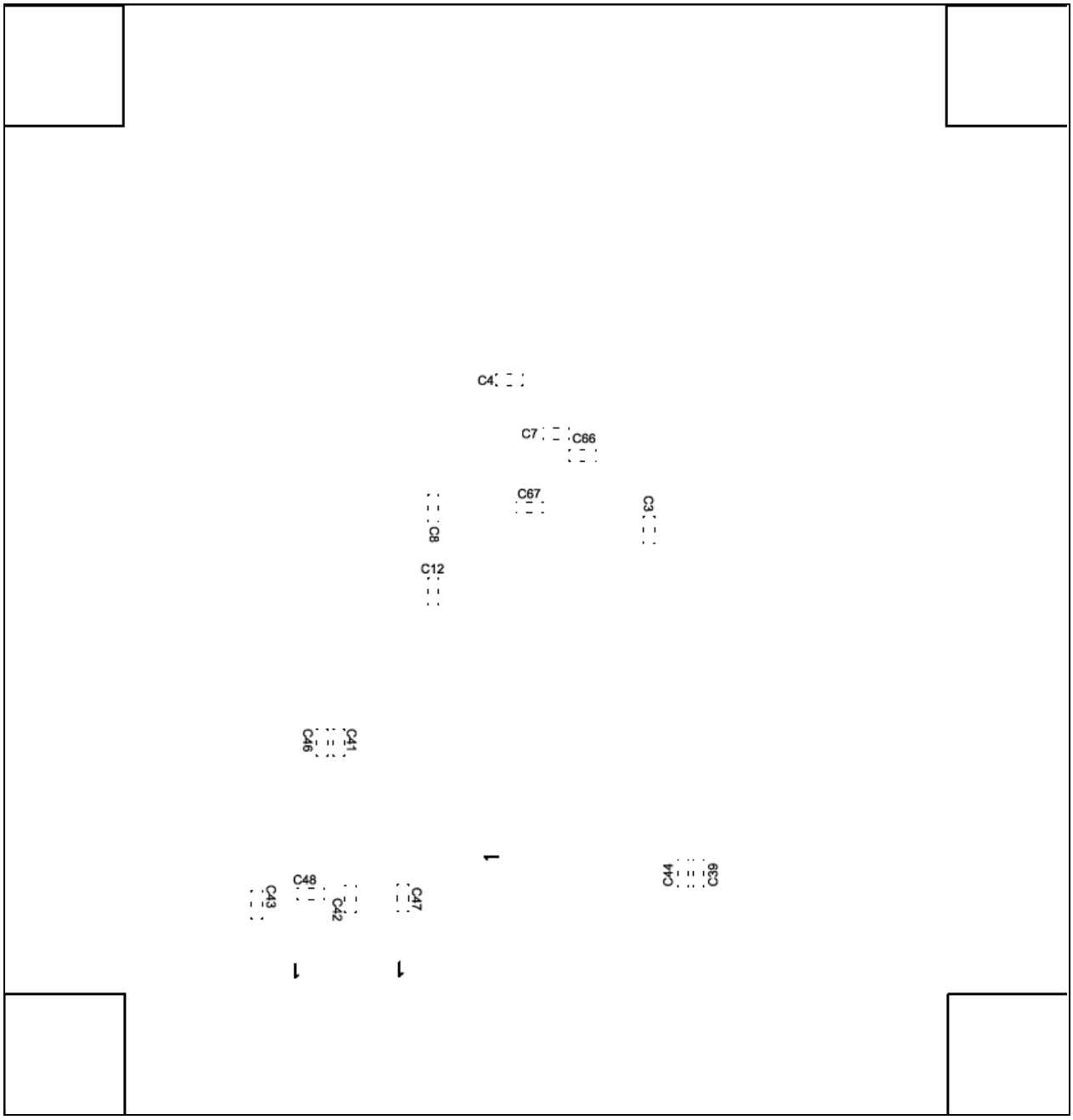


Figure 4 PCB Layout: Bottom

6. Detailed Description

6.1. Hardware Description

The PE0403 as shipped may not have the optimum configuration or component values for all function images. Check the PE0403 schematic against recommendations in the specific CMX734x datasheet.

6.1.1. Power Supplies

The board is fitted with four voltage regulators and has a footprint for a fifth regulator.

U12 and U14 provide the digital and analogue supply rails respectively. The input to these two regulators should be provided by an external 5V dc regulated power supply, which can be daisy chained from the PE0002 or connected to the board via connector J19, a push type connector. LED illumination confirms the on-board presence of the +3.3V dc digital voltage supply.

U15 and U16 provides the +/-4V required for the instrumentation interface, the input to these regulators should be provided by an external +/-5V dc regulated power supply connected to the board via connector J19, if required.

Each supply has a test point where it can be monitored; see Table 2 Test Points

U13 is supplied as an empty footprint for a LP2985IM5 1.8 volt regulator; this can be fitted to supply an external voltage to the CMX7240/CMX7340's VDEC pin. To do this JP1 will need to be fitted, footprints are also supplied for the regulator's supporting components, C55 and C56, where C55 = 10nF and C56 = 10µF. Note: The CMX7240/CMX7340 internal regulator must then be reduced to minimum voltage (1.4V) by writing $77 to C-BUS register $BF.

6.1.2. Clock Options

The PCB is designed to provide three CMX7240/CMX7340 device clock options. The board is supplied with a 19.2MHz oscillator module fitted. This option allows convenient RF synthesiser configuration for typical channel spacings.

Other options are an external clock source at J4 or a 6.144MHz quartz crystal oscillator circuit (C18, C19 and X1).

Header J5 is used with jumper sockets to select the required option as shown in the table below. Shaded cells illustrate locations where a jumper socket should be fitted.

Table 5 Clock Select Jumper Positions

J5 Jumper Position	Clock Option		
	19.2MHz oscillator (default)	External	Quartz crystal
1-2			
3-4			
5-6			
7-8			
9-10			

6.1.3. Control Interface

The C-BUS and CMX7240/CMX7340 boot control signals are brought out on connector J7. This is a right angle male header designed to plug directly into the PE0002 interface card that has a matching female header.

Alternatively, if not using the PE0002, the CMX7240/CMX7340 boot control signals can be manually set with jumpers on header J2.

6.1.4. Baseband Interfacing

The availability and usage of these signals are Function Image™ dependent.

PE0403-724x only:

The CMX7240 single ended inputs are fed through a RC network. Specific requirements for this network are FI dependent. Single-ended signals can be input to the RC networks at header, J9, but must be biased around AVDD/2.

PE0403-734x only:

The CMX7340 differential inputs are fed through a RC network. Specific requirements for this network are FI dependent. Differential signals can be input to the RC networks at header, J9. The 'P' and 'N' signals should each be biased, nominally, around AVDD/2 for maximum use of the available dynamic range. CML evaluation kits for RF receiver products have matching headers, but the signal polarity must be observed. Alternatively, check Function Image™ documentation for the possibility of a programmable signal inversion.

The MIC input and Audio output connections can be made via 3.5mm jack sockets, see section 6.1.6.

The MOD1 and MOD2 outputs can be accessed by using J14 and J17 respectively. Both MOD outputs have the option of using 50 Ohm drivers; this can be configured with J13 and J16 for MOD1 and MOD2 respectively. To configure the outputs, short pin 2 and pin 1 to use the 50 Ohm driver, or short pin 2 and pin 3 to bypass the driver. Use of this section of the PE0403 requires an additional negative supply rail, nominally –5 volts.

For example: to use the 50 Ohm driver with the MOD1 output connect J13 pin 1 to pin 2.

Connector J8 provides access to Auxiliary ADCs 1 to 4 and Auxiliary DACs 1 to 4 of the CMX7240/CMX7340 reference device.

6.1.5. Instrumentation Interface

An instrumentation interface has been provided to enable connection of the signal inputs to laboratory equipment that has only single-ended connections. Use of this section of the PE0403 requires an additional negative supply rail, nominally –5 volts.

PE0403-724x only:

The input path has a gain of 0dB.

The input path is configured to give a signal biased around AVDD/2 at the input to the CMX7240, assuming that the input signal is biased around GNDA. This can be made adjustable by removing resistors R34 and R31 then replacing them with 50k Ohm potentiometers in positions VR2 and VR1 for the DISC and ALT input paths respectively. Bourns type 3386P or similar will fit the footprints provided.

PE0403-734x only:

The input path has an effective gain of 6dB.

The input path is configured for, nominally, 0 volts offset in the differential signal input to the CMX7340, assuming that the input signal is biased around GNDA. This can be made adjustable by removing resistors

R34 and R31 then replacing them with 50k Ohm potentiometers in positions VR2 and VR1 for the DISC and ALT input paths respectively. Bourns type 3386P or similar will fit the footprints provided.

6.1.6. Audio Interfaces

All Audio Interface connectors can be configured to support different types of signal connections and a variety of external equipment such as SoundBlaster™ compatible headsets and PC-based soundcards. The Mic input connector has an optional ground connection to avoid ground loops via external connections.

The Mic/Line In interface is a 3.5mm jack socket J21 connected to the CMX7240/CMX7340 Microphone inputs, via a configurable jumper field J15. See Figure 5 for details of single ended input configuration.

The J21 input can be configured for use as a line or mic input, JP6 selects what type of input is supported; short for a mic input or open circuit for a line input.

DC bias is provided for an electret microphone. This can be selected as 3.3V (fit J12: 1-2) or VIN_FILT (the external supply to the board - fit J12: 2-3), or disabled (remove jumpers from J12).

Signal level and gain settings should be selected to ensure the signal level at all stages in the signal processing chain is kept within the recommended limits.

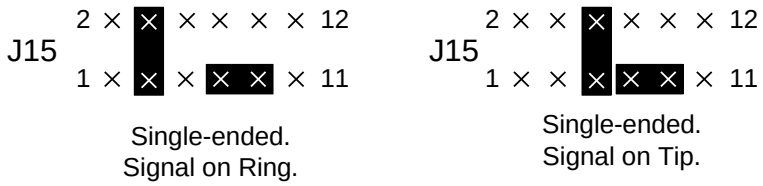


Figure 5 Audio Input Jumper Settings

To DC couple the MIC input short pins 12 and 11 of J15.

The Line Out interface is a 3.5mm jack socket J1 connected to the CMX7240/CMX7340's audio output. The output is connected to the tip of J1. If JP4 is fitted, the signal is also connected to the ring. The sleeve of J1 is connected to the analogue ground of the PCB.

6.1.7. Digital Interfacing

Connector J6 provides access to four general purpose I/O lines, the two sysclk outputs and a synchronous serial port.

Use of these signals is Function Image™ dependent. In some cases they will have no function. See relevant Function Image™ documentation.

Connector J20 is configured as a C-BUS master and compatible with CML evaluation kits with C-BUS slave connectors. Use of this feature is also Function Image™ dependent.

6.2. Adjustments and Controls

The boot state of the CMX7240/CMX7340 device can be set manually, using jumpers on header, J2. When used with the PE0002, these jumpers should be left open circuit.

6.3. Function Image™

There are two methods by which a FI may be loaded into the CMX7240/CMX7340 device.

Whenever power is removed from the PE0403 the FI data will be erased from the CMX7240/CMX7340 device. Therefore, whenever power is applied a FI must be loaded via the C-BUS interface.

If the PE0403 is used with the PE0002 PC interface, Function Images can be loaded as described in sections 6.3.1, 6.3.2 and 6.3.3.

6.3.1. Load Function Image™ via C-BUS

Use the Function Image™ Load tab. Select Function Image™ Source: 'C-BUS'.

- Enter the name of the file containing the Function Image™, or navigate to the required file using the 'Browse' button.
- Enter the activation code in the lower edit box. Alternatively select one of two previously used codes in the drop down list.
- Select Target Board.
- Click the "Load" button. The progress of the download is shown visually on the progress bar and when the download has completed a message box will be displayed indicating if the result of the download operation was successful or not.

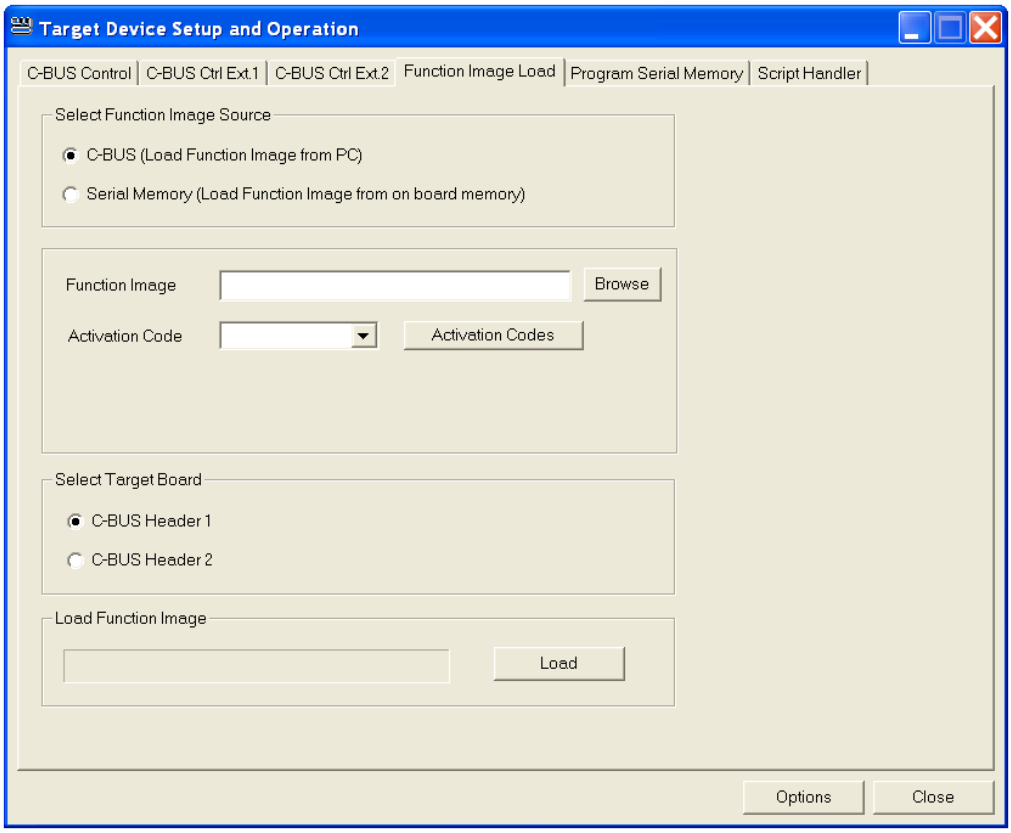


Figure 6 Function Image™ Load Tab – via C-BUS

6.3.2. Load Function Image™ from Serial Memory Device

Note: This option is not supported on PE0403.

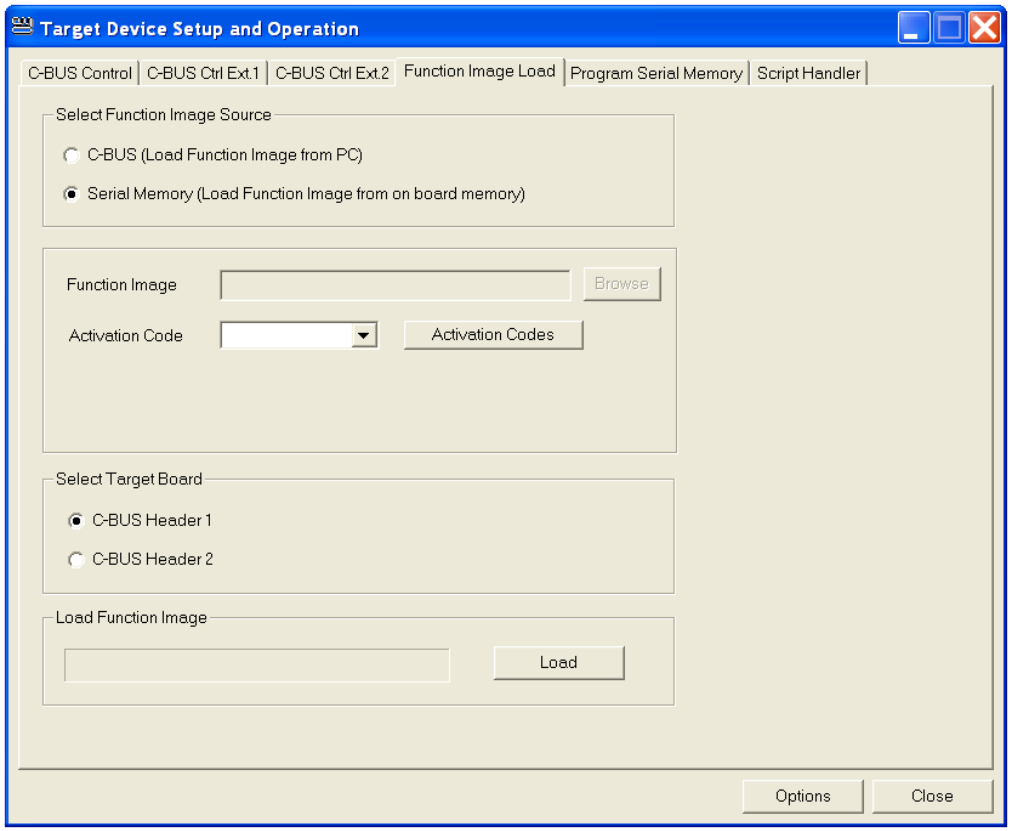


Figure 7 Function Image™ Load Tab – from Serial Memory (not supported)

6.3.3. Program Serial Memory

Note: This option is not supported on PE0403.

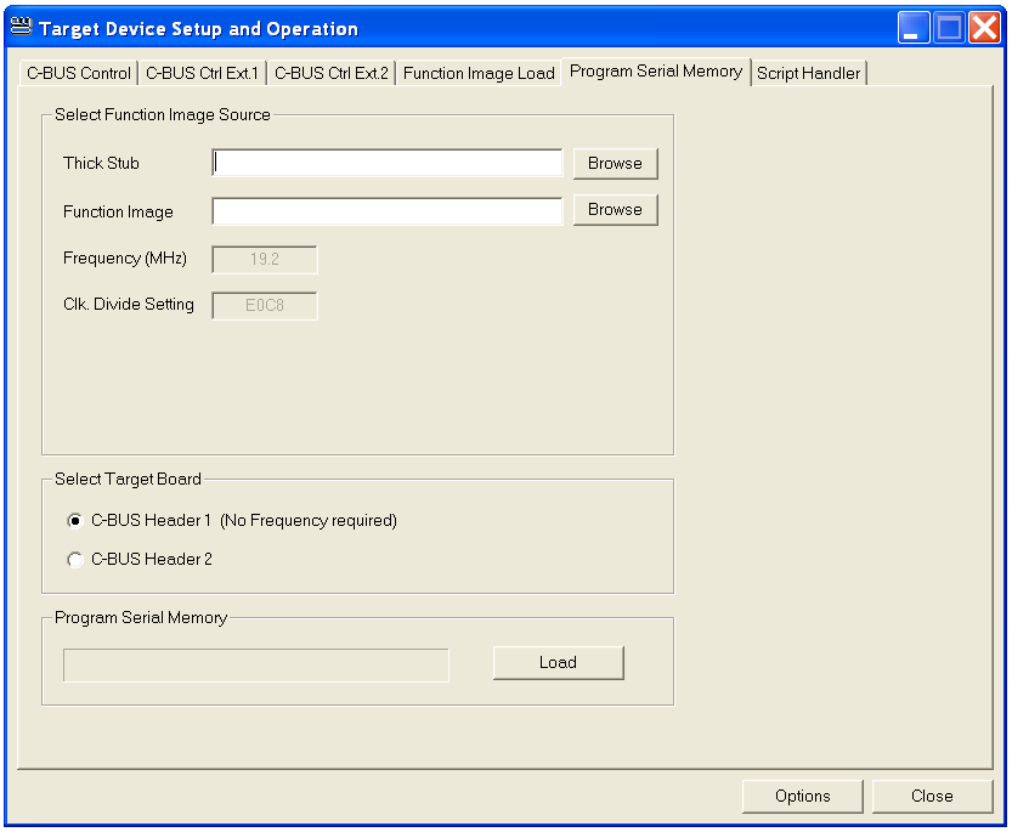


Figure 8 Program Serial Memory Tab (not supported)

6.4. Evaluation Tests

Before a Function Image™ is loaded into the CMX7240/CMX7340 reference device; there is a limited functionality that can be demonstrated directly by programming the C-BUS registers. The following examples can be used to verify control of the CMX7240/CMX7340 via the C-BUS interface. These registers can be programmed using the 'C-BUS Control' tab in the PE0002 software.

6.4.1. Write to and Read from a Register

- Write any 16-bit number to register $C0. The data transferred to the device on the Command Data pin looks like this:

  { C0 } { <ms byte> } { <ls byte> } ..... Command Data

- The value written to this register (the Powerdown Control register) can be read back from register $C4 by issuing a single command byte, then reading two data bytes from the Reply Data pin, as follows:

  { C4 } ..... Command Data
  { <ms byte> } { <ls byte> } ..... Reply Data

Note that the power consumption of the device will increase once this register has been written to, since some parts of the device will no longer be powersaved.

6.4.2. Check Analogue Path and Set Input Gain

Configure the CMX7240/CMX7340 with the C-BUS register data given in Table 6.

Table 6 CMX7240/CMX7340 Register Settings – Analogue Path and Input Gain

	C-BUS Register	
Write Data	Address	Name
$5061	$C0	Powerdown Control
$770F	$B0	Analogue Gain
$0830	$B1	Input Gain and Signal Routing
$0008	$CF	Test Mode

Apply a 1kHz, audio signal to the input, IP3 (J21), at a level of -10dBm (the maximum signal level before distortion is about +1dBm).

Check the audio signal coming out of the AUDIO OUT pin (TP2). The level should be nominally 6.4dB, above the level of the input signal.

6.4.3. Check Analogue Path and Set Output Gain

Configure the CMX7240/CMX7340 with the C-BUS register data given in Table 7.

Table 7 CMX7240/CMX7340 Register Settings – Analogue Path and Output Gain

	C-BUS Register	
Write Data	Address	Name
$A3E1	$C0	Powerdown Control
$650C	$B0	Analogue Gain
$0001	$CF	Test Mode

Apply a differential 1kHz, audio signal across the inputs, IP1 (J11) and IP2 (J10), at a level of 0dBm between them.

Check the audio signal coming out of the AUDIO OUT pin (TP2). The level should be –9.2dBm.

Check the audio signal coming out of the MOD1 pin (J14 or TP18). The level should be -8.0dBm.

Check the audio signal coming out of the MOD2 pin (J17 or TP19). The level should be -10.0dBm.

The MOD1 and MOD2 outputs should have a DC bias level of approximately 1.65 volts.

6.4.4. Generate Two External Digital Clocks

Configure the CMX7240/CMX7340 with the C-BUS register data given in Table 8.

Table 8 CMX7240/CMX7340 Register Settings – External Digital Clocks

	C-BUS Register	
Write Data	Address	Name
$0021	$C0	Powerdown Control
$1900	$AB	System Clock 1 PLL Configuration
$E0C8	$AC	System Clock 1 Reference and Source Configuration
$0E00	$AD	System Clock 2 PLL Configuration
$E6C8	$AE	System Clock 2 Reference and Source Configuration

With the default 19.2MHz clock input, a digital clock frequency of 4.096MHz should be observed at the system clock 1 output (TP4) and a frequency of 16.384MHz should be observed at the system clock 2 output (TP3).

Now write 0xC0C8 to either $AC or $AE registers, to turn off the system clock 1 or system clock 2 outputs, respectively.

6.5. Troubleshooting

After loading a Function Image™ the ES0002xx application writes the activation code that has been typed into the Activation Code edit box to the CMX7240/CMX7340 reference device. If this code is incorrect for the Function Image™ that has just been loaded, the CMX7240/CMX7340 will be locked and will not respond to further input from the ES0002xx application. It is recoverable only by closing the ES0002xx application, power cycling the PE0403 and PE0002 cards, and then restarting the application. Keep the power off for at least 10 seconds during this process.

7. Performance Specification

7.1. Electrical Performance

7.1.1. Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the evaluation kit.

	Min.	Max.	Units
Supply (+V – 0V)	-0.3	9.0	V
Supply (-V – 0V)	0.3	-9.0	V
Voltage on any connector pin to V_{SS}	-0.3	3.6	V
Current into or out of +V and V_{SS} pins	0	+0.45	A
Current into or out of any other connector pin	-20	+20	mA

7.1.2. Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (+V – 0V)		4.5	5.5	V
External Clock Frequency		3.0	24.576	MHz

7.1.3. Operating Characteristics

For the following conditions unless otherwise specified:

Evaluation Device Clock Frequency = 19.2MHz, +V = 5.0V, -V = -5V, Tamb = +25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (PE0403 - 724x)	1, 2	–	50	–	mA
- I_{DD} (PE0403 - 724x)	1, 2	–	40	–	mA
I_{DD} (PE0403 - 734x)	1, 2	–	40	–	mA
- I_{DD} (PE0403 - 734x)	1, 2	–	30	–	mA
+3V3A		3.15	3.3	3.45	V
+3V3D		3.15	3.3	3.45	V
+4V0		3.82	4.0	4.18	V
-4V0		-3.82	-4.0	-4.18	V
Analogue Parameters					
Output Impedances					
MOD1, MOD2	4	–	51	–	Ω
AUDIO	4	–	0.1	–	Ω
Input Impedances					
DISC, ALT	4	–	51	–	Ω
MIC	4	–	100	–	kΩ
External Clock Input	3				
'High' pulse width		21	–	–	ns
'Low' pulse width		21	–	–	ns
Input impedance		10	–	–	MΩ

Notes:

1. PCB current consumption, not current consumption of the CMX7240/CMX7340.
2. Not including any current drawn from pins by external circuitry.
3. CMX7240/CMX7340 parameter only, see relevant CMX724x/CMX734x datasheet.
4. Small signal impedance.

7.1.4. Operating Characteristics – Timing Diagrams

Please refer to relevant CMX724x/CMX734x datasheets for details.

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New function images may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's). *FirmASIC*® and Function Image™ are trademarks of CML Microsystems plc.

CML Microcircuits (UK) Ltd COMMUNICATION SEMICONDUCTORS	CML Microcircuits (USA) Inc. COMMUNICATION SEMICONDUCTORS	CML Microcircuits (Singapore) Pte Ltd COMMUNICATION SEMICONDUCTORS
Tel: +44 (0)1621 875500 **Fax:** +44 (0)1621 875600 **Sales:** sales@cmlmicro.com **Tech Support:** techsupport@cmlmicro.com	**Tel:** +1 336 744 5050 800 638 5577 **Fax:** +1 336 744 5054 **Sales:** us.sales@cmlmicro.com **Tech Support:** us.techsupport@cmlmicro.com	**Tel:** +65 62 888129 **Fax:** +65 62 888230 **Sales:** sg.sales@cmlmicro.com **Tech Support:** sg.techsupport@cmlmicro.com
- www.cmlmicro.com -		