

LINEAR SYSTEMS

Over Three Decades of Quality Through Innovation

SD-SST210/214

N-CHANNEL LATERAL DMOS SWITCH

PART NUMBER	$V_{(BR)DS}$ Min (V)	$V_{(GS)th}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD210DE	30	1.5	45 @ $V_{GS}=10V$	0.5	2
SD214DE	20	1.5	45 @ $V_{GS}=10V$	0.5	2
SST210	30	1.5	50 @ $V_{GS}=10V$	0.5	2
SST214	20	1.5	50 @ $V_{GS}=10V$	0.5	2

PRODUCT SUMMARY

Features

- Ultra-High Speed Switching— t_{ON} : 1ns
- Ultra-Low Reverse Capacitance: 0.2pF
- Low Guaranteed r_{DS} @5V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

Description

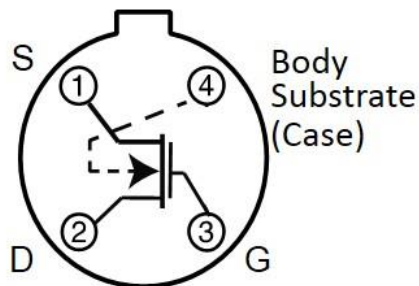
The SD210DE/214 and SST210/214 are enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video and high-frequency applications. The SD214DE and SST214 are normally used for ± 10 -V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These MOSFETs do not

have a gate protection Zener diode which results in lower gate leakage and \pm voltage capability from gate to substrate. A polysilicon gate is featured for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, Zener protected—SD211DE/SST211 Series.

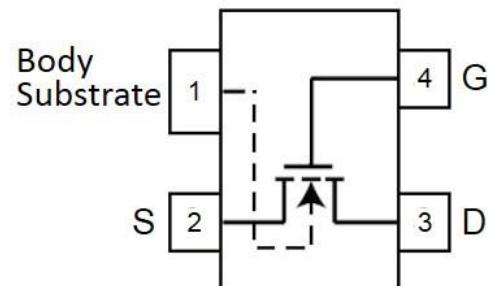
Top Views

SD210DE, SD214DE



TO-206AF
(TO-72)

SST210, SST214



TO-253
(SOT-143)

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Gate-Drain, Gate-Source Voltage ± 40V	Source-Substrate Voltage	(SD210DE/SST210) 15V
Gate-Substrate Voltage ± 30V		(SD210DE/SST210) 25V
Drain-Source Voltage	(SD210DE/SST210) 30V	Drain Current50mA
	(SD214DE/SST214) 20V	Lead Temperature (1/16" from case for 10 seconds) 300°C
Source-Drain Voltage	(SD210DE/SST210) 10V	Storage Temperature -65 to 150°C
	(SD214DE/SST214) 20V	Operating Junction Temperature -55 to 125°C
Drain-Substrate Voltage	(SD210DE/SST210) 30V	Power Dissipation*300mW
	(SD214DE/SST214) 25V		

Note:

* Derate 3mW/°C above 25°C

Specifications^a

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS				UNIT	
				210 Series		214 Series			
				Min	Max	Min	Max		
Static									
Drain - Source Breakdown Voltage	V _{(BR)DS}	V _{GS} = V _{BS} = 0V, I _D = 10 μA	35	30				V	
		V _{GS} = V _{BS} = -5V, I _D = 10 nA	30	10		20			
Source - Drain Breakdown Voltage	V _{(BR)SD}	V _{GD} = V _{BD} = -5V, I _S = 10 nA	22	10		20			
Drain - Substrate Breakdown Voltage	V _{(BR)DBO}	V _{GB} = 0V, I _D = 10 nA Source Open	35	15		25			
Source - Substrate Breakdown Voltage	V _{(BR)SBO}	V _{GB} = 0V, I _S = 10 μA Drain Open	35	15		25			
Drain - Source Leakage	I _{DS(off)}	V _{GS} = V _{BS} = -5V	V _{DS} = 10V	0.4		10		nA	
			V _{DS} = 20V	0.9			10		
Source - Drain Leakage	I _{SD(off)}	V _{GD} = V _{BD} = -5V	V _{SD} = 10V	0.5		10			
			V _{SD} = 20V				10		
Gate Leakage	I _{GBS}	V _{DB} = V _{SB} = 0V, V _{GB} = ±40V	±0.001		±100		±100	pA	
Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 μA, V _{SB} = 0V	0.8	0.5	1.5	0.1	1.5	V	
Drain - Source On-Resistance	r _{DS(on)}	V _{SB} = 0V I _D = 1mA	V _{GS} = 5V (SD Series)	58		70		70	Ω
			V _{GS} = 5V (SST Series)	60		75		75	
			V _{GS} = 10V (SD Series)	38		45		45	
			V _{GS} = 10V (SST Series)	40		50		50	
			V _{GS} = 15V	30					
			V _{GS} = 20V	26					
			V _{GS} = 25V	24					

Specifications^a

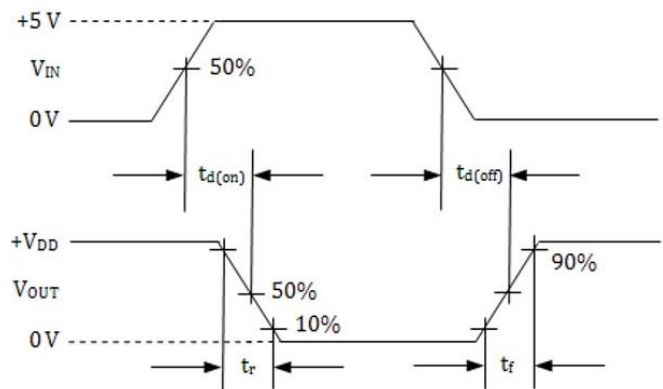
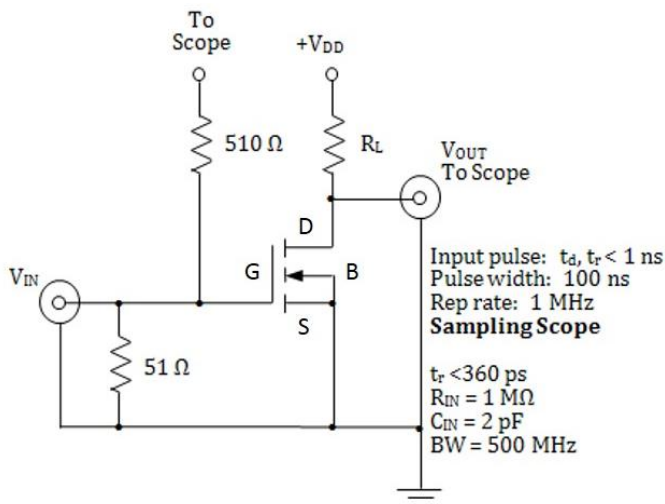
PARAMETER	SYMBOL ^b	TEST CONDITIONS ^b	TYP ^c	LIMITS				UNIT	
				210 Series		214 Series			
				Min	Max	Min	Max		
Dynamic									
Forward Transconductance	g_{fs}	$V_{DS} = 10V, V_{SB} = 0V, I_D = 20mA, f = 1kHz$	SD Series	11	10		10		mS
			SST Series	10.5	9		9		
			All	0.9					
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10V, f = 1MHz, V_{GS} = V_{BS} = -15V$	SD Series	2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}		SST Series	4.2					
			SD Series	0.2		0.5		0.5	
Switching									
Turn-On Time	$t_{D(on)}$	SD Series Only $V_{SB} = 0V, V_{IN} 0 \text{ to } 5V, R_G = 25\Omega, V_{DD} = 5V, R_L = 680\Omega$	0.5		1		1	ns	
	t_r		0.6		1		1		
Turn-Off Time	$t_{D(off)}$		2						
	t_f		6						

NOTES:

- $T_A = 25^\circ C$ unless otherwise notes.
- B is the body (substrate) and $V_{(BR)}$ is breakdown voltage.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

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Switching Time Test Circuit



Linear Integrated Systems (LIS), established in 1987, is third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company Founder John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.