190426529 Si5395/94/92 Data Sheet Rev 1.0

PCN Issue Date: 4/26/2019 **Effective Date:** 8/1/2019

PCN Type: Datasheet

Description of Change

Silicon Labs is pleased to announce the release of the Si5395/94/92 Data Sheet from document revision 0.96 to document revision 1.0.

A detailed description of the changes to the data sheet are summarized in the change impact section of this document.

Customers are encouraged to download the most recent version of CBPro, 2.32 or later, to take advantage of the latest software features and algorithms. A detailed description of changes for each CBPro release is available at https://www.silabs.com/documents/public/release-notes/ClockBuilder-Pro-README.pdf.

Reason for Change

The data sheet was updated to reflect improved P-grade device performance and to add additional features like standard CMOS thresholds. The core die did not change - the device configuration options have been expanded. A list of specific changes are below.

Impact on Form, Fit, Function, Quality, Reliability

There is no impact on form, fit, quality and reliability.

Si5395/94/92 Data Sheet Revision 1.0 changes
• Updated Figure 4.3. Crystal Resonator and External Reference Clock Connection Options
• Updated section 4.9.2 Grade P section to support up to 3 time domains for Si5395, 2 domains for Si5394 and 1 domain for Si5392 (previous version only specified 2 domains for Si5395)
• Updated Table 5.2 DC Characteristics
- Core supply current IDD/IDDA limits clarified for each device
- Output Buffer supply conditions clarified
- Total power dissipation numbers updated
- Updated test configuration diagrams
• Updated Table 5.3 Input clock specifications
- Update Input voltage section of "LVCMOS / Pulsed CMOS DC-Coupled Input Buffer" to include standard CMOS
• Table 5.5 Differential Clock Output Specifications
- Clarified duty cycle specs for when MultiSynth is used/not used
- Increased max Rise and Fall times from 150ps to 200ps based on final characterization
• Table 5.6. LVCMOS Clock Output Specifications
- Updated Min and Max limits for duty cycle
- Updated test configuration diagrams
• Table 5.8. Performance Characteristics
- Updated Initial startup time for P-grade devices
- Updated P-grade jitter numbers to include more domains and finalize test conditions
• Updated Table 5.10. SPI Timing Specifications (4-Wire) table and timing diagram
• Updated Table 5.11. SPI Timing Specifications (3-Wire)
• Changed NC/XA, NC/XB, NC/X1, NC/X2 to XA, XB, X1, X2 respectively since integrated crystal devices are getting their own datasheet.

Product Identification

```
Existing Part #
SI5392A-A#####-GM
SI5392A-A#####-GMR
SI5392A-A-GM
SI5392A-A-GMR
```

```
SI5392B-A#####-GM
SI5392B-A#####-GMR
SI5392B-A-GM
SI5392B-A-GMR
SI5392C-A#####-GM
SI5392C-A#####-GMR
SI5392C-A-GM
SI5392C-A-GMR
SI5392D-A#####-GM
SI5392D-A#####-GMR
SI5392D-A-GM
SI5392D-A-GMR
SI5392P-A#####-GM
SI5392P-A#####-GMR
SI5392P-A-GM
SI5392P-A-GMR
SI5394A-A#####-GM
SI5394A-A#####-GMR
SI5394A-A-GM
SI5394A-A-GMR
SI5394B-A#####-GM
SI5394B-A#####-GMR
SI5394B-A-GM
SI5394B-A-GMR
SI5394C-A#####-GM
SI5394C-A#####-GMR
SI5394C-A-GM
SI5394C-A-GMR
SI5394D-A#####-GM
SI5394D-A#####-GMR
SI5394D-A-GM
SI5394D-A-GMR
SI5394P-A#####-GM
SI5394P-A#####-GMR
SI5394P-A-GM
SI5394P-A-GMR
SI5395A-A#####-GM
SI5395A-A#####-GMR
SI5395A-A-GM
SI5395A-A-GMR
SI5395B-A#####-GM
SI5395B-A#####-GMR
SI5395B-A-GM
SI5395B-A-GMR
SI5395C-A#####-GM
SI5395C-A#####-GMR
SI5395C-A-GM
SI5395C-A-GMR
SI5395D-A#####-GM
SI5395D-A#####-GMR
SI5395D-A-GM
SI5395D-A-GMR
SI5395P-A#####-GM
SI5395P-A#####-GMR
SI5395P-A-GM
SI5395P-A-GMR

Where '#' represents the custom part number.
```

Last Date of Unchanged Product: 8/1/2019

Qualification Samples

N/A

Customer Response

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change, Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.

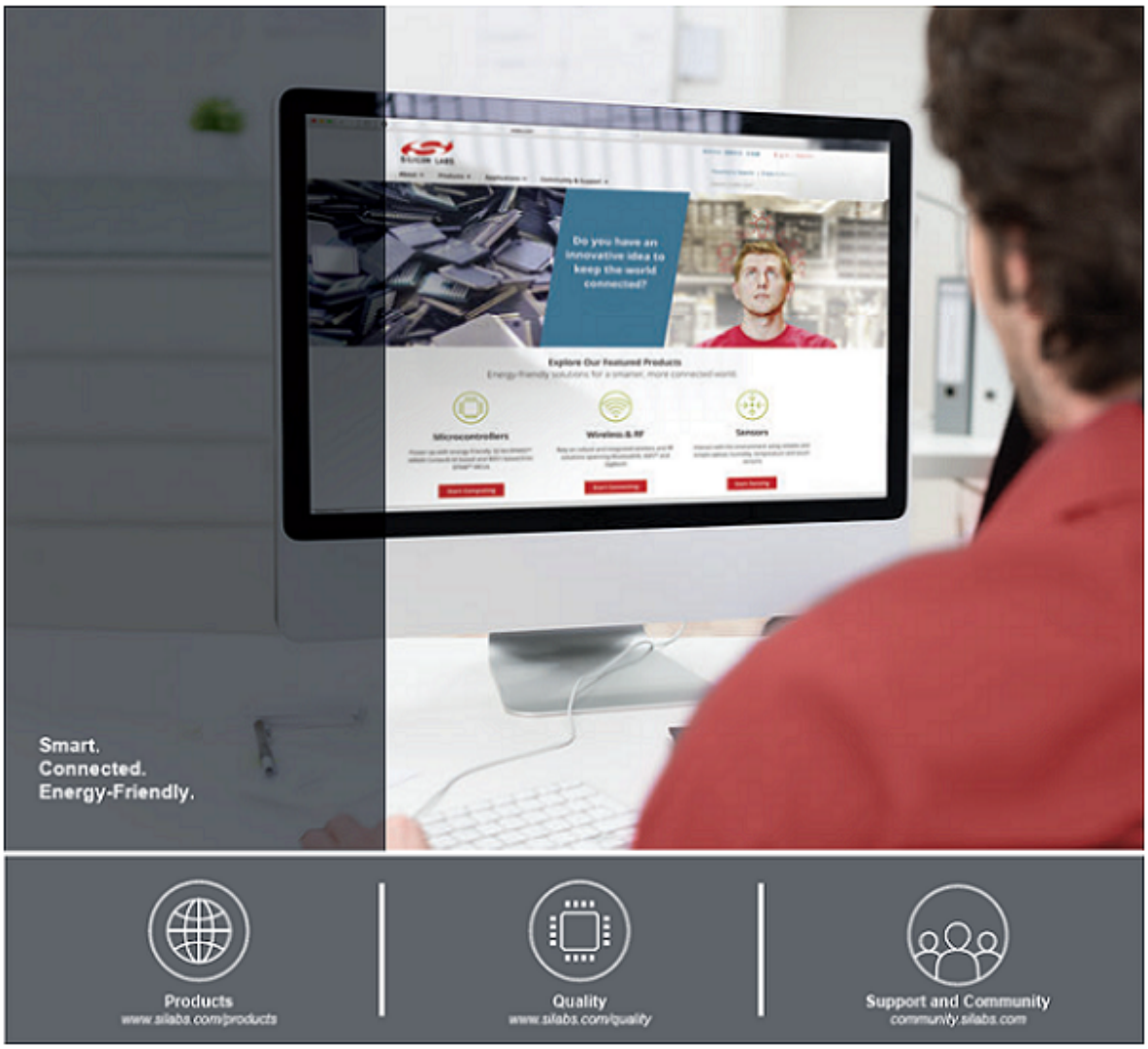
Customers may approve early PCN acceptance by emailing approval, along with PCN # to PCNEarlyAcceptance@silabs.com

User Registration

Register today to create your account on Silabs.com. Your personalized profile allows you to receive technical document updates, new product announcements, “how-to” and design documents, product change notices (PCN) and other valuable content available only to registered users. **http://www.silabs.com/profile**

Qualification Data

N/A



Disclaimer
Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Labs shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any Life Support System without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information
Silicon Laboratories Inc.® , Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, Clockbuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, ISOmodem®, Micrium, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701

http://www.silabs.com