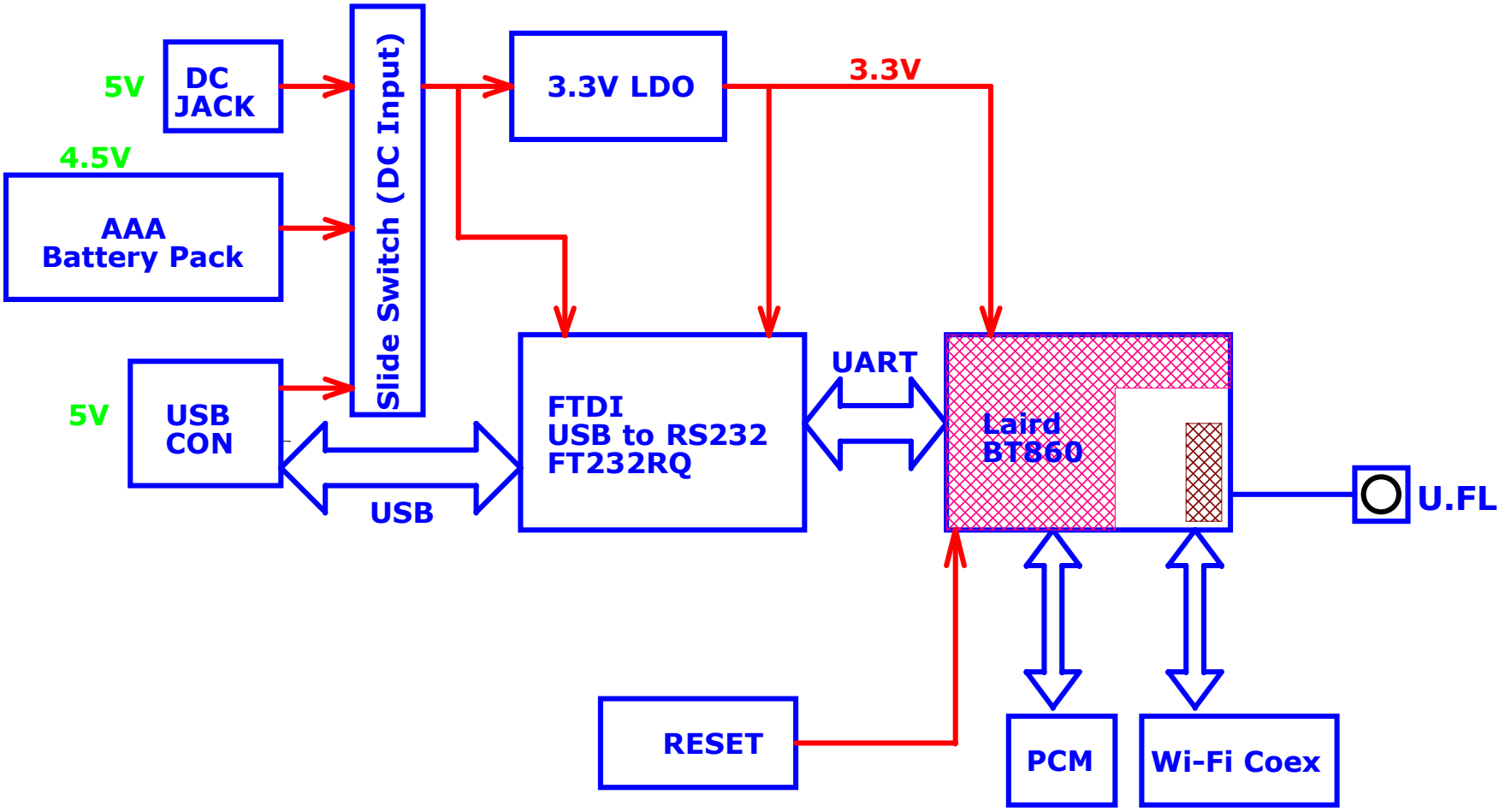
DVK-BT860 BLOCK DIAGRAM



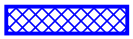
Laird Technologies CS		
Project Name : DVK-BT860	Schematic Name : Block Diagram	Drawing By : Jacky Kuo
Date : Wednesday, August 23, 2017	Sheet : 1 of 4	Revision : 1.0

DATE	REVISION NUMBER	INITIALS	Initial Release
2017/05/18	A0	Jacky Kuo	Initial draft
2017/08/02	B0	Jacky Kuo	1. Change C31 to 1.2nH 2. Added GPIO_5 signal 3. Added R67 & LED4 for GPIO_5
2017/08/23	1.0	Jacky Kuo	MP release

PCB design specification

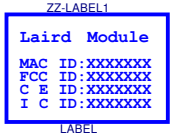
1. Substrate: FR4 ROHS compliant, High TG 140 degree.
2. Solder mask, color=BLUE, Silkscreen color=WHITE
3. Surface finish to be Immersion Nickel/Gold (ENIG) with 1-2 u"
4. Start with 1/2 oz. copper on all layers.

ZZ-PCB1



PCB

ZZ-LABEL1



LABEL

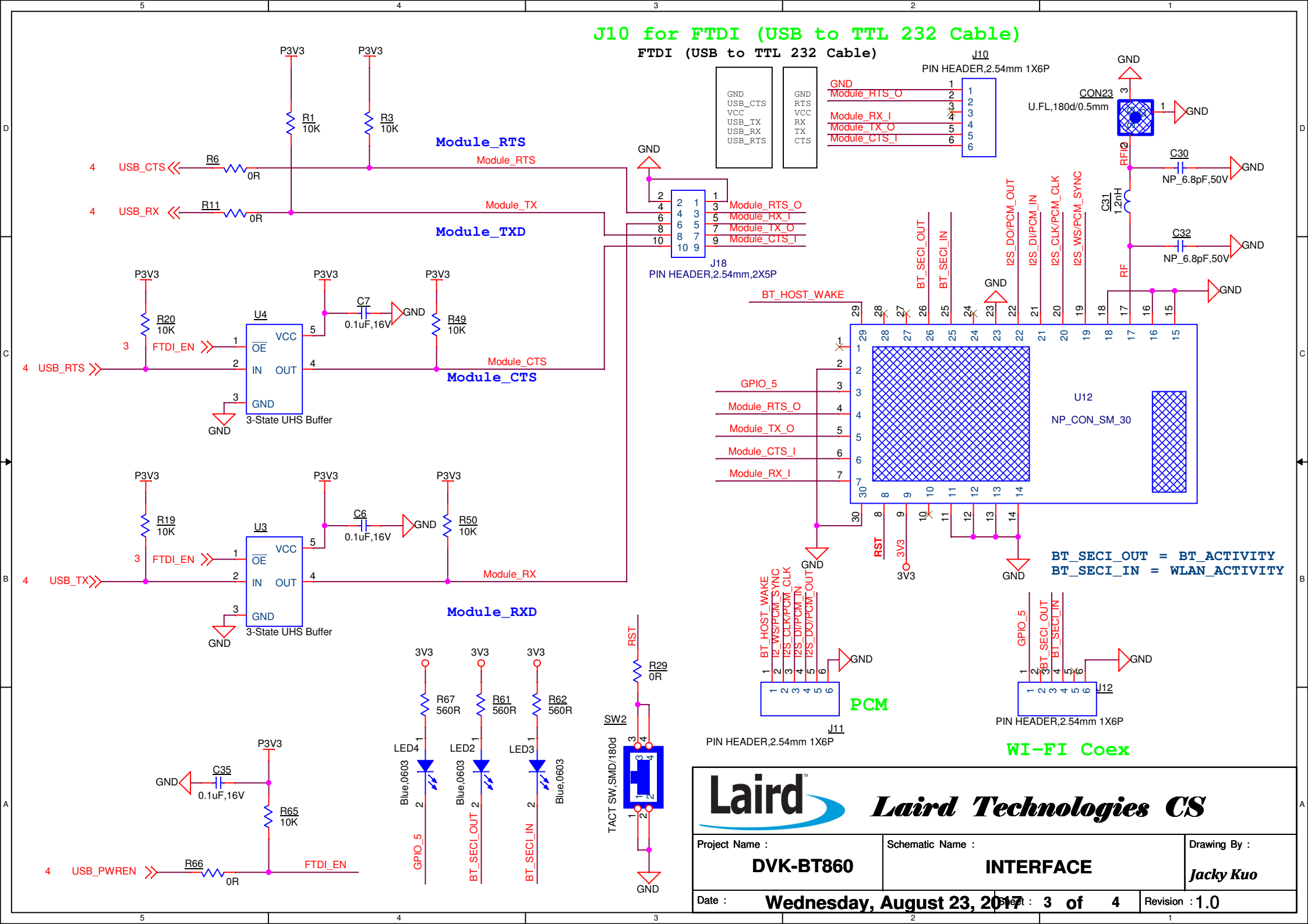
Laird Technologies CS

Project Name :	Schematic Name :	Drawing By :
DVK-BT860	HISTORY	Jacky Kuo

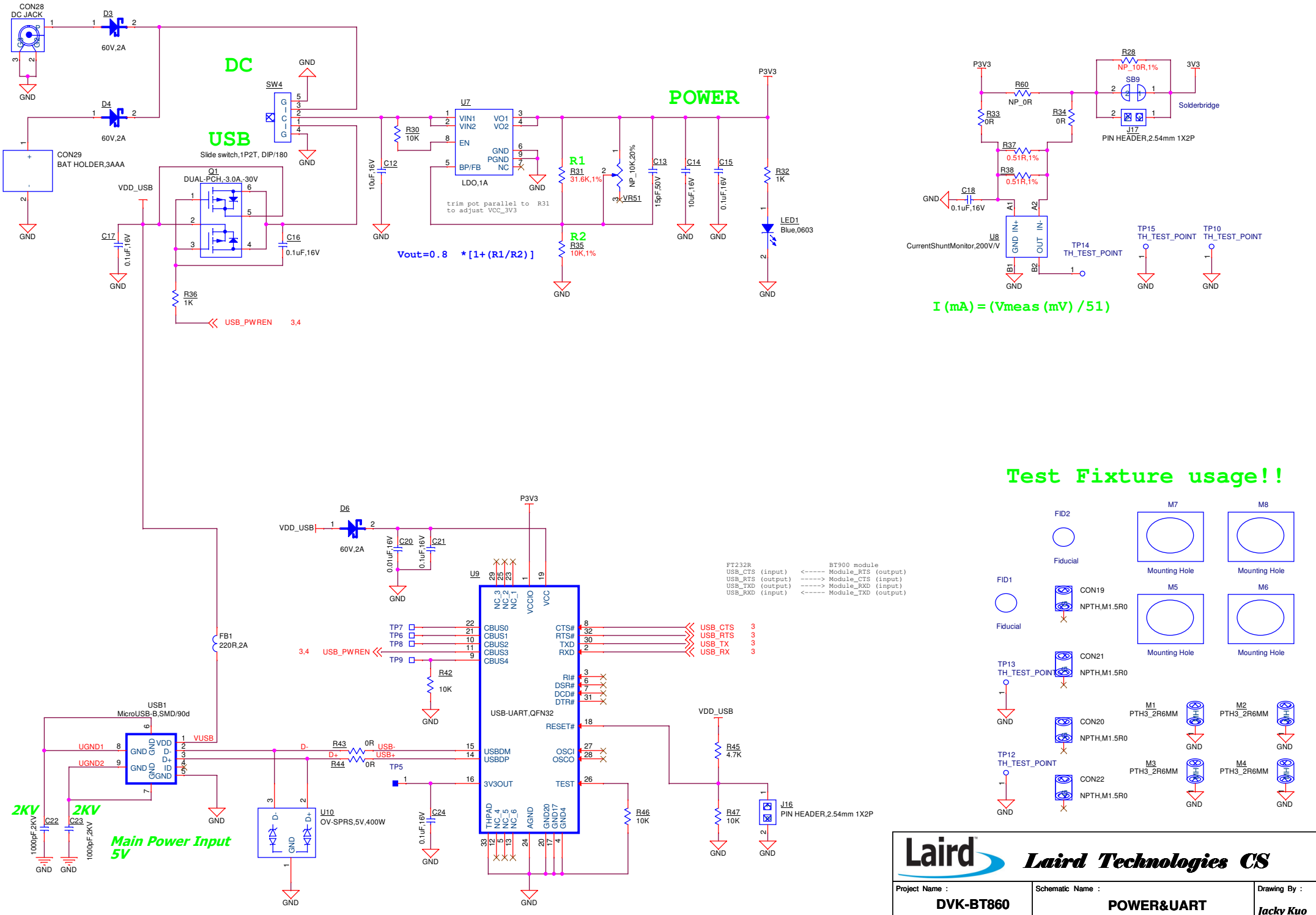
Date : Wednesday, August 23, 2017 | Sheet : 2 of 4 | Revision : 1.0

J10 for FTDI (USB to TTL 232 Cable)

FTDI (USB to TTL 232 Cable)



Laird Technologies CS		
Project Name : DVK-BT860	Schematic Name : INTERFACE	Drawing By : Jacky Kuo
Date : Wednesday, August 23, 2017	Sheet : 3 of 4	Revision : 1.0



Laird Technologies CS			
Project Name : DVK-BT860	Schematic Name : POWER&UART	Drawing By : Jacky Kuo	
Date : Wednesday, August 23, 2017	Sheet : 4 of 4	Revision : 1.0	