AN_8430_002

April 2011

78Q8430 Layout Guidelines

Introduction

The TSC 78Q8430 is a single chip 10Base-T/100Base-TX capable Fast Ethernet Media Access Controller (MAC) and Physical Layer (PHY) transceiver. The PHY includes an analog front end which requires special considerations for PCB layout.

This document provides the PCB layout recommendations that must be followed to enhance the PHY performance while minimizing EMC emissions. In general, circuit performance can be attributed to careful consideration of analog signal routing and the placement of components.

This document includes layout recommendations related to the following areas:

- Plane Architecture Recommendations – PCB architecture and materials specification.
- Power/Ground and Analog/Digital Plane Recommendations – power and ground plane layout, analog and digital power plane separation.
- Analog Trace and Termination Recommendations.
- Digital Trace and Termination Recommendations.
- Analog and Digital Circuit Isolation Recommendations.
- Power Supply Decoupling Recommendations.
- Miscellaneous Recommendations, including RJ-45 connector and crystal compensation capacitors.

The following figures and tables are included in the document:

Plane Architecture Recommendations

Figure 1 illustrates the recommended overall PCB architecture as well as the material specifications for each layer.

- Use a multi-layer PCB with the inner layers dedicated to ground (GND) and power (VCC).
- The top layer has the major components and signal routes.
- The bottom layer has bypass capacitors and miscellaneous discrete components, as well as additional signal routes.
- The internal two layers have ground and power supply planes only.
- The ground layer is directly under the component side of the board, followed by the power plane layer, then the bottom layer.
- FR-4 material is recommended for this design.

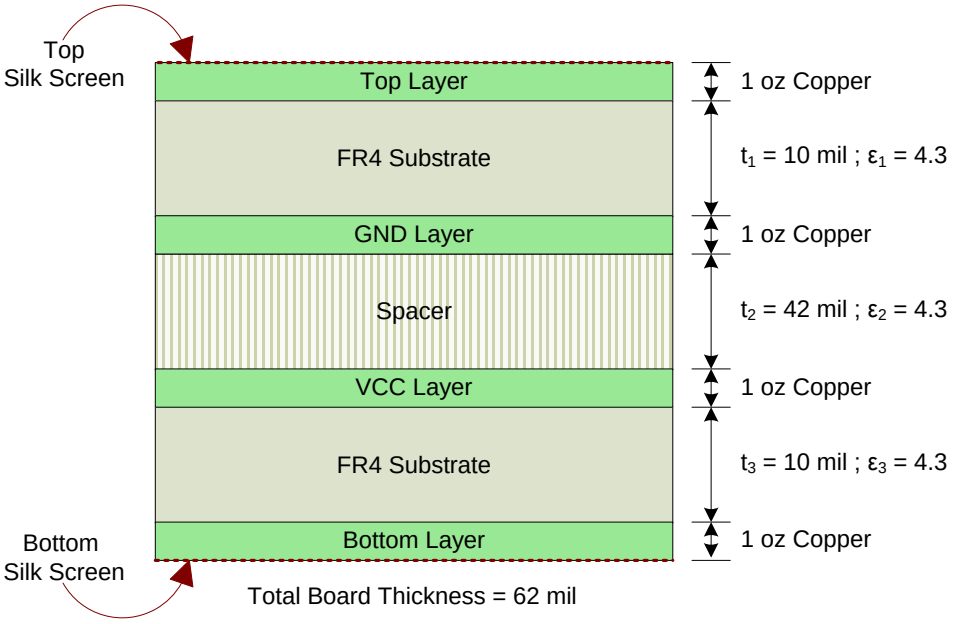

Figure 1: PCB Stack-up Diagram

Power/Ground and Analog/Digital Plane Recommendations

Internally, the device has a separate digital power plane and analog power plane to ensure the transmit signal integrity for its PHY analog front-end. It is important to maintain the analog and digital isolation on the PCB. The following recommendations apply to the power and ground plane architecture as well as the digital and analog isolation:

- If a transformer is used in the design, extend the GND plane out to the PHY side of transformer. Remove the VCC and GND planes from the line side of the transformer to the RJ-45 connector.
- If an integrated RJ-45 is used in the design, extend the VCC and GND planes out to the RJ-45 pins. Please refer to Figure 2 for details.
- The chassis GND plane extends from the backplate and RJ-45 to the line side termination components only. Do not allow the chassis GND plane to cross over the PHY GND plane. The minimum separation of these planes must accommodate over 1.5 kV. A 75 mil separation is recommended.
- A dedicated analog power (VCCA) plane is employed for the PHY transmit section. Isolate the PHY VCCA power plane from the digital VCC power plane. The PHY VCCA power connections must have the lowest possible series impedance.
- Pouring copper to the solder side achieves better EMC performance.

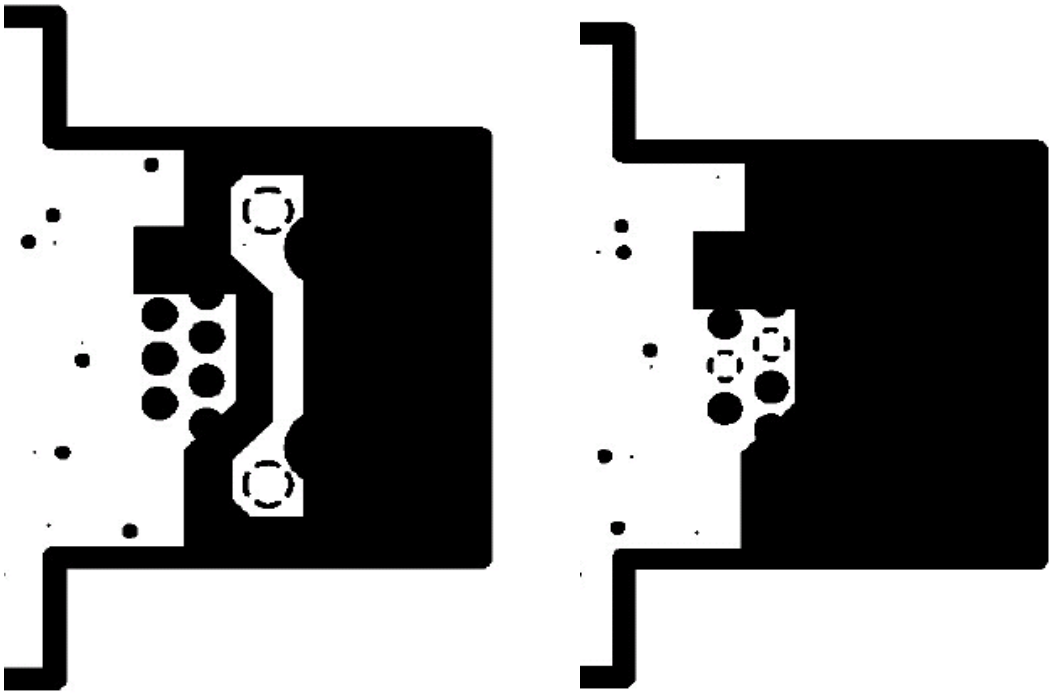

Figure 2: GND and VCC Plane Arrangement for Integrated RJ-45

Analog Trace and Termination Recommendations

The following recommendations apply to the analog traces:

- The traces from the PHY to the transformer (or integrated RJ-45) must be 100 Ω differential transmission lines. This design can be achieved using PCB trace impedance simulation tools, such as a CITS25 Differential Controlled Impedance Calculator. Figure 3 illustrates a simulation example for a coated micro-strip line.

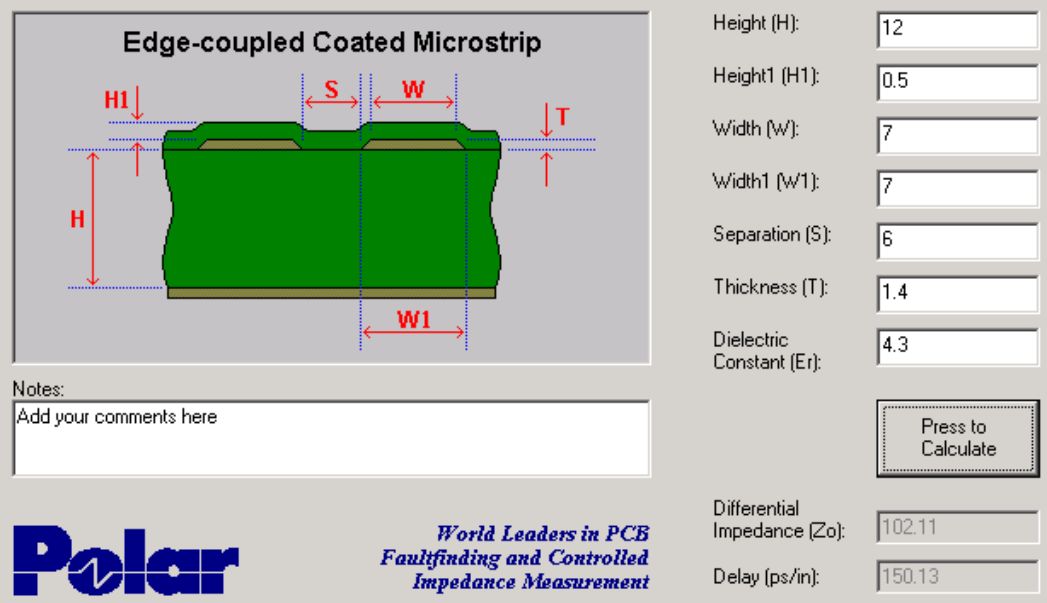

Figure 3: CITS25 Simulation Example

- Always make all differential signal pairs short and have the same length.
- Place the highest speed signals on the layer adjacent to the GND layer.
- Keep clock routes away from the analog side of the device as well as its associated analog signal routes.
- Minimize the use of vias when routing the analog signal traces.

The following recommendations apply to the analog terminations:

- Place the termination network components near the input data pins of the PHY (RXP/RXN) or transformer (TXP/TXN).
- If a transformer is used, locate the transformer adjacent to the RJ-45 to minimize the shunt capacitance to the line.
- Place two 0.1 µF capacitors right next to the transformer / integrated RJ-45 center tap pins.
- Additional components may be added for maximum EMC containment. Please refer to document AN-2123-002-v2.0 for additional recommendations on EMC.

Digital Trace and Termination Recommendations

- Pay special attention to the routing of high-speed clock traces. Preferably, these signals should be on the top layer and as short as possible.
- Keep clock routes away from the analog side of the device as well as its associated analog signal routes.
- Series digital signal termination schemes can be used to terminate the data/clock interface between the 78Q8430 and the host. This can reduce excessive EMI noise coupling due to over and under-shoot ringing at signal edges.
- Series source termination is most commonly used as a series digital signal termination scheme. The impedance of the termination resistors can be varied, depending on the system layout condition.

Analog and Digital Circuit Isolation Recommendations

- Physically separate the analog-front-end section from the digital section. Refer to the Power/Ground and Analog/Digital Plane Recommendations section for more details.
- Physically separate the analog signals from the digital signals by placing them on opposite layers or routing them away from each other.
- Keep clock routes away from the analog side of the device as well as its associated analog signal routes.

Power Supply Decoupling Recommendations

Decoupling (bypass) capacitors squelch high frequency noise and switching transients from the supply to the ground plane. Use the following recommendations for power supply decoupling:

- Two decades of capacitors are recommended, e.g. a mix of 0.1 µF and 0.001 µF. This provides a much broader bypass bandwidth than a single value bypass scheme.
- Use low inductance (ESR), ceramic, surface mount decoupling capacitors. Generally, X7R dielectric capacitors provide the best price/performance trade-off. Ceramic, low ESR caps are recommended for best frequency response.
- A 0603 size bypass capacitor with the via as close as possible to the device pads provides a minimal lead inductance, further enhancing the effectiveness of the bypass.
- Locate the decoupling capacitors as close as possible to the respective VCC and GND pins.
- All decoupling capacitors and PHY VCC and GND connections must tie immediately to a VCC or GND plane via with minimum trace inductance. Please see the example in Figure 4.

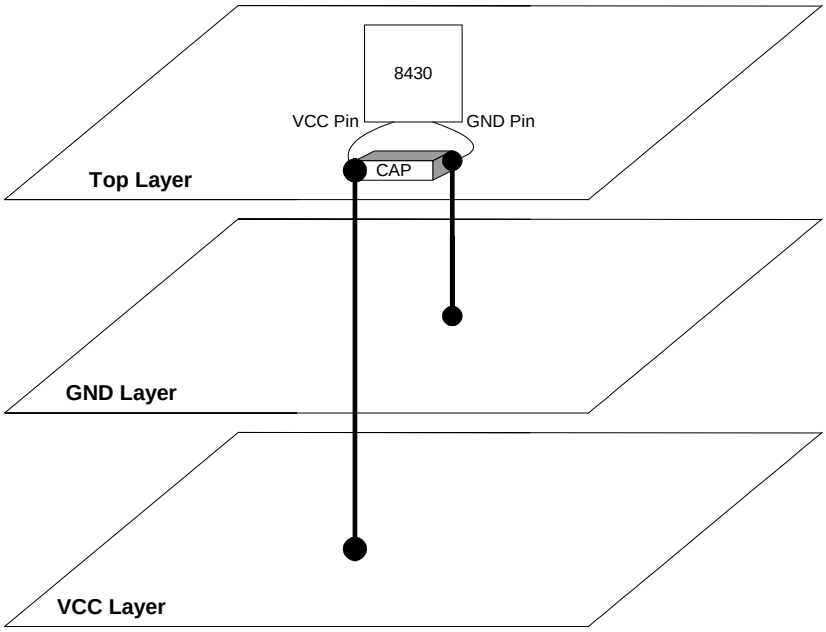

Figure 4: Decoupling Capacitor Connections

Miscellaneous Recommendations

- **RJ-45 connector**: Use a shielded RJ-45 connector with its case stakes soldered to the chassis ground. Isolate the crystal and its capacitors from the analog signals with a GND guard ring. Refer to Table 1 and Table 2 for a list of recommended devices that integrate the transformers, RJ45 connector, LEDs, and termination resistors.
- **Crystal compensation capacitors:** The C2 and C3 compensation capacitor values must be selected to trim the oscillator's frequency to 25.0000 MHz ± 50 ppm. The optimum capacitor value is layout dependent. A mere ± 4 pF can shift the 25 MHz by ± 100 Hz. The IEEE specifies the 25.0000 MHz ± 50 ppm value. System vendors must select the proper crystal according to their applications, such as operating environment, product lifetime, etc. since crystal aging, operating temperature, and other factors can affect the crystal frequency tolerance.

Table 1: Commercial Temperature Integrated Connectors

Vendor	Part number	Tab up /down	LED	LED color (L/R)	Shielding	Lead-free	Compatible Footprints [1]
Pulse	J0011D21	Down	No	N/A	Yes	No	a
	J0011D21NL	Down	No	N/A	Yes	Yes	a
	J0011D21B	Down	Yes	G/Y	Yes	No	b
	J0011D21BNL	Down	Yes	G/Y	Yes	Yes	b
	J0011D21E	Down	Yes	G/G	Yes	No	b
	J0011D21ENL	Down	Yes	G/G	Yes	Yes	b
	J0011D01	Down	No	N/A	Yes	No	a
	J0011D01NL	Down	No	N/A	Yes	Yes	a
	J0011D01B	Down	Yes	G/Y	Yes	No	b
	J0011D01BNL	Down	Yes	G/Y	Yes	Yes	b
	J0012D21	Down	No	N/A	Yes	No	a
	J0012D21NL	Down	No	N/A	Yes	Yes	a
	J1011F01P	Up	Yes	G/Y	Yes	No	A
	J1011F01PNL	Up	Yes	G/Y	Yes	Yes	A
	J1011F21P	Up	Yes	G/Y	Yes	No	A
	J1011F21PNL	Up	Yes	G/Y	Yes	Yes	A
Halo	HFJ11-2450EURL	Down	No	N/A	No	Yes	e
	HFJ11-2450EU-L11RL	Down	Yes	G/G	No	Yes	f
	HFJ11-2450ERL	Down	No	N/A	Yes	Yes	c
	HFJ11-2450E-L11RL	Down	Yes	G/G	Yes	Yes	d
	HFJT1-S003-L11RL	Up	Yes	G/G	Yes	Yes	C
	HFJT1-S003	Up	No	N/A	Yes	Yes	D
Wurth/Midcom	MIC24010-5101T-LF3	Down	No	N/A	Yes	Yes	b
	MIC24010-5104T-LF3	Down	No	N/A	Yes	Yes	b
	MIC24011-0101T	Down	Yes	Y/G	Yes	No	b
	MIC24011-0101T-LF3	Down	Yes	Y/G	Yes	Yes	b
	MIC24011-0101W-LF3	Down	Yes	Y/G	Yes	Yes	b
	MIC24011-0104T	Down	Yes	Y/G	Yes	No	b
	MIC24012-5101T-LF3	Down	Yes	G/G	Yes	Yes	b

	MIC24012-5204T-LF3	Down	Yes	G/G	Yes	Yes	b
	MIC24013-5104T	Down	Yes	G/Y	Yes	No	b
	MIC24018-5101T-LF3	Down	Yes	R/G	Yes	Yes	b
	MIC24019-0101T	Down	Yes	G/R	Yes	No	b
	MIC24111-0101T	Up	Yes	Y/G	Yes	No	A
	MIC24111-0101T-LF3	Up	Yes	Y/G	Yes	Yes	A
	MIC24412-0128T-LF3	Up	Yes	G/G	No	Yes	E
	MIC24F11-0101T-LF3	Up	Yes	Y/G	No	Yes	F
Falco	LJ0004	Down	No	N/A	Yes	Yes	a
	LJ0012	Down	No	N/A	Yes	No	a
	LJ1011	Down	Yes	G/Y	Yes	No	d
BelFuse	SI-10021	Down	No	N/A	Yes	No	a
	SI-60002-F	Down	No	N/A	Yes	Yes	a
	SI-40139	Down	Yes	G/G	Yes	No	d
	SI-60001-F	Down	Yes	G/G	Yes	Yes	d
	SI-50170	Up	Yes	G/G	Yes	No	A
	SI-50170-F	Up	Yes	G/G	Yes	Yes	A
	SI-50177	Up	No	N/A	Yes	No	D
	SI-50177-F	Up	No	N/A	Yes	Yes	D
	SI-50193	Up	No	N/A	No	No	G
	SI-50193-F	Up	No	N/A	No	Yes	G
	SI-50196	Up	Yes	G/G	No	No	F
	SI-50196-F	Up	Yes	G/G	No	Yes	F
TDK	TLA-6T704	Down	No	N/A	Yes	Yes	a
	TLA-6T707	Down	No	N/A	Yes	Yes	a

Table 2: Industrial Temperature Integrated Connectors

Vendor	Part number	Tab up /down	LED	LED color (L/R)	Shielding	Lead-free	Compatible Footprints [1]
Wurth/Midcom	MIC24011-5108T-LF3	Down	Yes	Y/G	Yes	Yes	b
	MIC24012-5117T-LF3	Down	Yes	G/G	Yes	Yes	b
	MIC2401D-5217T-LF3	Down	Yes	GY/GY	Yes	Yes	b
	MIC24111-0108T	Up	Yes	Y/G	Yes	No	A
	MIC2411D-0117T-LF3	Up	Yes	GY/GY	Yes	Yes	A
BelFuse	SI-10128	Down	No	N/A	Yes	No	a
	SI-60136-F	Down	No	N/A	Yes	Yes	a
	SI-40091	Down	Yes	G/G	Yes	No	d
	SI-60118-F	Down	Yes	G/G	Yes	Yes	d

[1] The letters indicate different footprint drawings. Lower case indicates the tab-down version; upper case the tab-up version. Compatible connectors are labeled with the same letter.

Revision History

Revision	Date	Description
1.0	2/8/2008	First publication.
1.1	4/8/2011	Removed the Appendix. The information previously contained in the Appendix is published in the *78Q8430 ARM9(920T) Embest Evaluation Board User Manual*.

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