CHANGE NOTIFICATION

Analog Devices, Inc.
1630 McCarthy Blvd., Milpitas CA
(408) 432-1900

November 08, 2017 PCN_110817

Dear Sir/Madam:

Subject: Notification of Change to LTC1867, LTC1867L Die and Datasheet

Please be advised that Analog Devices, Inc. Milpitas, California has made a change to the LTC1867 family of parts to improve device operation in a specific application corner case. The change provides robustness to power cycling scenarios where there is an incomplete power down, resulting in the Power On Reset (POR) circuit not providing a reset signal for proper initialization. This application specific behavior can cause the SDO pin to become unresponsive.

In addition, the following note was added to the datasheet:

"When powering up the LTC1867/LTC1867L, or any time VDD falls below the minimum specified operating voltage, one dummy conversion must be initiated by providing a rising edge on the $\overline{CS}$/CONV pin. The first conversion result may be invalid and should be ignored. Once the $\overline{CS}$/CONV pin is returned low, a DIN word can be shifted into SDI to program the configuration for the next conversion. Wait at least t7, the SLEEP Mode Wake-Up Time of 80ms, before initiating the second conversion to obtain a valid conversion result."

No other functional or parametric specifications are affected and remain unchanged. The die change was qualified by performing characterization over the full operating junction temperature range and through rigorous engineering evaluation across a broad range of application conditions. In addition, the product successfully completed 1,000 hours of High Temperature Operating Life (HTOL) stress testing. Revised silicon samples are now available. Product built using the new die will be shipped with a datecode of approximately 1810.

Should you have any questions or concerns please contact your local Analog Devices sales representatives or you may contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@ANALOG.COM. If I do not hear from you by January 08, 2018, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

For questions on this PCN, please contact Jason Hu or you may send an email to your regional contacts below or contact your local ADI sales representatives.			
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		Rest of Asia:	PCN_ROA@analog.com

PIN FUNCTIONS

CH0-CH7/COM (Pins 1-8): Analog Input Pins. Analog inputs must be free of noise with respect to GND. CH7/COM can be either a separate channel or the common minus input for the other channels.

REFCOMP (Pin 9): Reference Buffer Output Pin. Bypass to GND with 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor (4.096V Nominal). To overdrive REFCOMP, tie V_{REF} to GND.

V_{REF} (Pin 10): 2.5V Reference Output. This pin can also be used as an external reference buffer input for improved accuracy and drift. Bypass to GND with 2.2µF tantalum capacitor in parallel with 0.1µF ceramic capacitor.

$\overline{CS}$/CONV (Pin 11): This input provides the dual function of initiating conversions on the ADC and also frames the serial data transfer.

SCK (Pin 12): Shift Clock. This clock synchronizes the serial data transfer.

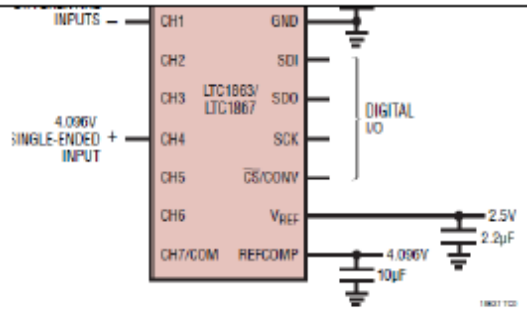
SDO (Pin 13): Digital Data Output. The A/D conversion result is shifted out of this output. Straight binary format for unipolar mode and two's complement format for bipolar mode.

SDI (Pin 14): Digital Data Input Pin. The A/D configuration word is shifted into this input.

GND (Pin 15): Analog and Digital GND.

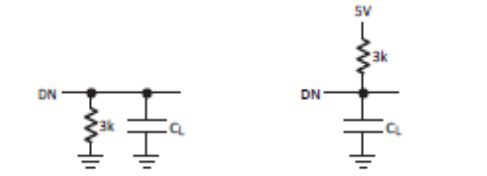
V_{DD} (Pin 16): Analog and Digital Power Supply. Bypass to GND with 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor.

When powering up the LTC1863/LTC1867, or any time VDD falls below the minimum specified operating voltage, one dummy conversion must be initiated by providing a rising edge on the $\overline{CS}$/CONV pin. The first conversion result may be invalid and should be ignored. Once the $\overline{CS}$/CONV pin is returned low, a DIN word can be shifted into SDI to program the configuration for the next conversion. Wait at least t7, the SLEEP Mode Wake-Up Time of 80ms, before initiating the second conversion to obtain a valid conversion result.



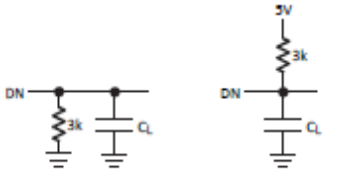
TEST CIRCUITS

Load Circuits for Access Timing



(A) Hi-Z TO V_{OH} AND V_{OL} TO V_{OH} (B) Hi-Z TO V_{OL} AND V_{OH} TO V_{OL}

Load Circuits for Output Float Delay

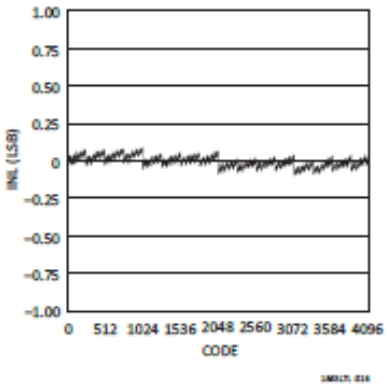


(A) V_{OH} TO Hi-Z (B) V_{OL} TO Hi-Z

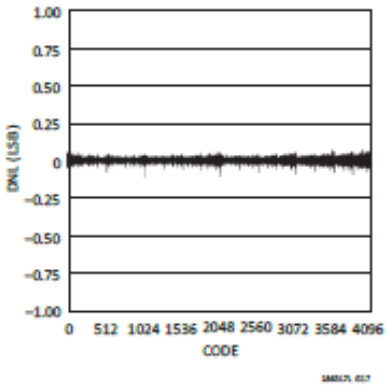
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC1863L/ LTC1867L)

Integral Nonlinearity vs Output Code (LTC1863L)



Differential Nonlinearity vs Output Code (LTC1863L)



PIN FUNCTIONS

CH0-CH7/COM (Pins 1-8): Analog Input Pins. Analog inputs must be free of noise with respect to GND. CH7/COM can be either a separate channel or the common minus input for the other channels. Unused channels should be tied to ground.

REFCOMP (Pin 9): Reference Buffer Output Pin. Bypass to GND with 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor (2.5V Nominal). To overdrive REFCOMP, tie V_{REF} to GND.

V_{REF} (Pin 10): 1.25V Reference Output. This pin can also be used as an external reference buffer input for improved accuracy and drift. Bypass to GND with 2.2µF tantalum capacitor in parallel with 0.1µF ceramic capacitor.

$\overline{CS}$/CONV (Pin 11): This input provides the dual function of initiating conversions on the ADC and also frames the serial data transfer.

SCK (Pin 12): Shift Clock. This clock synchronizes the serial data transfer.

SDO (Pin 13): Digital Data Output. The A/D conversion result is shifted out of this output. Straight binary format for unipolar mode and two's complement format for bipolar mode.

SDI (Pin 14): Digital Data Input Pin. The A/D configuration word is shifted into this input.

GND (Pin 15): Analog and Digital GND.

V_{DD} (Pin 16): Analog and Digital Power Supply. Bypass to GND with 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor.

When powering up the LTC1863L/LTC1867L, or any time VDD falls below the minimum specified operating voltage, one dummy conversion must be initiated by providing a rising edge on the $\overline{CS}$/CONV pin. The first conversion result may be invalid and should be ignored. Once the $\overline{CS}$/CONV pin is returned low, a DIN word can be shifted into SDI to program the configuration for the next conversion. Wait at least t7, the SLEEP Mode Wake-Up Time of 80ms, before initiating the second conversion to obtain a valid conversion result