Evaluating the ADMV4640 10.7 GHz to 12.7 GHz, Microwave Downconverter

FEATURES

▸ Fully featured evaluation board for the ADMV4640
▸ On-board SDP-S connector for SPI control
▸ Simplified power-up with on-board LDO regulators
▸ 5 V operation
▸ ACE software interface for SPI control

EVALUATION KIT CONTENTS

▸ EVAL-ADMV4640Z evaluation board
▸ Mini USB to USB cable
▸ SDP-S controller board

EQUIPMENT NEEDED

▸ 5 V dc power supply
▸ DC clips
▸ RF signal generator
▸ Spectrum analyzer
▸ Power supply cables, 2.92 mm coaxial cables
▸ PC for ACE software

DOCUMENTS NEEDED
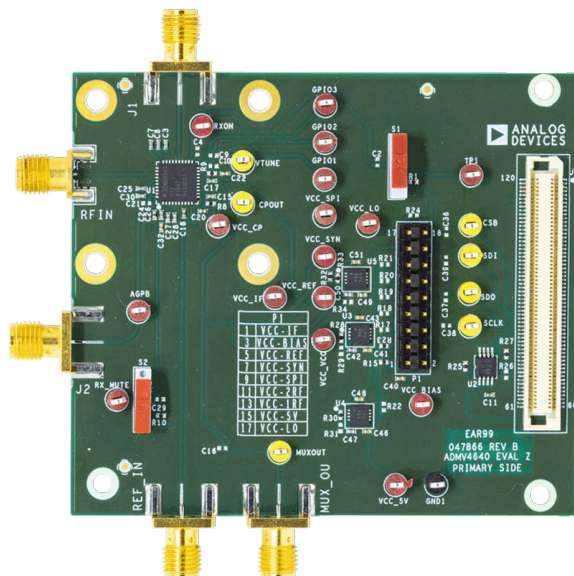
▸ ADMV4640 data sheet

EVALUATION BOARD PHOTOGRAPH

SOFTWARE NEEDED

▸ ACE software
▸ ADMV4640 plugins

GENERAL DESCRIPTION

The EVAL-ADMV4640Z evaluation board incorporates the ADMV4640, low dropout (LDO) regulators, and the EVAL-SDP-CS1Z (SDP-S) controller board to allow simplified, efficient evaluation of the ADMV4640. The SDP-S controller board allows the configuration of the ADMV4640 register map through the Analysis, Control, Evaluation (ACE) software. The LDO regulators allow the EVAL-ADMV4640Z to be powered by a 5 V single supply.

The ADMV4640 is a microwave downconverter optimized for various satellite communication (SATCOM) user terminals operating in the 10.7 GHz to 12.7 GHz frequency range.

The ADMV4640 downconverter comes in a compact, thermally enhanced, 6 mm × 6 mm, 40-lead frame chip scale package (LFCSP). The ADMV4640 operates over the −40°C to +85°C case temperature range.

For full details on the ADMV4640, see the ADMV4640 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADMV4640Z.

Figure 1.

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REVISION HISTORY

7/2022—Revision A: Initial Version

EVALUATION BOARD HARDWARE

The EVAL-ADMV4640Z comes with an on-board ADMV4640 chip. When evaluating the ADMV4640 device, connect the IF input to an RF signal generator. The EVAL-ADMV4640Z runs on a 5 V dc supply. Connect the 5 V dc supply to the VCC_5V test point, and the ground to the GND1 test point.

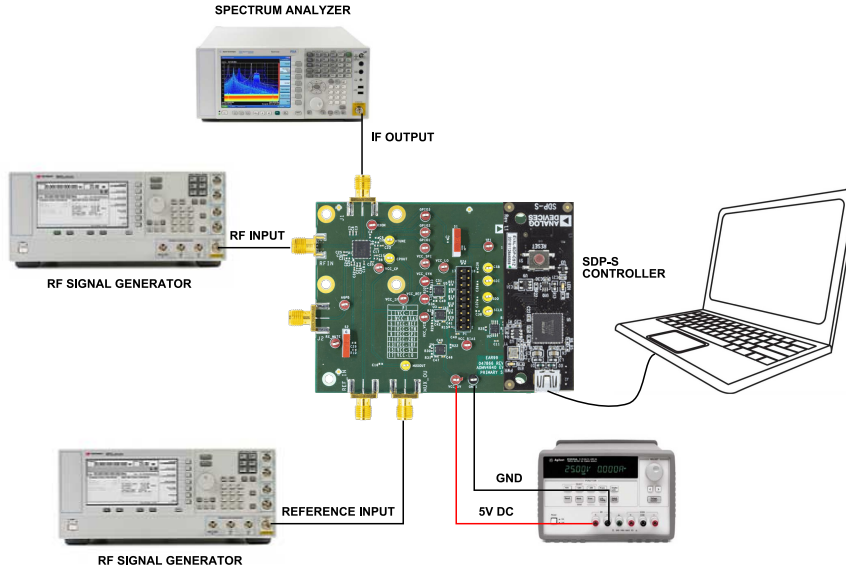Figure 2 shows the block diagram of the EVAL-ADMV4640Z lab bench setup.

Figure 2. Lab Bench Setup

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

INSTALLING THE ACE SOFTWARE AND ADMV4640 PLUGINS AND DRIVERS

The EVAL-ADMV4640Z software uses the Analog Devices, Inc., ACE software. Ensure that the ACE software is installed before setting up or using the EVAL-ADMV4640Z. For instructions on how to install and use the ACE software, go to www.analog.com/ACE.

If the ACE software has already been installed on the PC, ensure that it is the latest version that is shown on the www.analog.com/ACE page.

1. Install the latest version of ACE software. In the **ACE Setup** window, ensure that the **SDP Drivers**, **LRF Drivers**, and **NET 4.8** installations are selected (see Figure 3). Then click **Install**.
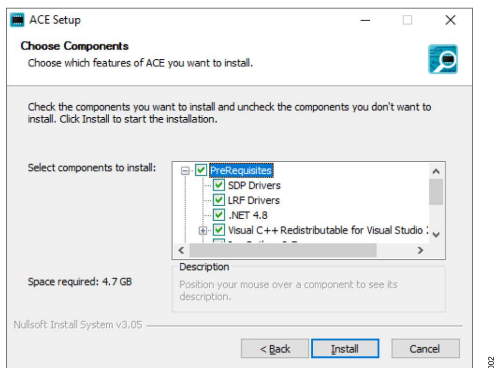

Figure 3. Drivers to Install with ACE Software

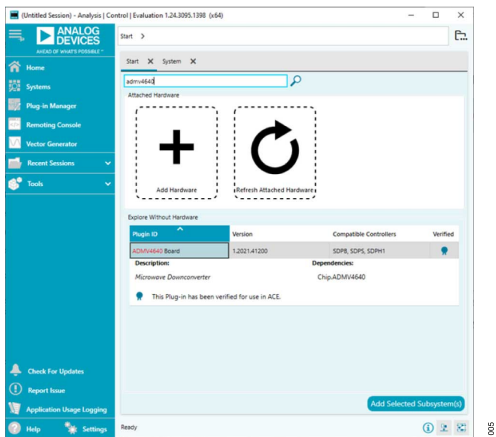2. Open the ACE software and the EVAL-ADMV4640Z plugin appears (see Figure 4).

Figure 4. EVAL-ADMV4640Z Plugin Window

CONFIGURING THE BOARD

To set up the EVAL-ADMV4640Z, take the following steps:

1. Connect the SDP-S controller board to the J3 connectors on the EVAL-ADMV4640Z.
2. Connect the USB cable to the PC and then to the SDP-S controller board.

3. Connect the 5 V clip lead on the power supply to the red VCC_5V test point on the EVAL-ADMV4640Z, and connect the GND clip lead on the power supply to the black GND1 test point. The power supply current limiting must be set to approximately 500 mA.

4. Open the ACE software. The **ADMV4640 Board** plugin appears in the **Attached Hardware** section. Double-click the EVAL-ADMV4640Z plugin. The **ADMV4640 Board** tab opens (see Figure 5).

5. Click off the **Poll Device** button and double-click the **ADMV4640** button (see Figure 5).
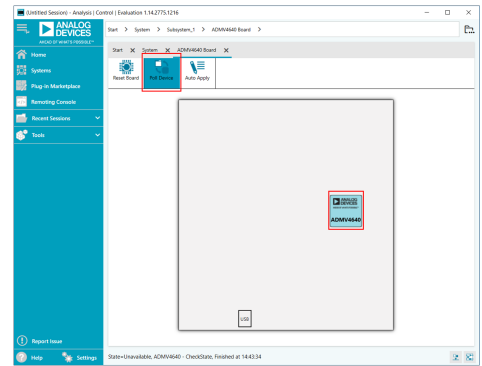

Figure 5. ADMV4640 Board Tab

6. The ADMV4640 block diagram appears (see Figure 6).
7. Click the **Initialization & Optimization** button in the ADMV4640 block diagram to initialize the device before operation.
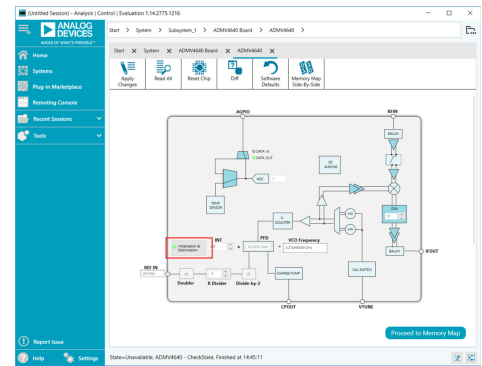
Figure 6. ADMV4640 Block Diagram in the ACE Software

8. To set up the RF, use the following settings and measure the output at the IFOUT port:
   - REF_IN port: reference frequency = 25 MHz, 3 dBm, and dc block is needed.
   - RF input: RF frequency = 12 GHz, −30 dBm.
   - The gain is at minimum attenuation. Note that the chip temperature is higher than 25°C for the reference frequency and RF frequency conditions and there is part to part variation. The gain may be lower than the typical specifications in the ADMV4640 data sheet.

ADMV4640 BLOCK DIAGRAM AND FUNCTIONS

The ADMV4640 block diagram user interface with labels is shown in Figure 7, and Table 1 describes the functionality of each block.

Figure 7. ADMV4640 Block Diagram with Labels

Table 1. ADMV4640 Block Diagram Label Functions (See Figure 7)
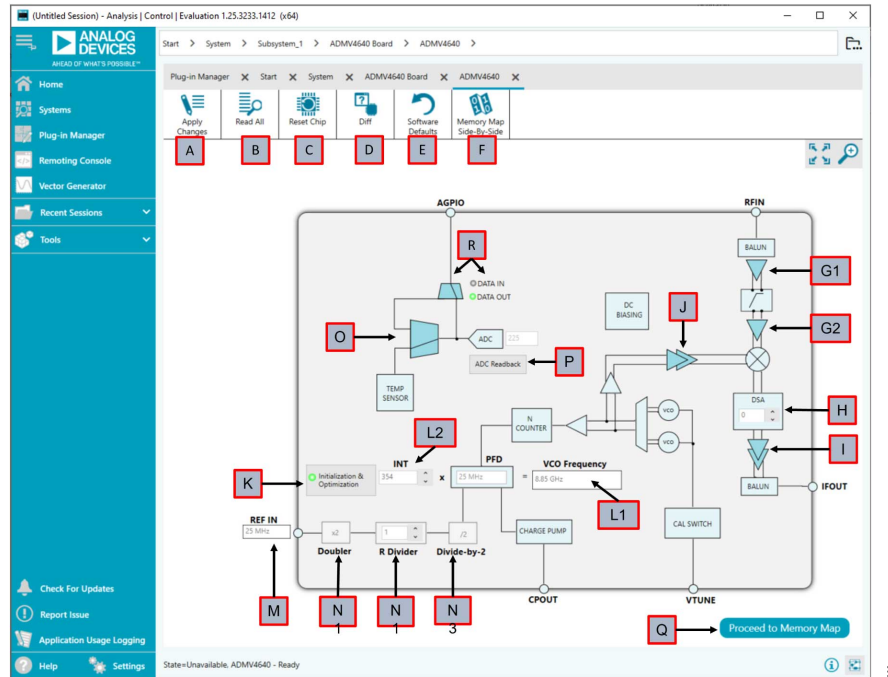
Label	Function
A	Click **Apply Changes** to apply all register values to the device. If **Auto Apply** is highlighted in the **ADMV4640 Board** tab, the **Apply Changes** feature continuously runs every few seconds, and does not need to be clicked to apply or read back the block diagram settings.
B	Click **Read All** to read back all SPI registers of the device.
C	Click **Rest Chip** to reset the ADMV4640 chip.
D	Click **Diff** to show registers that are different on the device.
E	Click **Software Defaults** to load the software defaults on to the device, and then click **Apply Changes**.
F	Click **Memory Map Side-By-Side** to open the memory map.
G1	Click the **LNA Stage 1 Enable** switch (represented by Label G1) to set the LNASTG1_BIAS_CONTROL bit (Bit 2, Register 0x100). When the **LNA Stage 1 Enable** switch is highlighted, the LNASTG1_BIAS_CONTROL bit is enabled. When the **LNA Stage 1 Enable** switch is not highlighted, the LNASTG1_BIAS_CONTROL bit is disabled.
G2	Click the **LNA Stage 2 Enable** switch (represented by Label G2) to set the LNASTG2_BIAS_CONTROL bit (Bit 3, Register 0x100). When the **LNA Stage 2 Enable** switch is highlighted, the LNASTG2_BIAS_CONTROL bit is enabled. When the **LNA Stage 2 Enable** switch is not highlighted, the LNASTG2_BIAS_CONTROL bit is disabled.
H	Use the **DSA** scroll to choose a value, or enter a value in the text box to set the SEL_DSA_ATTEN bit (Bit[4:0], Register 0x300).
I	Click the **IF Amp Enable** switch (represented by Label I) to set the AMPIF_BIAS_CONTROL bit (Bit 0, Register 0x100). When the **IF Amp Enable** switch is highlighted, the AMPIF_BIAS_CONTROL bit is enabled. When the **IF Amp Enable** switch is not highlighted, the AMPIF_BIAS_CONTROL bit is disabled.
J	Click the **LO Amp Enable** (represented by Label I) switch to set the AMPLO_BIAS_CONTROL bit (Bit 1, Register 0x100). When the **LO Amp Enable** switch is highlighted, the AMPLO_BIAS_CONTROL bit is enabled. When the **LO Amp Enable** switch is not highlighted, the AMPLO_BIAS_CONTROL bit is disabled.
K	Click **Initialization & Optimization** to initialize and lock the synthesizer.
L1	Enter a value in the **VCO Frequency** text box to set the VCO frequency. The **INT** value (Label L2) is calculated based on the **VCO Frequency** value. Alternatively, change the **INT** value to calculate the **VCO Frequency** value.
L2	Use the **INT** scroll to choose a value, or enter a value in the text box to set the 16-bit integer value (Register 0x200, Register 0x201) of the PLL. The **VCO Frequency** value is calculated based on the **INT** value. Alternatively, change the **VCO Frequency** value to calculate the **INT** value.

ADMV4640 BLOCK DIAGRAM AND FUNCTIONS

Table 1. ADMV4640 Block Diagram Label Functions (See Figure 7)

| Label	Function
M	Enter a value in the **REF IN** text box to set the reference frequency.
N1	Click the **Doubler** switch to set the DOUBLER_EN bit (Bit 3, Register 0x20E). When the **Doubler** switch is highlighted, the DOUBLER_EN bit is enabled. When the **Doubler** switch is not highlighted, the DOUBLER_EN bit is disabled.
N2	Use the **R Divider** scroll to choose a value, or enter a value in the text box to change the R divider value (Bit[4:0], Register 0x20C).
N3	Click the **Divide-by-2** switch to set the RDIV2_EN (Bit 0, Register 0x20E). When the **Divide-by-2** switch is highlighted, the RDIV2_EN bit is enabled. When the **Divide-by-2** switch is not highlighted, the RDIV2_EN bit is disabled.
O	Click the **AMUX** switch (represented by Label O) to set the SEL_AMUX bit (Bit[2:0], Register 0x301). There are two options for AMUX, AGPIO and temperature sensor (PTAT).
P	ADC blocks. Click **Read from ADC** to readback ADC values. See the ADMV4640 data sheet for further details.
Q	Click **Proceed to Memory Map** to open the ADMV4640 memory map (see Figure 8).
R	Click the **AGPIO** switch (represented by Label F) to set the SEL_AGPIO bit (Bit 3, Register 0x301). When the **AGPIO** switch is set to the right, the SEL_AGPIO bit is disabled and the AGPIO pin is used as data output. When the **AGPIO** switch is set to the left, the SEL_AGPIO bit is enabled and the AGPIO pin is used as external data input. See the ADMV4640 data sheet for further details.
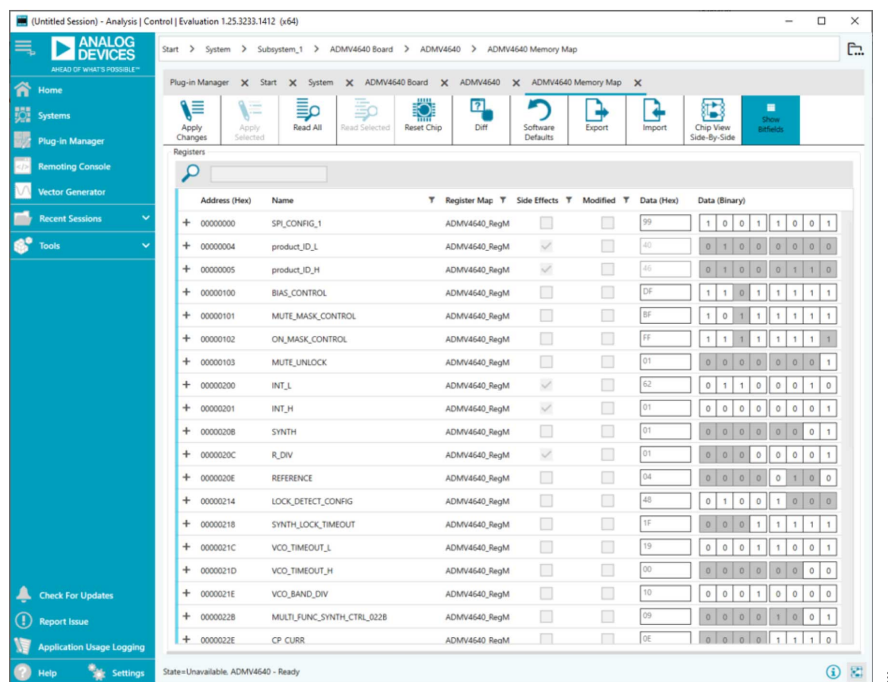
Figure 8. ADMV4640 Memory Map in the ACE Software

EVAL-ADMV4640

EVALUATION BOARD SCHEMATICS

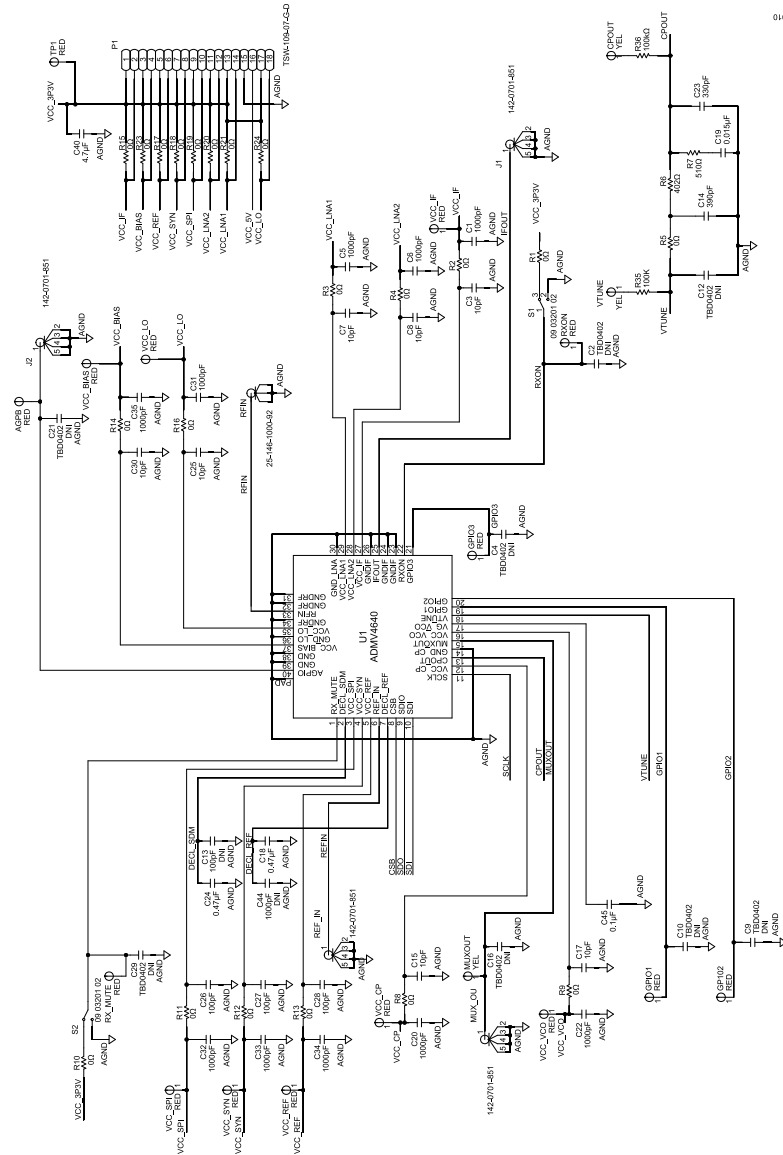*Figure 9. EVAL-ADMV4640Z Schematic, Page 1*
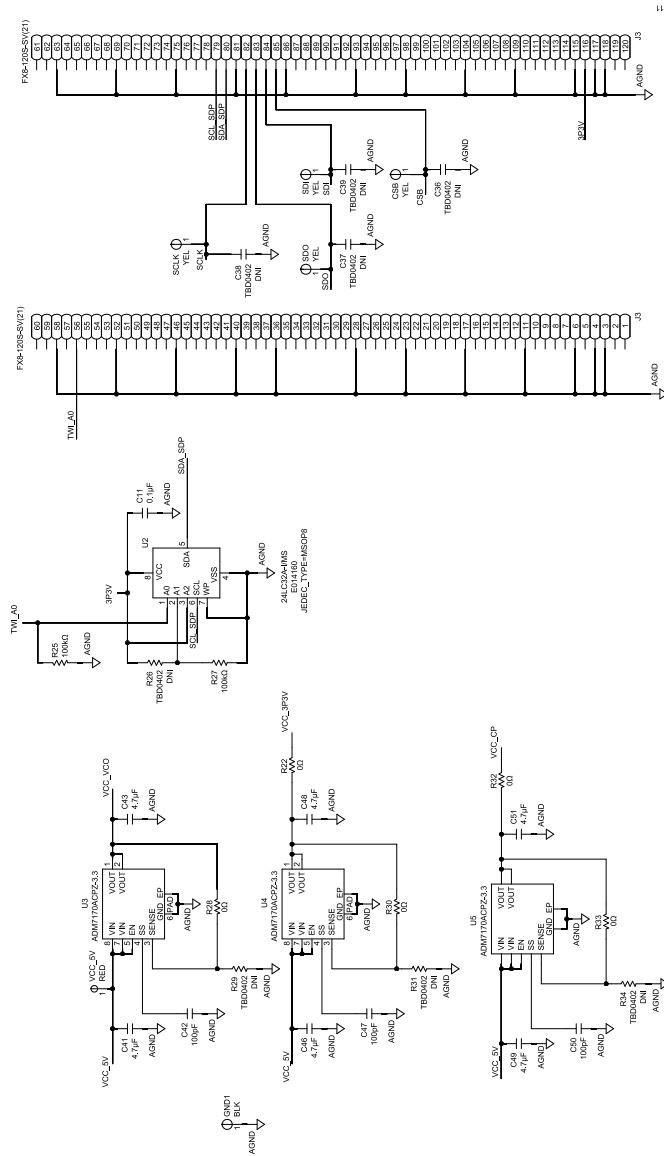
EVALUATION BOARD SCHEMATICS

Figure 10. EVAL-ADMV4640Z Schematic, Page 2

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Qty	Reference Designators	Description	Manufacturer	Part Number
16	AGPB, GP102, GPIO1, GPIO3, RXON, RX_MUTE, TP1, VCC_5V, VCC_BIAS, VCC_CP, VCC_IF, VCC_LO, VCC_REF, VCC_SPI, VCC_SYN, VCC_VCO	Test points, red	Components Corporation	TP-104-01-02
10	C1, C5, C6, C20, C22, C31 to C35	1000 pF ceramic capacitors	Murata	GRM1555C1H102JA01
2	C11, C45	0.1 µF ceramic capacitors	American Technical Ceramics	530L104KT16T
1	C14	390 pF ceramic capacitor	Murata	GCM1555C1H391JA16D
7	C3, C7, C8, C15, C17, C25, C30	10 pF ceramic capacitors	Yageo	CC0402JRNP09BN100
2	C18, C24	0.47 µF ceramic capacitors	Samsung	dCL05A474KA5NNNC
1	C19	0.015 µF ceramic capacitor	Murata	GCM155R71H153JA55D
1	C23	330 pF ceramic capacitor	Murata	GCM1555C1H331JA16D
6	C26, C27, C28, C42, C47, C50	100 pF ceramic capacitors	TDK	C1005NP01H101J050BA
7	C40, C41, C43, C46, C48, C49, C51	4.7 µF ceramic capacitors	Murata	GRM155R60J475ME87D
14	C2, C4, C9, C10, C12, C13, C16, C21, C29, C36 to C39, C44	Do not install	TBD0402	TBD0402
7	CPOUT, CSB, MUXOUT, SCLK, SDI, SDO, VTUNE	Test points, yellow	Components Corporation	TP-104-01-04
1	GND1	Test point, black	Components Corporation	TP-104-01-00
4	J1, J2, MUX_OU, REF_IN	SMA connectors	Johnson	142-0701-851
1	J3	120-pin connector	Hirose Electric	FX8-120S-SV(21)
1	P1	18-pin head connector	Samtec Inc.	TSW-109-07-G-D
26	R1 to R5, R8 to R24, R28, R30, R32, R33	0 Ω chip resistors	Panasonic	ERJ-2GE0R00X
2	R25, R27	100 kΩ chip resistors	Panasonic	ERJ-2RKF1003X
2	R35, R36	100 kΩ chip resistors	Vishay	CRCW0402100KJNED
1	R6	402 kΩ chip resistor	Panasonic	ERJ-2RKF4020X
1	R7	510 Ω chip resistor	Yageo	RC0402FR-07510RL
4	R26, R29, R31, R34	Do not install	TBD0402	TBD0402
1	RFIN	2.92 mm RF connector	SRI Connector Gage Company	25-146-1000-92
2	S1, S2	Switches	EAO	09-03-201-02
1	U1	ADMV4640	Analog Devices	ADMV4640BCPZN
1	U2	EEPROM	Microchip Technology	24LC32A-I/MS
3	U3, U4, U5	LDO regulators	Analog Devices	ADM7170ACPZ-3.3-R7

ORDERING INFORMATION

NOTES

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