

Product Change Notification - SYST-18AQAK665

Date:

19 Sep 2019

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

Affected CPNs:**Notification subject:**

Data Sheet - dsPIC33CH128MP508 Family Datasheet

Notification text:

SYST-18AQAK665

Microchip has released a new Product Documents for the dsPIC33CH128MP508 Family Datasheet of devices. If you are using one of these devices please read the document located at [dsPIC33CH128MP508 Family Datasheet](#).

Notification Status: Final**Description of Change:** This revision incorporates the following updates::

1) Registers:

a) Updates Register 3-21, Register 3-134, Register 3-135, Register 3-172, Register 3-173, Register 3-174, Register 3-179, Register 3-184, Register 4-21, Register 4-102, Register 4-103, Register 4-104, Register 4-109, Register 4-111, Register 6-10, Register 6-20, Register 9-10, Register 9-13, Register 9-14, Register 9-19, Register 9-32, Register 10-1, Register 10-2, Register 10-4 and Register 10-5.

b) Adds Register 6-12.

2) Tables:

a) Updates Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 3-12, Table 3-13, Table 3-34, Table 3-47, Table 4-9, Table 4-31, Table 8-2, Table 8-3, Table 24-4, Table 24-43, Table 24-48, Table 24-49, Table 25-1, Table 25-5, Table 25-7, Table 25-8, Table 25-11, Table 25-12, Table 25-13, Table 25-14, Table 25-15, Table 25-16, Table 25-17, Table 25-19, Table 25-20, Table 25-21 and Table 25-22.

b) Adds Table 3-23, Table 4-20 and Table 25-23.

c) Removes Table 4-25: 5V Input Tolerant Ports and Table 25-8: Doze Current (IDOZE).

3) Figures:

a) Updates Figure 4-18, Figure 6-2, Figure 6-3 and Figure 10-1.

4) Sections:

a) Adds FRM HTML links to all intro notes.

b) Adds Section 3.9.2 "Temperature Sensor", Section 4.7.2 "Temperature Sensor", Section 6.7 "Backup Internal Fast RC (BFRC) Oscillator" and Section 9.3 "PWM4H/L Output on Peripheral Pin Select".

c) Updates Operating Conditions, Section 4.3 "Slave PRAM Program Memory", Section 5.0 "Master Slave Interface (MSI)", Section 6.1 "Primary PLL", Section 6.2 "Auxiliary PLL", Section 15.2 "Setting Baud Rate When Operating as a Bus Master", Section 18.1 "Control Registers" and Section 24.0 "Electrical Characteristics".

d) Minor grammatical and formatting corrections throughout the document.

Impacts to Data Sheet: None**Reason for Change:** To Improve Manufacturability**Change Implementation Status:** Complete



Date Document Changes Effective: 19 September 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

[dsPIC33CH128MP508 Family Datasheet](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

DSPIC33CH128MP508-E/PT

DSPIC33CH128MP508-E/PTVAO

DSPIC33CH128MP508-I/PT

DSPIC33CH128MP508T-I/PT