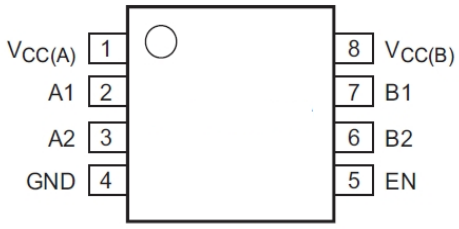
Level Translating I²C-Bus/SMBus Repeater with Tiny Package

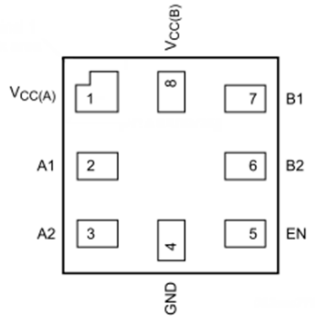
Features

- Bidirectional Buffer Isolates Capacitance and Allows 400pF on Port B of the Device
- Port A Operating Supply Voltage Range of 1.1V to $V_{CC(B)}$ - 1.0V
- Port B Operating Supply Voltage Range of 2.5V to 5.5V
- Voltage Level Translation from 1.1V to $V_{CC(B)}$ - 1.0V and from 2.5V to 5.5V
- Requires no External Pullup Resistors on Lower Voltage Port A
- Open-Drain Port B Inputs/Outputs
- Lockup-Free Operation
- Supports Arbitration and Clock Stretching Across the Repeater
- Accommodates Standard Mode and Fast Mode I²C-Bus Devices and Multiple Masters
- Powered-off High-Impedance I²C-bus Pins
- 5V Tolerant B SCL, SDA and Enable Pins
- 0Hz to 400kHz Clock Frequency
  (Note: The maximum system operating frequency can be less than 400kHz because of delays added by the repeater.)
- ESD Protection Exceeds 8KV HBM per JESD22-A114
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Package: MSOP-8, SOIC-8 and UQFN1.6x1.6-8L

Pin Configuration



SOIC-8 and MSOP-8



UQFN1.6x1.6-8L(Top View)

Description

The PI6ULS5V9509 is a level-translating I²C-bus/SMBus repeater. It can provide bidirectional-level translation between low voltage (down to 1.1V) and high voltage (2.5V to 5.5V) in mixed-mode applications, and it enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The PI6ULS5V9509 enables the system designer to isolate two halves of a bus for both voltage and capacitance, accommodating more I²C devices or longer trace length. It also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus allowing two buses of 400pF to be connected in an I²C application.

The bus port B drivers are compliant with SMBus I/O levels, while port A uses a current sensing mechanism to detect the input or output LOW signal, which prevents bus lockup. Port A uses a 1mA current source for pullup and a 200Ω pulldown driver. This result in a LOW on the port A accommodating smaller voltage swings. The output pulldown on the port A internal buffer LOW is set for approximately 0.2V, while the input threshold of the internal buffer is set about 50mV lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lockup condition from occurring. The output pulldown on the port B drives a hard LOW, and the input level is set at 0.3 of SMBus or I²C-bus voltage level, which enables port B to connect to any other I²C-bus devices or buffer.

The PI6ULS5V9509 drivers are not enabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

Pin Description

Pin No	Pin Name	Description
1	$V_{CC(A)}$	Port A Supply Voltage
2	A1	Port A (Lower Voltage Side)
3	A2	Port A (Lower Voltage Side)
4	GND	Supply Ground (0V)
5	EN	Active HIGH Repeater Enable Input
6	B2	Port B (SMBus/I²C-Bus Side)
7	B1	Port B (SMBus/I²C-Bus Side)
8	$V_{CC(B)}$	Port B Supply Voltage

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram

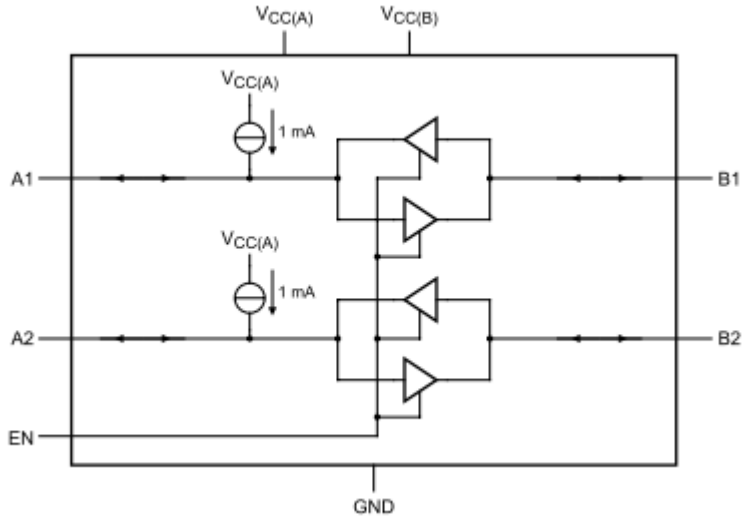


Figure 1: Block Diagram

EN	Function
H	A1 = B1; A2= B2;
L	Disabled

Maximum Ratings

Storage Temperature	-55°C to +125°C
Supply Voltage Port B	-0.5V to +6.0V
Supply Voltage Port A	-0.5V to+6.0V
DC Input Voltage	-0.5V to +6.0V
Control Input Votage(EN)	-0.5V to+6.0V
Total Power Dissipation	100mA
Input/Output Current (Port A & B)	20mA
Input Current (EN, $V_{CC(A)}$, $V_{CC(B)}$, GND)	20mA
ESD: HBM Mode	8000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

GND = 0V; T_{amb} = -40°C to +85°C; unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
$Vcc_{(B)}$	Supply Voltage Port B	—	2.5	—	5.5	V
$Vcc_{(A)}$	Supply Voltage Port A	—	1.1	—	$V_{CC(B)}$ - 1.0	V
$I_{CC(A)}$	Supply Current on Pin $V_{CC(A)}$	All port A static HIGH	0.25	0.45	0.9	mA
		All port A static LOW	1.25	3.0	5	
$I_{CC(B)}$	Supply Current on Pin $V_{CC(B)}$	All port B static HIGH	0.5	0.9	1.1	mA

Note:
1. Typical values with $V_{CC(A)}$ = 1.1 V, $V_{CC(B)}$ = 5 V.

DC Electrical Characteristics

GND = 0V; T_{amb} = -40°C to +85°C; unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ[1]	Max	Unit
Input and Output of Port A (A1 & A2)						
V_{IH}	HIGH-Level Input Voltage	—	$0.7V_{CC(A)}$	—	$V_{CC(A)}$	V
V_{IL}[2]	LOW-Level Input Voltage	—	-0.5	—	+0.3	V
V_{ILc}	Contention LOW-Level Input Voltage	—	−0.5	+0.15	—	V
V_{IK}	Input Clamping Voltage	I_L= -18 mA	-1.5	—	-0.5	V
I_{LI}	Input Leakage Current	$V_I = V_{CC(A)}$	—	—	±1	µA
I_{IL}	LOW-Level Input Current	SDA, SCL; V_I = 0.2 V	-1.5	-1.0	-0.45	mA
V_{OL}	LOW-Level Output Voltage	$V_{CC(A)}$ = 0.95 V to 1.2V	—	0.18	0.25	V
		$V_{CC(A)}$ = > 1.2V to ($V_{CC(B)}$ − 1 V)	—	0.2	0.3	
V_{OL}-V_{ILc}	Difference Between LOW-Level Output and LOW-Level Input Voltage Contention	Guaranteed by design	—	50	—	mV
I_{LOH}	HIGH-Level Output Leakage Current	$V_O = V_{CC(A)}$	—	—	10	µA
C_{io}	Input/Output Capacitance	—	—	6	—	pF
Input and Output of Port B (B1 & B2)						
V_{IH}	HIGH-Level Input Voltage	—	$0.7V_{CC(B)}$	—	$V_{CC(B)}$	V
V_{IL}	LOW-Level Input Voltage	—	-0.5	—	+0.3 $V_{CC(B)}$	V
V_{IK}	Input Clamping Voltage	I_I = -18 mA	-1.5	—	-0.5	V
I_{LI}	Input Leakage Current	V_I = 3.6 V	-1	—	1	µA
I_{IL}	LOW-Level Input Current	V_I = 0.2 V	—	—	10	µA
V_{OL}	LOW-Level Output Voltage	I_{OL} = 6 mA	—	0.1	0.2	V
I_{LOH}	HIGH-Level Output Leakage Current	V_O = 3.6 V	—	—	10	µA
C_{io}	Input/Output Capacitance	—	—	3	—	pF
Enable						
V_{IH}	HIGH-Level Input Voltage	—	$0.9V_{CC(A)}$	—	$V_{CC(B)}$	V
V_{IL}	LOW-Level Input Voltage	—	-0.5	—	+0.1 $V_{CC(A)}$	V
I_{IL}	LOW-Level Input Current	V_I = 0.2 V, EN; V_{CC} = 3.6 V	-1	—	+1	µA
I_{LI}	Input Leakage Current	$V_I = V_{CC}$	-1	—	+1	µA
C_i	Input Capacitance	V_I = 3.0 V or 0V	—	2	—	pF

Note:
1. Typical values with $V_{CC(A)}$ = 1.1 V, $V_{CC(B)}$ = 5 V.
2. V_{IL} specification is for the falling edge seen by the port A input. V_{ILC} is for the static LOW levels seen by the port A input resulting in port B output staying LOW.

Dynamic Characteristics

$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH Propagation Delay	Port B to port A	—	65	216	ns
t_{PHL}	HIGH-to-LOW Propagation Delay	Port B to port A	—	25	140	ns
t_{TLH}	LOW-to-HIGH Output Transition Time	Port A	14	22	96	ns
t_{THL}	HIGH-to-LOW Output Transition Time	Port A	—	20	—	ns
t_{PLH}	LOW-to-HIGH Propagation Delay	Port A to port B	—	-69	-139	ns
t_{PLH} 2	LOW-to-HIGH Propagation Delay	Port A to port B measured from the 50% initial LOW on port A to 1.5V rising on port B	—	100	226	ns
t_{PHL}	HIGH-to-LOW Propagation Delay	Port A to port B	20	50	183	ns
t_{TLH} [2]	LOW-to-HIGH Output Transition Time	Port B	-	61	—	ns
t_{THL}	HIGH-to-LOW Output Transition Time	Port B	1	2	40	ns
t_{su}	Setup Time	EN HIGH before START condition	100	—	—	ns
t_h	Hold Time	EN HIGH after STOP condition	100	—	—	ns

$V_{CC(A)}$ = 1.9 V; $V_{CC(B)}$ = 5.0 V [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH Propagation Delay	Port B to port A	—	75	216	ns
t_{PHL}	HIGH-to-LOW Propagation Delay	Port B to port A	—	20	140	ns
t_{TLH}	LOW-to-HIGH Output Transition Time	Port A	14	27	96	ns
t_{THL}	HIGH-to-LOW Output Transition Time	Port A	—	20	—	ns
t_{PLH}	LOW-to-HIGH Propagation Delay	Port A to port B	—	-69	-139	ns
t_{PLH2}	LOW-to-HIGH Propagation Delay	Port A to port B; measured from the 50 % of initial LOW on port A to 1.5 V rising on port B	—	91	226	ns
t_{PHL}	HIGH-to-LOW Propagation Delay	Port A to port B	20	50	183	ns
t_{TLH} 2	LOW-to-HIGH Output Transition Time	Port B	—	65	—	ns
t_{THL}	HIGH-to-LOW Output Transition Time	Port B	1	2	40	ns
t_{su}	Setup Time	EN HIGH before START condition	100	—	—	ns
t_h	Hold Time	EN HIGH after STOP condition	100	—	—	ns

Note:
1. Load capacitance = 50 pF; load resistance on port B = 1.35 kΩ.
2. Value is determined by RC time constant of bus line.

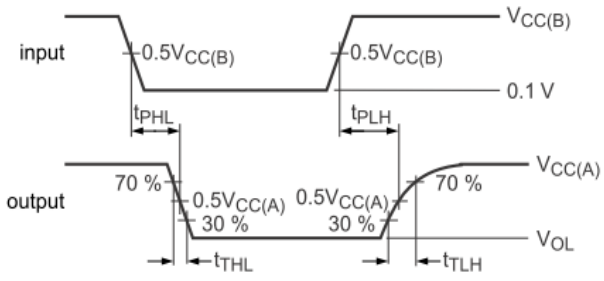


Figure 2: Propagation Delay and Transition Times B→A

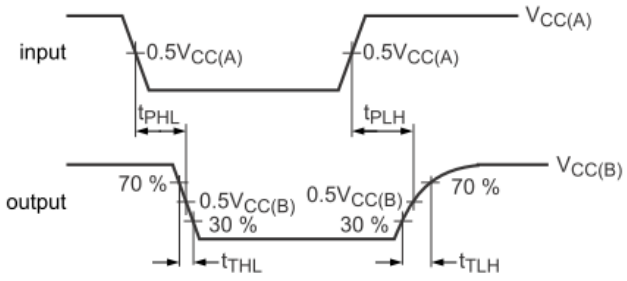


Figure 3: Propagation Delay and Transition Times A→B

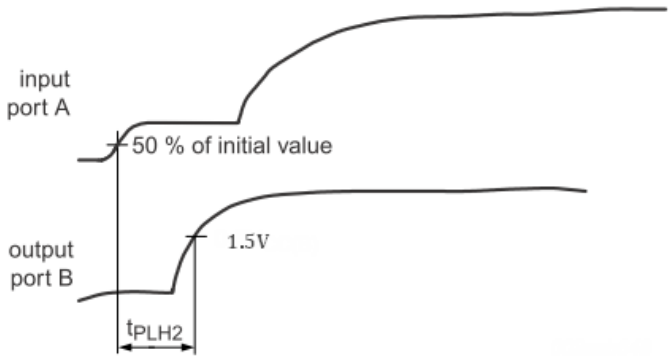
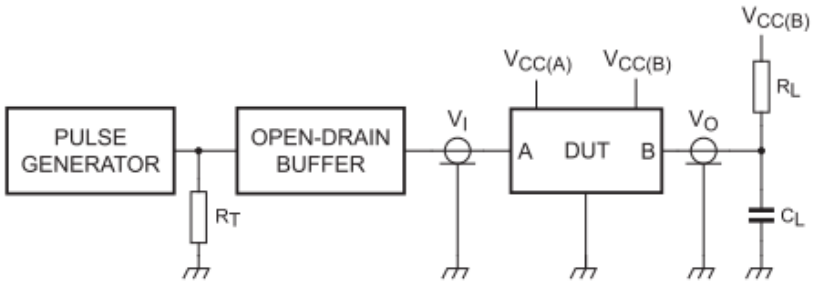


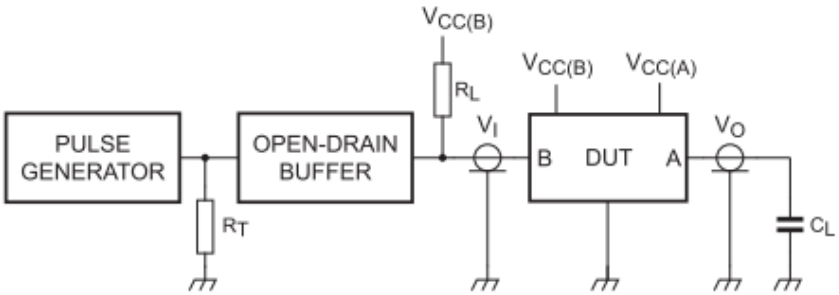
Figure 4: Propagation Delay from Port A's External Driver Switching off to Port B LOW-to-HIGH Transition; (A→B)



R_L = load resistor; 1.35 kΩ on port B

C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators



R_L = load resistor; 1.35 kΩ on port B

C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Figure 5: Test Circuit

Functional Description

The PI6ULS5V9509 is a level-translating I^2C-bus/SMBus repeater. It can provide bidirectional level translation between low voltage (down to 1.1V) and high voltage (2.5V to 5.5V) in mixed-mode applications, and it enables I^2C and similar bus systems to be extended without degradation of performance even during level shifting.

The PI6ULS5V9509 enables the system designer to isolate two halves of a bus for both voltage and capacitance, accommodating more I^2C devices or longer trace length. It also permits extension of the I^2C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus allowing two buses of 400pF to be connected in an I^2C application.

The bus port B drivers are compliant with SMBus I/O levels, while port A uses a current-sensing mechanism to detect the input or output LOW signal, which prevents bus lockup. Port A uses a 1mA current source for pullup and a 200Ω pulldown driver. This result in a LOW on the port A accommodating smaller voltage swings. The output pulldown on the port A internal buffer LOW is set for approximately 0.2V, while the input threshold of the internal buffer is set about 50mV lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lockup condition from occurring. The output pulldown on the port B drives a hard LOW, and the input level is set at 0.3 of SMBus or I^2C-bus voltage level, which enables port B to connect to any other I^2C-bus devices or buffer.

The PI6ULS5V9509 drivers are not enabled unless $V_{CC(A)}$ is above 0.8V and $V_{CC(B)}$ is above 2.5V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

Application Information

A typical application is shown in Figure 6. In this example, the system master is running on a 1.1V I^2C-bus while the slave is connected to a 3.3 V bus. Both buses run at 400kHz. Master devices can be placed on either bus.

When port B of the PI6ULS5V9509 is pulled LOW by a driver on the I^2C-bus, a CMOS hysteresis detects the falling edge when it goes below $0.3V_{CC(B)}$ and causes the internal driver on port A to turn on, causing port A to pull down to about 0.2 V. When port A of the PI6ULS5V9509 falls, first a comparator detects the falling edge and causes the internal driver on port B to turn on and pull the port B pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 7 and Figure 8. If the bus master in Figure 6 writes to the slave through the PI6ULS5V9509, waveforms shown in Figure 7 are observed on the B bus. This looks like a normal I^2C-bus transmission.

On the A bus side of the PI6ULS5V9509, the clock and data lines have a positive offset from ground equal to the V_{OL} of the PI6ULS5V9509. After the eighth clock pulse, the data line is pulled to the VOL of the master device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PI6ULS5V9509 for a short delay while the B bus side rises above $0.5\ V_{CC(B)}$, then it continues HIGH. It is important to note that any arbitration or clock-stretching events require that the LOW level on the A bus side at the input of the PI6ULS5V9509 (V_{IL}) is below V_{ILC} to be recognized by the PI6ULS5V9509 and then transmitted to the B bus side.

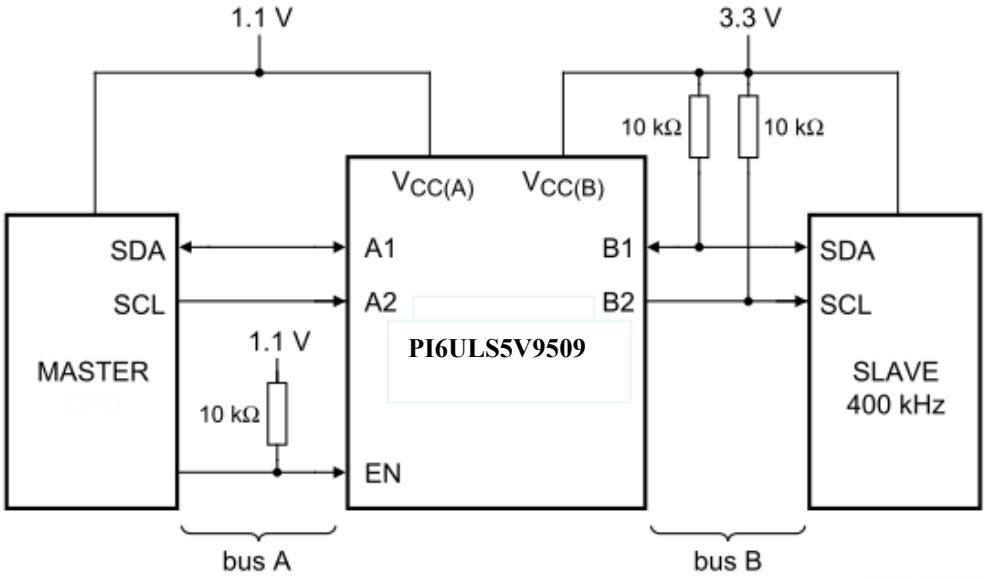


Figure 6: Typical Application

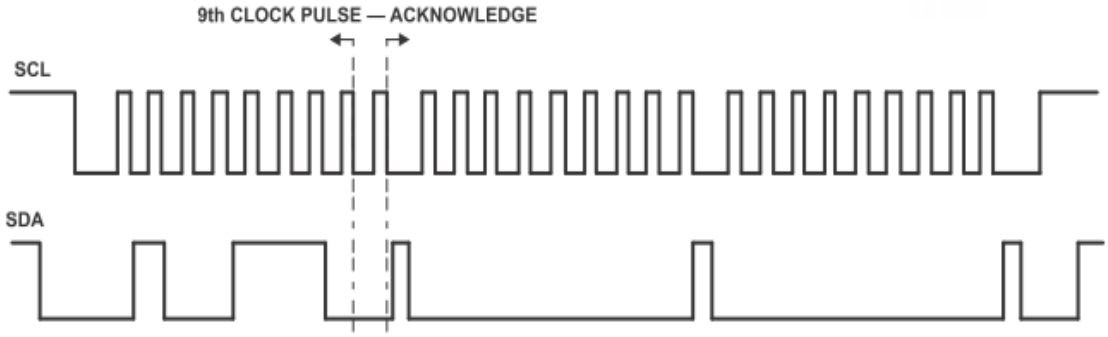


Figure 7: Bus B I²C/SMBus Waveform

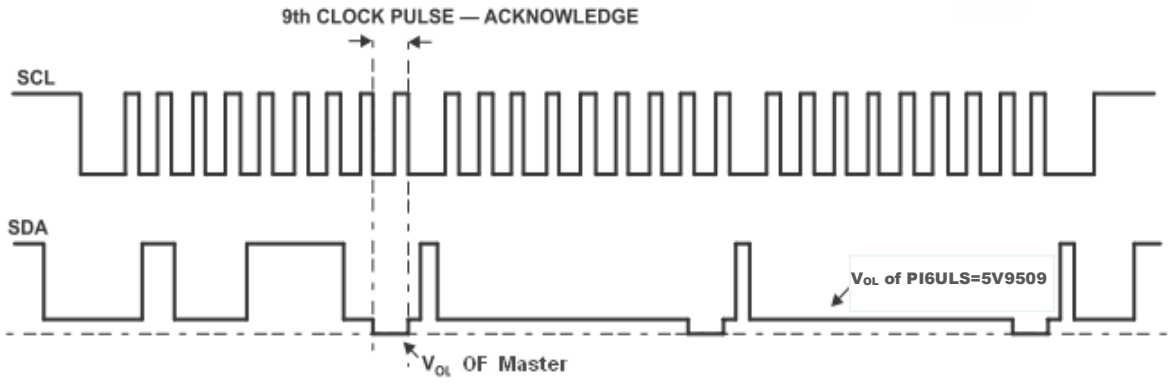


Figure 8: Bus A Lower Voltage Waveform

Part Marking

U Package

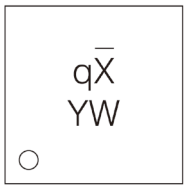
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above "L" means Fab3 of MGN
Bar above fab code means Cu wire

W Package

Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above "I" means Fab3 of MGN
Bar above fab code means Cu wire

XT Package

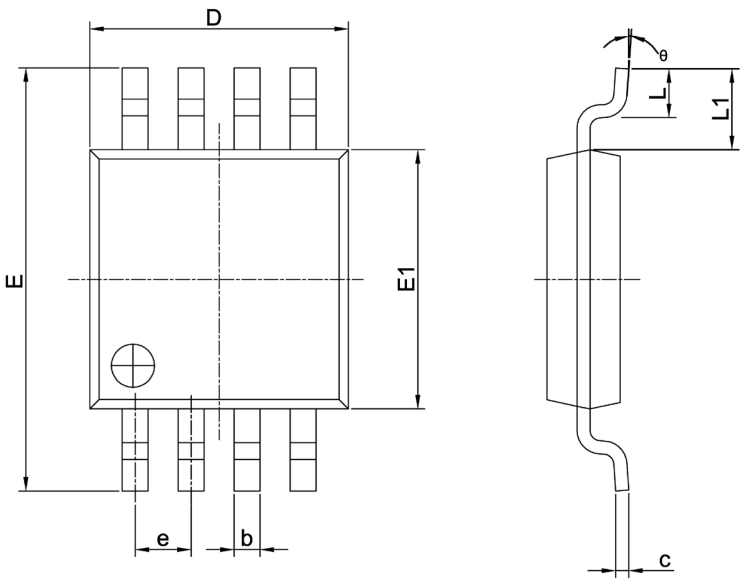
qX: PI6ULS5V9509XT

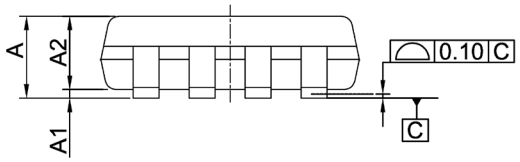


Y: Date Code (Year)
W: Date Code (Workweek)
Bar above X means Fab3 of MGN

Packaging Mechanical

8-MSOP (U)





PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. REFER JEDEC MO-187F/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

DATE: 11/03/16

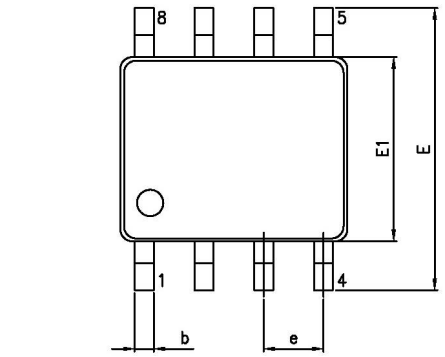
DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP

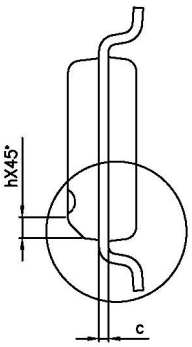
PACKAGE CODE: U (U8)

DOCUMENT CONTROL #: PD-1261 REVISION: G

16-0242

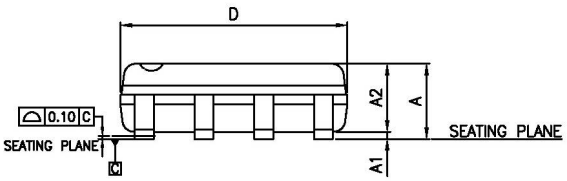
8-SOIC (W)

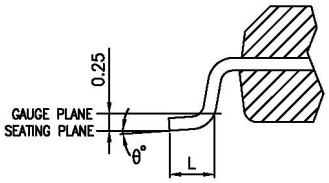




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

UNIT : mm





NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012

PERICOM Enabling Serial Connectivity

DATE: 02/21/14

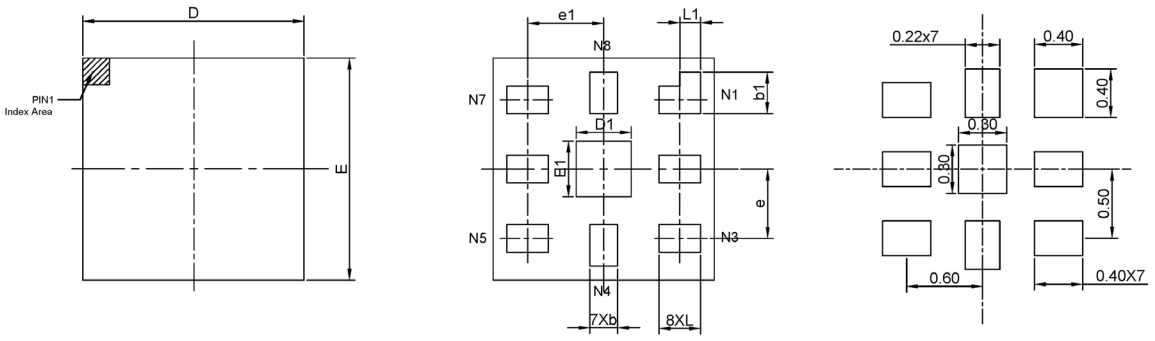
DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

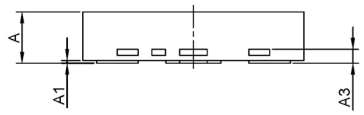
DOCUMENT CONTROL #: PD-1001 REVISION: G

15-0103

8-UQFN (XT)



PKG. DIMENSIONS(MM)			
SYMBOL	Min	Nom	Max
A	0.32	0.36	0.40
A1	0.00	0.03	0.05
A3		0.10 REF	
D	1.55	1.60	1.65
E	1.55	1.60	1.65
D1	0.30	0.40	0.50
E1	0.30	0.40	0.50
b	0.15	0.20	0.25
e		0.50 TYP	
e1		0.55 TYP	
L	0.25	0.30	0.35
b1	0.25	0.30	0.35
L1		0.15 REF	



Note:
1. Comply with MO-248E, except 'A' and 'A3'

DATE: 12/30/16

DESCRIPTION: 8-Pin, UQFN, 1.6X1.6, COL

PACKAGE CODE: XT (XT8)

DOCUMENT CONTROL #: PD-2132 REVISION: A

16-0286

For latest package information:
See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Part No.	Package Code	Package Description
PI6ULS5V9509UEX	U	8-Pin, Mini Small Outline Package (MSOP)
PI6ULS5V9509WEX	W	8-Pin, 150mil-Wide (SOIC)
PI6ULS5V9509XTEX	XT	8-Pin, 1.6x1.6, COL (UQFN)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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