PRELIMINARY

CYW20710

Single-Chip Bluetooth® Transceiver and Baseband Processor

General Description

The Cypress CYW20710 is a monolithic, single-chip, Bluetooth 4.0 compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. Manufactured using the industry's most advanced 65 nm CMOS low-power process, the CYW20710 employs the highest level of integration, eliminating all critical external components, and thereby minimizing the device's footprint and costs associated with the implementation of Bluetooth solutions.

The CYW20710 is the optimal solution for voice and data applications that require a Bluetooth SIG standard Host Controller Interface (HCI) via UART H4 or H5 and PCM audio interface support. The CYW20710 radio transceiver's enhanced radio performance meets the most stringent industrial temperature application requirements for compact integration into mobile handset and portable devices. The CYW20710 is fully compatible with all standard TCXO frequencies and provides full radio compatibility, enabling it to operate simultaneously with GPS and cellular radios.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Cypress to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20710	CYW20710
BCM20710A1KUFBXG	CYW20710A1KUFBXG
BCM20710A1KUBXG	CYW20710A1KUBXG

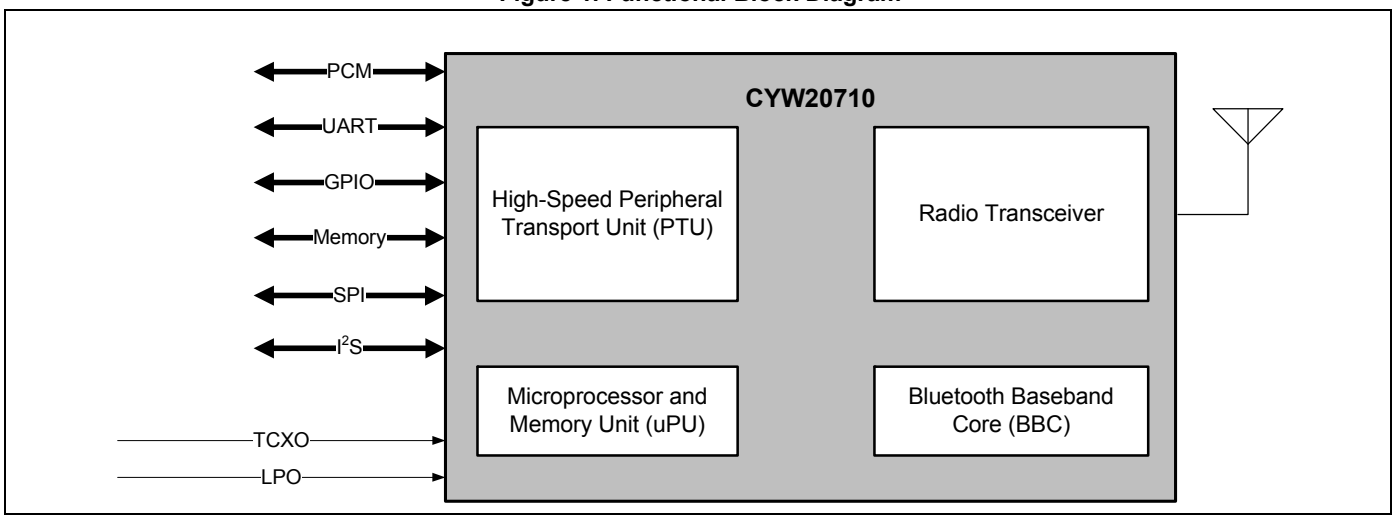
Features

- Bluetooth 4.0 + EDR compliant
- Class 1 capable with built-in PA
- Programmable output power control meets Class 1, Class 2, or Class 3 requirements
- Use supply voltages up to 5.5V
- Supports Cypress SmartAudio™, wide-band speech, SBC codec, and packet loss concealment.
- Fractional-N synthesizer supports frequency references from 12 MHz to 52 MHz
- Automatic frequency detection for standard crystal and TCXO values when an external 32.768 kHz reference clock is provided.
- Ultra-low power consumption
- Supports serial flash interfaces
- Available in 42-bump WLBGA and 50-ball FPBGA packages.
- ARM7TDMI-S™–based microprocessor with integrated ROM and RAM
- Supports mobile without external memory

Applications

- Mobile handsets and smart phones
- Personal digital assistants
- Automotive telematic systems

Figure 1. Functional Block Diagram



Contents

1. Overview

The Cypress CYW20710 complies with the Bluetooth Core Specification, version 4.0 and is designed for use with a standard Host Controller Interface (HCI) UART. The combination of the Bluetooth Baseband Core (BBC), a Peripheral Transport Unit (PTU), and an ARM®-based microprocessor with on-chip ROM provides a complete lower layer Bluetooth protocol stack, including the Link Controller (LC), Link Manager (LM), and HCI.

1.1 Major Features

Major features of the CYW20710 include:

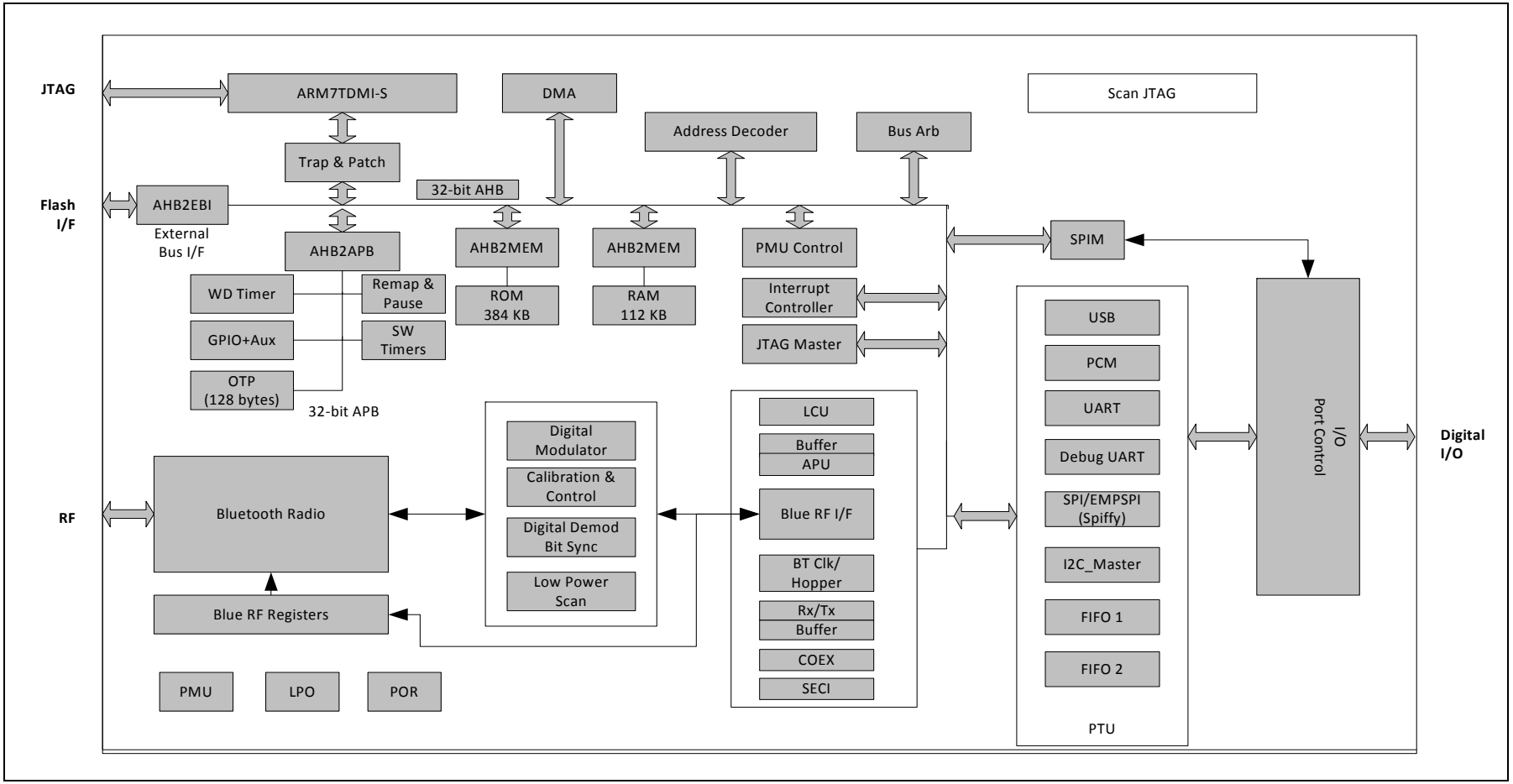
- Support for Bluetooth 4.0 + EDR, including the following options:
  - A whitelist size of 25.
  - Enhanced Power Control
  - HCI Read Encryption Key Size command
- Full support for Bluetooth 2.1 + EDR additional features:
  - Secure Simple Pairing (SSP)
  - Encryption Pause Resume (EPR)
  - Enhance Inquiry Response (EIR)
  - Link Supervision Time Out (LSTO)
  - Sniff SubRating (SSR)
  - Erroneous Data (ED)
  - Packet Boundary Flag (PBF)
- Built-in Low Drop-Out (LDO) regulators (2)
  - 1.63 to 5.5V input voltage range
  - 1.8 to 3.3V intermediate programmable output voltage
- Integrated RF section
  - Single-ended, 50 ohm RF interface
  - Built-in TX/RX switch functionality
  - TX Class 1 output power capability
  - -88 dBm RX sensitivity basic rate
- Supports maximum Bluetooth data rates over HCI UART and SPI interfaces
- Multipoint operation, with up to 7 active slaves
  - Maximum of 7 simultaneous active ACL links
  - Maximum of 3 simultaneous active SCO and eSCO links, with Scatternet support
- Scatternet operation, with up to 4 active piconets (with background scan and support for ScatterMode)
- High-speed HCI UART transport support
  - H4 five-wire UART (four signal wires, one ground wire)
  - H5 three-wire UART (two signal wires, one ground wire)
  - Maximum UART baud rates of 4 Mbps
  - Low-power out-of-band BT_WAKE and HOST_WAKE signaling
  - VSC from host transport to UART
  - Proprietary compressing scheme (allows more than two simultaneous A2DP packets and up to five devices at a time)
- Channel Quality-Driven Data Rate (CQDDR) and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features

- Full support for power savings modes:
  - Bluetooth standard Hold and Sniff
  - Deep sleep modes and regulator shutdown
- Supports Wide-Band Speech (WBS) over PCM and Packet Loss Concealment (PLC) for better audio quality
- 2-, 3-, and 4-wire coexistence
- Power Amplifier (PA) shutdown for externally controlled coexistence, such as WIMAX
- Built-in LPO clock or operation using an external LPO clock
- TCXO input and auto-detection of all standard handset clock frequencies (supports low-power crystal, which can be used during Power Saving mode with better timing accuracy)
- OR gate for combining a host clock request with a Bluetooth clock request (operates even when the Bluetooth core logic is powered off)
- Larger patch RAM space to support future enhancements
- Serial flash Interface with native support for devices from several manufacturers
- One-Time Programmable (OTP) memory

1.2 Block Diagram

Figure 2 shows the interconnect of the major CYW20710 physical blocks and associated external interfaces.

Figure 2. Functional Block Diagram



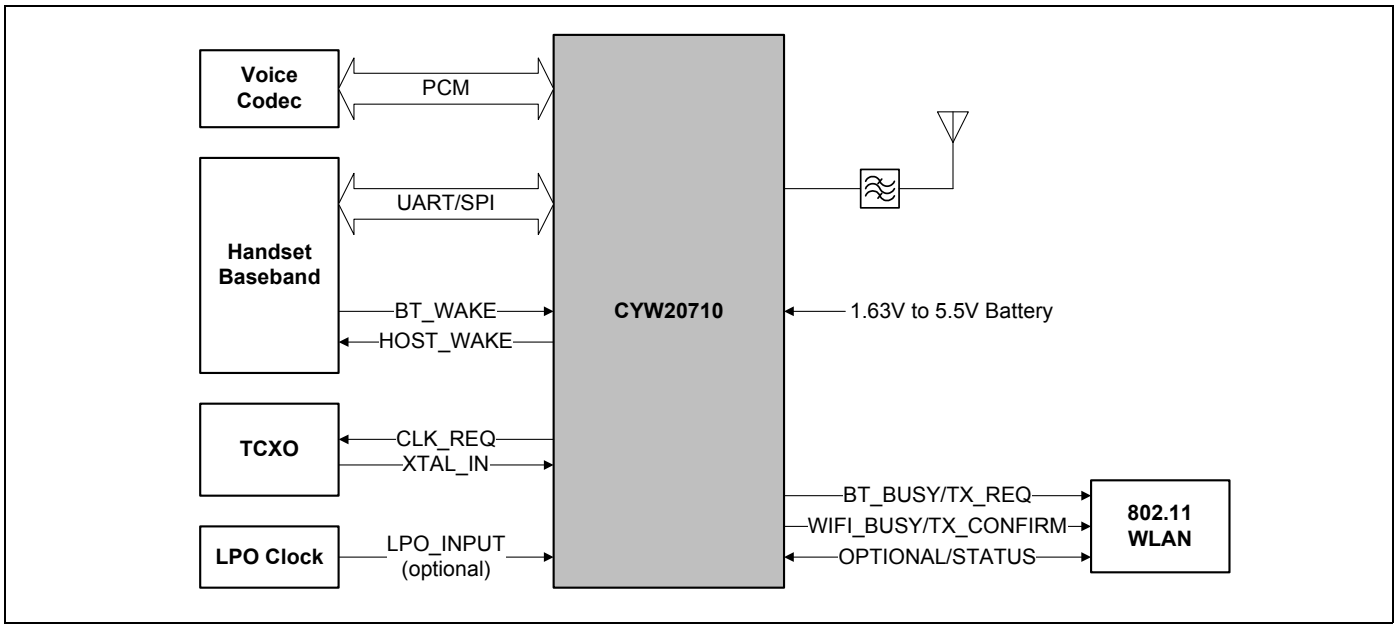
1.3 Mobile Phone Usage Model

The CYW20710 is designed to provide a direct interface to new and existing handset designs, as shown in Figure 3. The device has flexible PCM and UART interfaces, enabling it to transparently connect to existing circuits. In addition, the TCXO and external LPO inputs allow the use of existing handset features, helping to minimize product size, power, and cost.

The device incorporates a number of unique features to accommodate integration into mobile phone platforms.

- The PCM interface provides multiple modes of operation to support both master and slave, as well as hybrid interfacing to one or more external codec devices.
- The UART interface supports hardware flow control with tight integration to power control sideband signaling to support the lowest power operation.
- The TCXO interface accommodates the typical reference frequencies used by cell phones.
- A programmable TCXO power-up or power-down signal (active-high or active-low) allows the device to indicate when the clock supplied to the device can be disabled for added power saving during Sleep mode.
- The TCXO and external LPO inputs are high-impedance with minimal loading on the driving source whether power is applied to the device or has been removed.
- The highly linear design of the radio transceiver ensures that the device has the lowest output spurious emissions, regardless of the state of operation, and has been fully characterized in the global cellular bands.
- The transceiver design has excellent blocking (eliminating desensitization of the Bluetooth receiver) and intermodulation performance (distortion of the transmitted signal caused by mixing the cellular and Bluetooth transmissions) in the presence of a cellular transmission (GSM, GPRS, CDMA, WCDMA, or iDEN). Minimal external filtering is required for integration within the handset.
- Few external components are required for integration and very compact WLBGA packaging is available.

Figure 3. Mobile Phone Usage Model



2. Integrated Radio Transceiver

The CYW20710 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The CYW20710 is fully compliant with the Bluetooth Radio Specification and enhanced data rate specification and meets or exceeds the requirements to provide the highest communication link quality of service.

2.1 Transmitter Path

The CYW20710 features a fully integrated zero IF transmitter. The baseband transmitted data is digitally modulated in the modem block and up-converted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q up-conversion, a high-output power amplifier (PA), and RF filtering.

The CYW20710 also incorporates modulation schemes to support enhanced data rates.

- P/4-DQPSK for 2 Mbps
- 8-DPSK for 3 Mbps

2.1.1 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, Π/4DQPSK, and 8-DPSK signals. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

2.1.2 Power Amplifier

The CYW20710 has an integrated PA that can be configured for Class 2 operation, transmitting up to +4 dBm. The PA can also be configured for Class 1 operation, transmitting up +10 dBm at the chip in gFSK mode, when a minimum supply voltage of 2.5V is applied to VDDTF.

Because of the linear nature of the PA, combined with integrated filtering, minimal external filtering is required to meet Bluetooth and regulatory harmonic and spurious requirements.

Using a highly linearized, temperature compensated design, the PA can transmit +10 dBm for basic rate and +8 dBm for enhanced data rates (2 to 3 Mbps). A flexible supply voltage range allows the PA to operate from 1.2V to 3.3V. A minimum supply voltage of 2.5V is required at VDDTF to achieve +10 dBm of transmit power.

2.2 Receiver Path

The receiver path uses a low IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the device to be used in most applications without off-chip filtering. For integrated handset operation where the Bluetooth function is integrated close to the cellular transmitter, minimal external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

2.2.1 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer uses the low IF received signal to perform an optimal frequency tracking and bit synchronization algorithm.

2.2.2 Receiver Signal Strength Indicator

The CYW20710 radio provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

2.3 Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The device uses fully-integrated PLL loop filters.

2.4 Calibration

The radio transceiver features an automated calibration scheme that is fully self-contained in the radio. User interaction is not required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all major blocks in the radio, including gain and phase characteristics of filters, matching between key components, and key gain blocks. Calibration, which takes process and temperature variations into account, occurs transparently during the settling time of the hops, adjusting for temperature variations as the device cools and heats during normal operation.

2.5 Internal LDO Regulator

Two internal Low Drop-Out (LDO) voltage regulators eliminate the need for external voltage regulators and therefore reduce the BOM. The first LDO is a preregulator (HV LDO). The second LDO (Main LDO) supplies the main power to the CYW20710 (see Figure 2).

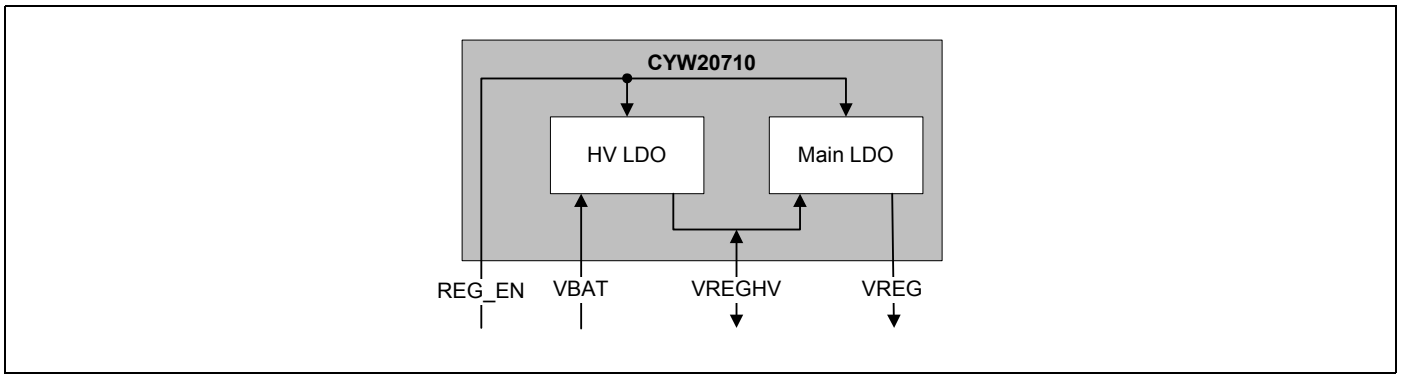
The HV LDO has an input voltage range of 2.3V to 5.5V. The input VBAT is ideal for batteries. The VREGHV output is programmable from 1.8V to 3.3V, in 100 mV steps. The dropout voltage is 200 mV. The HV LDO can supply up to 95 mA, which leaves spare power for external circuitry such as an RF power amp for higher transmit power. If the HV LDO is not used, to turn off the HV LDO and minimize current consumption, connect the VBAT input to the VREGHV output. Firmware can then disable the HV LDO, saving the quiescent current.

The HV LDO default output voltage is 2.9V, allowing this regulator to be used to power external NV memory devices, as well as the VDDO rail. The firmware can then adjust this output to as low as 1.8V, if desired, to power VDDTF.

The main LDO has a 1.22V output (VREG) and is used to supply main power to the CYW20710. The input of this LDO (VREGHV) has an input voltage range of from 1.63V to 3.63V. The output of the HV LDO is internally connected to the input to the main LDO. Power can be applied to VREGHV when the HV LDO is not used. The main LDO supplies power to the entire device for Class 2 operation. The main LDO can drive up to 60 mA, which leaves spare power for external circuitry. The main LDO is bypassed by not connecting anything to its output (VREG) and driving 1.12V–1.32V directly to VDDC and VDDRF.

REG_EN provides a control signal for the host to control power to the CYW20710. When power is enabled, the CYW20710 will require complete initialization.

Figure 4. LDO Functional Block Diagram



3. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements the time critical functions required for high-performance Bluetooth operation. The BBC manages buffering, segmentation, and data routing for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL Tx/Rx transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

3.1 Transmit and Receive Functions

The following transmit and receive functions are implemented in the BBC hardware to increase the reliability and security of the Tx/Rx data before sending the data over the air:

In the transmitter:

- Data framing
- Forward Error Correction (FEC) generation
- Header Error Control (HEC) generation
- Cyclic Redundancy Check (CRC) generation
- Key generation
- Data encryption
- Data whitening

In the receiver:

- Symbol timing recovery
- Data deframing
- FEC
- HEC
- CRC
- Data decryption
- Data dewhitening

3.2 Bluetooth 4.0 + EDR Features

The CYW20710 supports Bluetooth 4.0 + EDR, including the following options:

- A whitelist size of 25
- Enhanced Power Control
- HCI Read Encryption Key Size command

The CYW20710 provides full support for Bluetooth 2.1 + EDR additional features:

- Secure Simple Pairing (SSP)
- Encryption Pause Resume (EPR)
- Enhance Inquiry Response (EIR)
- Link Supervision Time Out (LSTO)
- Sniff SubRating (SSR)
- Erroneous Data (ED)
- Packet Boundary Flag (PBF)

3.3 Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number, based on the link controller state, Bluetooth clock, and device address.

3.4 Link Control Layer

The Link Control layer is part of the Bluetooth link control functions implemented in dedicated logic in the Link Control Unit (LCU). This layer consists of the Command Controller that takes commands from the software and other controllers that are activated or configured by the Command Controller to perform the link control tasks.

There are two major states–Standby and Connection. Each task establishes a different state in the Bluetooth Link Controller. In addition, there are eight substates—Page, Page Scan, Inquiry, Inquiry Scan, Park, Sniff Subrate, and Hold.

3.5 Test Mode Support

The CYW20710 fully supports Bluetooth Test Mode, including the transmitter tests, normal and delayed Loopback tests, and the reduced hopping sequence.

In addition to the standard Bluetooth Test mode, the device supports enhanced testing features to simplify RF debugging and qualification and type approval testing.

These test features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Directs receiver output to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant bit stream transmission
  - Unmodulated, 8-bit fixed pattern, PRBS-9, or PRBS-15
  - Enables modulated signal measurements with standard RF test equipment
- Packetized connectionless transmitter test
  - Hopping or fixed frequency
  - Multiple packet types supported
  - Multiple data patterns supported
- Packetized connectionless receiver test
  - Fixed frequency
  - Multiple packet types supported
  - Multiple data patterns supported

3.6 Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked through power management registers or packet handling in the baseband core. This section contains descriptions of the PMU features.

3.6.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions, accordingly.

3.6.2 Host Controller Power Management

The host can place the device in a sleep state, in which all nonessential blocks are powered off and all nonessential clocks are disabled. Power to the digital core is maintained so that the state of the registers and RAM is not lost. In addition, the LPO clock is applied to the internal sleep controller so that the chip can wake automatically at a specified time or based on signaling from the host. The goal is to limit the current consumption to a minimum, while maintaining the ability to wake up and resume a connection with minimal latency.

If a scan or sniff session is enabled while the device is in Sleep mode, the device automatically will wake up for the scan/sniff event, then go back to sleep when the event is done. In this case, the device uses its internal LPO-based timers to trigger the periodic wake up. While in Sleep mode, the transports are idle. However, the host can signal the device to wake up at any time. If signaled to wake up while a scan or sniff session is in progress, the session continues but the device will not sleep between scan/sniff events. Once Sleep mode is enabled, the wake signaling mechanism can also be thought of as a sleep signaling mechanism, since removing the wake status will often cause the device to sleep.

In addition to a Bluetooth device wake signaling mechanism, there is a host wake signaling mechanism. This feature provides a way for the Bluetooth device to wake up a host that is in a reduced power state.

There are two mechanisms for the device and the host to signal wake status to each other:

Bluetooth WAKE (BT_WAKE) and Host WAKE (and HOST_WAKE) signaling	The BT_WAKE pin (GPIO_0) allows the host to wake the BT device, and HOST_WAKE (GPIO_1) is an output that allows the BT device to wake the host.
In-band UART signaling	The CTS and RTS signals of the UART interface are used for BT wake (CTS) and Host wake (RTS) functions in addition to their normal function on the UART interface. Note that this applies for both H4 and H5 protocols.

When running in SPI mode, the CYW20710 has a mode where it enters Sleep mode when there is no activity on the SPI interface for a specified (programmable) amount of time. Idle mode is detected when the SPI_CSN is left deasserted. Whether to sleep on an idle interface and the amount of time to wait before entering Sleep mode can be programed by the host. Once the CYW20710 enters sleep, the host can wake it by asserting SPI_CSN. If the host decides to sleep, the CYW20710 will wake up the host by asserting SPI_INT when it has data for it.

Note: Successful operation of the power management handshaking signals requires coordinated support between the device firmware and the host software.

Table 2. Power Control Pin Summary

Pin	Direction	Description
BT_WAKE (GPIO_0)	Host output BT input	Bluetooth device wake-up: Signal from the host to the Bluetooth device that the host requires attention. • Asserted = Bluetooth device must wake up or remain awake. • Deasserted = Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. By default, BT_WAKE is active-low (if BT-WAKE is low it requires the device to wake up or remain awake).
HOST_WAKE (GPIO_1)	BT output Host input	Host wake-up. Signal from the Bluetooth device to the host indicating that Bluetooth device requires attention. • Asserted = Host device must wake up or remain awake. • Deasserted = Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ (GPIO_5)	BT output	Clock request • Asserted = External clock reference required • Deasserted = External clock reference may be powered down The polarity of CLK_REQ is software configurable and can be set to active high (TM0 = 1) or active low (TM0 = 0).
REG_EN	BT input	Enables the internal preregulator and main regulator outputs. REG_EN is active-high. • 1 = Enabled • 0 = Disabled

3.6.3 Bluetooth Baseband Core Power Management

The device provides the following low-power operations for the Bluetooth Baseband Core (BBC):

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth specified low-power connection modes—Sniff, Hold, and Park. While in these low-power connection modes, the device runs on the Low Power Oscillator and wakes up after a predefined time period.

Backdrive Protection

The CYW20710 provides a backdrive protection feature that allows the device to be turned off while the host and other devices in the system remain operational. When the device is not needed in the system, VDD_RF and VDDC are shut down and VDDO remains powered. This allows the device to be effectively off, while keeping the I/O pins powered so that they do not draw extra current from other devices connected to the I/O.

Note: VDD_RF collectively refers to the VDDTF, VDDIF, VDDLNA, VDDPX, and VDDRF RF power supplies.

Note: Never apply voltage to I/O pins if VDDO is not applied.

During the low power shutdown state and as long as VDDO remains applied to the device, all outputs are tristated and all digital and analog clocks are disabled. Input voltages must remain within the limits defined for normal operation. This is done to either prevent current draw and back loading on digital signals in the system. It also enables the device to be fully integrated in an embedded device and take full advantage of the lowest power savings modes. If VDDC is powered up externally (not connected to VREG), VDDC requires 750K ohms to ground during low-power shutdown. If VDDC is powered up by VREG, VDDC does not require 750K ohms to ground because the internal main LDO has about 750 K ohms to ground when turned off.

Several signals, including the frequency reference input (XTAL_IN) and external LPO input (LPO_IN), are designed to be high-impedance inputs that will not load down the driving signal, even if VDDO power is not applied to the chip. The other signals with back drive prevention are RST_N, COEX_OUT0, COEX_OUT1, COEX_IN, PCM_SYNC, PCM_CLK, PCM_OUT, PCM_IN, UART_RTS_N, UART_CTS_N, UART_RXD, UART_TXD, GPIO_0, GPIO_1, GPIO_2, GPIO_4, GPIO_7, CFG_SEL, and OTP_DIS.

All other IO signals must remain at VSS until VDDO is applied. Failing to do this can result in unreliable startup behavior.

When powered on, using REG_EN is the same as applying power to the CYW20710. The device does not have information about its state before being powered-down.

3.7 Adaptive Frequency Hopping

The CYW20710 supports host channel classification and dynamic channel classification Adaptive Frequency Hopping (AFH) schemes, as defined in the Bluetooth specification.

Host channel classification enables the host to set a predefined hopping map for the device to follow.

If dynamic channel classification is enabled, the device gathers link quality statistics on a channel-by-channel basis to facilitate channel assessment and channel map selection. To provide a more accurate frequency hop map, link quality is determined using both RF and baseband signal processing.

3.8 Collaborative Coexistence

The CYW20710 provides extensions and collaborative coexistence to the standard Bluetooth AFH for direct communication with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously in a single device. The device supports industry-standard coexistence signaling, including 802.15.2, and supports Cypress and third-party WLAN solutions.

Using a multitiered prioritization approach, relative priorities between data types and applications can be set. This approach maximizes the performance-WLAN data throughput vs. voice quality vs. link performance.

A PA shutdown pin is available to allow full external control of the RF output for other types of coexistence, such as WIMAX.

3.9 Serial Enhanced Coexistence Interface

The Serial Enhanced Coexistence Interface (Serial ECI or SECI) is a proprietary Cypress interface between Cypress WLAN devices and Bluetooth devices. It is an optional replacement to the legacy 3- or 4-wire coexistence feature, which is also available.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over SECI_IN and SECI_OUT.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronizaton upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

3.9.1 SECI Advantages

The advantages of the SECI over the legacy 3-wire coexistence interface are:

- Only two wires are required: SECI_IN and SECI_OUT.
- Up to 48-bits of coexistence data can be exchanged.

Previous Cypress stand-alone Bluetooth devices such as the CYW2070 supported only a 3-wire or 4-wire coexistence interface. Previous Cypress WLAN and Bluetooth combination devices such as the CYW4325, CYW4329, and CYW4330 support an internal parallel enhanced coexistence interface for more efficient WLAN and Bluetooth information exchange. The SECI allows enhanced coexistence information to be passed to a companion Cypress WLAN chip through a serial interface using fewer I/O than the 3-wire coexistence scheme.

The 48-bits of the SECI significantly enhance WLAN and Bluetooth coexistence by sharing such information as frequencies used and radio usage times. The exact contents of the SECI are Cypress confidential.

3.9.2 SECI I/O

The CYW20710 does not have dedicated SECI_IN or SECI_OUT pins, but the two pin functions can be mapped to the following digital I/O: the UART, GPIO, SPIM (or BSC), PCM, and COEX pins. Pin function mapping is controlled by the config file that is either stored in NVRAM or downloaded directly into on-chip RAM from the host.

4. Microprocessor Unit

The CYW20710 microprocessor unit runs software from the Link Control (LC) layer up to the Host Controller Interface (HCI). The microprocessor is based on the ARM7TDMIS 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The microprocessor also includes 384 KB of ROM memory for program storage and boot ROM, 112 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations, including automatic host transport selection from SPI or UART, with or without external NVRAM. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded from the host to the device through the SPI or UART transports, or using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

4.1 NVRAM Configuration Data and Storage

4.1.1 Serial Interface

The CYW20710 includes an SPI master controller that can be used to access serial flash memory. The SPI master contains an AHB slave interface, transmit and receive FIFOs, and the SPI core PHY logic. Data is transferred to and from the module by the system CPU. DMA operation is not supported.

The CYW20710 supports serial flash vendors Atmel, MXIC, and Numonyx. The most commonly used parts from two of these vendors are:

- AT25BCM512B, manufactured by Atmel
- MX25V512ZUI-20G, manufactured by MXIC

4.2 EEPROM

The CYW20710 includes a Broadcom® Serial Control (BSC) master interface. The BSC interface supports low-speed and fast mode devices and is compatible with I^2C slave devices. Multiple I^2C master devices and flexible wait state insertion by the master interface or slave devices are not supported. The CYW20710 provides 400 kHz, full speed clock support.

The BSC interface is programmed by the CPU to generate the following BSC transfer types on the bus:

- Read-only
- Write-only
- Combined read/write
- Combined write-read

NVRAM may contain configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data

4.3 External Reset

The CYW20710 has an integrated power-on reset circuit which completely resets all circuits to a known power on state. This action can also be driven by an external reset signal, which can be used to externally control the device, forcing it into a power-on reset state. The RST_N signal input is an active-low signal for all versions of the CYW20710. The CYW20710 requires an external pull-up resistor on the RST_N input. Alternatively, the RST_N input can be connected to REG_EN or driven directly by a host GPIO.

4.4 One-Time Programmable Memory

The CYW20710 includes a One-Time Programmable (OTP) memory, allowing manufacturing customization and avoiding the need for an on-board NVRAM.If customization is not required, then the OTP does not need to be programmed. Whether the OTP is programmed or not, it is disabled after the boot process completes to save power.

The OTP size is 128 bytes.

The OTP is designed to store a minimal amount of information. Aside from OTP data, most user configuration information will be downloaded into RAM after the CYW20710 boots up and is ready for host transport communication. The OTP contents are limited to:

- Parameters required prior to downloading user configuration to RAM.
- Parameters unique to a customer design.

4.4.1 Contents

The following are typical parameters programmed into the OTP memory:

- BD_ADDR
- Software license key
- Output power calibration
- Frequency trimming
- Initial status LED drive configuration

The OTP contents also include a static error correction table to improve yield during the programming process as well as forward error correction codes to eliminate any long-term reliability problems. The OTP contents associated with error correction are not visible by customers.

4.4.2 Programming

OTP memory programming takes place through a combination of Cypress software integrated with the manufacturing test software and code embedded in CYW20710 firmware.

Programming the OTP requires a 3.3V supply. The OTP programming supply comes from the VDDO pin. The OTP power supply can be as low as 1.8V in order to read the OTP contents. OTP_DIS is brought out to a pin on the WLBGA package but not on the FPBGA package, and is internally pulled low. If the OTP_DIS pin is left floating or externally pulled low, then the OTP will be enabled. if the OTP_DIS pins is externally pulled high, then the OTP will be disabled.

5. Peripheral Transport Unit

This section discusses the PCM, UART, and SPI peripheral interfaces. The CYW20710 has a 1040 byte transmit and receive fifo, which is large enough to hold the entire payload of the largest EDR BT packet (3-DH5).

5.1 PCM Interface

The CYW20710 PCM interface can connect to linear PCM codec devices in master or slave mode. In master mode, the device generates the PCM_BCLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface as inputs to the device.

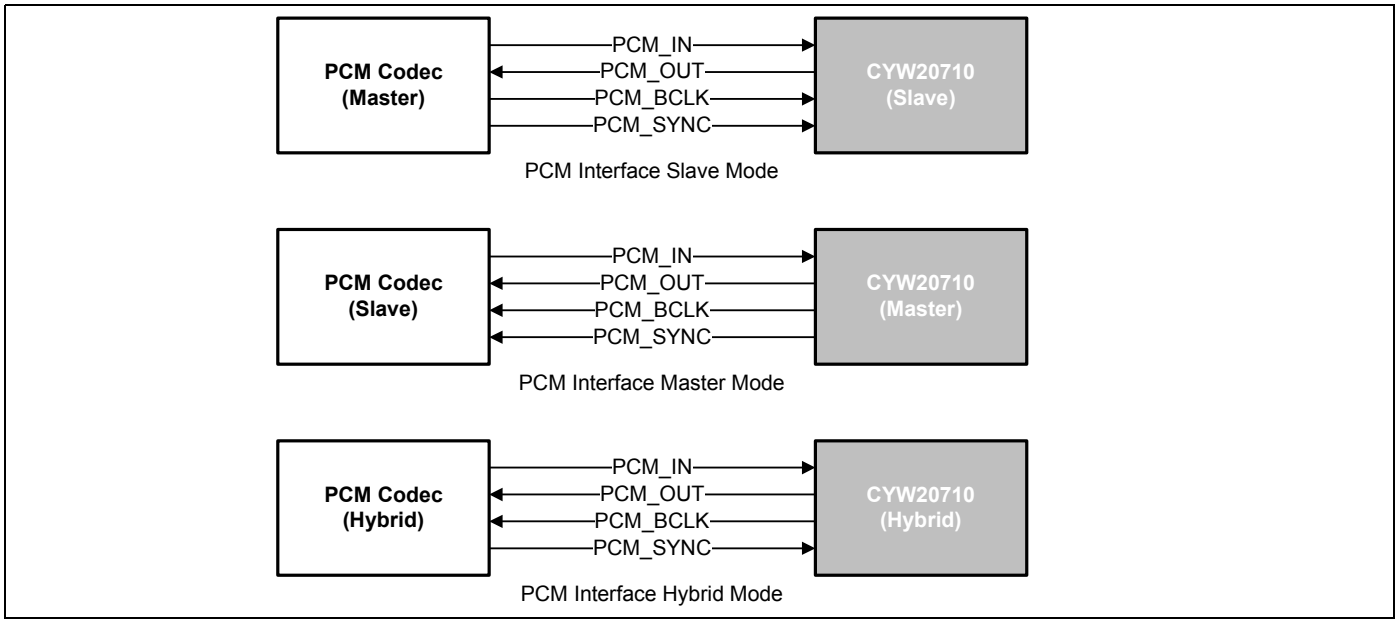
The device supports up to three SCO or eSCO channels through the PCM interface and each channel can be independently mapped to any available slot in a frame.

The host can adjust the PCM interface configuration using vendor-specific HCI commands or it can be setup in the configuration file.

5.1.1 System Diagram

Figure 5 shows options for connecting the device to a PCM codec device as a master or a slave.

Figure 5. PCM Interface with Linear PCM Codec



5.1.2 Slot Mapping

The device supports up to three simultaneous, full-duplex SCO or eSCO channels. These channels are time-multiplexed onto the PCM interface using a time slotting scheme based on the audio sampling rate, as described in Table 3.

Table 3. PCM Interface Time Slotting Scheme

Audio Sample Rate	Time Slotting Scheme
8 kHz	The number of slots depends on the selected interface rate, as follows: **Interface rate** **Slot** 128 1 256 2 512 4 1024 8 2048 16
16 kHz	The number of slots depends on the selected interface rate, as follows: **Interface rate** **Slot** 256 1 512 2 1024 4 2048 8

Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tri-states its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tri-states its output after the falling edge of the PCM clock during the last bit of the slot.

5.1.3 Wideband Speech

The CYW20710 provides support for Wideband Speech (WBS) in two ways:

- Transparent mode The host encodes WBS packets and the encoded packets are transferred over the PCM bus for SCO or eSCO voice connections. In Transparent mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate.
- On-chip SmartAudio® technologyThe CYW20710 can perform Subband-Codec (SBC) encoding and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

5.1.4 Frame Synchronization

The device supports both short and long frame synchronization types in both master and slave configurations. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate (which is a single bit period in width) and synchronized to the rising edge of the bit clock. The PCM slave expects PCM_SYNC to be high on the falling edge of the bit clock and the first bit of the first slot to start at the next rising edge of the clock. In the long frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate. However, the duration is 3-bit periods and the pulse starts coincident with the first bit of the first slot.

5.1.5 Data Formatting

The device can be configured to generate and accept several different data formats. The device uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits is configurable to support various data formats on the PCM interface. The remaining three bits are ignored on the input, and may be filled with zeros, ones, a sign bit, or a programmed value on the output. The default format is 13-bit two's complement data, left justified, and clocked most significant bit first.

5.2 HCI Transport Detection Configuration

The CYW20710 supports the following interface types for the HCI transport from the host:

- UART (H4 and H5)
- SPI

Only one host interface can be active at a time. The firmware performs a transport detect function at boot-time to determine which host is the active transport. It can auto-detect the UART interface, but the SPI interface must be selected by strapping the SCL pin to 0.

The complete algorithm is summarized as follows:

1. Determine if SCL is pulled low. If it is, select SPI as HCI host transport.
2. Determine if any local NVRAM contains a valid configuration file. If it does and a transport configuration entry is present, select the active transport according to entry, and then exit the transport detection routine.
3. Look for CTS_N = 0 on the UART interface. If it is present, select UART.
4. Repeat Step 3 until transport is determined.

5.3 UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate can be selected via a vendor-specific UART HCI command. The interface supports Bluetooth UART HCI (H4) specifications. The default baud rate for H4 is 115.2 Kbaud.

The following baud rates are supported:

9600	115200	2000000
14400	230400	3000000
19200	460800	3250000
28800	921600	3692000
38400	1444444	4000000
57600	1500000	

Normally, the UART baud rate is set by a configuration record downloaded after reset or by automatic baud rate detection. The host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is provided through a vendor-specific command.

The CYW20710 UART operates with the host UART correctly, provided the combined baud rate error of the two devices is within ±2%.

5.3.1 HCI 3-Wire Transport (UART H5)

The CYW20710 supports H5 UART transport for serial UART communications. H5 reduces the number of signal lines required by eliminating CTS and RTS, when compared to H4. In addition, in-band sleep signaling is supported over the same interface so that the 4-wire UART and the 2-wire sleep signaling interface can be reduced to a 2-wire UART interface, saving four IOs on the host.

H5 requires the use of an external LPO. CTS must be pulled low.

5.4 SPI

The CYW20710 supports a slave SPI HCI transport with an input clock range of up to 16 MHz. Higher clock rates may be possible. The physical interface between the SPI master and the CYW20710 consists of the four SPI signals (SPI_CSB, SPI_CLK, SPI_SI, and SPI_SO) and one interrupt signal (SPI_INT). The CYW20710 can be configured to accept active-low or active-high polarity on the SPI_CSB chip select signal. It can also be configured to drive an active-low or active-high SPI_INT interrupt signal. Bit ordering on the SPI_SI and SPI_SO data lines can be configured as either little-endian or big-endian. Additionally, proprietary sleep mode, half-duplex handshaking is implemented between the SPI master and the CYW20710.

SPI_INT is required to negotiate the start of a transaction. The SPI interface does not require flow control in the middle of a payload. The FIFO is large enough to handle the largest packet size. Only the SPI master can stop the flow of bytes on the data lines, since it controls SPI_CSB and SPI_CLK. Flow control should be implemented in higher layer protocols.

6. Frequency References

The CYW20710 uses two different frequency references for normal and low-power operational modes. An external crystal or frequency reference driven by a Temperature Compensated Crystal Oscillator (TCXO) signal is used to generate the radio frequencies and normal operation clocking. Either an external 32.768 kHz or fully integrated internal Low-Power Oscillator (LPO) is used for low-power mode timing.

6.1 Crystal Interface and Clock Generation

The CYW20710 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing, enabling it to operate from any of a multitude of frequency sources. The source can be external, such as a TCXO, or a crystal interfaced directly to the device.

The default frequency reference setting is for a 20 MHz crystal or TCXO. The signal characteristics for the crystal interface are listed in Table 4.

Table 4. Crystal Interface Signal Characteristics

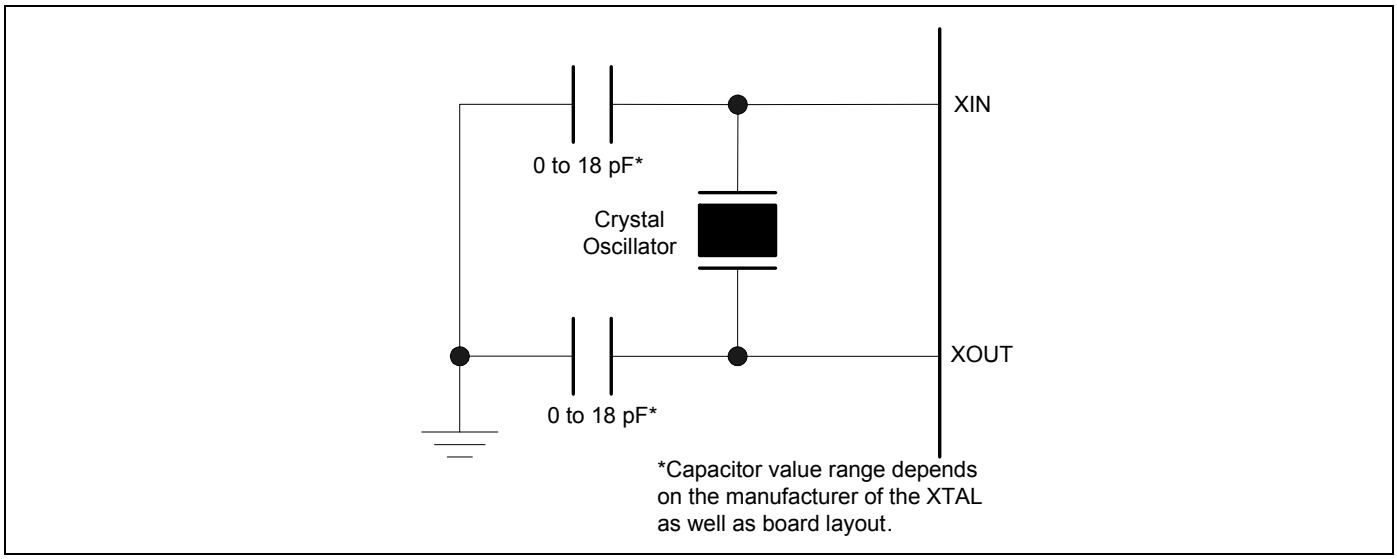
Parameter	Crystal	External Frequency Reference	Units
Acceptable frequencies	12–52 MHz in 2 ppm[1] steps	12–52 MHz in 2 ppm[1] steps	–
Crystal load capacitance	12 (typical)	N/A	pF
ESR	60 (max)	–	Ω
Power dissipation	200 (max)	–	µW
Input signal amplitude	N/A	400 to 2000 2000 to 3300 (requires a 10 pF DC blocking capacitor to attenuate the signal)	mVp-p
Signal type	N/A	Square-wave or sine-wave	–
Input impedance	N/A	≥ 1 ≤ 2	MΩ pF
Phase noise @ 1 kHz @ 10 kHz @ 100 kHz @ 1 MHz	N/A N/A N/A N/A N/A	– < –120[2] < –131[2] < –136[2] < –136[2]	– dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Auto-detection frequencies when using external LPO[3]	12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 33.6, 37.4, and 38.4	12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 33.6, 37.4, and 38.4	MHz
Tolerance without frequency trimming[4]	±20	±20	ppm
Initial frequency tolerance trimming range	±50	±50	ppm

1. The frequency step size is approximately 80 Hz resolution.
2. With a 26 MHz reference clock. For a 13 MHz clock, subtract 6 dB. For a 52 MHz clock, add 6 dB.
3. Auto-detection of the frequency requires the crystal or external frequency reference to have less than ±50 ppm of variation and also requires an external LPO frequency which has less than ±250 ppm of variation at the time of detection.
4. AT-Cut crystal or TXCO recommended.

6.2 Crystal Oscillator

The CYW20710 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 6.

Figure 6. Recommended Oscillator Configuration

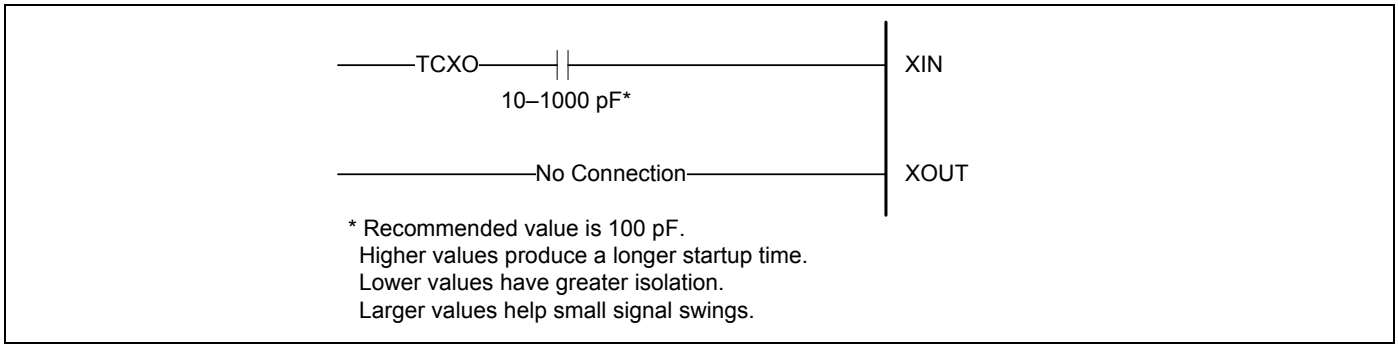


6.3 External Frequency Reference

An external frequency reference generated by a TCXO signal that may be directly connected to the crystal input pin on the CYW20710, as shown in Figure 7. The external frequency reference input is designed to not change loading on the TCXO when the CYW20710 is powered up or powered down.

When using the CYW20710 with the TXCO OR gate option, GPIO 6 must be driven active high or active low. Excessive leakage current results if GPIO6 is allowed to float.

Figure 7. Recommended TCXO Connection



6.3.1 TCXO Clock Request Support

If the application utilizes an external TCXO as a clock reference, the CYW20710 provides a clock request output to allow the system to power off the TCXO when not in use. Optionally, some packages support a TCXO OR function that allows a clock request in the system to be combined with the CYW20710 clock request output, without requiring an extra component on the board.

Clock Request Output

The CLK_REQ signal on the GPIO_5 lead is asserted whenever the CYW20710 is in the Awake state. It is deasserted when in Sleep state. When the CYW20710 is sleeping, it uses an LPO clock (external or internal) as the timing reference.

The TM0 lead controls the polarity of the CLK_REQ output on GPIO_5 as follows:

TM0 = 0 CLK_REQ is active low TM0 = 1 CLK_REQ is active high

If the clock request feature is not desired, GPIO_5 can be configured for other functions.

TCXO OR Option

The CYW20710 has an optional feature that allows the application to perform a logical OR function on a system TCXO clock request signal and the CYW20710 clock request to form one clock request output to the TCXO device. This logical OR function is embedded in the pad ring so that it is available at any time, as long as the pad ring is receiving a VDDO supply. The function works even if the CYW20710's digital core is sleeping or completely powered off.

To use this feature, the TCXO_MODE lead must be tied high. In this mode, the GPIO_6 lead functions as the external clock request input. Without TCXO_MODE asserted, GPIO_5 functions as the clock request output (based only on the internal clock requirements of the CYW20710) and the state of GPIO_6 is ignored.

As mentioned earlier, the TM0 lead controls the polarity of the CLK_REQ output on GPIO_5. However, it assumes that GPIO_6 input polarity is already consistent with the desired polarity on GPIO_5/CLK_REQ. Therefore, when TM0 is 1 for an active high output, the function is a simple OR between the external GPIO_6 and the internal clock request state. However, when TM0 is 0 for an active low output, the logic inverts the internal clock request signal and performs an AND between it and the GPIO_6 input. Even though it is using an OR gate, it still provides a logical AND on the two clock request states.

Since the logic assumes that it is also active low (similar to GPIO_5 output), it does not invert the GPIO_6 input first. Table 5 shows the truth table.

Table 5. Truth Table

GPIO_6 CLK_REQ_IN	Internal Clock Request State (0 = sleep)	TM0 (0 = active low output)	GPIO_5 CLK_REQ
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	0
0	0	1	0
0	1	1	1
1	0	1	1
1	1	1	1

Package Options and TCXO Mode

Only a few package options bring out TM0 to balls, allowing the application to configure them. In most packages, these pins are already configured.

Table 6 lists available package options.

Table 6. Package Options

Part Number	Package Description	TM0
CYW20710A1KUFBXG	50-ball FPBGA, optimized for cell phone applications	Brought to ball
CYW20710A1KUBXG	42-ball WLBGA	1

6.4 Frequency Selection

Any frequency within the range specified for the crystal and TCXO reference can be used. These frequencies include standard handset reference frequencies (12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 33.6, 37.4, and 38.4 MHz) and any frequency between these reference frequencies, as desired by the system designer. Since bit timing is derived from the reference frequency, the CYW20710 must have the reference frequency set correctly in order for the UART and PCM interfaces to function properly.

The CYW20710 reference frequency can be set in one of three ways.

- Use the default 20 MHz frequency
- Designate the reference frequency in external NVRAM
- Auto-detect the standard handset reference frequencies using an external LPO clock

The CYW20710 is set to a default frequency of 20 MHz at the factory. For a typical design using a crystal, it is recommended that the default frequency be used, since this simplifies the design by removing the need for either external NVRAM or external LPO clock.

If the application requires a frequency other than the default, the value can be stored in an external NVRAM. Programming the reference frequency in NVRAM provides the maximum flexibility in the selection of the reference frequency, since any frequency within the specified range for crystal and external frequency reference can be used. During power-on reset (POR), the device downloads the parameter settings stored in NVRAM, which can be programmed to include the reference frequency and frequency trim values. Typically, this is how a PC Bluetooth application is configured.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the CYW20710 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for auto-frequency detection to work properly, the CYW20710 must have a valid and stable 32.768 kHz external LPO clock present during POR. This eliminates the need for NVRAM in applications where the external LPO clock is available and an external NVRAM is typically not used.

6.5 Frequency Trimming

The CYW20710 uses a fractional-N synthesizer to digitally fine-tune the frequency reference input to within ±2 ppm tuning accuracy. This trimming function can be applied to either the crystal or an external frequency source such as a TCXO. Unlike the typical crystal-trimming methods used, the CYW20710 changes the frequency using a fully digital implementation and is much more stable and unaffected by crystal characteristics or temperature. Input impedance and loading characteristics remain unchanged on the TCXO or crystal during the trimming process and are unaffected by process and temperature variations.

The option to use or not use frequency trimming is based on the system designer's cost trade-off between bill-of-materials (BOM) cost of the crystal and the added manufacturing cost associated with frequency trimming. The frequency trimming value can either be stored in the host and written to the CYW20710 as a vendor-specific HCI command or stored in NVRAM and subsequently recalled during POR.

Frequency trimming is not a substitute for the poor use of tuning capacitors at an crystal oscillator (XTAL). Occasionally, trimming can help alleviate hardware changes.

6.6 LPO Clock Interface

The LPO clock is the second frequency reference that the CYW20710 uses to provide low-power mode timing for park, hold, and sniff. The LPO clock can be provided to the device externally, from a 32.768 kHz source or the CYW20710 can operate using the internal LPO clock.

The LPO can be internally driven from the main clock. However, sleep current will be impacted.

The accuracy of the internal LPO limits the maximum park, hold, and sniff intervals.

Table 7. External LPO Signal Requirements

Parameter	External LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Input signal amplitude	200 to 3600	mVp-p
Signal type	Square-wave or sine-wave	–
Input impedance (when power is applied or power is off)	>100 <5	kΩ pF

7. Pin-Out and Signal Descriptions

7.1 Pin Descriptions

Table 8. CYW20710 Signal Descriptions

Signal	FPBGA 50-Ball	WLBGA 42-Bump	I/O	Power Domain	Description
Radio					
RES	G4	D6	O	VDD_RF	External calibration resistor, 15 kΩ @ 1%
RFP	D1	C7	I/O	VDD_RF	RF I/O antenna port
XIN	G2	F5	I	VDD_RF	Crystal or reference input
XOUT	G3	E5	O	VDD_RF	Crystal oscillator output
Analog					
LPO_IN	A4	B4	I	VDDRF	External LPO input
Voltage Regulators					
REG_EN	B2	B5	I	VDDO	HV LDO and main enable
VBAT	A3	A5	I	N/A	HV LDO input
VREGHV	A2	A6	I/O	N/A	HV LDO output: main LDO input
VREG	A1	A7	O	N/A	Main LDO output
Straps					
RST_N	B4	C5	I	VDDO	Active-low reset input
TM0	C4	–	I	VDDO	Clock request polarity select
TM1	–	–	I	VDDO	Internally connected to ground
TM2	F3	C6	I	VDDO	Reserved: connect to ground.
Digital I/O					
GPIO_0	B5	C3	I/O	VDDO	GPIO/BT_WAKE
GPIO_1	B3	B3	I/O	VDDO	GPIO/HOST_WAKE
GPIO_2	–	–	I/O	VDDO	GPIO
GPIO_3	–	–	I/O	VDDO	GPIO/LINK_IND **Note:** Can be configured for active high or low as well as open drain.
GPIO_4	–	–	I/O	VDDO	GPIO
GPIO_5	E6	F4	I/O	VDDO	GPIO/CLK_REQ TCXO-OR Function Out available on some packages. See Section 11.“Ordering Information”.
GPIO_6	E3	D5	I/O	VDDO	GPIO TCXO-OR Function In available on some packages. See Section 11.“Ordering Information”.
GPIO_7	B7	–	I/O	VDDO	DETATCH/CARD_DETECT
UART_RXD	D8	D2	I/O	VDDO	UART receive data
UART_TXD	C8	C2	I/O	VDDO	UART transmit data
UART_RTS_N	D7	F2	I/O	VDDO	UART request to send output
UART_CTS_N	E8	E3	I/O	VDDO	UART clear to send input
SCL	F7	E1	I/O	VDDO	I^2C clock
SDA	E7	D1	I/O	VDDO	I^2C data

Table 8. CYW20710 Signal Descriptions (Cont.)

Signal	FPBGA 50-Ball	WLBGA 42-Bump	I/O	Power Domain	Description
SPIM_CLK	A8	C1	I/O	VDDO	Serial flash SPI clock
SPIM_CS_N	C7	E2	I/O	VDDO	Serial flash active-low chip select
PCM_IN	F6	D4	I/O	VDDO	PCM/I2S data input
PCM_OUT	G6	E4	I/O	VDDO	PCM/I2S data output
PCM_CLK	F4	C4	I/O	VDDO	PCM/I2S clock
PCM_SYNC	F5	A4	I/O	VDDO	PCM sync/I2S word select
COEX_IN	B6	–	I/O	VDDO	Coexistence input
COEX_OUT0	E4	–	I/O	VDDO	Coexistence output
COEX_OUT1	E5	–	I/O	VDDO	Coexistence output
OTP_DIS	–	A2	I/O	VDDO	OTP disable pin. By default, leave this pin floating.
Supplies					
VDDIF	B1	–	I	N/A	Radio IF PLL supply
VDDTF	C1	B7	I	N/A	Radio PA supply
VDDLNA	E1	–	I	N/A	Radio LNA supply
VDDRF	F1	E7	I	N/A	Radio supply
VDDPX	G1	F7	I	N/A	Radio RF PLL supply
VDDC	A5	A3	I	N/A	Core logic supply
VDDC	B8	F1	I	N/A	Core logic supply
VDDC	F8	–	I	N/A	Core logic supply
VDDO	G5	D3	I	N/A	Digital I/O supply voltage
VDDO	A6	–	I	N/A	Digital I/O supply voltage
VDDO	G8	–	I	N/A	Digital I/O supply voltage
NC	–	B1	I	N/A	No connect
VSS	C2	D7	–	N/A	Ground
VSS	D2	B6	–	N/A	Ground
VSS	F2	E6	–	N/A	Ground
VSS	D3	F6	–	N/A	Ground
VSS	C6	F3	–	N/A	Ground
VSS	A7	A1	–	N/A	Ground
VSS	G7	–	–	N/A	Ground
VSS	–	B2	–	N/A	Ground

8. Ball Grid Arrays

Figure 8 shows the top view of the 50-ball 4.5 x 4 x 0.6 mm (FPBGA).

Figure 8. 50-Ball 4.5 x 4 x 0.6 mm (FPBGA) Array

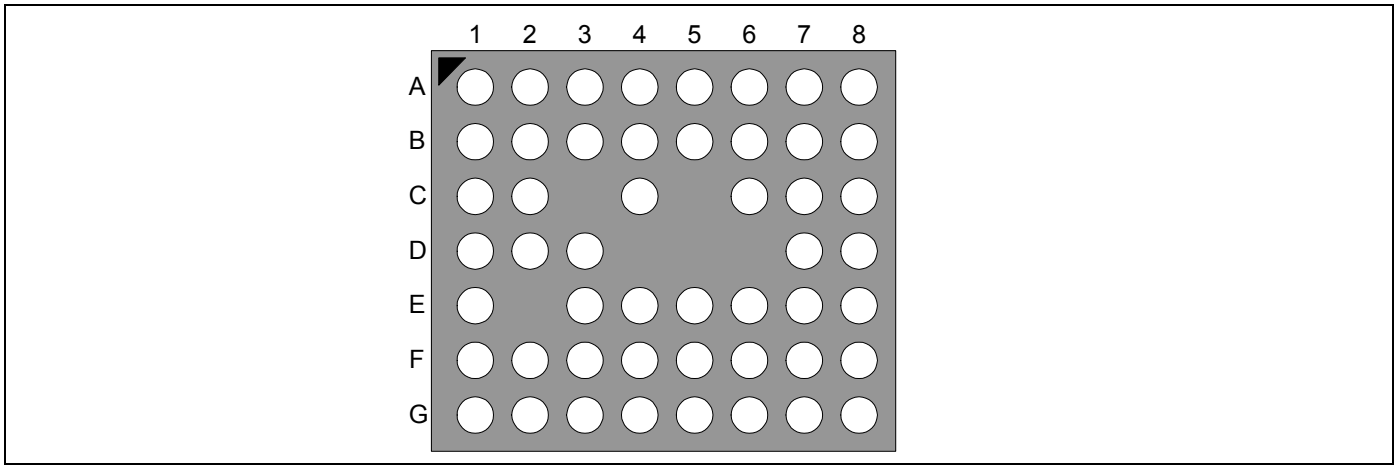


Table 9. Ball-Out for the 50-Ball CYW20710A1KUFBXG

	1	2	3	4	5	6	7	8
A	VREG	VREGHV	VBAT	LPO_IN	VDDC	VDDO	VSS	SPIM_CLK
B	VDDIF	REG_EN	GPIO_1	RST_N	GPIO_0	COEX_IN	GPIO_7	VDDC
C	VDDTF	VSS	–	TM0	–	VSS	SPIM_CS_N	UART_TXD
D	RFP	VSS	VSS	–	–	–	UART_RTS_N	UART_RXD
E	VDDLNA	–	GPIO6	COEX_OUT0	COEX_OUT1	GPIO_5	SDA	UART_CTS_N
F	VDDRF	VSS	TM2	PCM_CLK	PCM_SYNC	PCM_IN	SCL	VDDC
G	VDDPX	XIN	XOUT	RES	VDDO	PCM_OUT	VSS	VDDO

Figure 9 shows the top view of the 42-bump, 2.97 x 2.46 x 0.5 mm array.

Figure 9. 42-Bump 2.97 x 2.46 x 0.5 mm Array (Top View)

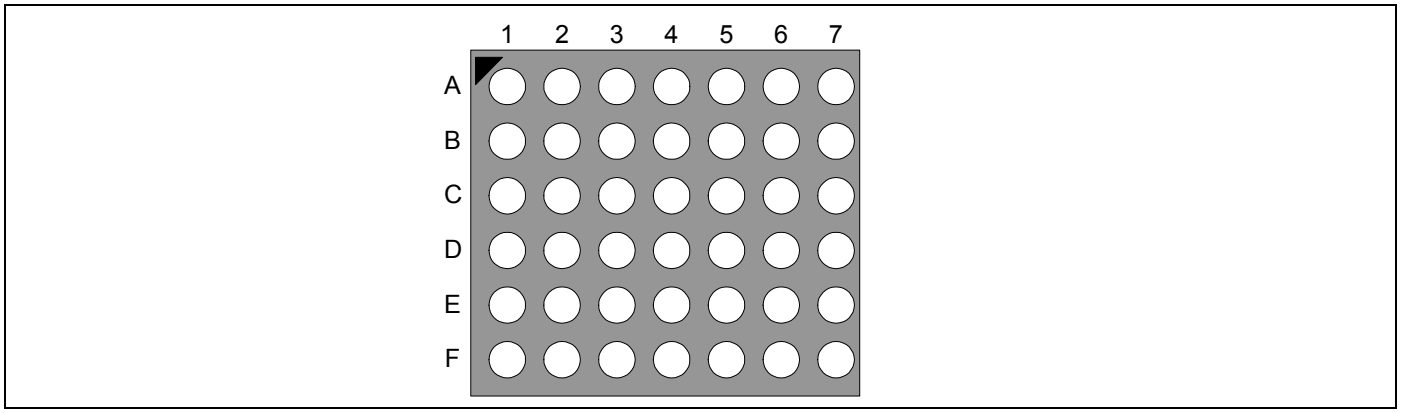


Table 10. Ball-Out for the 42-Bump CYW20710A1KUBXG

	1	2	3	4	5	6	7
A	VSS	OTP_DIS	VDDC	PCM_SYNC	VBAT	VREGHV	VREG
B	N/C	VSS	GPIO_1	LPO_IN	REG_EN	VSS	VDDTF
C	SPIM_CLK	UART_TXD	GPIO_0	PCM_CLK	RST_N	TM2	RFP
D	SDA	UART_RXD	VDDO	PCM_IN	GPIO_6	RES	VSS
E	SCL	SPIM_CS_N	UART_CTS_N	PCM_OUT	XOUT	VSS	VDDRF
F	VDDC	UART_RTS_N	VSS	GPIO_5	XIN	VSS	VDDPX

9. Electrical Characteristics

Note: All voltages listed in Table 11 are referenced to V_{DD}.

Table 11. Absolute Maximum Ratings

Rating	Signal\Parameter	Value	Unit
DC supply voltage for RF	VDD_RF[1]	1.32	V
DC supply voltage for core	VDDC	1.32	V
DC supply voltage for I/O	VDDO[2]	3.6	V
DC supply voltage for PA	VDDTF	3.3	V
Maximum voltage on input or output pins	VIMAX	VDDO + 0.3	V
Minimum voltage on input or output pins	VIMIN	VSS – 0.3	V
Storage temperature	TSTG	–40 to 125	°C

1. VDD_RF collectively refers to the VDDIF, VDDLNA, VDDPX, and VDDRF RF power supplies.
2. If VDDO is not applied, voltage should never be applied to any digital I/O pins (I/O pins should never be driven or pulled high). The list of digital I/O pins includes the following (these pins are listed in Section 7.“Pin-Out and Signal Descriptions” with VDDO shown as their power domain):
   GPIO[3], GPIO[5], GPIO[6]
   SCL, SDA
   N_MODE
   SPIM_CS_N, SPIM_CLK

Table 12. Power Supply

Parameter	Symbol	Minimum	Typical	Maximum	Unit
DC supply voltage for RF	VDD_RF [1]	1.159	1.22	1.281	V
DC supply noise for RF, from 100 kHz to 1 MHz	VDD_RF [2]	–	–	150	µV rms
DC supply voltage for core	VDDC	1.159	1.22	1.281	V
DC supply voltage for I/O	VDDO	1.7	–	3.6	V
DC supply	VDDTF [3]	1.12	–	3.3	V

1. VDD_RF collectively refers to the VDDIF, VDDLNA, VDDPX, VDDLNA, VDDRF RF power supplies.
2. Overall performance defined using integrated regulation.
3. VDDTF for Class 2 must be connected to VREG (main LDO output). VDDTF for Class 1 must be connected to VREGHV (HV LDO output) or an external voltage source. Refer to the Cypress compatibility guide for configuration details. VDDTF requires a capacitor to ground. The value of the capacitor must be tuned to ensure optimal RF RX sensitivity. The typical capacitor value is 10 pF for both packages. The value may depend on board layout.

Table 13. High-Voltage Regulator (HV LDO) Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	2.3	–	5.5	V
Output voltage	1.8	–	3.3	V
Max current load	–	–	95	mA
Load capacitance	1	–	10	µF
Load capacitor ESR	0.01	–	2	Ω
PSRR	20	–	40	dB
Turn-on time (C_{load} = 2.2 µF)	–	–	200	µs
Dropout voltage	–	–	200	mV

Table 14. Main Regulator (Main LDO) Electrical Specifications

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	1.63	–	3.63	V
Output voltage	1.159	1.22	1.281	V
Load current	–	–	60	mA
Load capacitance	1	–	2.2	µF
ESR	0.1	–	0.5	Ω
Turn-on time	–	–	300	µs
PSRR	15	–	–	dB
Dropout voltage	–	–	200	mV

Note: By default, the drive strength settings specified in Table 15 are for 3.3V. To achieve the required drive strength for a VDDIO of 2.5V or 1.8V, contact a Cypress technical support representative (see "Technical Support" for contact information).

Table 15. Digital I/O Characteristics

Characteristics	Symbol	Minimum	Typical	Maximum	Unit
Input low voltage (VDDO = 3.3V)	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3.3V)	V_{IH}	2.0	–	–	V
Input low voltage (VDDO = 1.8V)	V_{IL}	–	–	0.6	V
Input high voltage (VDDO = 1.8V)	V_{IH}	1.1	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	VDDO – 0.4V	–	–	V
Input low current	I_{IL}	–	–	1.0	µA
Input high current	I_{IH}	–	–	1.0	µA
Output low current (VDDO = 3.3V, V_{OL} = 0.4V)	I_{OL}	–	–	3.0	mA
Output high current (VDDO = 3.3V, V_{OH} = 2.9V)	I_{OH}	–	–	3.0	mA
Output low current (VDDO = 1.8V, V_{OL} = 0.4V)	I_{OL}	–	–	3.0	mA
Output high current (VDDO = 1.8V, V_{OH} = 1.4V)	I_{OH}	–	–	3.0	mA
Input capacitance	C_{IN}	–	–	0.4	pF

Table 16. Pad I/O Characteristics[1]

I/O Pad Characteristics		
Pad Name	**Pull-Up/Pull-Down**	**Fail-Safe**
COEX_OUT0	Y	Y
COEX_OUT1	Y	Y
COEX_IN	Y	Y
PCM_CLK	Y	Y
PCM_OUT	Y	Y
PCM_IN	Y	Y
PCM_SYNC	Y	Y
UART_RTS_N	Y	Y
UART_CTS_N	Y	Y
UART_RXD	Y	Y
UART_TXD	Y	Y
GPIO_0	Y	Y
GPIO_1	Y	Y
GPIO_2	Y	Y
GPIO_4	Y	Y
GPIO_7	Y	Y
RST_N	N/A	Y
OTP_DIS	Y	N

1. All digital I/O internal pull-up or pull-down values are around 60 kΩ.

Table 17. Current Consumption—Class 1(10 dBm)

Operational Mode	Conditions	Typical	Units
Receive (1 Mbps)	Current level during receive of a basic rate packet	31	mA
Transmit (1 Mbps)	Current level during transmit of a basic rate packet, GFSK output power = 10 dBm	65	mA
Receive (EDR)	Current level during receive of a 2 or 3 Mbps rate packet	32	mA
Transmit (EDR)	Current level during transmit of a 2 or 3 Mbps rate packet, GFSK output power = 10 dBm	59	mA
DM1/DH1	Average current during basic rate max throughput connection which includes only this packet type.	45	mA
DM3/DH3	Average current during basic rate max throughput connection which includes only this packet type.	46	mA
DM5/DH5	Average current during max basic rate throughput connection which includes only this packet type.	48	mA
HV1	Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.	38	mA
HV2	Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.	23	mA
HV3	Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.	17	mA
HCI only active	Average current when waiting for HCI command UART or SPI transports.	4.8	mA
Sleep	UART transport active, external LPO clock available.	55	µA
Sleep, HV Reg Bypass	UART transport active, external LPO clock available, HV LDO disabled and in bypass mode.	45	µA
Inquiry Scan (1.28 sec)	Periodic scan rate is 1.28 sec.	350	µA
Page Scan (R1)	Periodic scan rate is R1 (1.28 sec).	350	µA
Inquiry Scan + Page Scan (R1)	Both inquiry and page scans are interlaced together at 1.28 sec periodic scan rate.	630	µA
Sniff master (500 ms)	Attempt and timeout parameters set to 4. Quality connection which rarely requires more than minimum packet exchange.	175	µA
Sniff slave (500 ms)	Attempt and timeout parameters set to 4. Quality connection which rarely requires more than minimum packet exchange. Sniff master follows optimal sniff protocol of CYW20710 master.	160	µA
Sniff (500 ms) + Inquiry/ Page Scan (R1)	Same conditions as Sniff master and Page Scan (R1). Scan maybe either Inquiry Scan or Page Scan at 1.28 sec periodic scan rate.	455	µA
Sniff (500ms) + Inquiry Scan + Page Scan (R1)	Same conditions as Sniff master and Inquiry Scan + Page Scan.	760	µA

Table 18. Current Consumption—Class 2 (2 dBm)

Operational Mode	Conditions	Typical	Unit
Receive (1 Mbps)	Current level during receive of a basic rate packet	31	mA
Transmit (1 Mbps)	Current level during transmit of a basic rate packet, GFSK output power = 2 dBm	44	mA
Receive (EDR)	Current level during receive of a 2 or 3 Mbps rate packet	32	mA
Transmit (EDR)	Current level during transmit of a 2 or 3 Mbps rate packet, GFSK output power = 2 dBm	41	mA
DM1/DH1	Average current during basic rate max throughput connection, which includes only this packet type.	35	mA
DM3/DH3	Average current during basic rate max throughput connection, which includes only this packet type.	36	mA
DM5/DH5	Average current during max basic rate throughput connection, which includes only this packet type.	37	mA
HV1	Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.	28	mA
HV2	Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.	17	mA
HV3	Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.	13	mA
HCI only active	Average current when waiting for HCI command UART or SPI transports.	4.8	mA
Sleep	UART transport active, external LPO clock available.	55	µA
Sleep, HV Reg Bypass	UART transport active, external LPO clock available, HV LDO disabled and in bypass mode.	45	µA
Inquiry Scan (1.28 sec)	Periodic scan rate is 1.28 sec.	350	µA
Page Scan (R1)	Periodic scan rate is R1 (1.28 sec).	350	µA
Inquiry Scan + Page Scan (R1)	Both inquiry and page scans are interlaced together at 1.28 sec periodic scan rate.	630	µA
Sniff master (500 ms)	Attempt and timeout parameters set to 4. Quality connection which rarely requires more than minimum packet exchange.	145	µA
Sniff slave (500 ms)	Attempt and timeout parameters set to 4. Quality connection which rarely requires more than minimum packet exchange. Sniff master follows optimal sniff protocol of CYW20710 master.	135	µA
Sniff (500 ms) + Inquiry/Page Scan (R1)	Same conditions as Sniff master and Page Scan (R1). Scan can be either Inquiry Scan or Page Scan at 1.28 sec periodic scan rate.	425	µA
Sniff (500 ms) + Inquiry Scan + Page Scan (R1)	Same conditions as Sniff master and Inquiry Scan + Page Scan.	730	µA

Table 19. Operating Conditions

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Temperature	Commercial	–30.0	–	85	°C
Power supply	RF, Core	1.14	1.22	1.32	V
PA supply (VDDTF)	–	1.14	2.9	3.3	V

9.1 RF Specifications

Table 20. Receiver RF Specifications[1, 2]

Parameter	Conditions	Minimum	Typical [3]	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity [4]	GFSK, 0.1% BER, 1 Mbps, FPBGA package	–	–89[5]	–85	dBm
	GFSK, 0.1% BER, 1 Mbps, WLBGA package	–	–88[5]	–84	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–91[5]	–85	dBm
	8-DPSK, 0.01% BER, 3 Mbps FPBGA package	–	–86[5]	–81	dBm
	8-DPSK, 0.01% BER, 3 Mbps, WLBGA package	–	–85[5]	–80	dBm
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Maximum input	π/4-DQPSK, 8-DPSK, 2/3 Mbps	–	–	–20	dBm
Interference Performance					
C/I cochannel	GFSK, 0.1% BER	–	–	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20.0	dB
C/I cochannel	π/4-DQPSK, 0.1% BER	–	–	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	–	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–	–13.0	dB
Out-of-Band Blocking Performance (CW) [6]					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm

Table 20. Receiver RF Specifications[1, 2] (Cont.)

Parameter	Conditions	Minimum	Typical [3]	Maximum	Unit
Out-of-Band Blocking Performance, Modulated Interferer					
776–764 MHz	CDMA	–	–15	–	dBm
824–849 MHz	CDMA	–	–15	–	dBm
1850–1910 MHz	CDMA	–	–20	–	dBm
824–849 MHz	EDGE/GSM	–	–10	–	dBm
880–915 MHz	EDGE/GSM	–	–10	–	dBm
1710–1785 MHz	EDGE/GSM	–	–15	–	dBm
1850–1910 MHz	EDGE/GSM	–	–15	–	dBm
1850–1910 MHz	WCDMA	–	–25	–	dBm
1920–1980 MHz	WCDMA	–	–25	–	dBm
Intermodulation Performance [7]					
BT, Df = 5 MHz	–	–39.0	–	–	dBm
Spurious Emissions [8]					
30 MHz to 1 GHz	–	–	–	–57	dBm
1 GHz to 12.75 GHz	–	–	–	–47	dBm
65 MHz to 108 MHz	FM Rx	–	–145	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–145	–	dBm/Hz
851–894 MHz	CDMA	–	–145	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–145	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–145	–	dBm/Hz
1930–1990 MHz	PCS	–	–145	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–145	–	dBm/Hz

1. All specifications are single ended. Unused inputs are left open.
2. All specifications, except typical, are for industrial temperatures. For details see Table 19.
3. Typical operating conditions are 1.22V operating voltage and 25°C ambient temperature.
4. The receiver sensitivity is measured at BER of 0.1% on the device interface.
5. Measured with the dirty transmitter OFF. Typically, there is approximately 1 dB less in Rx sensitivity when the dirty transmitter is ON.
6. Meets this specification using front-end band pass filter.
7. f0 = -64 dBm Bluetooth-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 5.
8. Includes baseband radiated emissions.

Table 21. Transmitter RF Specifications [1, 2]

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class1: GFSK Tx power [3]	–	6.5	10	–	dBm
Class1: EDR Tx power [4]	–	4.5	8	–	dBm
Class 2: GFSK Tx power	–	–1.5	2	–	dBm
Power control step	–	2	4	6	dB
Modulation Accuracy					
p/4-DQPSK Frequency Stability	–	–10	–	10	kHz
p/4-DQPSK RMS DEVM	–	–	–	20	%
p/4-QPSK Peak DEVM	–	–	–	35	%
p/4-DQPSK 99% DEVM	–	–	–	30	%
8-DPSK frequency stability	–	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	–	13	%
8-DPSK Peak DEVM	–	–	–	25	%
8-DPSK 99% DEVM	–	–	–	20	%
In-Band Spurious Emissions					
+500 kHz	–	–	–	–20	dBc
1.0 MHz < |M – N| < 1.5 MHz	–	–	–	–26	dBc
1.5 MHz < |M – N| < 2.5 MHz	–	–	–	–20	dBm
|M – N| ≥ 2.5 MHz	–	–	–	–40	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [5]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 [5, 6]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
GPS Band Noise Emission (without a front-end band pass filter)					
1572.92 MHz to 1577.92 MHz	–	–	–150	–127	dBm/Hz
Out-of-Band Noise Emissions (without a front-end band pass filter)					
65 MHz to 108 MHz	FM Rx	–	–145	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–145	–	dBm/Hz
869 MHz to 960 MHz	CDMA	–	–145	–	dBm/Hz
925 MHz to 960 MHz	EDGE/GSM	–	–145	–	dBm/Hz
1805 MHz to 1880 MHz	EDGE/GSM	–	–145	–	dBm/Hz
1930 MHz to 1990 MHz	PCS	–	–145	–	dBm/Hz
2110 MHz to 2170 MHz	WCDMA	–	–145	–	dBm/Hz

1. All specifications are for industrial temperatures. For details, see Table 19.
2. All specifications are single-ended. Unused input are left open.
3. +10 dBm output for GFSK measured with VDDTF = 2.9 V.
4. +8 dBm output for EDR measured with VDDTF = 2.9 V.
5. Maximum value is the value required for Bluetooth qualification.
6. Meets this spec using a front-end bandpass filter.

9.2 Timing and AC Characteristics

In this section, use the numbers listed in the reference column to interpret the timing diagrams.

9.2.1 Startup Timing

There are two basic startup scenarios. In one scenario, the chip startup and firmware boot is held off while the RST_N pin is asserted. In the second scenario, the chip startup and firmware boot is directly triggered by the chip power-up. In this case, an internal power-on reset (POR) is held for a few ms, after which the chip commences startup.

The global reset signal in the CYW20710 is a logical OR (actually a wired AND, since the signals are active low) of the RST_N input and the internal POR signals. The last signal to be released determines the time at which the chip is released from reset. The POR is typically asserted for 3 ms after VDDC crosses the 0.8V threshold, but it may be as soon as 1.5 ms after this event.

After the chip is released from reset, both startup scenarios follow the same sequence, as follows:

1. After approximately 120 µs, the CLK_REQ (GPIO_5) signal is asserted.
2. The chip remains in sleep state for a minimum of 4.2 ms.
3. If present, the TCXO and LPO clocks must be oscillating by the end of the 4.2 ms period.

If a TCXO clock is not in the system, a crystal is assumed to be present at the XIN and XOUT pins. If an LPO clock is not used, the firmware will detect the absence of a clock at the LPO_IN lead and use the internal LPO clock instead.

Figure 10 and Figure 11 illustrate the two startup timing scenarios.

Figure 10. Startup Timing from RST_N

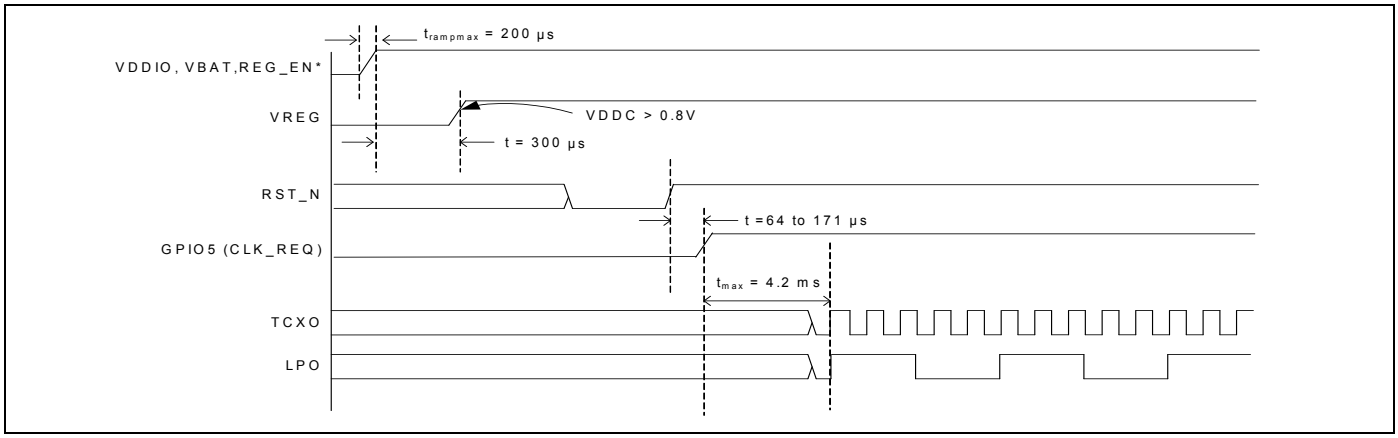
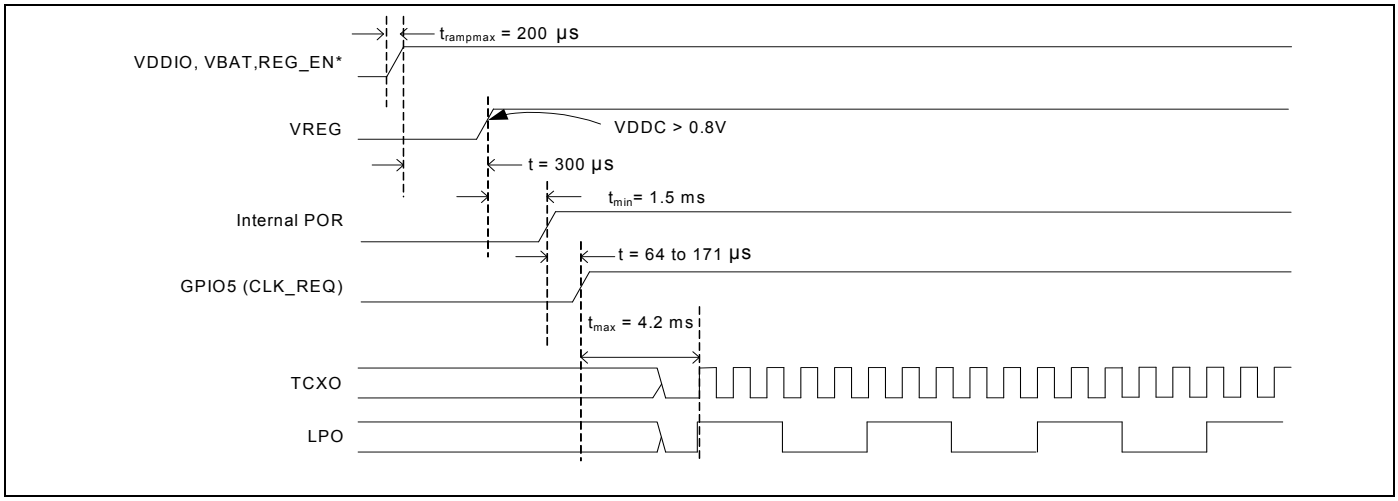


Figure 11. Startup Timing from Power-on Reset

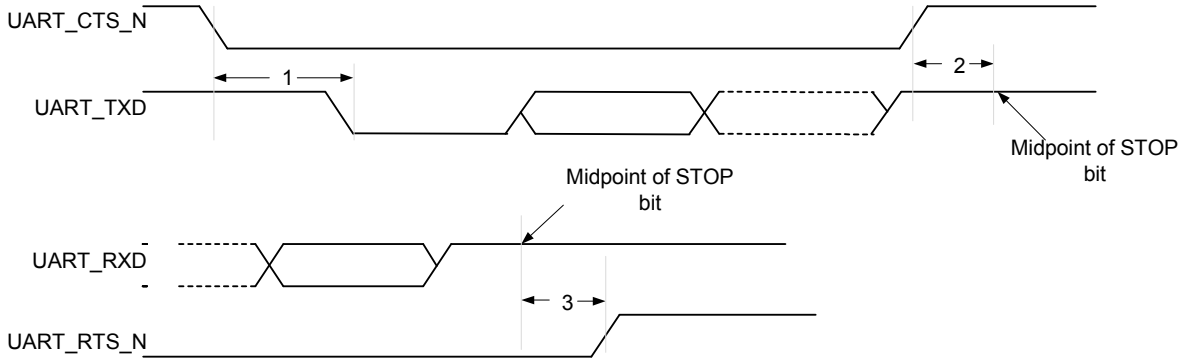


9.2.2 UART Timing

Table 22. UART Timing Specifications

Reference	Characteristics	Minimum	Maximum	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baudout cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baudout cycles

Figure 12. UART Timing



9.2.3 PCM Interface Timing

Table 23. PCM Interface Timing Specifications (Short Frame Synchronization, Master Mode)

Reference	Characteristics	Minimum	Maximum	Unit
1	PCM bit clock frequency	128	2048	kHz
2	PCM bit clock HIGH time	128	–	ns
3	PCM bit clock LOW time	209	–	ns
4	Delay from PCM_BCLK rising edge to PCM_SYNC high	–	50	ns
5	Delay from PCM_BCLK rising edge to PCM_SYNC low	–	50	ns
6	Delay from PCM_BCLK rising edge to data valid on PCM_OUT	–	50	ns
7	Setup time for PCM_IN before PCM_BCLK falling edge	50	–	ns
8	Hold time for PCM_IN after PCM_BCLK falling edge	10	–	ns
9	Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	–	50	ns

Figure 13. PCM Interface Timing (Short Frame Synchronization, Master Mode)

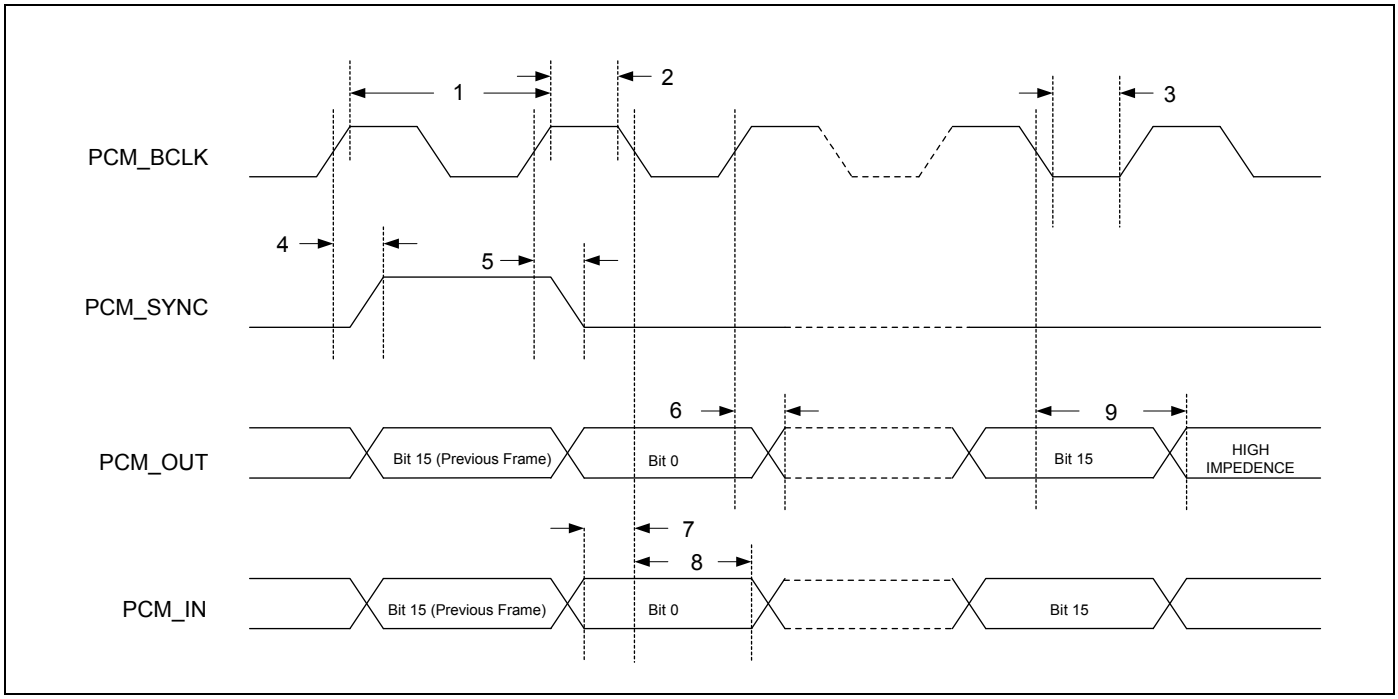


Table 24. PCM Interface Timing Specifications (Short Frame Synchronization, Slave Mode)

Reference	Characteristics	Minimum	Maximum	Unit
1	PCM bit clock frequency	128	2048	kHz
2	PCM bit clock HIGH time	209	–	ns
3	PCM bit clock LOW time	209	–	ns
4	Setup time for PCM_SYNC before falling edge of PCM_BCLK	50	–	ns
5	Hold time for PCM_SYNC after falling edge of PCM_BCLK	10	–	ns
6	Hold time of PCM_OUT after PCM_BCLK falling edge	–	175	ns
7	Setup time for PCM_IN before PCM_BCLK falling edge	50	–	ns
8	Hold time for PCM_IN after PCM_BCLK falling edge	10	–	ns
9	Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	–	100	ns

Figure 14. PCM Interface Timing (Short Frame Synchronization, Slave Mode)

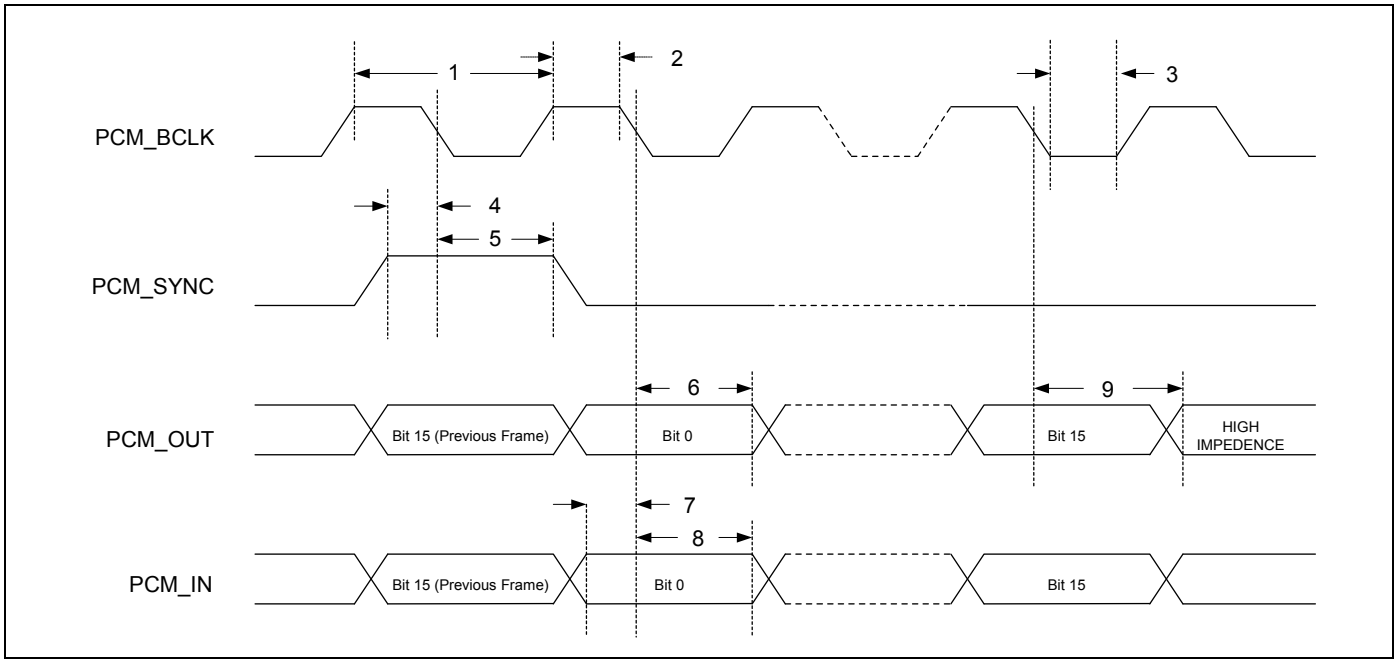


Table 25. PCM Interface Timing Specifications (Long Frame Synchronization, Master Mode)

Reference	Characteristics	Minimum	Maximum	Unit
1	PCM bit clock frequency	128	2048	kHz
2	PCM bit clock HIGH time	209	–	ns
3	PCM bit clock LOW time	209	–	ns
4	Delay from PCM_BCLK rising edge to PCM_SYNC HIGH during first bit time	–	50	ns
5	Delay from PCM_BCLK rising edge to PCM_SYNC LOW during third bit time	–	50	ns
6	Delay from PCM_BCLK rising edge to data valid on PCM_OUT	–	50	ns
7	Setup time for PCM_IN before PCM_BCLK falling edge	50	–	ns
8	Hold time for PCM_IN after PCM_BCLK falling edge	10	–	ns
9	Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	–	50	ns

Figure 15. PCM Interface Timing (Long Frame Synchronization, Master Mode)

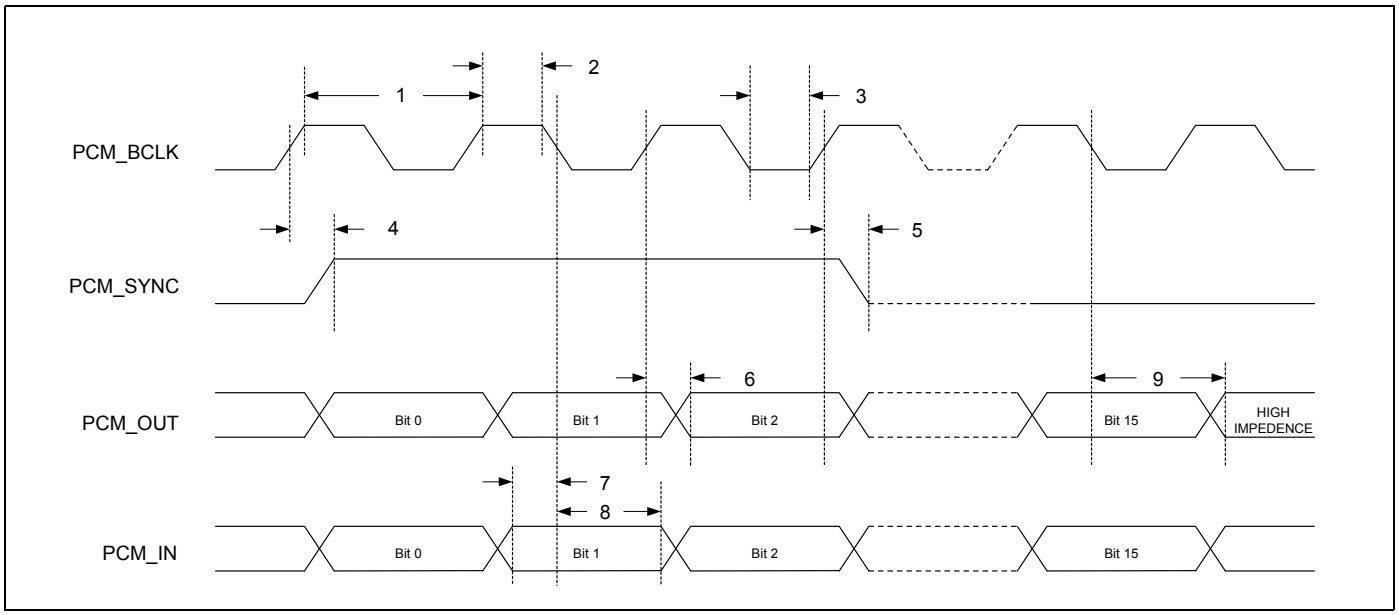
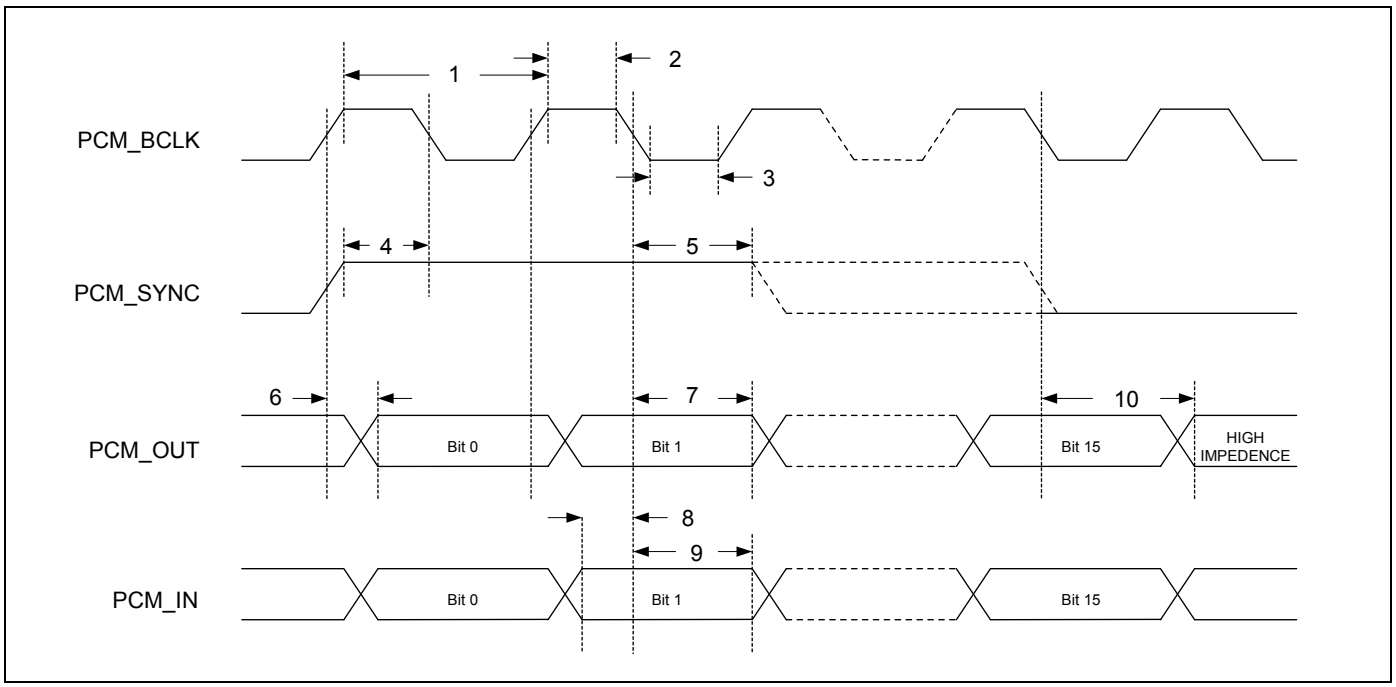


Table 26. PCM Interface Timing Specifications (Long Frame Synchronization, Slave Mode)

Reference	Characteristics	Minimum	Maximum	Unit
1	PCM bit clock frequency.	128	2048	kHz
2	PCM bit clock HIGH time.	209	–	ns
3	PCM bit clock LOW time.	209	–	ns
4	Setup time for PCM_SYNC before falling edge of PCM_BCLK during first bit time.	50	–	ns
5	Hold time for PCM_SYNC after falling edge of PCM_BCLK during second bit period. (PCM_SYNC may go low any time from second bit period to last bit period).	10	–	ns
6	Delay from rising edge of PCM_BCLK or PCM_SYNC (whichever is later) to data valid for first bit on PCM_OUT.	–	50	ns
7	Hold time of PCM_OUT after PCM_BCLK falling edge.	–	175	ns
8	Setup time for PCM_IN before PCM_BCLK falling edge.	50	–	ns
9	Hold time for PCM_IN after PCM_BCLK falling edge.	10	–	ns
10	Delay from falling edge of PCM_BCLK or PCM_SYNC (whichever is later) during last bit in slot to PCM_OUT becoming high impedance.	–	100	ns

Figure 16. PCM Interface Timing (Long Frame Synchronization, Slave Mode)



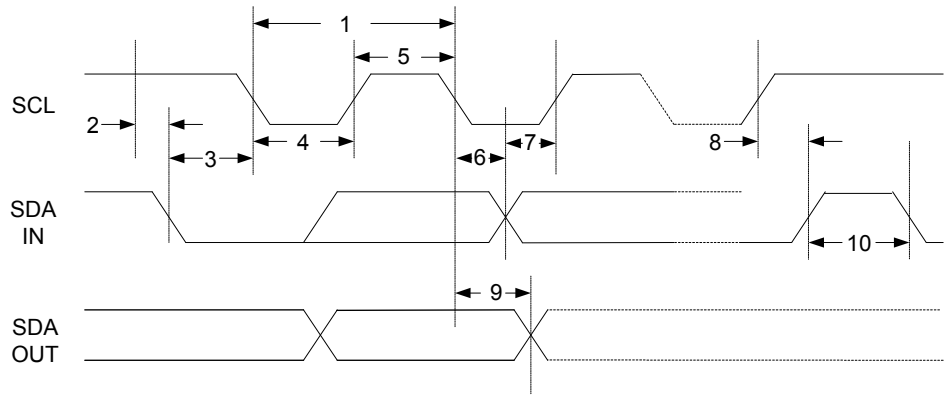
9.2.4 BSC Interface Timing

Table 27. BSC Interface Timing Specifications

Reference	Characteristics	Minimum	Maximum	Unit
1	Clock frequency	–	100 400 800 1000	kHz
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[1]	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[2]	650	–	ns

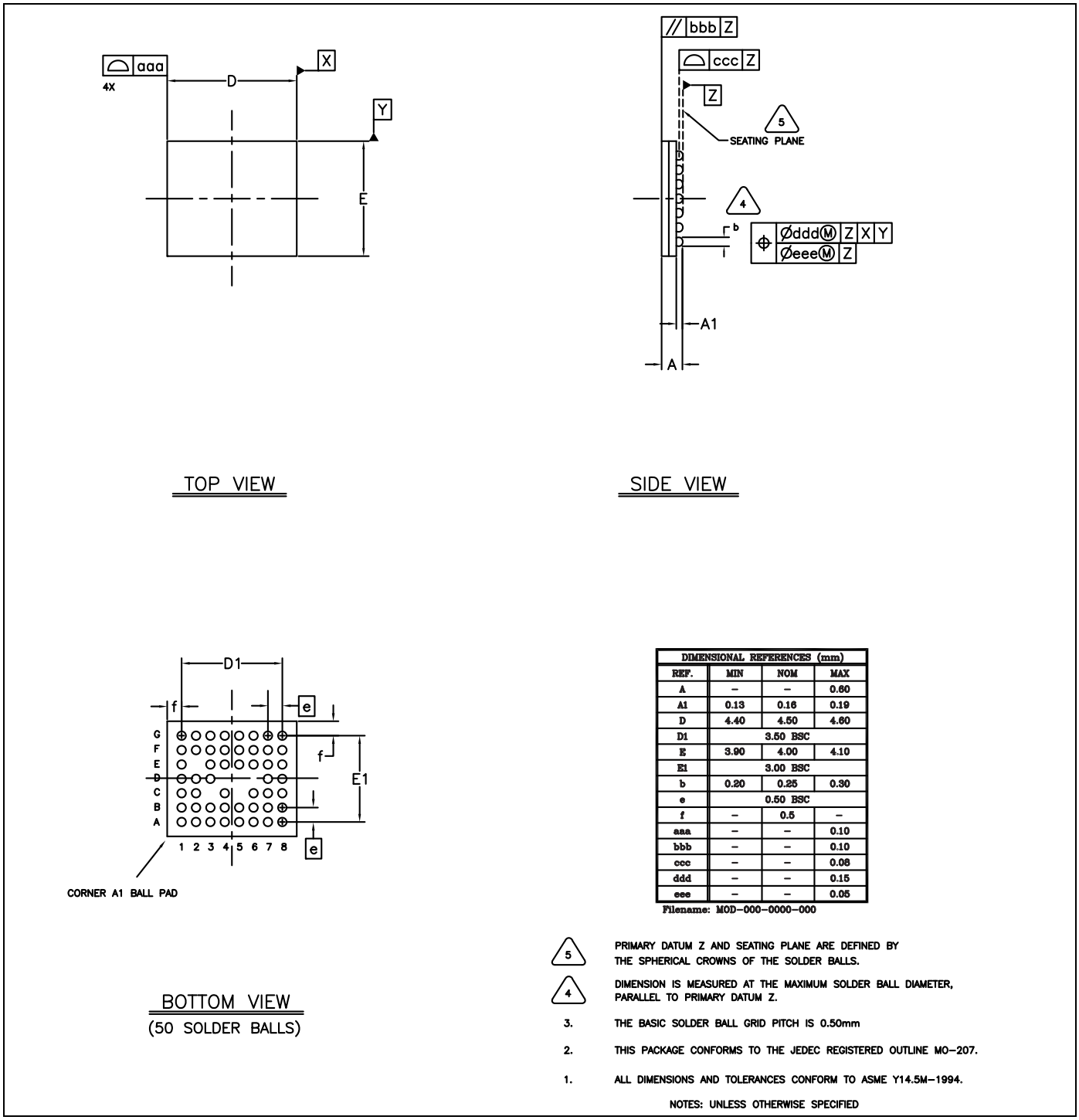
1. As a transmitter, 300 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions
2. Time that the cbus must be free before a new transaction can start.

Figure 17. BSC Interface Timing Diagram



10. Mechanical Information

Figure 18. CYW20710A1KUFBXG Mechanical Drawing



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.60
A1	0.13	0.16	0.19
D	4.40	4.50	4.60
D1		3.50 BSC	
E	3.90	4.00	4.10
E1		3.00 BSC	
b	0.20	0.25	0.30
e		0.50 BSC	
f	–	0.5	–
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.05

Filename: MOD–000–0000–000

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

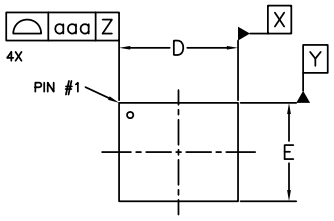
3. THE BASIC SOLDER BALL GRID PITCH IS 0.50mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–207.

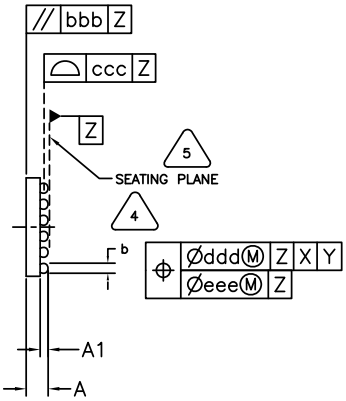
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

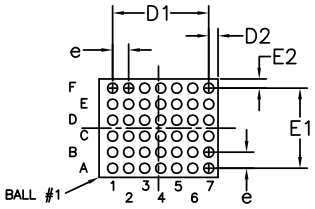
Figure 19. 42-Bump CYW20710A1KUBXG Mechanical Drawing



TOP VIEW



SIDE VIEW



BOTTOM VIEW
(42 SOLDER BALLS)

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.160	0.190	0.220
D	2.950	3.019	3.044
E	2.440	2.509	2.534
D1		2.400 REF.	
E1		2.000 REF.	
D2		0.255 REF.	
E2		0.255 REF.	
b	0.230	0.270	0.320
e		0.40 BSC	
f	–	–	–
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.03
ddd	–	–	0.15
eee	–	–	0.05

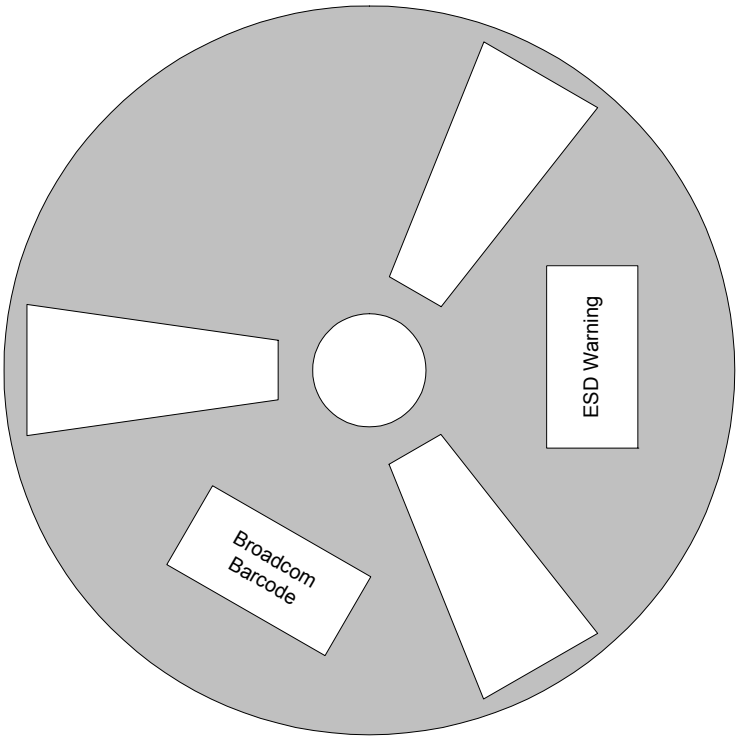
Filename: P-MOD-XXXX-000

5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.
3. THE BASIC SOLDER BALL PITCH IS 0.40mm
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

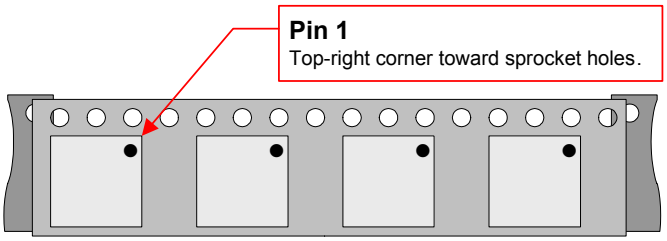
10.1 Tape, Reel, and Packing Specification

Figure 20. Reel, Labeling, and Packing Specification



Device Orientation/Mix Lot Number

Each reel may contain up to three lot numbers, independent of the date code. Individual lots must be labeled on the box, moisture barrier bag, and the reel.



Moisture Barrier Bag Contents/Label

Desiccant pouch (minimum 1)
Humidity indicator (minimum 1)
Reel (maximum 1)

11. Ordering Information

The following table lists available part numbers and describes differences in package type, available I/O, and functional configuration. See the referenced figures and tables for mechanical drawings and package I/O information.

All packages are rated from –30°C to +85°C.

Part Number	Package Type	Functional I/O Features	Strapped Configuration
CYW20710A1KUFBXG	Commercial 50-ball FPBGA, 4.5 mm x 4.0 mm x 0.6 mm. See Figure 18.	Dedicated Coex[1], more GPIO, TM0[2] Table 9	TCXO AND/OR mode enabled
CYW20710A1KUBXG	Commercial 42-bump WLBGA, 3.02 mm x 2.51 mm x 0.55 mm. See Figure 19.	Table 10	TCXO AND/OR mode enabled

1. All packages support coexistence features through the ability to re-purpose most digital I/O based on the desired user configuration. Package include balls coexistence functionality (default).
2. TM0 allows configuration of CLK_REQ output polarity.

12. Additional Information

12.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

12.2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (https://community.cypress.com/)

Document History Page

Document Title: CYW20710 Single-Chip Bluetooth® Transceiver and Baseband Processor Document Number: 002-14804				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	6/09/2010	20710-DS100-R Initial release
*A	-	-	6/23/2010	20710-DS100-R **Updated:** • "Programming". • "Frequency Selection" on page 37 by adding 24 MHz as a reference frequency. • Table 9: "Ball-Out for the 42-Bump CYW20710A0KUBXG".
*B	-	-	8/16/2010	20710-DS102-R **Updated:** • Table 10: "Absolute Maximum Voltages" • Table 11: "Power Supply" • Table 13: "Main Regulator (Main LDO) Electrical Specifications"
*C	-	-	2/16/2010	20710-DS103-R **Updated:** • Part numbers changed to CYW20710A1KUFBXG (50-ball FPBGA) and CYW20710A1KUBXG (42-ball WLBGA) throughout the document
*D	-	-	7/28/2011	20710-DS104-R **Updated:** • "Simultaneous UART Transport and Bridging" (removed) • Changed "UFBGA" to "FPBGA" throughout.
*E	-	-	10/17/2011	20710-DS105-R **Updated:** • Table 20: "Transmitter RF Specifications"
*F	-	-	12/16/2011	20710-DS107-R **Updated:** • Table 7: "CYW20710 Signal Descriptions" • Table 10: "Absolute Maximum Ratings" • Table 17: "Current Consumption — Class 2 (2 dBm)" • Table 18: "Operating Conditions" • Table 19: "Receiver RF Specifications"
*G	-	-	10/4/2013	20710-DS107-R • **Updated:** • "UART Interface" • "External Frequency Reference" • Table15. "Digital I/O Characteristics" • Figure 10. "Startup Timing from RST_N • Figure 11. "Startup Timing from Power-on Reset
*H	5484548	UTSV	11/25/2016	Added Cypress Part Numbering Scheme and Mapping Table on Page 1. Updated to Cypress template.
*I	5969756	AESATP12	11/17/2017	Updated logo and copyright.

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