PM5450 HyPHY-20Gflex

High-Capacity Single-Chip Multi-Rate/Multi-Protocol OTN Processor

Summary

The PM5450 HyPHY-20Gflex device represents Microchip's 2nd generation of OTN-enabled, high-capacity system-on-a-chip solutions for Multi-Service Provisioning Platforms (MSPPs), Wavelength Division Multi-plexing (WDM) Platforms, Reconfigurable Optical Add-Drop Multiplexers (ROADMs), Optical Transport Platforms (OTPs), Packet-OTPs and Optical Access Platforms. The HyPHY-20Gflex brings ODU0 and ODUflex capabilities to universal multi-rate, multiservice line, transponder and muxponder cards.

The HyPHY-20Gflex is pin-compatible to the PM5420 HyPHY 20G and delivers unprecedented single-chip scalability and feature integration to enable optimal footprint, power and cost efficiency. The HyPHY-20Gflex provides a rich set of framing, mapping and multiplexing resources for a variety of protocols, including OTN, SONET/SDH, Ethernet, Fibre Channel, ESCON, FICON and multi-rate bit transparent services such as video.

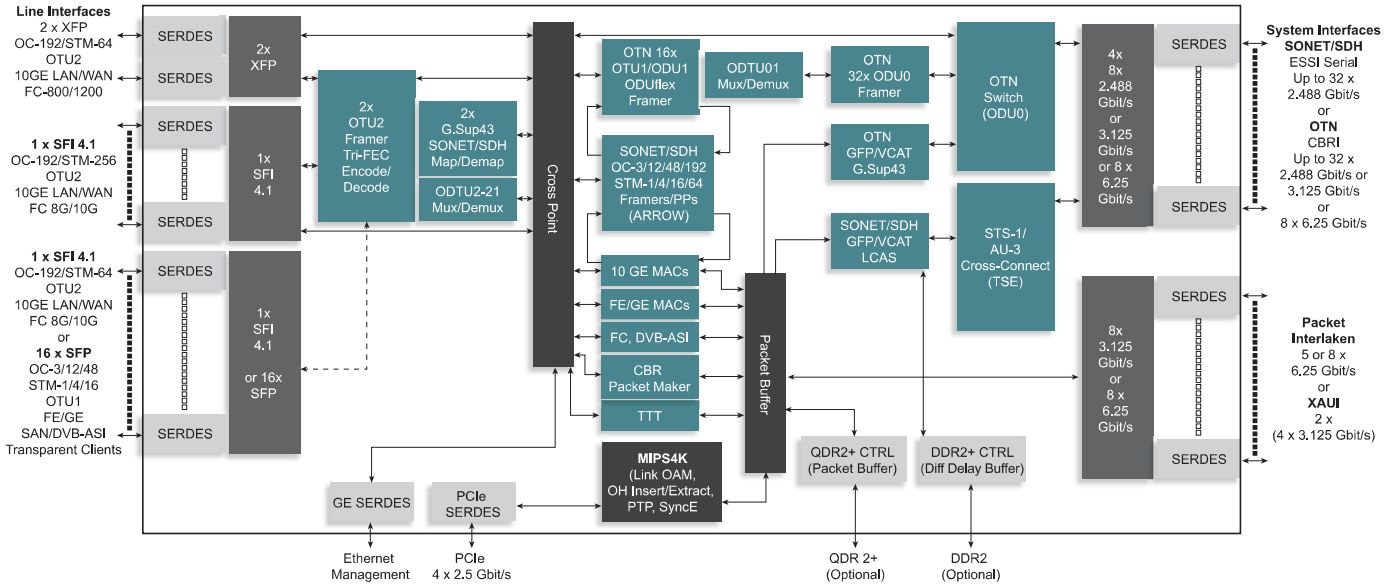
The HyPHY-20Gflex Adds Several Capabilities to the HyPHY Family

- Support for 32x ODU0 and 16x ODUflex
- G.709 compliant GMP mapping
- G.709 compliant mapping of FC-1200
- Full suite of Ethernet and SONET/SDH ingress and egress PMON
- Two stage ODUjk multiplexing
- 16x OTU1 support (8 more than HyPHY 20G)
- VLAN aggregation of GE traffic onto XAUI interface
- OIF compliant OTN over packet format header extensions

Benefits

- Carrier OPEX and CAPEX savings
  - Simplifies equipment deployment and network management by enabling hybrid TDM/packet platforms
  - Dramatically reduces cost of ownership by simplifying line card inventory management
- Unprecedented service delivery flexibility
  - Supports per-port configurable OTN, SONET/SDH, Ethernet, SAN and bit transparent client services
  - Rich suite of client service mappings into OTN & SONET/SDH
  - OTN Tri-FEC for maximum network interoperability
  - Enables full SNCP-base protection switching for meshed network topologies
- Processor-based Carrier Ethernet
  - Flexible implementations of Synchronous Ethernet, IEEE 1588 Precision Timing Protocol (PTP) and Ethernet Link OAM (IEEE 802.3ah)
- Optimized power and footprint for OEMs
  - Direct connect to SFP, SFP+ (limiting) and XFP modules for all rates with no external SERDES or PLL components required
  - All frequencies derived from a single 155.52 MHz reference clock
  - Single-chip solution for muxponders, transponders and optical access platforms
  - Glueless interconnect to many off-the-shelf NPs and fabrics

Block Diagram



Product Highlights

SFP Client Interfaces

- 16x multi-rate SERDES for direct connection to SFP optical transceivers, independently tunable from 16 Mbit/s to 5 Gbit/s
- Any-Service Any-Port configurability
  - OTU1 (up to 16)
  - OC-3/12/48 or STM-1/4/16
  - 100/1000 Mbps full-duplex Ethernet
  - Bit transparent clients, including, but not limited to DVB-ASI, SD-SDI, HD-SDI, DV6000, ISC, ISCIII and 2.5G/5G Infiniband
  - Fibre Channel FC-15, FC-25, FC-50, FC-100, FC-200, FC-400, FICON and ESCON
  - CPRI clients up to 4.9 Gbit/s

10G Client and WAN Interfaces

- 2x multi-rate SERDES for direct connection to XFP/SFP+ (limiting) modules, independently tunable from 8.5 Gbit/s to 11.32 Gbit/s
- 2x SFI 4.1 interface for chip-to-chip interconnect or for direct connection to MSA modules
- Any-Service Any-Port configurability
  - OTU2 (including overclocked rates up to 11.32 Gbit/s)
  - OC-192/STM-64
  - 10GE-LAN
  - 10GE-WAN
  - Fibre Channel (FC-800 and FC-1200)
  - CPRI 9.8304 Gbit/s client

SONET/SDH Subsystem (ARROW + TSE)

- Integration of field-proven CHESS SONET/SDH IP, reducing development cycles through reuse of CHESS software base
- SONET/SDH framing, overhead and high-order pointer processing
- Tandem connection monitoring
- Transport overhead transparency
- BLSR and MSSPRing protection switching with alarm processing, K-byte express, automatic payload configuration
- Non-blocking 100 Gbit/s STS-1/AU-3 cross-connect
- 50 Gbit/s of floating delay management to adapt between frame alignment domains
- TOH byte insertion and extraction
- Active and standby configuration memory page support permits new switch settings to be updated in one page while the TSE operates from the control settings of the other page

Fibre Channel Subsystem

- FICON, ESCON and Fibre Channel (FC-12, 25, 50, 100, 200, 400, 800)
- Performs 8B/10B Physical Coding Sub-layer (PCS) on a per-link basis with loss of signal and transmission error monitoring
- Per-link rate adaptation to bridge between local and transmit link timing domains
- FC-1200 is supported as a transparent client

Ethernet Subsystem

- Integrated IEEE 802.3 compliant media access controllers (MAC)
- Integrated 10 GE WAN Interface sublayer (WIS) framing and descrambling
- 4B/5B, 8B/10B and 64B/66B physical coding sub-layer (PCS) on a per link basis for FE, GE and 10GE respectively
- Lossless IEEE 802.3 local flow control; integrated packet buffers
- Comprehensive per-port Ethernet statistics
- Frame delineation and generation with configurable IPG, Preamble and CRC
- Transparent transmission of VLAN tagged Ethernet frames
- Frame sizes of 64 bytes to 9.6 Kbytes
- Dynamic programmable depth full-packet store-and-forward buffers for burst tolerance and rate adaptation
- Transmit and receive of IEEE 802.3ah Link OAM, LACP and Management VLAN messages
- Firmware-based (MIPS4K CPU), hardware assisted G.8261 Synchronous Ethernet and IEEE 1588v2 PTP Ethernet timing
- On-chip central packet buffer

OTN Subsystem

- Compatible with ITU-T G.709, ITU-T G.798 and ITU-T G.975
- Supports 32x ODU0 and 16x ODUflex(CBR) and ODUflex(GFP)
- Flexible OTU, ODU and OPU overhead/data processing and frame alignment
- Transmit and receive facility and terminal loop back configurations
- Two-stage ODU multiplexing
- Support for GMP multiplexing as well as 1.25G Timeslots
- Up to six levels of Tandem Connection Monitoring (TCM)
- Independent performance counters for the accumulation of BIP-8, BEI and other error conditions with optional interrupts
- O-E-O regeneration with adaptive clocking using Microchip's OTN Phase Signaling Algorithm (OPSA)

Forward Error Correction (FEC)

- Two instantiations of independently-configurable Tri-FEC for OTU2
  - Interoperable G.709 RS (255, 239) FEC with 6.2 dB coding gain at 10-15 BERout
  - Interoperable G.975.1 Annex I.4 Strong FEC (8.9 db gain at BERout = 10-15 @ 7% OH)
  - Interoperable G.975.1 Annex I.7 Strong FEC (8.4 db gain at BERout = 10-15 @ 7% OH)
- Comprehensive statistics for use in EDC tuning, limited amplifier tuning and performance monitoring

Client Mapping into OTN and SONET/SDH

- Maps a wide variety of protocols into OTN and SONET/SDH
- Encapsulates packet streams into ITU-T G.7041 GFP-F, GFP-T, HDLC, LAPS or PPP
- Inserts and extracts GFP client management frames (CMF) as well as LCP, NCP and BCP control frames
- OTN client mapping
  - AMP, BMP, and GMP as per G.709
  - TTT mode for mapping clients such as GE into ODU0
  - ODUflex(CBR) and ODUflex(GFP)
  - High-order (ODU1) virtual and contiguous concatenation performed according to G.709
  - Available OPTM for mapping/multiplexing of sub-ODU1 client data into OTN
  - GFP with extension headers for multiplexing of sub-ODU1 client data streams into ODUks or OPTM tributary slots
  - OPSA for rate encoding and adaptation of transparent client data streams over OTN
  - 10GE mapping into OTN compliant with ITU G.Sup43 6.1, 6.2, 7.1, 7.2 and 7.3
  - FC-1200 mapping as per G.709
- SONET/SDH client mapping
  - High-order (STS-1-Xv/VC-3-xv & STS-3c-Xv/VC-4-Xv) virtual and contiguous concatenation performed according to ITU-T G.707 and ANSI T1.105
  - Up to 64 SONET/SDH virtual concatenation groups (VCGs) supported
  - Hitless Link Capacity Adjustment Scheme (LCAS) according to ITU-TG.7042
  - Up to 128 ms of differential delay between VCG members

System Expansion Interfaces

- SONET/SDH
  - 4 x 8 x 2.488 Gbit/s ESSI serial links (up to 16 x working/16 x protect) supporting slicing and de-slicing for byte, nibble, di-bit, and bit modes
- OTN
  - 4 x 8 x lanes of CBRI links (up to 16 x working/16 x protect) configurable to 2.48832 Gbit/s or 3.125 Gbit/s
  - 1 x 8 lanes of CBRI links operating at 6.25 Gbit/s
  - Enables grooming of ODUk using off-the-shelf packet fabric
  - CBRI and ESSI can be configured to run simultaneously (in groups of eight links)
- Packet traffic
  - 1 Interlaken v1.1 interface configurable to 5 or 8 lanes at 6.25 Gbit/s
  - 2 x XAUI interfaces (2 x 4 lanes at 3.125 GHz), including support for VLAN aggregation
  - 2 x extended XAUI mode (2 x 4 lanes at 3.125 GHz) that adds format and flow-control channelization extensions to 802.3ae

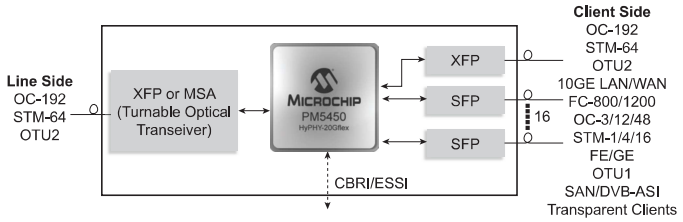
System Support Interfaces

- PCIe v1.1 (x1/x4) bus for microprocessor and OH access
- Two-Wire interface
- Optional DDR2 (required for STS1/STS3 rate VCAT)
- Optional QDR2+ (required for extended reach Ethernet applications)
- Dedicated Management Ethernet interface
- Standard IEEE 1149.6 compliant JTAG
- IRIG/1PPS interface for PTP synchronization
- OTN Multiframe interfaces for OTN frame synchronization

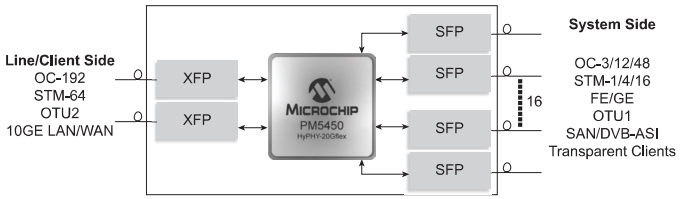
Applications

- Universal line cards for MSPPs and OTPs
- Single-chip optical access platforms
- Transponder, Muxponder and MSPP-on-a-wavelength cards for ROADMs
- Ported or portless packet/TDM interworking server cards
- Multi-Service aggregation cards for switches and routers
- WAN network cards for OLTs and DSLAMs

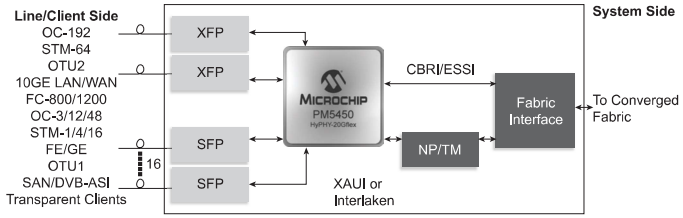
Muxponder/Transponder Card



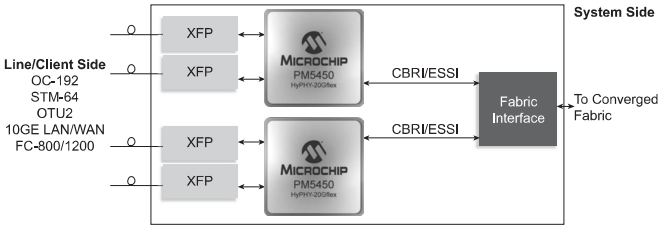
Optical Access Platform



Multi-Service Transport Line Card With L2+



XFP-based 40G Transport Line Card



For More Information

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