EVALUATION KIT AVAILABLE

MAX16928

Automotive TFT-LCD Power Supply with Boost Converter and Gate Voltage Regulators

General Description

The MAX16928 is a highly integrated power supply for automotive TFT-LCD applications. The device integrates one boost converter, one 1.8V/3.3V regulator controller, and two gate voltage regulators. The device comes in several versions to satisfy common automotive TFT-LCD power-supply requirements (see the *Ordering Information* table).

The boost converter uses spread-spectrum modulation to reduce peak interference and to optimize EMI performance.

The sequencing input (SEQ) allows flexible sequencing of the positive-gate and negative-gate voltage regulators. The power-good indicator (PGOOD) indicates a failure on any of the converters or regulator outputs. Integrated thermal shutdown circuitry protects the device from overheating.

The MAX16928 is available in a 20-pin TSSOP package with exposed pad and operates over the -40°C to +105°C temperature range.

Applications

Automotive Dashboards

Automotive Central Information Displays

Automotive Navigation Systems

Features

- **High-Power (Up to 6W) Boost Output Providing Up to 18V**
- **1.8V or 3.3V Regulator Provides 500mA with External npn Transistor**
- **One Positive-Gate Voltage Regulator Capable of Delivering 20mA at 28V**
- **One Negative-Gate Voltage Regulator**
- **High-Frequency 2.2MHz Operation**
- **Flexible Stand-Alone Sequencing**
- **True Shutdown™ Boost Converter**
- **Internal Soft-Start**
- **Overtemperature Shutdown**
- **-40°C to +105°C Operation**
- **AEC-Q100 Qualified**

***Ordering Information** appears at end of data sheet.*

***Typical Operating Circuit** appears at end of data sheet.*

*For related parts and recommended products to use with this part, refer to: **www.maximintegrated.com/MAX16928.related***

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-5991; Rev 2; 3/13

ABSOLUTE MAXIMUM RATINGS

INA, COMPV, FBP to GND ..... -0.3V to +6V
PGOOD to GND ..... -0.3V to +6V
CP, GH to GND ..... -0.3V to +31V
CP, GH to GND (V_{INA} = 3.3V) ..... -0.3V to +29V
LXP to GND ..... -0.3V to +20V
DRVN to GND ..... -25V to +0.3V
ENP, DR, FB, GATE, COMPI, FBGH, FBGL, REF, SEQ to GND ..... -0.3V to (V_{INA} + 0.3V)
GND to PGNDP ..... -0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 26.5mW/°C above +70°C) 2122mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 37.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{INA} = 5V, V_{GND} = V_{PGNDP} = 0V, T_A = T_J = -40°C to +105°C, typical values are at T_A = +25°C unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BOOST, POSITIVE (GH), NEGATIVE (GL), 1.8V/3.3V CONVERTERS						
INA Input Supply Range			3		5.5	V
INA Undervoltage Lockout Threshold		V_{INA} rising, hysteresis = 200mV, T_A = +25°C	2.5	2.7	2.9	V
INA Supply Current	I_{INA}	V_{FBP} = V_{FBGH} = 1.3V, V_{FBGL} = 0V, LXP not switching		1.5	2.0	mA
INA Shutdown Current	I_{SHDN}	V_{ENP} = 0V, T_A = +25°C		0.5		µA
Thermal Shutdown Temperature	T_{SHDN}	Temperature rising		+165		°C
Thermal Shutdown Hysteresis	T_H			15		°C
Duration to Trigger Fault Condition		V_{FBP}, V_{FBGH}, or V_{FBGL} below its threshold		238		ms
Autoretry Time				1.9		s
REFERENCE (REF)						
REF Output Voltage	V_{REF}	No output current	1.236	1.25	1.264	V
REF Load Regulation		0 < I_{REF} < 80µA, REF sourcing	-2		+2	%
REF Undervoltage Lockout Threshold		Rising edge, hysteresis = 200mV			1.165	V
OSCILLATOR						
Spread-Spectrum Factor	SSR	As a percentage of switching frequency, f_{SW}		±4		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{INA} = 5V, V_{GND} = V_{PGNDP} = 0V, T_A = T_J = -40°C to +105°C, typical values are at T_A = +25°C unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BOOST CONVERTER							
Switching Frequency	f_{SW}			1.98	2.20	2.42	MHz
Maximum Duty Cycle				82		93.5	%
LXP Current Limit	I_{LIM}	Duty cycle = 70%, C_{COMPI} = 220pF	Low boost current-limit option	0.625	0.78		A
			High boost current-limit option	1.25	1.56	1.87	
LXP On-Resistance	$R_{DS\_ON(LXP)}$	I_{LXP} = 200mA			110	250	mΩ
LXP Leakage Current	I_{LK_LXP}	V_{LXP} = 20V, T_A =+25°C			8.5	20	µA
Soft-Start Time		(Note 3)			30		ms
Output Voltage Range	V_{SH}			V_{INA}		18	V
FBP Regulation Voltage	V_{FBP}	V_{INA} = +3V to +5.5V, 0 < I_{LOAD} < full load	T_A = +25°C	0.985	1.0	1.015	V
			T_A = -40°C to +105°C	0.98	1.0	1.02	
PGOOD Threshold	V_{PG_FBP}	Measured at FBP		0.74	0.85	0.96	V
FBP Load Regulation		0 < I_{LOAD} < full load			-1		%
FBP Line Regulation		V_{INA} = +3V to +5.5V			0.1		%/V
FBP Input Bias Current		V_{FBP} = +1V, T_A = +25°C				±1	µA
FBP to COMPV Transconductance		ΔI = ±2.5µA at COMPV, T_A = +25°C			400		µS
POSITIVE-GATE VOLTAGE REGULATOR (GH)							
Output Voltage Range	V_{GH}	With external charge pump, T_A = +25°C (maximum V_{CP} = 29.5V)		5		29	V
CP Overvoltage Threshold		T_A = +25°C (Note 4)		29.5	30.5		V
FBGH Regulation Voltage	V_{FBGH}	I_{GH} = 1mA		0.96	1.0	1.034	V
PGOOD Threshold	V_{PG_FBGH}	Measured at FBGH		0.83	0.85	0.87	V
FBGH Load Regulation		I_{GH} = 0 to 20mA			2		%
FBGH Line Regulation		V_{CP} = 12V to 20V at V_{GH} = 10V, I_{GH} = 10mA			2		%
FBGH Input Bias Current		V_{FBGH} = 1V, T_A = +25°C				±1	µA
GH Output Current	I_{GH}	V_{CP} - V_{GH} = 2V		20			mA
GH Current Limit	I_{LIM_GH}			35	56		mA
GH Soft-Start Time					7.45		ms
NEGATIVE-GATE VOLTAGE REGULATOR (GL)							
Output Voltage Range	V_{DRVN}			-24		-2	V
FBGL Regulation Voltage	V_{FBGL}	I_{DRVN} = 100µA		0.212	0.242	0.271	V
PGOOD Threshold	V_{PG_FBGL}	Measured at FBGL		0.38	0.4	0.42	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{INA} = 5V, V_{GND} = V_{PGNDP} = 0V, T_A = T_J = -40°C to +105°C, typical values are at T_A = +25°C unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FBGL Input Bias Current		V_{FBGL} = +0.25V				±1	µA
DRVN Source Current		V_{FBGL} = +0.5V, V_{DRVN} = -10V		2			mA
DRVN Source Current Limit				2.5	4		mA
GL Soft-Start Time					7.45		ms
1.8V/3.3V REGULATOR CONTROLLER							
Output Voltage	V_{FB}	V_{DR} = V_{FB}	3.3V regulator option	3.18	3.3	3.38	V
			1.8V regulator option	1.746	1.8	1.854	
FB PGOOD Threshold	V_{PG_FB}	Measured at FB (Notes 4, 6)	3.3V regulator option, FB rising	2.4	2.57	2.7	V
			1.8V regulator option, FB rising	1.364	1.38	1.396	
FB Input Bias Current		V_{FB} = 1.8V			2.5		µA
		V_{FB} = 3.3V			4.5		
DR Drive Current		V_{FB} = 1.8V		4.5	6		mA
INPUT SERIES SWITCH CONTROL							
p-Channel FET GATE Sink Current		V_{GATE} = 0.5V		33	55	75	µA
GATE Voltage Threshold		Measured at GATE; below this voltage, the external p-channel FET is considered on			1.25		V
DIGITAL LOGIC							
ENP, SEQ Input Pulldown Resistor Value	R_{PD}				500		kΩ
ENP, SEQ Input-Voltage Low	V_{IL}					0.3 x V_{INA}	V
ENP, SEQ Input-Voltage High	V_{IH}			0.7 x V_{INA}			V
PGOOD Leakage Current	I_{LK_IN}	T_A = +25°C				±1	µA
PGOOD Output-Voltage Low	V_{OL}	2mA sink current, T_A = +25°C				0.4	V

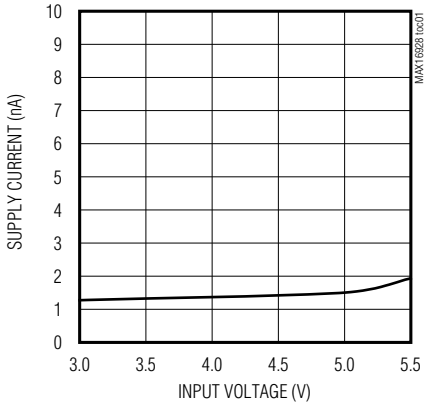
Note 2: Specifications over temperature are guaranteed by design and not production tested.
Note 3: 50% of the soft-start voltage time is due to the soft-start ramp and the other 50% is due to the settling of the output voltage.
Note 4: After the voltage at CP exceeds this overvoltage threshold, the entire circuit switches off and autoretry is started.
Note 5: Guaranteed by design; not production tested.
Note 6: FB power good is indicated by PGOOD. The condition V_{FB} < V_{PG_FB} does not shut down/restart the device.

Automotive TFT-LCD Power Supply with Boost Converter and Gate Voltage Regulators

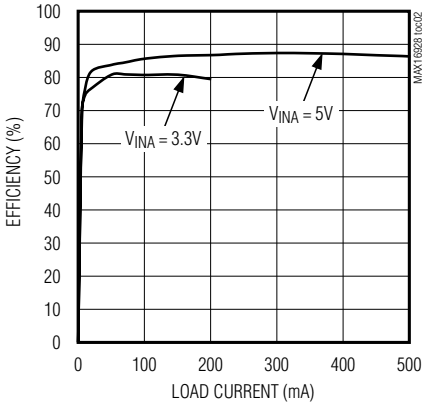
Typical Operating Characteristics

(V_{INA} = +5V, V_{SH} = +12V, V_{GH} = +18V, V_{GL} = -6V, V_{REG} = 3.3V, T_A = +25°C, unless otherwise noted.)

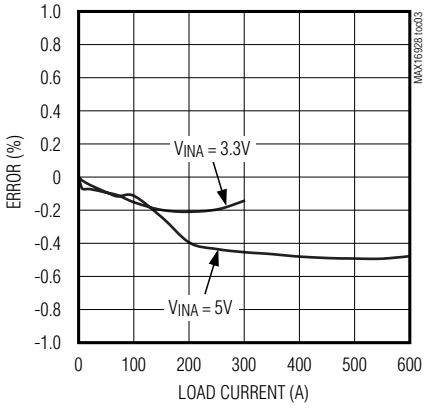
SHUTDOWN SUPPLY CURRENT



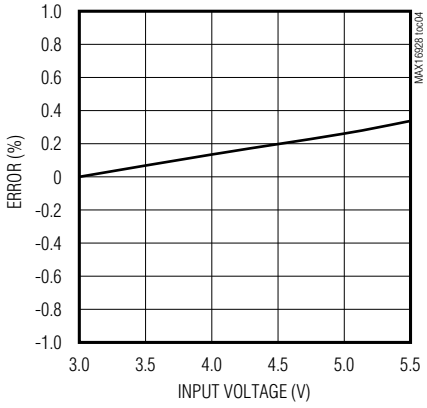
EFFICIENCY vs. LOAD CURRENT (BOOST)



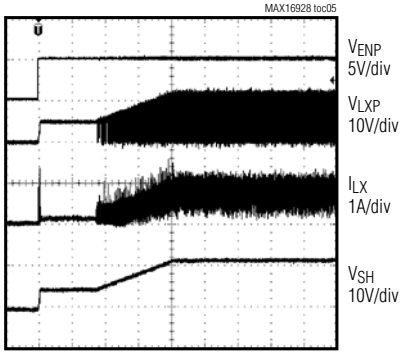
LOAD REGULATION (BOOST)



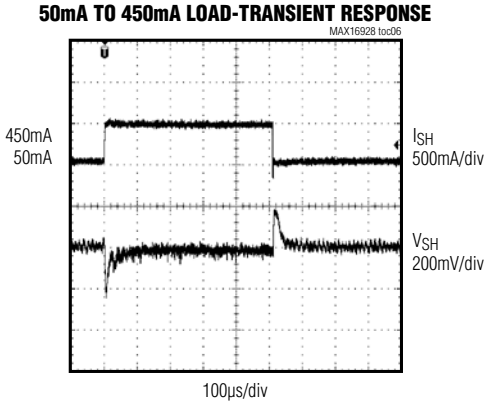
LINE REGULATION (BOOST)



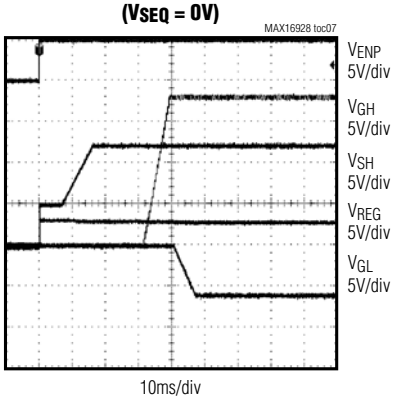
BOOST STARTUP WAVEFORMS



50mA TO 450mA LOAD-TRANSIENT RESPONSE



SUPPLY SEQUENCING WAVEFORMS (V_{SEQ} = 0V)

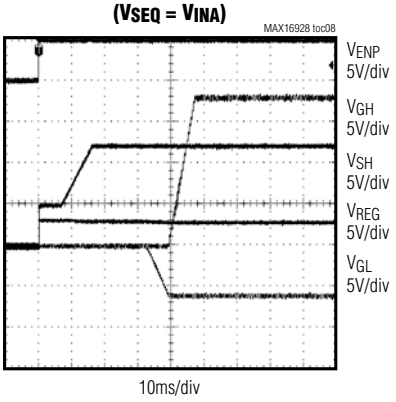


Automotive TFT-LCD Power Supply with Boost Converter and Gate Voltage Regulators

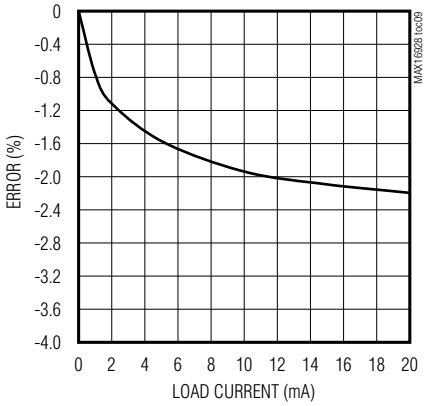
Typical Operating Characteristics (continued)

(V_{INA} = +5V, V_{SH} = +12V, V_{GH} = +18V, V_{GL} = -6V, V_{REG} = 3.3V, T_A = +25°C, unless otherwise noted.)

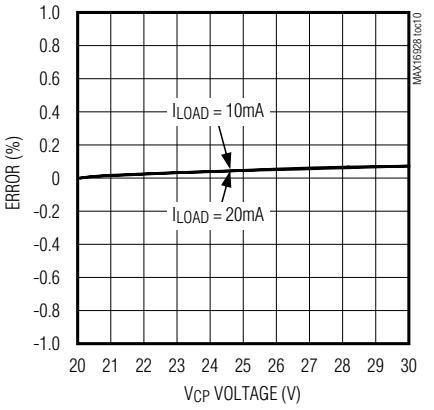
SUPPLY SEQUENCING WAVEFORMS (V_{SEQ} = V_{INA})



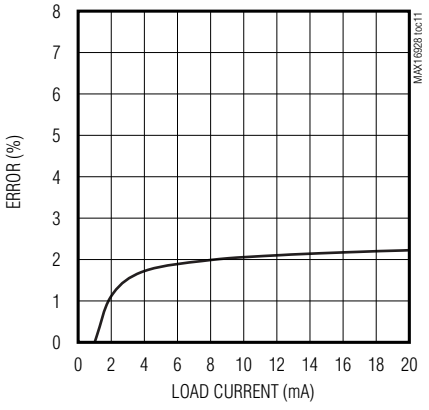
LOAD REGULATION (POSITIVE-GATE VOLTAGE REGULATOR)



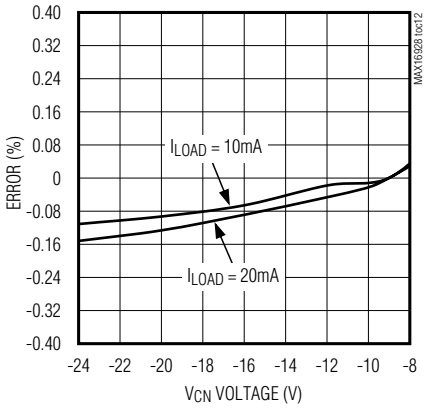
LINE REGULATION (POSITIVE-GATE VOLTAGE REGULATOR)



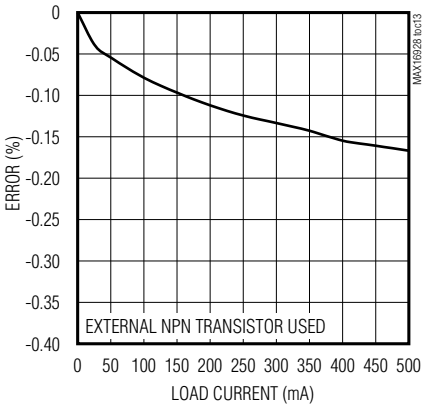
LOAD REGULATION (NEGATIVE-GATE VOLTAGE REGULATOR)



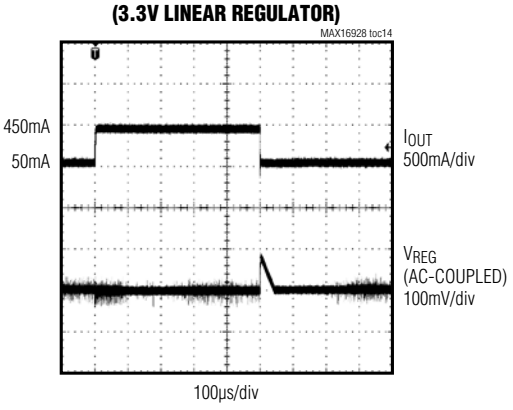
LINE REGULATION (NEGATIVE-GATE VOLTAGE REGULATOR)



LOAD REGULATION (3.3V REGULATOR)

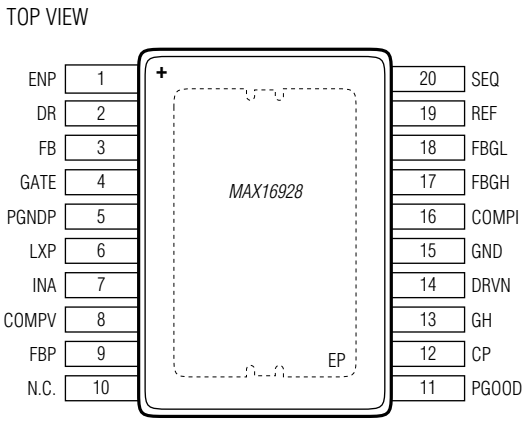


LOAD-TRANSIENT RESPONSE (3.3V LINEAR REGULATOR)



Automotive TFT-LCD Power Supply with Boost Converter and Gate Voltage Regulators

Pin Configuration



TSSOP

Pin Description

PIN	NAME	FUNCTION
1	ENP	Boost Circuitry and 1.8V/3.3V Regulator Controller Enable Input. ENP has an internal 500kΩ pulldown resistor. Drive high for normal operation and drive low to place the device in shutdown.
2	DR	1.8V or 3.3V Regulator Output. DR has a 4.5mA (min) drive capability. For greater output current capability, use an external npn bipolar transistor whose base is connected to DR.
3	FB	1.8V or 3.3V Regulator Feedback Input. FB is regulated to 1.8V or 3.3V. Connect FB to DR when powering loads demanding less than 4.5mA. For greater output current capability, use an external npn bipolar transistor whose emitter is connected to FB.
4	GATE	External p-Channel FET Gate Drive. GATE is an open-drain driver connected to the gate of the external input series p-channel FET. Connect a pullup resistor between GATE and INA. During a fault condition, the gate driver turns off and the pullup resistor turns off the FET.
5	PGNDP	Boost Converter Power Ground
6	LXP	Boost Converter Switching Node. Connect LXP to the inductor and catch diode of the boost converter.
7	INA	Boost Circuitry and 1.8V/3.3V Regulator Controller Power Input. Connect INA to a 3V to 5.5V supply.
8	COMPV	Boost Error Amplifier Compensation Connection. Connect a compensation network between COMPV to GND.
9	FBP	Boost Converter Feedback Input. FBP is regulated to 1V. Connect FBP to the center of a resistive divider connected between the boost output and GND.
10	N.C.	No Connection. Not internally connected.
11	PGOOD	Open-Drain Power-Good Output. Connect PGOOD to INA through an external pullup resistor.
12	CP	Positive-Gate Voltage Regulator Power Input. Connect CP to the positive output of the external charge pump. Ensure that V_{CP} does not exceed the CP overvoltage threshold as given in the *Electrical Characteristics* table.

Pin Description (continued)

PIN	NAME	FUNCTION
13	GH	Positive-Gate Voltage Regulator Output
14	DRVN	Negative-Gate Voltage Regulator Driver Output. DRVN is the open drain of an internal p-channel FET. Connect DRVN to the base of an external npn pass transistor.
15	GND	Analog Ground
16	COMPI	Boost Slope Compensation Connection. Connect a capacitor between COMPI and GND to set the slope compensation.
17	FBGH	Positive-Gate Voltage Regulator Feedback Input. FBGH is regulated to 1V. Connect FBGH to the center of a resistive divider connected between GH and GND.
18	FBGL	Negative-Gate Voltage Regulator Feedback Input. FBGL is regulated to 0.25V. Connect FBGL to the center of a resistive divider connected between REF and the output of the negative-gate voltage regulator.
19	REF	1.25V Reference Output. Bypass REF to GND with a 0.1µF ceramic capacitor.
20	SEQ	Sequencing Input. SEQ has an internal 500kΩ pulldown resistor. SEQ determines the sequence in which V_{GH} and V_{GL} power up. See Table 1 for supply sequencing options.
—	EP	Exposed Pad. Connect to a large contiguous copper ground plane for optimal heat dissipation. Do not use EP as the only electrical ground connection.

Detailed Description

The MAX16928 is a highly integrated power supply for automotive TFT-LCD applications. The device integrates one boost converter, one 1.8V/3.3V regulator controller, one positive-gate voltage regulator, and one negative-gate voltage regulator.

The device achieves enhanced EMI performance through spread-spectrum modulation. Digital input control allows the device to be placed in a low-current shutdown mode and provides flexible sequencing of the gate voltage regulators.

Internal thermal shutdown circuitry protects the device from overheating. The device is designed to shut down when its die temperature reaches +165°C (typ) and to resume normal operation once its die temperature has fallen 15°C.

The device is factory-trimmed to provide a variety of power options to meet the most common automotive TFT-LCD display power requirements, as outlined in the *Ordering Information* table.

Boost Converter

The boost converter employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads typical of TFT-LCD panel source drivers. The 2.2MHz switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated low on-resistance MOSFET and the device's built-in digital soft-start functions reduce the number of external components required while controlling inrush currents. The output voltage can be set from V_{INA} to 18V with an external resistive voltage-divider. The regulator controls the output voltage by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D = 1 - \frac{\eta V_{INA}}{V_O}$$

where V_{INA} is the voltage at INA, $V_O = V_{SH}$ (the boost output voltage), and η is the efficiency of the boost converter as shown in the *Typical Operating Characteristics*.

Figure 1 shows the functional diagram of the boost regulator. An error amplifier compares the signal at FBP to 1V and changes the COMPV output. The voltage at COMPV sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMPV output accordingly to produce the peak inductor current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal (set by the capacitor at COMPI) is summed with the current-sense signal. On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current feedback signal and the slope compensation exceeds the COMPV voltage, the controller turns off the MOSFET. The inductor current then flows through the diode to the output. The MOSFET remains off for the rest of the clock cycle.

The external p-channel FET controlled by GATE protects the output during fault conditions and provides True Shutdown of the converter. Connect a pullup resistor between GATE and INA (see the *Boost Converter* section to select the value for the pullup resistor). Under normal operation, GATE turns on the p-channel FET, connecting the supply to the boost input. During a fault condition or in shutdown, GATE is off and the pullup resistor turns off the p-channel FET, disconnecting the supply from the boost input.

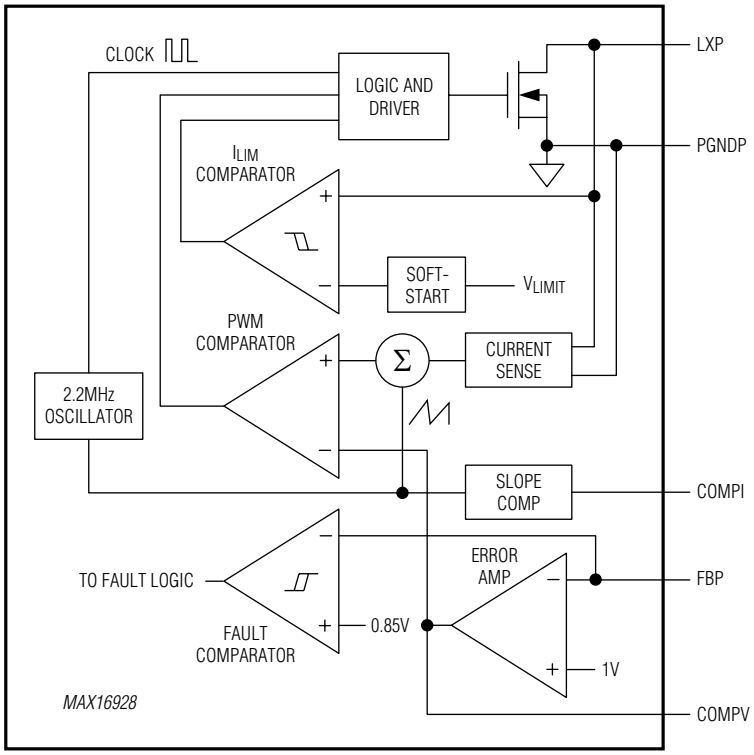


Figure 1. Boost Converter Functional Diagram

Spread-Spectrum Modulation

The high-frequency 2.2MHz operation of the boost converter moves switching noise outside of the AM band. The device achieves enhanced EMI performance by modulating the switching frequency by ±4%. The modulating signal is pseudorandom and changes each switching period (i.e., f_{SS} = 2.2MHz).

Startup

Immediately after power-up, coming out of shutdown, or going into autoretry, the boost converter performs a short-circuit detection test on the output by connecting the input (INA) to the switching node (LXP) through an internal 50Ω resistor.

If the resulting voltage on LXP exceeds 1.2V, the device turns on the external pMOS switch by pulling GATE low. The boost output ramps to its final value in 15ms.

An overloaded or shorted output is detected if the resulting voltage on LXP is below 1.2V. The external pMOS switch remains off and the converter does not switch. After the fault blanking period of 238ms, the device pulls PGOOD low and starts the autoretry timer.

The short-circuit detection feature places a lower limit on the output load of approximately 46Ω when the input voltage is 3V.

Fault Conditions and PGOOD

PGOOD signals whether all the regulators and the boost converter are operating normally. PGOOD is an open-drain output that pulls low if any of the following faults occur:

1) The boost output voltage falls below 85% of its set value.
2) The positive-gate voltage regulator output (V_{GH}) falls below 85% of its set value.
3) The negative-gate voltage regulator output (V_{GL}) falls below 85% of its set value.
4) The LXP voltage is greater than 21V (typ).
5) The positive charge-pump voltage (V_{CP}) is greater than 30.5V (typ).
6) The 1.8V/3.3V regulator output voltage falls below 85% of its nominal value.

If any of the first three fault conditions persists for longer than the 238ms fault blanking period, the device pulls PGOOD low, turns off all outputs, and starts the autoretry timer.

If either condition 4 or 5 occurs, the device pulls PGOOD low and turns off all outputs immediately. The device initiates startup only after the fault has cleared.

If the last condition occurs, the device pulls PGOOD low, but does not turn off any of the outputs.

During startup, PGOOD is masked and goes high as soon as the 1.8V/3.3V regulator controller turns on. This regulator turns on as soon as V_{INA} exceeds the INA undervoltage lockout threshold.

Autoretry

When the autoretry counter finishes incrementing after 1.9s, the device attempts to turn on the boost converter and gate voltage regulators in the order shown in Table 1. The device continues to autoretry as long as the fault condition persists. A fault on the 1.8V/3.3V regulator output causes PGOOD to go low, but does not result in the device shutting down and going into autoretry.

Current Limit

The effective current limit of the boost converter is reduced by the internally injected slope compensation by an amount dependent on the duty cycle of the converter. The effective current limit is given by:

$$I_{LIM(EFF)} = 192 \times 10^{-12} \times I_{LIM\_DC\_0} \times \frac{D}{C_{COMPI}}$$

where $I_{LIM(EFF)}$ is the effective current limit, $I_{LIM\_DC\_0}$ = 1.1A or 2.2A, depending on the boost converter current-limit option, D is the duty cycle of the boost converter, and C_{COMPI} is the value of the capacitor at the COMPI input. Estimate the duty cycle of the converter using the formulas shown in the *Design Procedure* section.

1.8V/3.3V Regulator Controller

The 1.8V/3.3V regulator controller delivers 4.5mA (min) to an external load. Connect FB to DR for a regulated 1.8V/3.3V output.

For higher output capability, use an external npn transistor as shown in the *Typical Operating Circuit*. The drive capability of the regulator is then increased by the current gain of the transistor (h_{FE}). When using an external transistor, use DR as the base drive and connect FB to the transistor's emitter. Bypass the base to ground with a 0.1µF ceramic capacitor.

If the boost output current is greater than 300mA, connect a 30kΩ resistor between DR and GND.

Positive-Gate Voltage Regulator (GH)

The positive-gate voltage regulator includes a p-channel FET output stage to generate a regulated output between 5V and (V_{CP} - 2V). The regulator maintains accuracy over wide line and load conditions. It is capable of at least 20mA of output current and includes current-limit protection. V_{GH} is typically used to provide the TFT-LCD gate drivers' gate-on voltage.

The regulator derives its positive supply voltage from a noninverting charge pump, a single-stage example of which is shown in the *Typical Operating Circuit*. A higher voltage using a multistage charge pump is possible, as described in the *Charge Pumps* section.

Negative-Gate Voltage Regulator (GL)

The negative-gate voltage regulator is an analog gain block with an open-drain p-channel output. It drives an external npn pass transistor with a 6.8kΩ base-to-emitter resistor (see the *Pass Transistor Selection* section). Its guaranteed base drive source current is at least 2mA. V_{GL} is typically used to provide the TFT-LCD gate drivers' gate-off voltage.

The output of the negative-gate voltage regulator (i.e., the collector of the external npn pass transistor) has load-dependent bypassing requirements. Connect a ceramic capacitor between the collector and ground with the value shown in Table 3.

The regulator derives its negative supply voltage from an inverting charge pump, a single-stage example of which is shown in the *Typical Operating Circuit*. A more negative voltage using a multistage charge pump is possible, as described in the *Charge Pumps* section.

The external npn transistor is not short-circuit protected. To maintain proper pulldown capability of the external npn transistor and optimal regulation, a minimum load of at least 500µA is recommended on the output of the GL regulator.

Enable (ENP)

Use the enable input (ENP) to enable and disable the boost section of the device. Connect ENP to INA for normal operation and to GND to place the device in shutdown. In shutdown, the INA supply current is reduced to 0.5µA.

Soft-Start and Supply Sequencing (SEQ)

When enabled, the boost output ramps up from V_{INA} to its set voltage. Once the boost output reaches 85% of the set voltage and the soft-start timer expires, the gate voltage regulators turn on in the order shown in Table 1. The 1.8V/3.3V regulator controller is enabled at the beginning of the boost converter's soft-start.

Both gate voltage regulators have a 7.45ms soft-start time. The second one turns on as soon as the output of the first reaches 85% of its set voltage.

Thermal Shutdown

Internal thermal shutdown circuitry shuts down the device immediately when the die temperature exceeds +165°C. A 15°C thermal shutdown hysteresis prevents the device from resuming normal operation until the die temperature falls below +150°C.

Design Procedure

Boost Converter

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). To determine the inductance value, select the ratio of inductor peak-to-peak ripple current to average output current (LIR) first. For LIR values that are too high, the RMS currents are high, and therefore, I^2R losses are high. Use high-valued inductors to achieve low LIR values. Typically, inductance is proportional to resistance for a given package type,

Table 1. Supply Sequencing

CONTROL INPUTS		SUPPLY SEQUENCING		
ENP	SEQ	FIRST	SECOND	THIRD
0	X	Device is in shutdown		
1	0	V_{SH}	V_{GH}	V_{GL}
1	1	V_{SH}	V_{GL}	V_{GH}

which again makes I^2R losses high for very low LIR values. A good compromise between size and loss is to select a 30%-to-60% peak-to-peak ripple current to average-current ratio. If extremely thin high-resistance inductors are used, as is common for LCD-panel applications, the best LIR can increase between 0.5 and 1.0. The size of the inductor is determined as follows:

$$L = \frac{V_{INA} \times D}{LIR \times I_{INA} \times f_{SW}} \text{ and } I_{INA} = \frac{V_O \times I_O}{\eta V_{INA}}$$

$$D = \frac{1 - \eta V_{INA}}{V_O}$$

where V_{INA} is the input voltage, V_O is the output voltage, I_O is the output current, I_{INA} is the average boost input current, η is the efficiency of the boost converter, D is the duty cycle, and f_{SW} is 2.2MHz (the switching frequency of the boost converter). The efficiency of the boost converter can be estimated from the *Typical Operating Characteristics* and accounts for losses in the internal switch, catch diode, inductor R_{DC}, and capacitor ESR.

Capacitor Selection

The input and output filter capacitors should be of a low-ESR type (tantalum, ceramic, or low-ESR electrolytic) and should have I_{RMS} ratings greater than:

$$I_{RMS} = \frac{LIR \times I_{INA}}{\sqrt{12}} \text{ for the input capacitor}$$

$$I_{RMS} = I_O \sqrt{\frac{D + \frac{LIR^2}{12}}{1 - D}} \text{ for the output capacitor}$$

where I_{INA} and D are the input current and duty cycle given above.

The output voltage contains a ripple component whose peak-to-peak value depends on the value of the ESR and capacitance of the output capacitor and is approximately given by:

$$\Delta V_{RIPPLE} = \Delta V_{ESR} + \Delta V_{CAP}$$

$$\Delta V_{ESR} = I_{INA} \times (1 + \frac{LIR}{2}) \times R_{ESR}$$

$$\Delta V_{CAP} = \frac{I_O \times D}{C_{OUT} \times f_{SW}}$$

where I_{INA} and D are the input current and duty cycle given above.

Rectifier Diode

The catch diode should be a Schottky type to minimize its voltage drop and maximize efficiency. The diode must be capable of withstanding a reverse voltage of at least V_{SH}. The diode should have an average forward current rating greater than:

$$I_D = I_{INA} \times (1\text{-}D)$$

where I_{INA} and D are the input current and duty cycle given above. In addition ensure that the peak current rating of the diode is greater than:

$$I_{INA} \times \left(1 + \frac{LIR}{2}\right)$$

Output Voltage Selection

The output voltage of the boost converter can be adjusted by using a resistive voltage-divider formed by R_{TOP} and R_{BOTTOM}. Connect R_{TOP} between the output and FBP and connect R_{BOTTOM} between FBP and GND. Select R_{BOTTOM} in the 10kΩ to 50kΩ range. Calculate R_{TOP} with the following equation:

$$R_{TOP} = R_{BOTTOM} \times (\frac{V_O}{V_{FBP}} - 1)$$

where V_{FBP}, the boost converter's feedback set point, is 1V. Place both resistors as close as possible to the device and connect R_{BOTTOM} to the analog ground plane.

Loop Compensation

Choose R_{COMPV} to set the high-frequency integrator gain for fast transient response. Choose C_{COMPV} to set the integrator zero to maintain loop stability. For low-ESR output capacitors, use Table 2 to select the initial values for R_{COMPV} and C_{COMPV}. Use a 22pF capacitor in parallel with R_{COMPV} + C_{COMPV}.

Table 2. Compensation Component Values

V_{SH} (V)	8	18
I_{SH} (mA)	200	200
V_{INA} (V)	3.3	5
P_{IN} (W)	1.75	3.75
L (µH)	5	5
R_{COMPV} (kΩ)	33	39
C_{COMPV} (pF)	220	180
C_{COMPI} (pF)	820	330

To further optimize transient response, vary R_{COMPV} in 20% steps and C_{COMPV} in 50% steps while observing transient-response waveforms. The ideal transient response is achieved when the output settles quickly with little or no overshoot. Connect the compensation network to the analog ground plane.

Use the following formula to calculate the value for C_{COMPI}:

$$C_{COMPI} \le 950 \times 10^{-6} \times L/(V_{SH} + V_{SCHOTTKY} - V_{INA})$$

p-Channel FET Selection

The p-channel FET used to gate the boost converter's input should have low on-resistance. Connect a resistor (R_{SG}) between the source and gate of the FET. Under normal operation, R_{SG} carries a gate drive current of 55µA and the resulting gate source voltage (V_{GS}) turns on the FET. When the gate drive is removed under a fault condition or in shutdown, R_{SG} bleeds off charge to turn off the FET. Size R_{SG} to produce the V_{GS} needed to turn on the FET.

1.8V/3.3V Regulator Controller

npn Bipolar Transistor Selection

There are two important considerations in selecting the pass npn bipolar transistor: current gain (h_{FE}) and power dissipation. Select a transistor with an h_{FE} high enough to ensure adequate drive capability. This condition is satisfied when I_{DR} x (h_{FE} + 1) is greater than the maximum load current. The regulator can source I_{DR} = 4.5mA (min). The transistor should be capable of dissipating:

$$P_{NPN\_REG} = (V_{INA} - V_{REG\_OUT}) \times I_{LOAD(MAX)}$$

where V_{REG_OUT} = 1.8V or 3.3V. Bypass DR to ground with a 0.1µF ceramic capacitor. For applications in which the boost output current exceeds 300mA, connect a 30kΩ resistor from DR to ground.

Supply Considerations

INA needs to be at least 4.5V for the 3.3V regulator to operate properly.

Charge Pumps

Selecting the Number of Charge-Pump Stages

For most applications, a single charge-pump stage is sufficient, as shown in the *Typical Operating Circuit*. Connect the flying capacitors to LXP. The output voltages generated on the storage capacitors are given by:

$$V_{CP} = 2 \times V_{SH} + V_{SCHOTTKY} - 2 \times V_D$$

$$V_{CN} = -(V_{SH} + V_{SCHOTTKY} - 2 \times V_D)$$

where V_{CP} is the positive supply for the positive-gate voltage regulator, and V_{CN} is the negative supply for the negative-gate voltage regulator. Where larger output voltages are needed, use multistage charge pumps (however, the maximum charge-pump voltage is limited by the absolute maximum ratings of CP and DRVN). Figure 2 and Figure 3 show the configuration of a multistage charge pump for both positive and negative output voltages.

For mutistage charge pumps the output voltages are:

$$V_{CP} = V_{SH} + n \times (V_{SH} + V_{SCHOTTKY} - 2 \times V_D)$$

$$V_{CN} = -n \times (V_{SH} + V_{SCHOTTKY} - 2 \times V_D)$$

For highest efficiency, choose the lowest number of charge-pump stages that meets the output requirement. The number of positive charge-pump stages needed is given by:

$$n_{CP} = \frac{V_{GH} + V_{DROPOUT} - V_{SH}}{V_{SH} + V_{SCHOTTKY} - 2 \times V_D}$$

and the number of negative charge-pump stages is given by:

$$n_{CN} = \frac{|V_{GL}| + V_{DROPOUT}}{V_{SH} + V_{SCHOTTKY} - 2 \times V_D}$$

where n_{CP} is the number of positive charge-pump stages, n_{CN} is the number of negative charge-pump stages, V_{GH} is the positive-gate voltage regulator output voltage, V_{GL} is the negative-gate voltage regulator output voltage, V_{SH} is the boost converter's output voltage, V_D

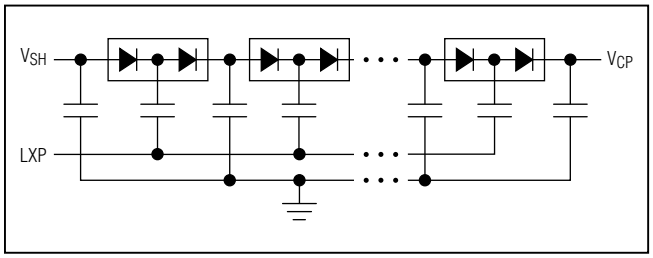


Figure 2. Multistage Charge Pump for Positive Output Voltage

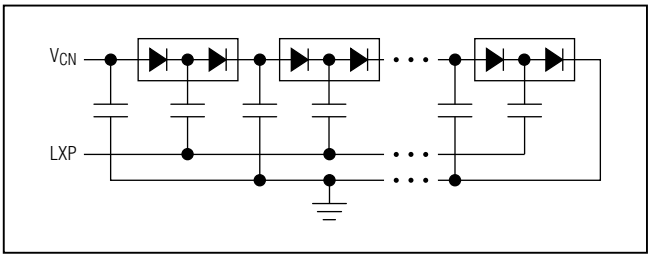


Figure 3. Multistage Charge Pump for Negative Output Voltage

is the forward-voltage drop of the charge-pump diode, $V_{SCHOTTKY}$ is the forward drop of the Schottky diode of the boost converter, and $V_{DROPOUT}$ is the dropout margin for the regulator. Use $V_{DROPOUT}$ = 0.3V for the negative voltage regulator and $V_{DROPOUT}$ = 2V at 20mA for the positive-gate voltage regulator.

Flying Capacitors

Increasing the flying capacitor (C_X) value lowers the effective source impedance and increases the output current capability. Increasing the capacitance indefinitely has a negligible effect on output current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The voltage rating of the flying capacitors for the positive charge pump should exceed V_{CP}, and that for the negative charge pump should exceed the magnitude of V_{CN}.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output-ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output-voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required output capacitance for the noninverting charge pump connected to CP:

$$C_{OUT\_CP} \geq \frac{D \times I_{LOAD\_CP}}{f_{SW} \times V_{RIPPLE\_CP}}$$

where C_{OUT_CP} is the output capacitor of the charge pump, D is the duty cycle of the boost converter, I_{LOAD_CP} is the load current of the charge pump, f_{SW} is the switching frequency of the boost converter, and V_{RIPPLE_CP} is the peak-to-peak value of the output ripple.

For the inverting charge pump connected to CN, use the following equation to approximate the required output capacitance:

$$C_{OUT\_CN} \geq \frac{(1\text{-}D) \times I_{LOAD\_CN}}{f_{SW} \times V_{RIPPLE\_CN}}$$

where C_{OUT_CN} is the output capacitor of the charge pump, D is the duty cycle of the boost converter, I_{LOAD_CN} is the load current of the charge pump, f_{SW} is the switching frequency of the boost converter, and V_{RIPPLE_CN} is the peak-to-peak value of the output ripple.

Charge-Pump Rectifier Diodes

Use high-speed silicon switching diodes with a current rating equal to or greater than two times the average charge-pump input current. If it helps avoid an extra stage, some or all of the diodes can be replaced with Schottky diodes with an equivalent current rating.

Positive-Gate Voltage Regulator

Output Voltage Selection

The output voltage of the positive-gate voltage regulator can be adjusted by using a resistive voltage-divider formed by R_{TOP} and R_{BOTTOM}. Connect R_{TOP} between the output and FBGH, and connect R_{BOTTOM} between FBGH and GND. Select R_{BOTTOM} in the 10kΩ to 50kΩ range. Calculate R_{TOP} with the following equation:

$$R_{TOP} = R_{BOTTOM} \times (\frac{V_{GH}}{V_{FBGH}} - 1)$$

where V_{GH} is the desired output voltage and V_{FBGH} = 1V (the regulated feedback voltage for the regulator). Place both resistors as close as possible to the device.

Avoid excessive power dissipation within the internal pMOS device of the regulator by paying attention to the voltage drop across the drain and source. The amount of power dissipation is given by:

$$P_{GL} = (V_{CP} - V_{GH}) \times I_{LOAD(MAX)}$$

where V_{CP} is the noninverting charge-pump output voltage applied to the drain, V_{GH} is the regulated output voltage, and $I_{LOAD(MAX)}$ is the maximum load current.

Stability Requirements

The positive-gate voltage regulator (GH) requires a minimum output capacitance for stability. For an output voltage of 5V to (V_{CP} - 2V) and an output current of 10mA to 15mA, use a minimum capacitance of 0.47µF.

Negative-Gate Voltage Regulator

Output Voltage Selection

The output voltage of the negative-gate voltage regulator can be adjusted by using a resistive voltage-divider formed by R_{TOP} and R_{BOTTOM}. Connect R_{TOP} between REF and FBGL and connect R_{BOTTOM} between FBGL and the collector of the external npn transistor. Select

R_{TOP} greater than 20kΩ to avoid loading down the reference output. Calculate R_{BOTTOM} with the following equation:

$$R_{BOTTOM} = R_{TOP} \times \frac{V_{FBGL} - V_{GL}}{V_{REF} - V_{FBGL}}$$

where V_{GL} is the desired output voltage, V_{REF} = 1.25V, and V_{FBGL} = 0.25V (the regulated feedback voltage of the regulator).

Pass Transistor Selection

The pass transistor must meet specifications for current gain (h_{FE}), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = (I_{DRVN} - \frac{V_{BE}}{R_{BE}}) \times h_{FE(MIN)}$$

where I_{DRVN} is the minimum guaranteed base-drive current, V_{BE} is the transistor's base-to-emitter forward voltage drop, and R_{BE} is the pulldown resistor connected between the transistor's base and emitter. Furthermore, the transistor's current gain increases the regulator's DC loop gain (see the *Stability Requirements* section), so excessive gain destabilizes the output.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the regulator can support. Also, the package's power dissipation limits the usable maximum input-to-output voltage differential. The maximum power-dissipation capability of the transistor's package and mounting must exceed the actual power dissipated in the device. The power dissipated equals the maximum load current ($I_{LOAD(MAX)\_GL}$) multiplied by the maximum input-to-output voltage differential:

$$P_{NPN\_GL} = (V_{GL} - V_{CN}) \times I_{LOAD(MAX)}$$

where V_{GL} is the regulated output voltage on the collector of the transistor, V_{CN} is the inverting charge-pump output voltage applied to the emitter of the transistor, and $I_{LOAD(MAX)}$ is the maximum load current. Note that the external transistor is not short circuit protected.

Stability Requirements

The device's negative-gate voltage regulator uses an internal transconductance amplifier to drive an external pass transistor. The transconductance amplifier, the pass transistor, the base-emitter resistor, and the output capacitor determine the loop stability.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. The total DC loop gain is approximately:

$$A_{V\_GL} \cong (\frac{4}{V_T}) \times (1 + \frac{I_{BIAS} \times h_{FE}}{I_{LOAD}}) \times V_{REF}$$

where V_T is 26mV at room temperature, and I_{BIAS} is the current through the base-to-emitter resistor (R_{BE}). For the device, the bias current for the negative-gate voltage regulator is 0.1mA. Therefore, the base-to-emitter resistor should be chosen to set 0.1mA bias current:

$$R_{BE} = \frac{V_{BE}}{0.1mA} = \frac{0.7V}{0.1mA} = 7k\Omega$$

Use the closest standard resistor value of 6.8kΩ. The output capacitor and the load resistance create the dominant pole in the system. However, the internal amplifier delay, pass transistor's input capacitance, and the stray capacitance at the feedback node create additional poles in the system, and the output capacitor's ESR generates a zero. For proper operation, use the following procedure to verify that the regulator is properly compensated:

1) First, determine the dominant pole set by the regulator's output capacitor and the load resistor:

$$f_{POLE\_GL} = \frac{I_{LOAD(MAX)\_GL}}{2\pi \times C_{OUT\_GL} \times V_{OUT\_GL}}$$

The unity-gain crossover frequency of the regulator is:

$$f_{CROSSOVER} = A_{V\_LR} \times f_{POLE\_LR}$$

2) The pole created by the internal amplifier delay is approximately 1MHz:

$$f_{POLE\_AMP} = 1MHz$$

3) Next, calculate the pole set by the transistor's input capacitance, the transistor's input resistance, and the base-to-emitter pullup resistor:

$$f_{POLE\_IN} = \frac{1}{2\pi \times C_{IN} \times (R_{BE} / R_{IN})}$$

where:

$$C_{IN} = \frac{g_m}{2\pi f_T}, R_{IN} = \frac{h_{FE}}{g_m}$$

g_m is the transconductance of the pass transistor, and f_T is the transition frequency. Both parameters can be

found in the transistor's data sheet. Because R_{BE} is much greater than R_{IN}, the above equation can be simplified:

$$f_{POLE\_IN} = \frac{1}{2\pi \times C_{IN} \times R_{IN}}$$

Substituting for C_{IN} and R_{IN} yields:

$$f_{POLE} = \frac{f_T}{h_{FE}}$$

4) Next, calculate the pole set by the regulator's feedback resistance and the capacitance between FBGL and GND (including stray capacitance):

$$f_{POLE\_FBGL} = \frac{1}{2\pi \times C_{FBGL} \times (R_{TOP}/R_{BOTTOM})}$$

where C_{FBGL} is the capacitance between FBGL and GND and is equal to 30pF, R_{TOP} is the upper resistor of the regulator's feedback divider, and R_{BOTTOM} is the lower resistor of the divider.

5) Next, calculate the zero caused by the output capacitor's ESR:

$$f_{ZERO\_ESR} = \frac{1}{2\pi \times C_{OUT\_LR} \times R_{ESR}}$$

where R_{ESR} is the equivalent series resistance of C_{OUT_LR}. To ensure stability, make C_{OUT_LR} large enough so the crossover occurs well before the poles and zero calculated in steps 2 to 5. The poles in steps 3 and 4 generally occur at several MHz and using ceramic capacitors ensures the ESR zero also occurs at several MHz. Placing the crossover frequency below 500kHz is sufficient to avoid the amplifier delay pole and generally works well, unless unusual component choices or extra capacitances move one of the other poles or the zero below 1MHz.

Table 3 is a list of recommended minimum output capacitance for the negative-gate voltage regulator and is applicable for output currents in the 10mA to 15mA range.

Table 3. Minimum Output Capacitance vs. Output Voltage Range for Negative-Gate Voltage Regulator (I_{OUT} = 10mA to 15mA)

OUTPUT VOLTAGE RANGE	MINIMUM OUTPUT CAPACITANCE (µF)
$-2V \geq V_{GL} \geq -4V$	2.2
$-5V \geq V_{GL} \geq -7V$	1.5
$-8V \geq V_{GL} \geq -13V$	1

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the boost converter, positive-gate voltage regulator, negative-gate voltage regulator, and the 1.8V/3.3V regulator controller.

Boost Converter

Power dissipation in the boost converter is primarily due to conduction and switching losses in the low-side FET. Conduction loss is produced by the inductor current flowing through the on-resistance of the FET during the on-time. Switching loss occurs during switching transitions and is a result of the finite time needed to fully turn on and off the FET. Power dissipation in the boost converter can be estimated with the following formula:

$$P_{LXP} \approx [(I_{IN(DC,MAX)} \times \sqrt{D})^2 \times R_{DS\_ON(LXP)}] + V_{SH} \times I_{IN(DC,MAX)} \times f_{SW} \times [(t_{R\text{-}V} + t_{F\text{-}I}) + (t_{R\text{-}I} + t_{F\text{-}V})]$$

where $I_{IN(DC,MAX)}$ is the maximum expected average input (i.e., inductor) current, D is the duty cycle of the boost converter, $R_{DS\_ON(LXP)}$ is the on-resistance of the internal low-side FET, V_{SH} is the output voltage, and f_{SW} is the switching frequency of the boost converter. $R_{DS\_ON(LXP)}$ is 110mΩ (typ) and f_{SW} is 2.2MHz.

The voltage and current rise and fall times at the LXP node are equal to t_{R-V} (voltage rise time), t_{F-V} (voltage fall time), t_{R-I} (current rise time), and t_{F-I} (current fall time), and are determined as follows:

$$t_{R-V} = \frac{V_{SH} + V_{SCHOTTKY}}{K_{R-V}}$$

$$t_{F-V} = \frac{V_{SH} + V_{SCHOTTKY}}{K_{F-V}}$$

$$t_{R-I} = \frac{I_{IN(DC,MAX)}}{K_{R-I}}$$

$$t_{F-I} = \frac{I_{IN(DC,MAX)}}{K_{F-I}}$$

K_{R-V}, K_{F-V}, K_{R-I}, and K_{F-I} are the voltage and current slew rates of the LXP node and are supply dependent. Use Table 4 to determine their values.

Positive-Gate Voltage Regulator

Use the lowest number of charge-pump stages possible in supplying power to the positive voltage regulator. Doing so minimizes the drain-source voltage of the integrated pMOS switch and power dissipation. The power dissipated in the switch is given as:

$$P_{GH} = (V_{CP} - V_{GH}) \times I_{LOAD(MAX)\_GH}$$

Ensure that the voltage on CP does not exceed the CP overvoltage threshold as given in the *Electrical Characteristics* table.

Negative-Gate Voltage Regulator

Use the lowest number of charge-pump stages possible to provide the negative voltage to the negative-gate voltage regulator. Estimate the power dissipated in the negative-gate voltage regulator using the following:

$$P_{GL} = (V_{INA} + |V_{CN}| - V_{BE}) \times I_{DRVN}$$

where V_{BE} is the base-emitter voltage of the external npn bipolar transistor, and I_{DRVN} is the current sourced from DRVN to the R_{BE} bias resistor and to the base of the transistor, which is given by:

$$I_{DRVN} = \frac{V_{BE}}{R_{BE}} + \frac{I_{GL}}{h_{FE}+1}$$

1.8V/3.3V Regulator Controller

The power dissipated in the 1.8V/3.3V regulator controller is given by:

$$P_{REG} = (V_{INA} - V_{OUT\_REG} - V_{BE}) \times I_{DR}$$

where V_{OUT_REG} = 1.8V or 3.3V, V_{BE} is the base-emitter voltage of the external npn bipolar transistor, and I_{DR} is the current sourced from DR to the base of the transistor. I_{DR} is given by:

$$I_{DR} = \frac{I_{LOAD}}{h_{FE}+1}$$

where I_{LOAD} is load current of the 1.8V/3.3V regulator controller, and h_{FE} is the current gain of the transistor.

Total Power Dissipation

The total power dissipated in the package is the sum of the losses previously calculated. Therefore, total power dissipation can be estimated as follows:

$$P_T = P_{LXP} + P_{GH} + P_{GL} + P_{REG}$$

Achieve maximum heat transfer by connecting the exposed pad to a thermal landing pad and connecting the thermal landing pad to a large ground plane through thermal vias.

Table 4. LXP Voltage and Current Slew Rates vs. Supply Voltage

V_{INA} (V)	LXP VOLTAGE AND CURRENT SLEW RATES			
	RISING VOLTAGE SLEW RATE, K_{R-V} (V/ns)	FALLING VOLTAGE SLEW RATE, K_{F-V} (V/ns)	RISING CURRENT SLEW RATE, K_{R-I} (A/ns)	FALLING CURRENT SLEW RATE, K_{F-I} (A/ns)
3.3	0.52	1.7	0.13	0.38
5	1.35	2	0.3	0.44

Layout Considerations

Careful PCB layout is critical in achieving stable and optimized performance. Follow these guidelines for good PCB layout:

1) Place decoupling capacitors as close as possible to the device. Connect the power ground planes and the analog ground plane together at one point close to the device.
2) Connect input and output capacitors to the power ground planes; connect all other capacitors to the analog ground plane.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching currents short.
4) Place the feedback resistors as close as possible to the device. Connect the negative end of the resistive divider and the compensation network to the analog ground plane.
5) Route the high-speed switching node LXP away from sensitive analog nodes (FB, FBP, FBGH, FBGL, and REF).

Refer to the MAX16928 Evaluation Kit data sheet for a recommended PCB layout.

Ordering Information

PART	TEMP RANGE	REGULATOR V_{REG} (V)	BOOST I_{LIM} (A)	PIN-PACKAGE
MAX16928AGUP/V+	-40°C to +105°C	3.3	1.5	20 TSSOP-EP*
MAX16928BGUP/V+	-40°C to +105°C	1.8	1.5	20 TSSOP-EP*
MAX16928CGUP/V+	-40°C to +105°C	3.3	0.75	20 TSSOP-EP*
MAX16928DGUP/V+	-40°C to +105°C	1.8	0.75	20 TSSOP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

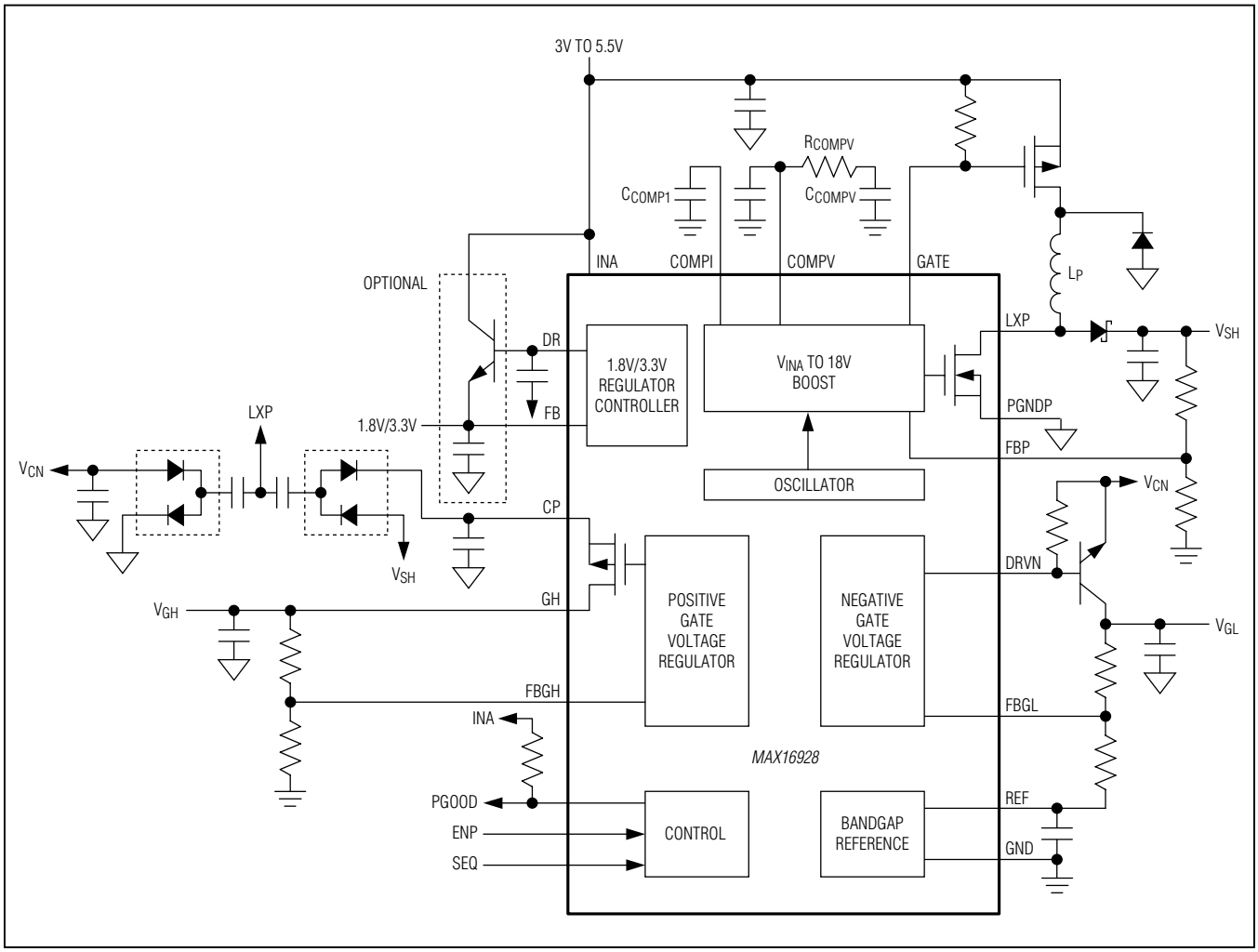
Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TSSOP-EP	U20E+1	21-0108	90-0114

Automotive TFT-LCD Power Supply with Boost Converter and Gate Voltage Regulators

Typical Operating Circuit



Automotive TFT-LCD Power Supply with Boost Converter and Gate Voltage Regulators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/11	Initial release	—
1	1/12	Corrected the C_{COMPI} formula in the *Loop Compensation* section	13
2	3/13	Corrected typo in package code	18