RAD-TOLERANT CLASS V, WIDEBAND OPERATIONAL AMPLIFIER

FEATURES

- **Wide Bandwidth: 1 GHz**
- **Minimum Gain of 2 V/V (6 dB)**
- **High Slew Rate: 800 V/µs**
- **Low Voltage Noise: 2.4 nV/$\sqrt{Hz}$**
- **Single Supply: 5 V, 3 V**
- **Quiescent Current: 18 mA**
- **Rad-Tolerant: 150 kRad (Si) TID**
- **QML-V Qualified, SMD 5962-07219**

APPLICATIONS

- **Active Filter**
- **ADC Driver**
- **Ultrasound**
- **Gamma Camera**
- **RF/Telecom**

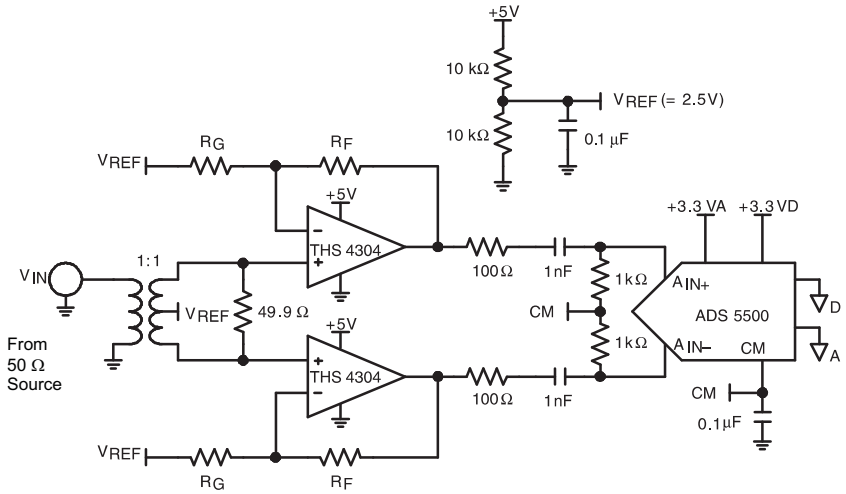
DESCRIPTION/ORDERING INFORMATION

The THS4304 is a wideband, voltage-feedback operational amplifier designed for use in high-speed analog signal processing chains operating with a single 5 V power supply. Developed in the BiCom3 silicon germanium process technology, the THS4304 offers best-in-class performance using a single 5 V supply as opposed to previous generations of operational amplifiers requiring ±5 V supplies.

The THS4304 is a traditional voltage-feedback topology that provides the following benefits: balanced inputs, low offset voltage and offset current, low offset drift, high common mode and power supply rejection ratio.

The THS4304 is offered in 10-pin ceramic flatpack (U) and is specified over the full military temperature range, –55°C to 125°C.

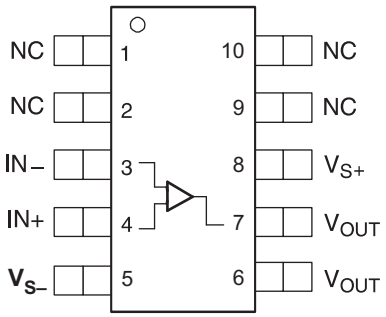
DIFFERENTIAL ADC DRIVE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

U PACKAGE
TOP VIEW



NC – No internal connection

ORDERING INFORMATION(1)

PACKAGED DEVICES	PACKAGE TYPE(2)	PACKAGE MARKINGS	TRANSPORT MEDIA, QUANTITY
5962-0721901VHA	Ceramic Flatpack	0721901VHA	Tubes, 25

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1)		
			$T_A \le 25°C$	$T_A = 85°C$	$T_A = 125°C$
U (10)	14.7	189	661 mW	344 mW	132 mW

(1) Power rating determined for a maximum junction temperature of 150°C. However, distortion starts to substantially increase above 125°C. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			UNIT
V_S	Supply voltage		+6.0 V
V_I	Input voltage		$\pm V_S$
I_O	Output current		150 mA
V_{ID}	Differential input voltage		±2 V
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature, any condition(2)		150°C
T_{stg}	Storage temperature range		–65°C to 150°C
	ESD Ratings	HBM	1600 V
		CDM	1000 V
		MM	100 V

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, (V_{S+} and V_{S-})	Dual supply	±1.35	±2.5	V
	Single supply	2.7	5	
Input common-mode voltage range		V_{S-} – 0.2	V_{S+} + 0.2	V

ELECTRICAL CHARACTERISTICS (Unchanged after 150 kRad)

Specifications: V_S = 5 V: R_F = 249 Ω, R_L = 100 Ω, and G = +3 unless otherwise noted

PARAMETER	CONDITIONS		TYP	OVER TEMPERATURE			
			25°C	25°C	–55°C to 125°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small-Signal Bandwidth	G = +2, V_O = 100 mVpp		1			GHz	Typ
	G = +3, V_O = 100 mVpp		800			MHz	Typ
	G = +5, V_O = 100 mVpp		220			MHz	Typ
Gain Bandwidth Product	G > +5		1			GHz	Typ
0.1 dB Flat Bandwidth	G= +3, V_O = 100 mVpp, C_F = 0 pF		100			MHz	Typ
Large-Signal Bandwidth	G = +3, V_O = 2 V_{PP}		290			MHz	Typ
Slew Rate	G = +3, V_O = 2-V Step		800			V/µs	Typ
Settling Time to 1%	G = +3, V_O = 2-V Step		11			ns	Typ
Rise/Fall Times	G = +3, V_O = 2-V Step		2.5			ns	Typ
Harmonic Distortion							
Second Harmonic Distortion	G = +3, V_O = 2 V_{PP}, f = 10 MHz	R_L= 100 Ω	–67			dBc	Typ
		R_L = 1 kΩ	–85			dBc	Typ
Third Harmonic Distortion		R_L = 100 Ω	–100			dBc	Typ
		R_L = 1 kΩ	–85			dBc	Typ
Third-Order Intermodulation Distortion (IMD_3)	G = +3, V_O= 2-V_{PP} envelope, 200 kHz tone spacing, f = 20 MHz		–80			dBc	Typ
Third-Order Output Intercept (OIP_3)			41			dBm	Typ
Noise Figure	G = +2, f = 1 GHz		15			dB	Typ
Input Voltage Noise	f = 1 MHz		2.4			nV/√Hz	Typ
Input Current Noise	f = 1 MHz		2.1			pA/√Hz	Typ

ELECTRICAL CHARACTERISTICS (Unchanged after 150 kRad)

Specifications: V_S = ±2.5 V, V_{CM} = 0 V, R_L = 500 Ω unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE			
		25°C	25°C	–55°C to 125°C	UNITS	MIN/ MAX
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})	V_O = ±0.8 V	58	54	49	dB	Min
Input Offset Voltage	V_O = 0 V	0.5	4	6	mV	Max
Input Offset Voltage Drift				5	µV/°C	Typ
Input Bias Current		7	12	20	µA	Max
Input Bias Current Drift				50	nA/°C	Typ
Input Offset Current		0.5	1	1.5	µA	Max
Input Offset Current Drift				10	nA/°C	Typ
INPUT CHARACTERISTICS						
Common-Mode Input Range		±2.7	±2.3	±2	V	Min
Common-Mode Rejection Ratio	V_O = 0 V, V_{CM} = ±1 V	86	78	52	dB	Min
Input Resistance	Each input, referenced to GND	100			kΩ	Typ
Input Capacitance		1.5			pF	Typ
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 100 Ω	±1.4	±1.3	±1.15	V	Min
	R_L = 1 kΩ	±1.5	±1.4	±1.25		
Output Current (Sourcing)	R_L = 10 Ω	98	80	70	mA	Min
Output Current (Sinking)	R_L = 10 Ω	95	70	55	mA	Min
Output Impedance	f = 100 kHz	0.016			Ω	Typ
POWER SUPPLY						
Maximum Operating Voltage		±2.5	±2.75	±2.75	V	Max
Minimum Operating Voltage		±2.5	±1.35	±1.35		Min
Maximum Quiescent Current	I_O = 0 mA	18	18.9	19.7	mA	Max
Minimum Quiescent Current	I_O = 0 mA	18	17.5	16.0	mA	Min
Power Supply Rejection (+PSRR)	V_{S+} = 3 V to 2 V, $V_{S–}$ = –2.5 V	78	72	64	dB	Min
Power Supply Rejection (–PSRR)	V_{S+} = 2.5 V, $V_{S–}$ = –2 V to –3 V	60	57	53	dB	Min

ELECTRICAL CHARACTERISTICS (Unchanged after 150 kRad)

Specifications: V_S = 3 V: R_F = 249 Ω, R_L = 500 Ω, and G = +3 unless otherwise noted

PARAMETER	CONDITIONS		TYP	OVER TEMPERATURE			
			25°C	25°C	–55°C to 125°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small-Signal Bandwidth	G = +2, V_O = 100 mVpp		1			GHz	Typ
	G = +5, V_O = 100 mVpp		230			MHz	Typ
Gain Bandwidth Product	G > +5		1			GHz	Typ
Slew Rate	G = +3, V_O = 1-V Step		675			V/µs	Typ
Rise/Fall Times	G = +3, V_O = 0.5-V Step		1.5			ns	Typ
HARMONIC DISTORTION							
Second Harmonic Distortion	G = +3, V_O = 0.5 V_{PP}, f = 10 MHz	R_L = 499 Ω	–82			dBc	Typ
Third Harmonic Distortion			–82			dBc	Typ
Noise Figure	G = +2, f = 1 GHz		15			dB	Typ
Input Voltage Noise	f = 1 MHz		2.4			nV/√Hz	Typ
Input Current Noise	f = 1 MHz		2.1			pA/√Hz	Typ

ELECTRICAL CHARACTERISTICS (Unchanged after 150 kRad)

Specifications: V_S = ±1.5 V, V_{CM} = 0 V, R_L = 500 Ω unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE			
		25°C	25°C	–55°C to 125°C	UNITS	MIN/ MAX
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})	V_O = ±0.3 V	57	52	50	dB	Min
Input Offset Voltage	V_O = 0 V	1	4	6	mV	Max
Input Offset Voltage Drift				5	µV/°C	Typ
Input Bias Current		6	12	20	µA	Max
Input Bias Current Drift				50	nA/°C	Typ
Input Offset Current		0.4	1	1.5	µA	Max
Input Offset Current Drift				10	nA/°C	Typ
INPUT CHARACTERISTICS						
Common-Mode Input Range		±1.7	±1.3	±1	V	Min
Common-Mode Rejection Ratio	V_O = 0 V, V_{CM} = ±0.3 V	68	62	50	dB	Min
Input Resistance	Each input, referenced to GND	100			kΩ	Typ
Input Capacitance		1.5			pF	Typ
OUTPUT CHARACTERISTIC						
Output Voltage Swing	R_L = 100 Ω	±0.4	±0.3	±0.2	V	Min
	R_L = 1 kΩ	±0.5	±0.4	±0.3		
Output Current (Sourcing)	R_L = 10 Ω	30	25	20	mA	Min
Output Current (Sinking)	R_L = 10 Ω	32	27	21	mA	Min
Output Impedance	f = 100 kHz	0.016			Ω	Typ
POWER SUPPLY						
Maximum Operating Voltage		±1.5	±2.75	±2.75	V	Max
Minimum Operating Voltage		±1.5	±1.35	±1.35		Min
Maximum Quiescent Current	I_O = 0 mA	17.2	17.9	18.6	mA	Max
Minimum Quiescent Current	I_O = 0 mA	17.2	16.5	15.0	mA	Min
Power Supply Rejection (+PSRR)	V_{S+} = 1.8 V to 1.2 V, $V_{S–}$ = –1.5 V	80	60	53	dB	Min
Power Supply Rejection (–PSRR)	V_{S+} = 1.5 V, $V_{S–}$ = –1.2 V to –1.8 V	60	55	52	dB	Min

TYPICAL CHARACTERISTICS

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	2nd Harmonic Distortion	vs Frequency	8, 10
	3rd Harmonic Distortion	vs Frequency	9, 11
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OIP_3	3rd Order Output Intercept Point	vs Frequency	14
SR	Slew Rate	vs Output voltage	15
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	Noise Figure	vs Frequency	17
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V_O	Small-signal Transient Response		24
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V_O	Overdrive Recovery Time		27
3 V			
	Frequency Response		28 through 30
	Harmonic Distortion	vs Frequency	31
	Harmonic Distortion	vs Output voltage	32
SR	Slew Rate	vs Output voltage	33
V_O	Output Voltage	vs Load resistance	34
I_{IB}/I_{IO}	Input Bias and Offset Current	vs Case temperature	35
V_{OS}	Input Offset Voltage	vs Case temperature	36

TYPICAL CHARACTERISTICS (5 V)

FREQUENCY RESPONSE

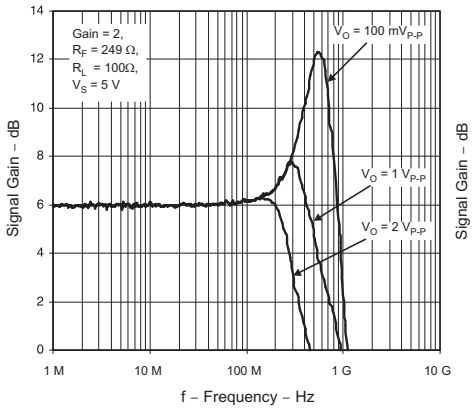


Figure 1.

FREQUENCY RESPONSE

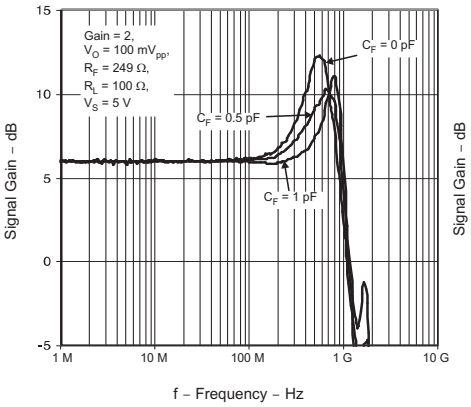


Figure 2.

FREQUENCY RESPONSE

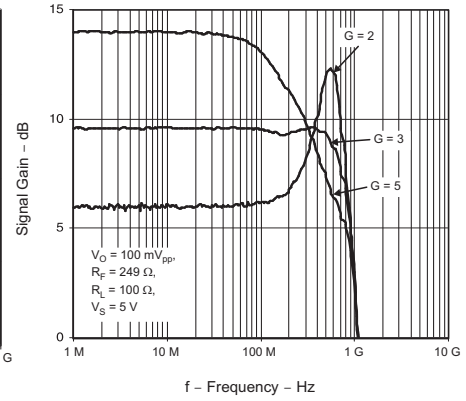


Figure 3.

0.1 dB FLATNESS

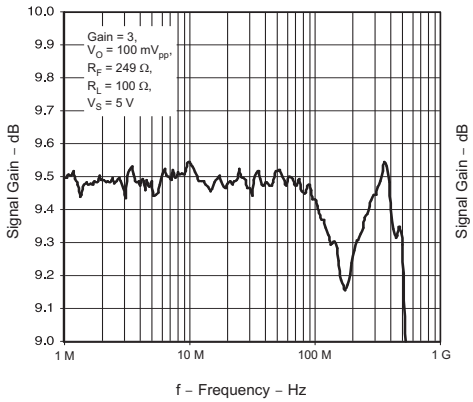


Figure 4.

FREQUENCY RESPONSE

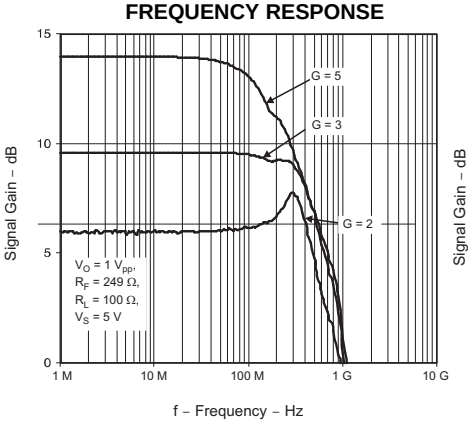


Figure 5.

FREQUENCY RESPONSE

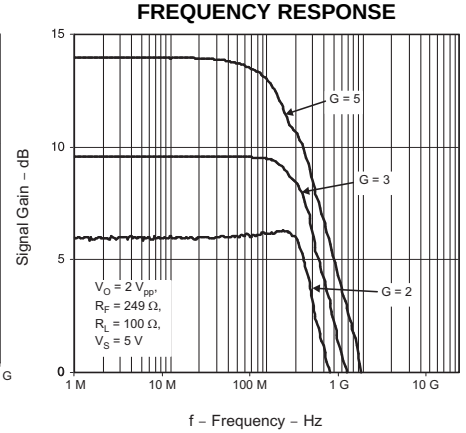


Figure 6.

S-PARAMETERS VS FREQUENCY

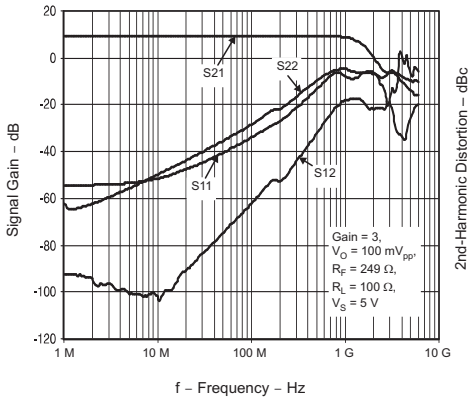


Figure 7.

2nd-HARMONIC DISTORTION VS FREQUENCY

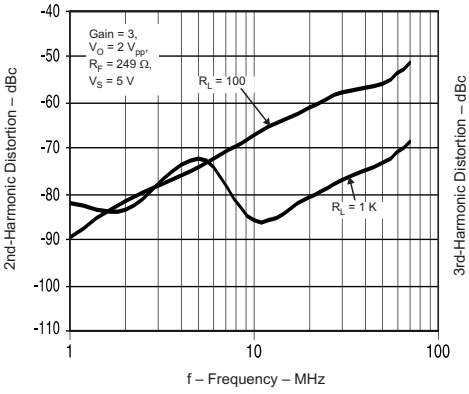


Figure 8.

3rd-HARMONIC DISTORTION VS FREQUENCY

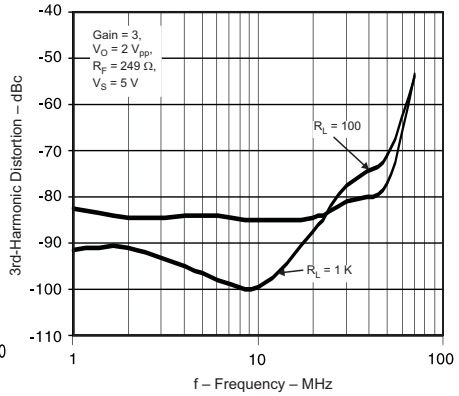


Figure 9.

TYPICAL CHARACTERISTICS (5 V) (continued)

2nd-HARMONIC DISTORTION vs FREQUENCY

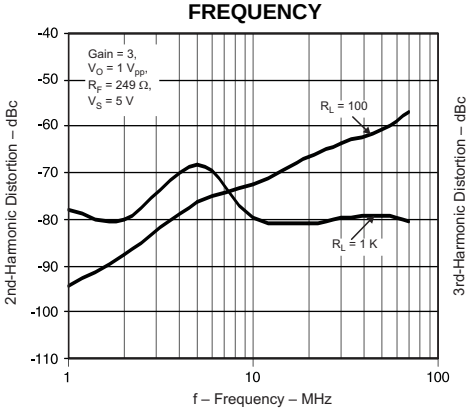


Figure 10.

3rd-HARMONIC DISTORTION vs FREQUENCY

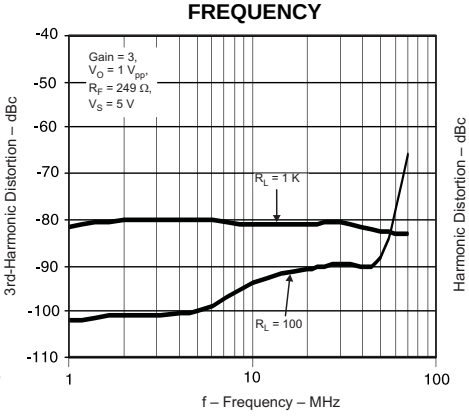


Figure 11.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

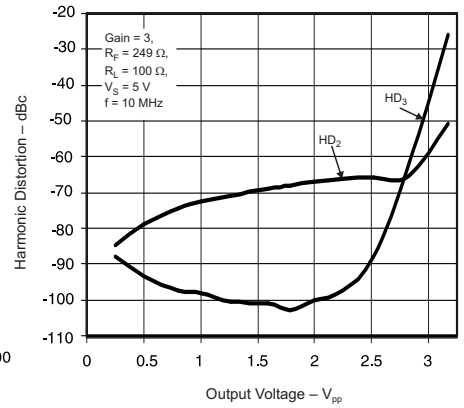


Figure 12.

3rd-ORDER INTERMODULATION DISTORTION vs FREQUENCY

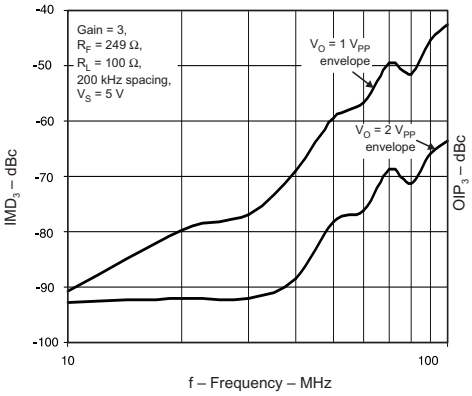


Figure 13.

3rd-ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

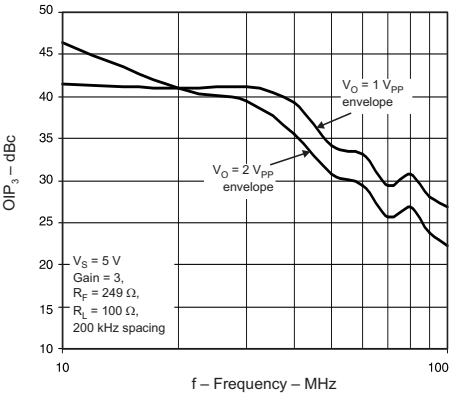


Figure 14.

SLEW RATE vs OUTPUT VOLTAGE

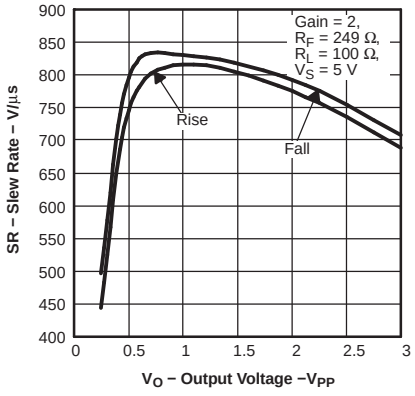


Figure 15.

NOISE vs FREQUENCY

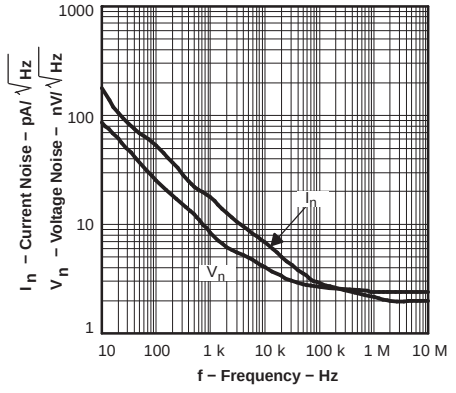


Figure 16.

NOISE FIGURE vs FREQUENCY

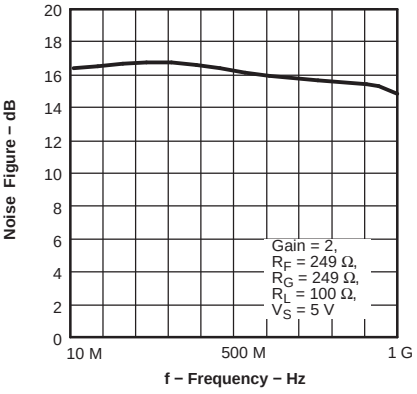


Figure 17.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

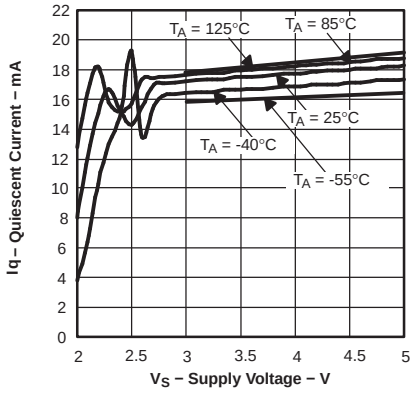


Figure 18.

TYPICAL CHARACTERISTICS (5 V) (continued)

REJECTION RATIO vs FREQUENCY

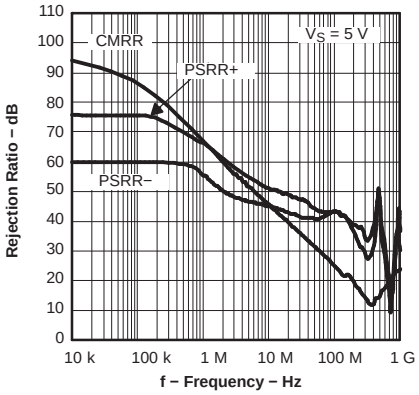


Figure 19.

OUTPUT VOLTAGE vs LOAD RESISTANCE

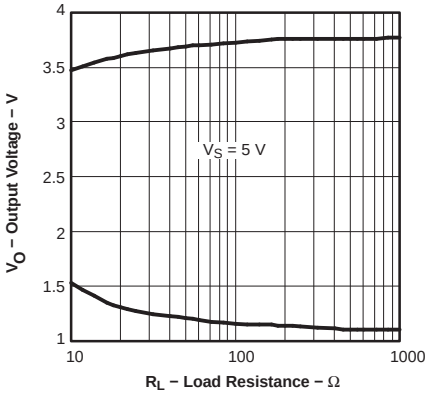


Figure 20.

INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE VOLTAGE

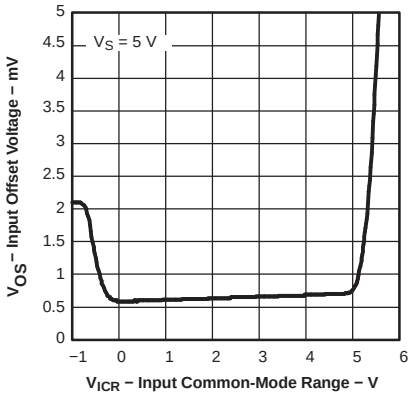


Figure 21.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

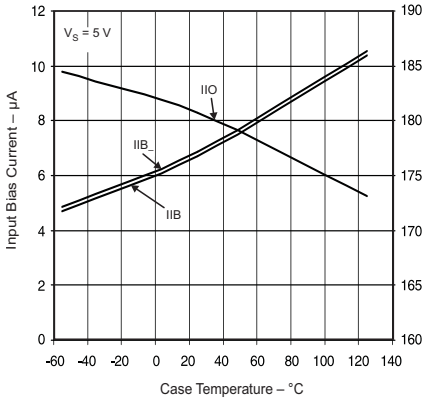


Figure 22.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

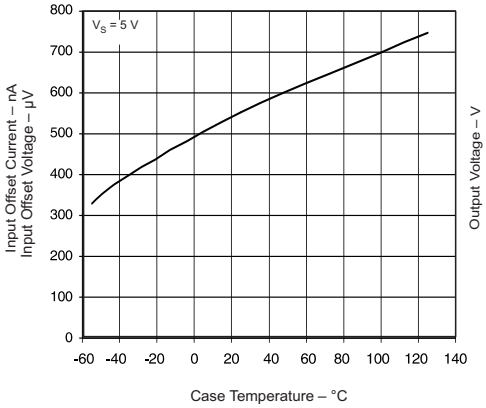


Figure 23.

SMALL-SIGNAL TRANSIENT RESPONSE

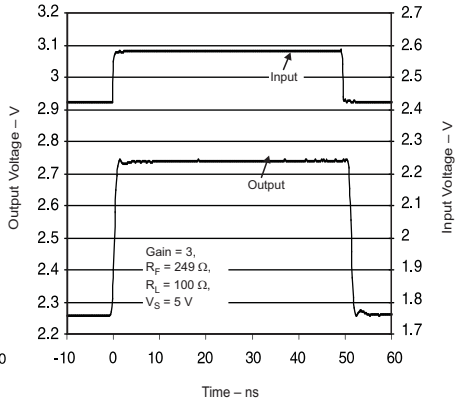


Figure 24.

LARGE-SIGNAL TRANSIENT RESPONSE

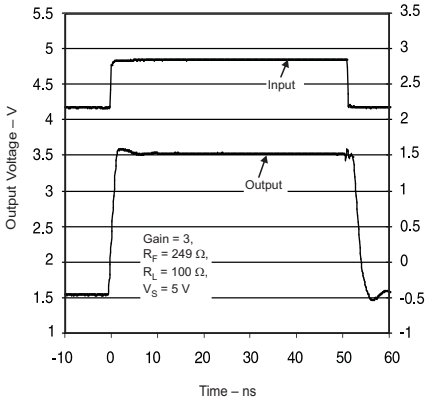


Figure 25.

SETTLING TIME

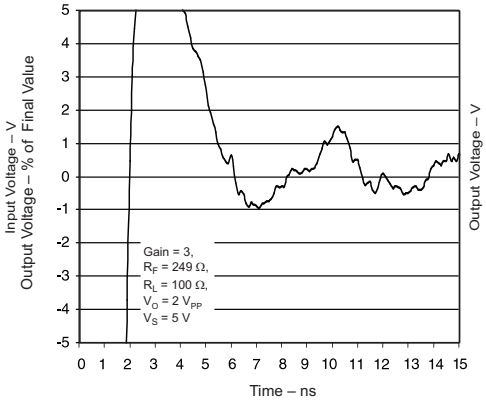


Figure 26.

OVERDRIVE RECOVERY TIME

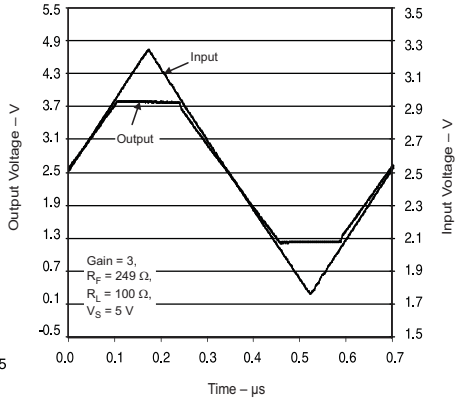


Figure 27.

TYPICAL CHARACTERISTICS (3 V)

FREQUENCY RESPONSE

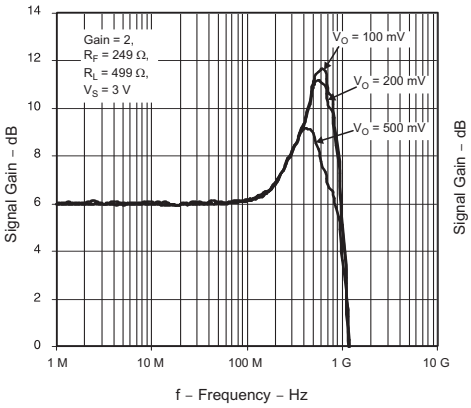


Figure 28.

FREQUENCY RESPONSE

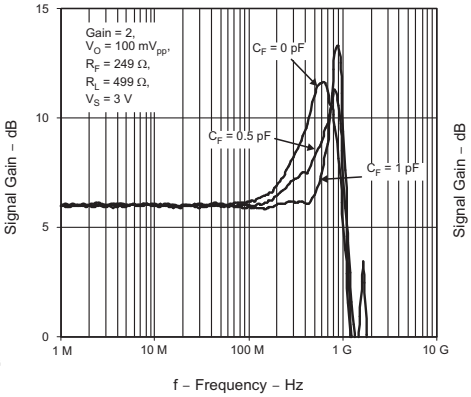


Figure 29.

FREQUENCY RESPONSE

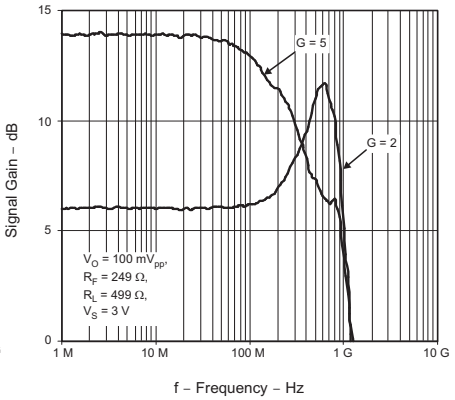


Figure 30.

HARMONIC DISTORTION vs FREQUENCY

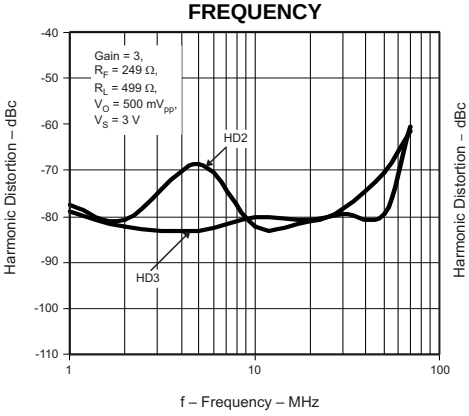


Figure 31.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

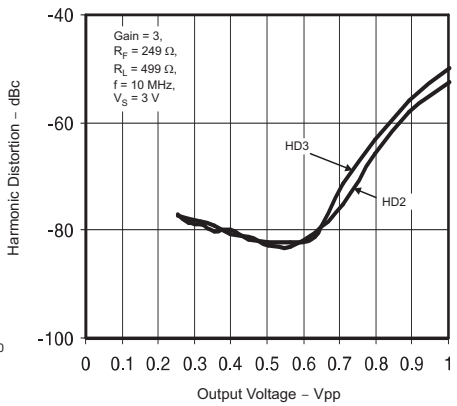


Figure 32.

SLEW RATE vs OUTPUT VOLTAGE

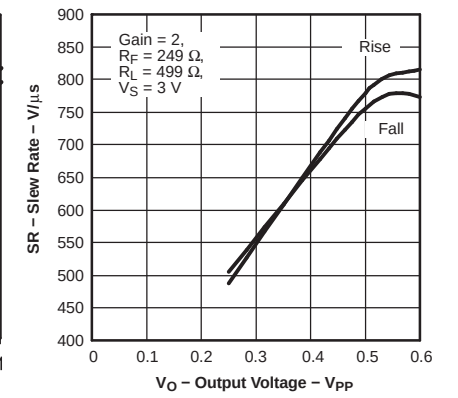


Figure 33.

OUTPUT VOLTAGE vs LOAD RESISTANCE

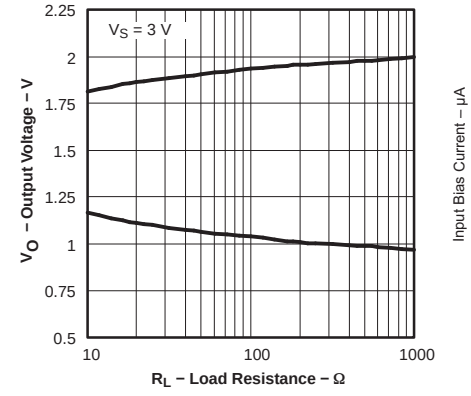


Figure 34.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

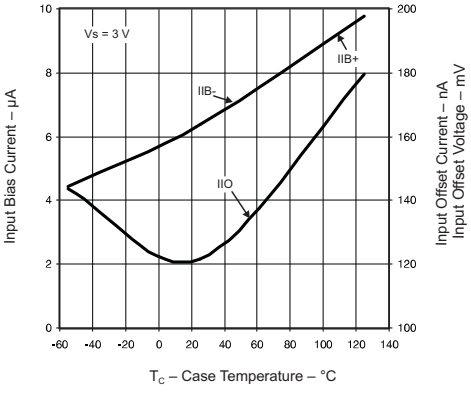


Figure 35.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

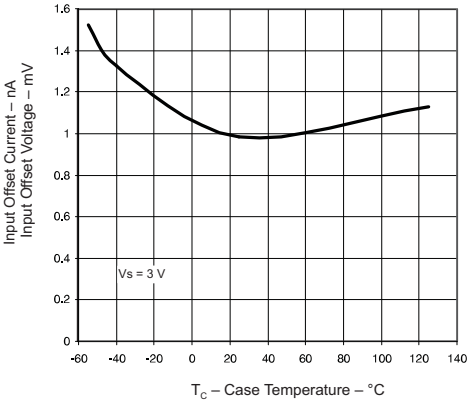


Figure 36.

APPLICATION INFORMATION

For many years, high-performance analog design has required the generation of split power supply voltages, like ±15 V, ±8 V, and more recently ±5 V, to realize the full performance of the amplifiers available. Modern trends in high-performance analog are moving toward single-supply operation at 5 V, 3 V, and lower. This reduces power-supply cost due to less voltage being generated and conserves energy in low-power applications. It also can take a toll on available dynamic range, a valuable commodity in analog design, if the available voltage swing of the signal also must be reduced.

Two key figures of merit for dynamic range are signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR).

SNR is simply the signal level divided by the noise:

$$\text{SNR} = \frac{\text{Signal}}{\text{Noise}}$$

and SFDR is the signal level divided by the highest spur:

$$\text{SFDR} = \frac{\text{Signal}}{\text{Spur}}$$

In an operational amplifier, reduced supply voltage typically results in reduced signal levels due to lower voltage available to operate the transistors within the amplifier. When noise and distortion remain constant, the result is a commensurate reduction in SNR and SFDR. To regain dynamic range, the process and the architecture used to make the operational amplifier must have superior noise and distortion performance with lower power supply overhead required for proper transistor operation.

The THS4304 BiCom3 operational amplifier is just such a device. It is able to provide 2 Vpp signal swing at its output on a single 5 V supply with noise and distortion performance similar to the best 10 V operational amplifiers on the market today

GENERAL APPLICATION

The THS4304 is a traditional voltage-feedback topology with wideband performance up to 1 GHz at a gain of 2 V/V. Care must be taken to ensure that parasitic elements do not erode the phase margin.

Capacitance at the output and inverting input, and resistance and inductance in the feedback path, can cause problems.

To reduce parasitic capacitance, the ground plane should be removed from under the part. To reduce inductance in the feedback, the circuit traces should be kept as short and direct as possible.

For a gain of +2V/V, it is recommended to use a 249 Ω feedback resistor. With good layout, this should keep the frequency response peaking to around 6 dB. This resistance is high enough to not load the output excessively, and the part is capable of driving 100 Ω load with good performance. Higher-value resistors can be used, with more peaking. Lower-value feedback resistors also can be used to reduce peaking, but degrade the distortion performance with heavy loads.

Power supply bypass capacitors are required for proper operation. The most critical are 0.1 µF ceramic capacitors; these should be placed as close to the part as possible. Larger bulk capacitors can be shared with other components in the same area as the operational amplifier.

HARMONIC DISTORTION

For best second harmonic (HD2), it is important to use a single-point ground between the power supply bypass capacitors when using a split supply. It also is recommended to use a single ground or reference point for input termination and gain-setting resistors (R8 and R11 in the non-inverting circuit). It is recommended to follow the EVM layout closely in your application.

EVALUATION MODULES

The THS4304 has two evaluation modules (EVMs) available. One is for the MSOP (DGK) package and the other for the SOT-23 (DBV) package. These provide a convenient platform for evaluating the performance of the part and building various different circuits. The full schematics, board layout, and bill of materials (as supplied) for the boards are shown in the following illustrations.

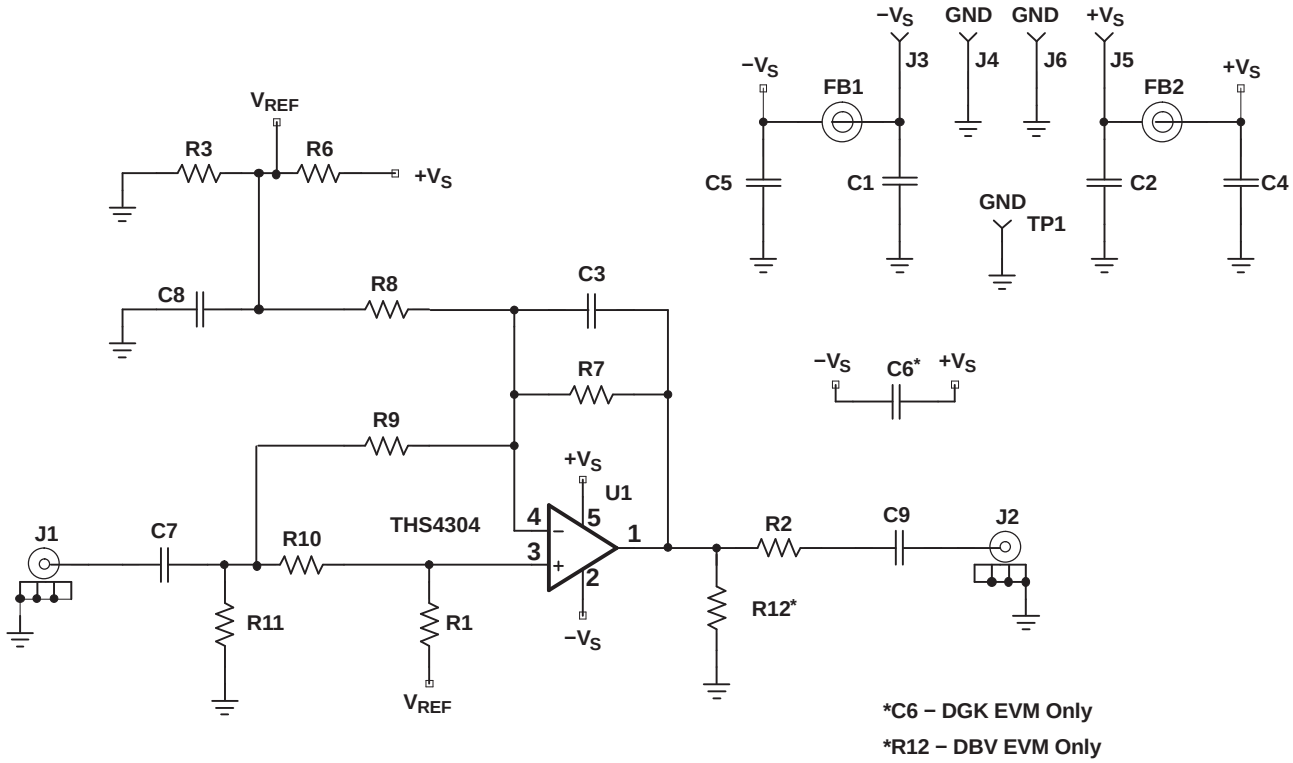


Figure 37. EVM Full Schematic

EVM BILL OF MATERIALS

THS4304 EVM[1]						
Item	**Description**	**SMD Size**	**Reference Designator**	**PCB Quantity**	**Manufacturer's Part Number**	**Distributor's Part Number**
1	Bead, ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(STEWARD) HI1206N800R-00	(DIGI-KEY) 240-1010-1-ND
2	Capacitor, 3.3 µF, Ceramic	1206	C1, C2	2	(AVX) 1206YG335ZAT2A	(GARRETT) 1206YG335ZAT2A
3	Capacitor, 0.1 µF, Ceramic	0603	C4, C5	2	(AVX) 0603YC104KAT2A	(GARRETT) 0603YC104KAT2A
4	Open	0603	C3, C6[2]	2		
5	Open	0603	R1, R3, R6, R9, R12[3]	5		
6	Resistor, 0 Ω, 1/10 W, 1%	0603	C7. C8, C9, C10	4	(KOA) RK73Z1JTTD	(GARRETT) RK73Z1JTTD
7	Resistor, 49.9 Ω, 1/10 W, 1%	0603	R2, R11	2	(KOA) RK73H1JLTD49R9F	(GARRETT) RK73H1JLTD49R9F
8	Resistor, 249 Ω, 1/10 W, 1%	0603	R7, R8	2	(KOA) RK73H1JLTD2490F	(GARRETT) RK73H1JLTD2490F
9	Jack, banana recepticle, 0.25 in. diameter hole		J3, J4, J5, J6	4	(HH SMITH) 101	(NEWARK) 35F865
10	Test point, black		TP1	1	(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
11	Connector, edge, SMA PCB jack		J1, J2	2	(JOHNSON) 142-0701-801	(NEWARK) 90F2624
12	Integrated Circuit, THS4304		U1	1	(TI) THS4304DGK, or (TI) THS4304DBV	
13	Standoff, 4-40 HEX, 0.625 in. Length			4	(KEYSTONE) 1808	NEWARK) 89F1934
14	Screw, Phillips, 4-40, 0.250 in.			4	SHR-0440-016-SN	
15	Board, printed-circuit			1	(TI) THS4304DGK ENG A, or (TI) THS4304DBV ENG A	

(1) NOTE: All items are designated for both the DBV and DGK EVMs unless otherwise noted.
(2) C6 used on DGK EVM only.
(3) R12 used on DBV EVM only.

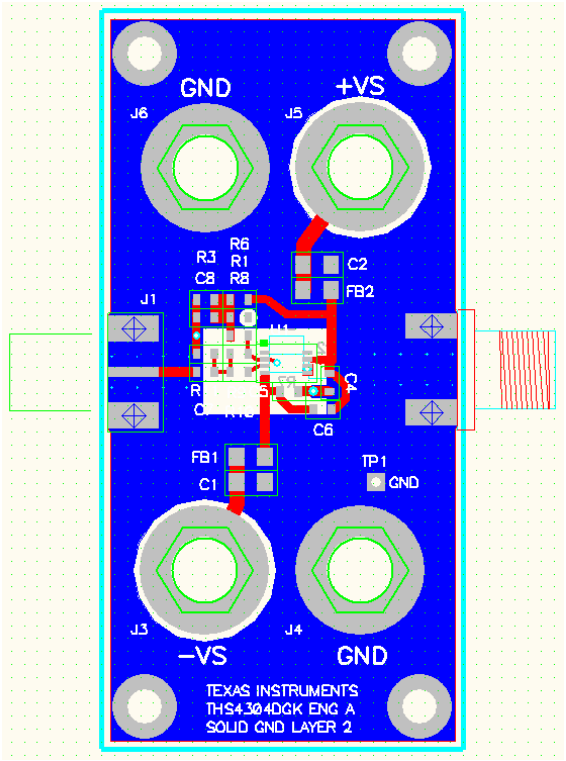


Figure 38. THS4304DGK EVM Layout Top and L2

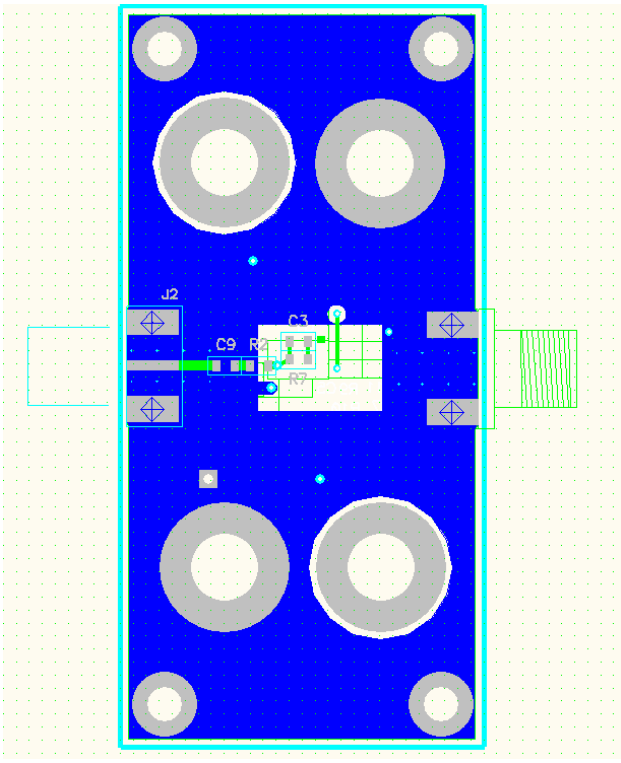


Figure 39. THS4304DGK EVM Layout Bottom and L3

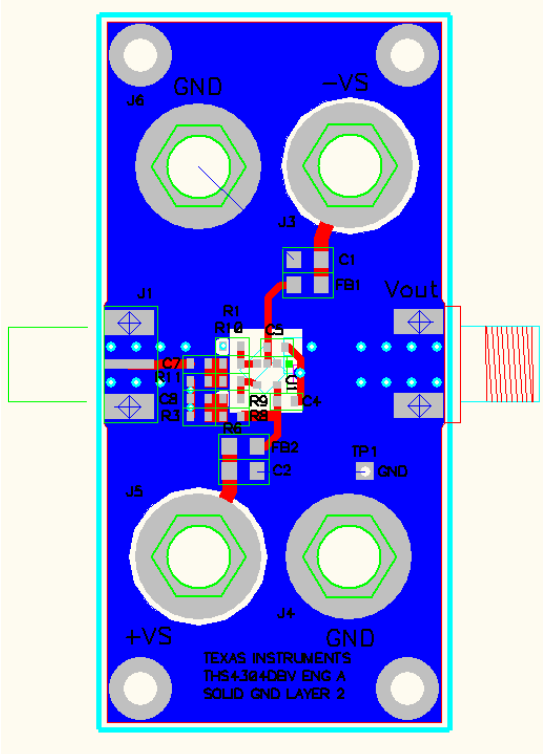


Figure 40. THS4304DBV EVM Layout Top and L2

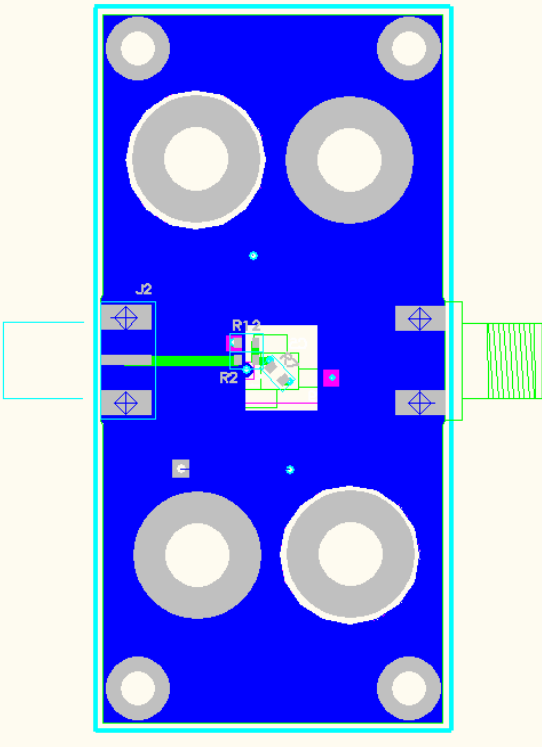


Figure 41. THS4304DBV EVM Layout Bottom and L3

NON-INVERTING GAIN WITH SPLIT SUPPLY

The following schematic shows how to configure the operational amplifier for non-inverting gain with split power supply (±2.5V). This is how the EVM is supplied from TI. This configuration is convenient for test purposes because most signal generators and analyzer are designed to use ground-referenced signals by default. Note the input and output provides 50 Ω termination.

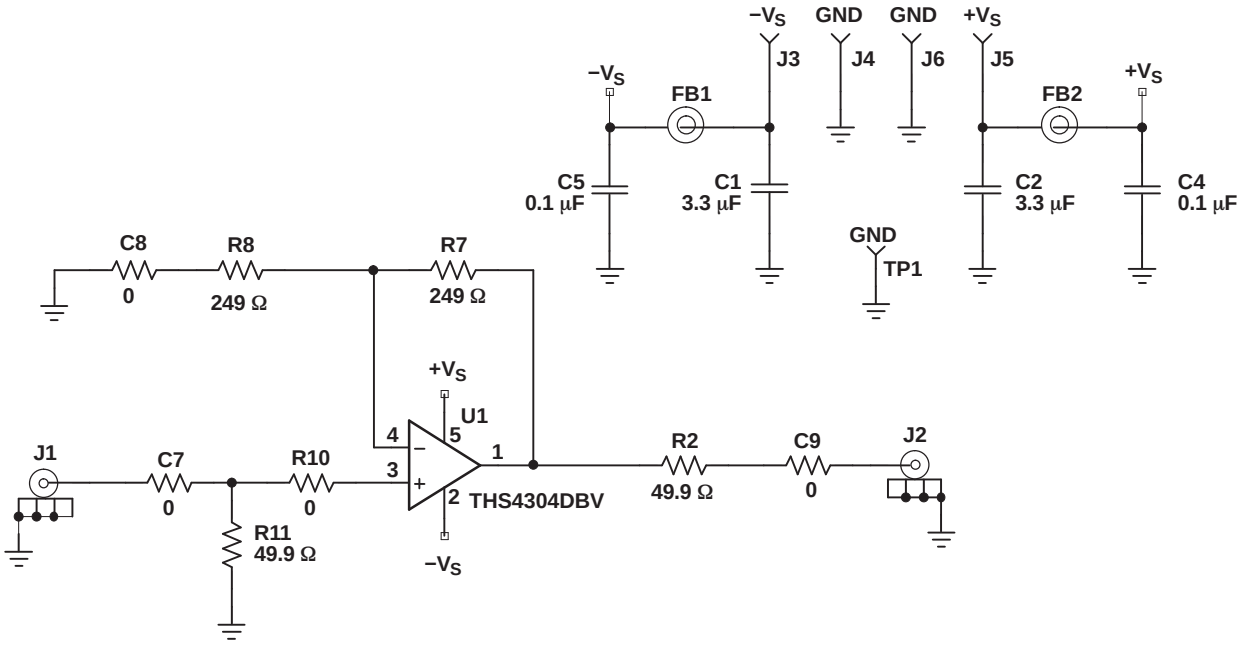


Figure 42. Non-Inverting Gain With Split Power Supply

INVERTING GAIN WITH SPLIT POWER SUPPLY

The following schematic shows how to configure the operational amplifier for inverting gain of 1 (–1 V/V) with split power supply (±2.5 V). Note the input and output provides 50 Ω termination for convenient interface to common test equipment.

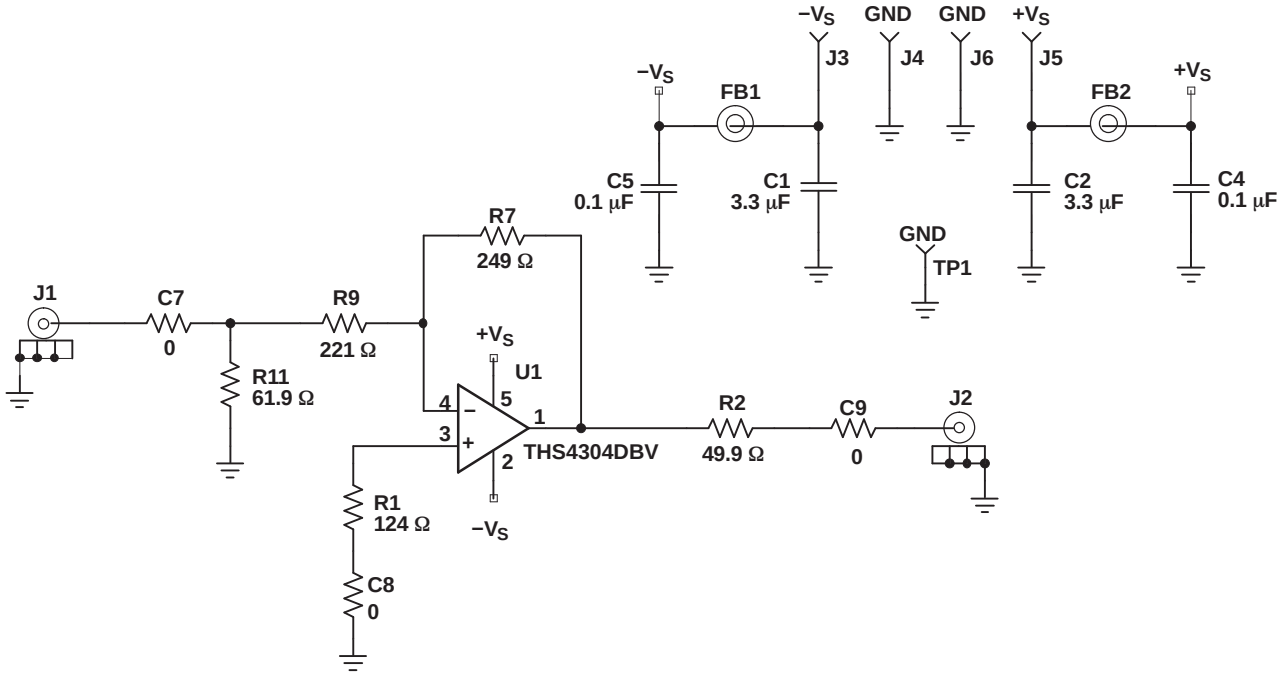


Figure 43. Inverting Gain With Split Power Supply

NON-INVERTING SINGLE-SUPPLY OPERATION

The THS4304 EVM can easily be configured for single 5 V supply operation, as shown in the following schematic, with no change in performance. This circuit passes dc signals at the input, so care must be taken to reference (or bias) the input signal to mid-supply.

If dc operation is not required, the amplifier can be ac coupled by inserting a capacitor in series with the input (C7) and output (C9).

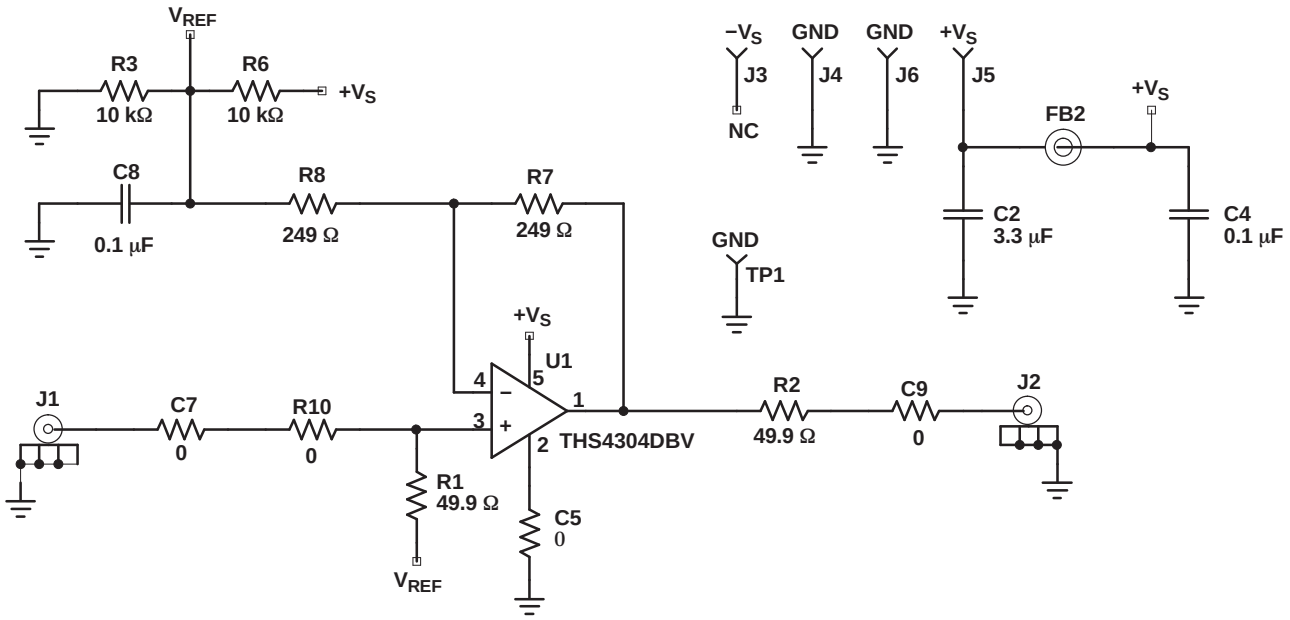


Figure 44. Non-Inverting 5-V Single-Supply Amplifier

DIFFERENTIAL ADC DRIVE AMPLIFIER

The circuit shown in Figure 44 is adapted as shown in Figure 45 to provide a high-performance differential amplifier drive circuit for use with high-performance ADCs, like the ADS5500 (14 bit 125 MSP ADC). For testing purposes, the circuit uses a transformer to convert the signal from a single-ended source to differential. If the input signal source in your application is differential and biased to mid-rail, no transformer is required.

The circuit employs two amplifiers to provide a differential signal path to the ADS5500. A resistor divider (two 10 kΩ resistors) is used to obtain a mid-supply reference voltage of 2.5 V (VREF) (the same as shown in the single-supply circuit of Figure 44). Applying this voltage to the one side of RG and to the positive input of the operational amplifier (via the center-tap of the transformer) sets the input and output common-mode voltage of the operational amplifiers to mid-rail to optimize their performance. The ADS5500 requires an input common-mode voltage of 1.5 V. Due to the mismatch in required common-mode voltage, the signal is ac coupled from the amplifier output, via the two 1 nF capacitors, to the input of the ADC. The CM voltage of the ADS5500 is used to bias the ADC input to the required voltage, via the 1 kΩ resistors. Note: 100 µA common-mode current is drawn by the ADS5500 input stage (at 125 MSPS). This causes a 100 mV shift in the input common-mode voltage, which does not impact the performance when driving the input to –1 dB of full scale. To offset this effect, a voltage divider from the power supply can be used to derive the input common-mode voltage reference.

Because the operational amplifiers are configured as non-inverting, the inputs are high impedance. This is particularly useful when interfacing to a high-impedance source. In this situation, the amplifiers provide impedance matching and amplification of the signal.

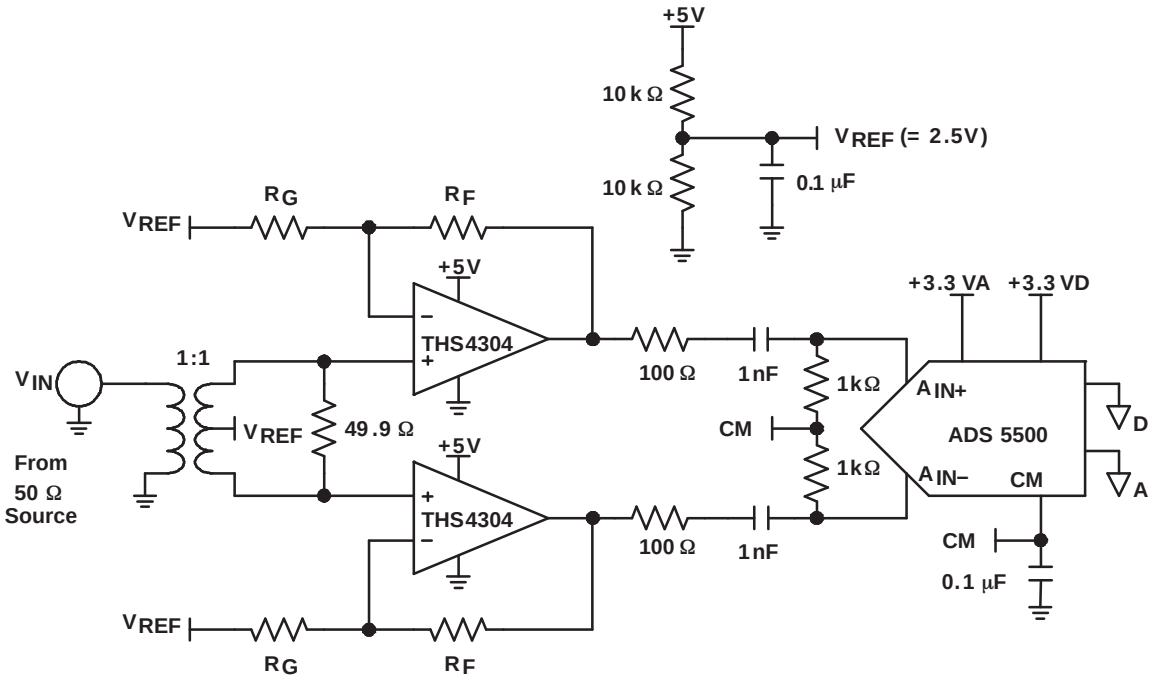


Figure 45. Differential ADC Drive Amplifier Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0721901VHA	ACTIVE	CFP	HKK	10	1	Non-RoHS & Green	AU	N / A for Pkg Type	-55 to 125	0721901VHA THS4304M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

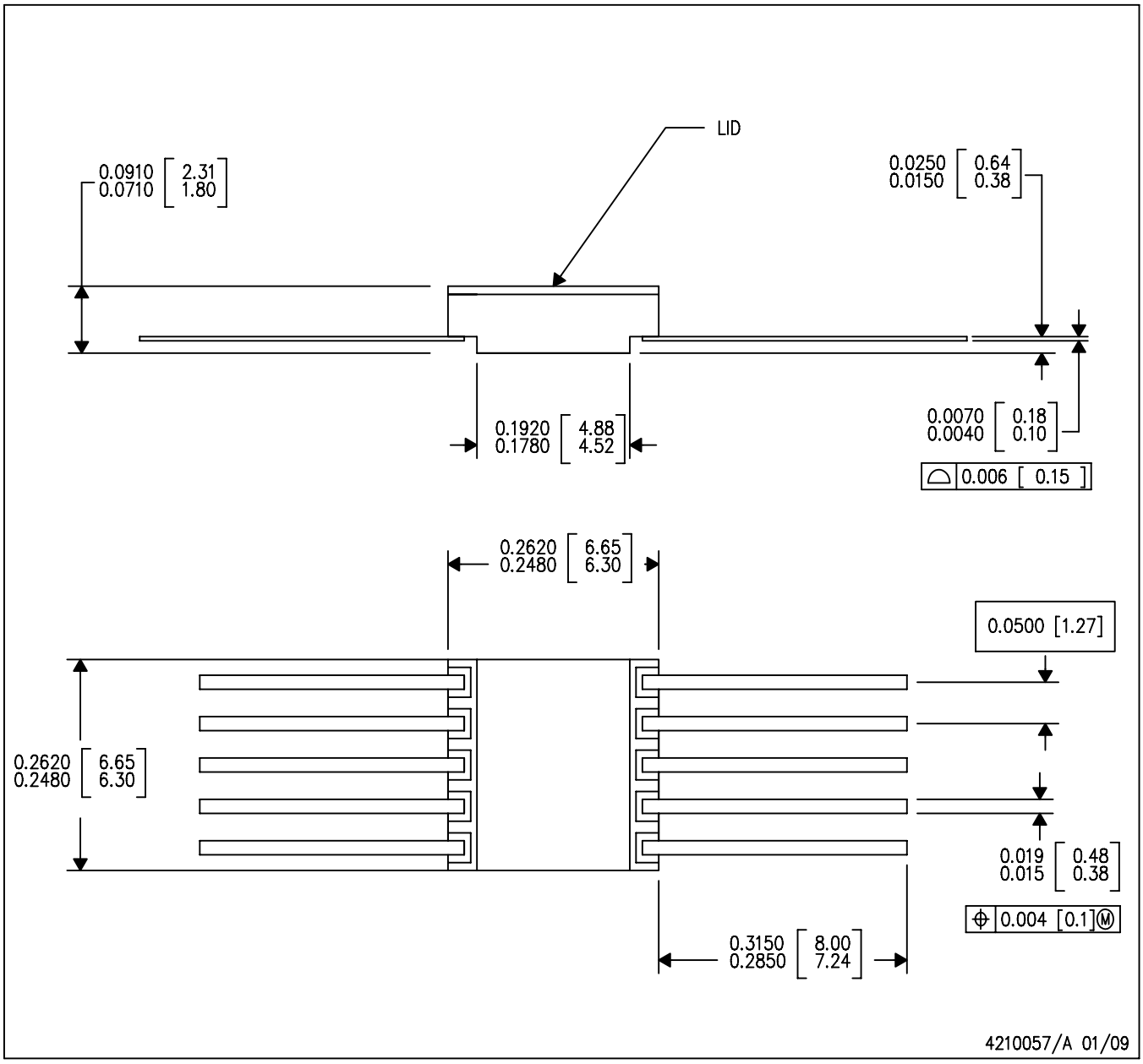
OTHER QUALIFIED VERSIONS OF THS4304-SP :

- Catalog : THS4304

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

HKK (R–CFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This drawing does not comply with Mil Std 1835. Do not use this package for compliant product.
D. The terminals will be gold plated.

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